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PROPOSAL OF MINIMUM SM VOLTAGE CONTROL FOR LOSSES REDUCTION AND RELIABILITY IMPROVEMENT IN MMC-BASED STATCOM

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"PROPOSAL OF MINIMUM SM VOLTAGE CONTROL FOR LOSSES REDUCTION AND RELIABILITY IMPROVEMENT IN MMC-BASED STATCOM"

RENATA OLIVEIRA DE SOUSA

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À minha família, mentores e amigos.

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In order to reach all important people, initially I will write some words in Portuguese.

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"Rien ne nous limitait, rien ne nous définissait,
rien ne nous assujettissait; nos liens avec
le monde c'est nous qui les créions; la
liberté était notre substance même."
(Simone de Beauvoir)

Resumo

Compensadores síncronos estáticos (STATCOMs, do inglês *static synchronous compensators*) têm sido amplamente empregados para atender os requerimentos de qualidade de energia no sistema elétrico. Os esforços de pesquisa mais recentes em STATCOMs visam melhorar a eficiência e confiabilidade desses conversores. Entre as topologias de STATCOM, o conversor modular multinível (MMC, do inglês *modular multilevel converter*) tem se mostrado uma opção atrativa para aplicação do STATCOM em média e alta tensão. No entanto, os custos de implementação do MMC-STATCOM ainda são elevados. Por este motivo, a redução de perdas melhoria da confiabilidade deste conversor é uma questão importante para reduzir os custos de operação e viabilizar o uso desta tecnologia. Este trabalho propõe uma nova estratégia de controle baseada em uma técnica de tensão de barramento c.c. variável que controla a tensão de referência do submódulo (SM) de acordo com a tensão mínima exigida em cada condição de operação do conversor. Esta técnica é denominada controle de tensão mínima do submódulo (MVC, do inglês *minimum voltage control*). Consequentemente, as tensões nos componentes do SM podem ser reduzidas, reduzindo perdas e melhorando a confiabilidade. Para tanto, o controle proposto é avaliado com duas estratégias de modulação populares: modulação por largura de pulso com portadoras deslocadas por fase (PSC-PWM, do inglês *phase-shifted carrier pulse-width modulation*), com frequência de comutação fixa, e controle de nível mais próximo (NLC, do inglês *nearest-level control*), com frequência de comutação variável. Além disso, quatro tensões de bloqueio de dispositivos semicondutores disponíveis comercialmente são consideradas para avaliar o conversor com diferentes números de SMs. Uma metodologia de projeto e ajuste de controladores para MMC-STATCOM é proposta. Uma metodologia de previsão de desgaste é apresentada como uma figura de mérito para avaliação da confiabilidade, na qual um algoritmo de *rainflow* modificado é introduzido. Os resultados de simulação e experimentais demonstraram a eficácia operacional das metodologias propostas para projeto, ajuste de controladores e da estratégia de MVC. Além disso, o MVC reduziu as perdas e a aumentou confiabilidade do conversor em todos os estudos de caso. De fato, o MVC reduziu em cerca de 53% o desgaste dos capacitores. Ademais, quanto maior a frequência de comutação e menor o número de SMs, maior a redução de perdas com MVC. Adicionalmente, modificações de *hardware* são evitadas para a estratégia proposta. Por esse motivo, pode-se afirmar que o MVC tem potencial para melhorar os custos operacionais e a confiabilidade do MMC-STATCOM.

Palavras-chaves: STATCOM; Conversor Modular Multinível; Redução de Perdas; Confiabilidade; Controle de Tensão Mínima do submódulo.

Abstract

Static synchronous compensators (STATCOMs) have been widely employed to fulfill power quality requirements in electrical systems. The most recent research efforts in STATCOMs aim to improve the efficiency and reliability of these converters. Among the STATCOM topologies, the modular multilevel converter (MMC) has proved to be an attractive option for medium- and high-voltage STATCOM. Nevertheless, the implementation costs of MMC-STATCOM are still high. For this reason, the losses reduction and reliability improvement of this converter is important to reduce operational costs and encourage the use of this technology. This work proposes a novel control strategy based on a variable dc-side voltage which controls the submodule (SM) voltage according to the minimum voltage required at each converter operation condition. This technique is named minimum SM voltage control (MVC). Consequently, the stress on SM components can be reduced, reducing losses and improving reliability. For this purpose, the MVC is evaluated with two popular modulation strategies: phase-shifted carrier pulse-width modulation (PSC-PWM), with fixed switching frequency, and nearest-level control (NLC), with variable switching frequency. Four commercially available semiconductor blocking voltages are considered to evaluate the converter with different number of SMs. A control tuning and design methodology of MMC-STATCOM is proposed. A wear-out prediction methodology is presented as a figure of merit for reliability evaluation, where a modified rainflown algorithm is introduced. The simulation and experimental results demonstrated the operational effectiveness of the methodologies proposed for design, control tuning, and MVC strategy. Moreover, MVC reduced the losses and increased the reliability of the converter in all case studies, where can be highlighted the reduction of capacitor wear-out by around 53%. Besides, the highest losses reduction is shown for higher switching frequencies and the lower number of SMs. Furthermore, hardware modifications are avoided for the proposed strategy. For this reason, it can be stated that MVC has the potential to improve operational costs and reliability in MMC-STATCOM systems.

Key-words: STATCOM; Modular Multilevel Converter; Losses Reduction; Reliability; Minimum SM Voltage Control.

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List of abbreviations and acronyms

ANPC	active neutral point clamped
BW	bondwire
BPCS	base plate and conductor solders
CAPEX	capital expenditure
CD-PWM	carrier-disposition pulse with modulation
CDF	cumulative density function
CHB	cascaded H-bridge converter
CS	chip solder
CTB	cell tolerance band algorithm
DCMC	diode clamped multilevel converter
DPWM	discontinuous pulse width modulation
ESL	equivalent series inductor
ESR	equivalent series resistor
FC	flying capacitor converter
FFT	fast Fourier transform
FIT	failure in time
GaN	gallium nitride
GTO	gate turn-off thyristor
HB	half-bridge
HV	high voltage
HVDC	high-voltage direct current
IGBT	insulated gate bipolar transistor
IGCT	integrated gate-commutated thyristor

LC	life consumption
LPF	low-pass filter
LT	lifetime
MAF	moving average filter
MV	medium voltage
MVC	minimum voltage control
MMC	modular multilevel converter
MTTR	mean time to repair
NLC	nearest-level control
NPC	neutral point clamped
OPEX	operational expenditure
PDF	probability density function
PI	proportional integral
PLL	phase-locked loop
PR	proportional resonant
PSC-PWM	phase-shifted carrier pulse width modulation
PWM	pulse width modulation
pu	per unit
rms	root mean square
SC	synchronous condenser
SHE	selective harmonic elimination
SiC	silicon carbide
SM	submodule
SSSC	static synchronous series compensator
SVC	static var compensator
STATCOM	static synchronous compensator

TCSC	thyristor-controlled series capacitor
TDD	total demand distortion
THD	total harmonic distortion
VSC	voltage source converter
Y-CHB	star-connected cascaded H-bridge converter
Δ-CHB	delta-connected cascaded H-bridge converter

List of symbols

A_h	heatsink surface area
A_{sw}	IGBT module parameter from empirical data
B_{sw}	IGBT module parameter from empirical data
B_{10}	number of cycles where 10 % of the elements of a population fail
C	SM capacitance
$C_{[1,2,3]}$	failure rate model coefficients
C_N	individual nominal capacitance
C_{N17}	case study with NLC-CTB and $V_{bk} = 1.7$ kV
C_{N33}	case study with NLC-CTB and $V_{bk} = 3.3$ kV
C_{N45}	case study with NLC-CTB and $V_{bk} = 4.5$ kV
C_{N65}	case study with NLC-CTB and $V_{bk} = 6.5$ kV
c_h	specific heat capacity
C_{h-w}	heatsink-to-water cooling thermal capacitance
C_{P17}	case study with PS-PWM and $V_{bk} = 1.7$ kV
C_{P33}	case study with PS-PWM and $V_{bk} = 3.3$ kV
C_{P45}	case study with PS-PWM and $V_{bk} = 4.5$ kV
C_{P65}	case study with PS-PWM and $V_{bk} = 6.5$ kV
C_{sw}	IGBT module parameter from empirical data
D_1	bottom diode
D_2	top diode
D_i	losses or disturbance in the i-th converter SM
d_h	heatsink thickness
E_{sw}	switching energy

f_2	NLC-CTB important frequency
F_{20}	unreliability in 20 years
$f_{c,b}$	frequency of pole in individual balancing control
$f_{c,s}$	frequency of the closed-loop-system bandwidth of global energy control
$f_{c,z}$	frequency of the closed-loop-system bandwidth of circulating current control
f_{ef}	effective output frequency
$f_{h,s}$	frequency of the resonant part bandwidth of global energy control
$f_{h,z}$	frequency of the resonant part bandwidth of circulating current control
f_i	frequency from Fast Fourier Transform
f_n	fundamental frequency
f_s	sampling frequency
f_{sw}	switching frequency
f_{us}	utilization factor
$f_{us,max}$	maximum utilization factor
$f_{v[1,2]}$	frequencies of the poles in global energy control
$f(x)$	probability distribution function
$F(x)$	component unreliability function
$F_f(x)$	structure unreliability function of each component in the SM
$F_{f,sm}(x)$	critical structure unreliability at SM-level
$F_{MMC}(x)$	MMC-STATCOM system-level unreliability function
h	altitude
h_c	water flow convection coefficient
i_C	collector current
$I_{c,i}$	harmonic amplitude of the capacitor current
i_F	forward current

I_N	rated current
$i_{SD,avg}$	semiconductor devices average current
$i_{SD,rms}$	semiconductor devices rms current
i_l	lower arm current
i_s	output current
$\hat{I}_s$	output current amplitude
$i^*_{s\alpha\beta}$	output current in stationary reference frame
i_u	upper arm current
i_z	circulating current
K	odd integer number
K_{off}	K_{sw} of turn-off losses
K_{on}	K_{sw} of turn-on losses
K_{rec}	K_{sw} of recovery losses
K_{sw}	blocking voltage dependence of the the switching energies
$k_{p,b}$	proportional gain of individual balancing control
$k_{i,v}$	integral gain of global energy control
$k_{p,s}$	proportional gain of output current control
$k_{p,v}$	proportional gain of global energy control
$k_{p,z}$	proportional gain of circulating current control
$k_{r,s}$	resonant gain of output current control
$k_{r,z}$	resonant gain of circulating current control
L_a	arm inductance
$L_{c,f}$	time-to-failure of a capacitor
L_{eq}	equivalent output inductance
L_0	rated lifetime of a capacitor
L_f	isolation transformer inductance

l_i	operating time of a capacitor
LC_C	life consumption of the capacitor
LC_{SD}	life consumption of the semiconductor device
$L[N]$	list of SMs
m_{max}	maximum modulation index
N	number of SMs per arm
N_f	number of cycles to failure
n_i	number of cycles
n_l	insertion indexes of lower arm
n_u	insertion indexes of upper arm
$n_{[u,l]}$	rounded signal
p	instantaneous active power
P_{3n}	three-phase instantaneous active power
P_{cap}	capacitor power
P_{cd}	conduction losses
$P_{cd,diode}$	diode conduction losses
$P_{cd,IGBT}$	IGBT conduction losses
$P_{cd,SD}$	semiconductor device conduction losses
$P_{cd,T}$	MMC-STATCOM conduction losses
p_{ib}	active power required for dc-voltage balancing
p_l	lower arm active power
$P_{losses,C}$	power losses of a capacitor
$P_{losses,SD}$	power losses of a semiconductor device
P_{sw}	switching losses
$P_{sw,diode}$	diode switching losses
$P_{sw,IGBT}$	IGBT switching losses

$P_{sw,SD}$	semiconductor device switching losses
$P_{sw,T}$	MMC-STATCOM switching losses
p_u	upper arm active power
q	instantaneous reactive power
r	semiconductor device resistance
R_a	arm inductor resistance
R_b	bleed resistance
R_{eq}	equivalent output resistance
R_f	isolation transformer resistance
R_{h-w}	heatsink-to-water cooling thermal resistance
R_s	equivalent series resistance
R_{th}	capacitor thermal resistance
R_{w-a}	water cooling-to-ambient thermal resistance
S_1	bottom IGBT
S_2	top IGBT
S_b	power base for per unit computation
S_n	rated power
S_T	bypass switch
$\tan(\delta_0)$	dielectric dissipation factor
T_a	ambient temperature
T_c	case temperature
T_d	delay time
T_{ds}	minimum on-time and dead time of the semiconductor devices
T_h	hotspot temperature
$T_{h,r}$	rated hotspot temperature
T_j	junction temperature

$T_{[j,c]m}$	junction and case average temperature
$t_{i,f}$	extreme points of temperature
T_{ma}	moving window time
t_{on}	heating time
T_s	sampling time
v_0	fixed semiconductor device voltage drop
$V_{bk,o}$	maximum operational dc blocking voltage
$V_{bk,n}$	nominal semiconductor blocking voltage
V_c	capacitor voltage
V_{CE}	collector-emitter voltage
$V_{CE,r}$	resistive collector-emitter voltage
$V_{c,r}$	rated capacitor voltage
v_{cl}^{Σ}	sum of the capacitor voltages of lower arm
v_{cu}^{Σ}	sum of the capacitor voltages of upper arm
v_{dc}	dc-side voltage
$v_{dc,0}$	minimum dc-side voltage at hot standby operation
$v_{dc,o}$	minimum dc-side voltage given by zero voltage
$v_{dc,lag}$	minimum dc-side voltage at rated lagging reactive power
$v_{dc,lea}$	minimum dc-side voltage at rated leading reactive power
$v_{dc,min}$	minimum dc-side voltage
$v_{dc,r}$	minimum dc-side voltage given by the polynomial equation
V_F	forward voltage
v_g	grid voltage
V_g	line-to-line rms grid voltage
$v_{g\alpha\beta}$	grid voltage stationary frame
v_i	lower arm inserted voltages

v_{ib}	output of voltage individual balancing control
v_l	lower arm voltage
v_{max}	maximum SM voltage
v_{min}	minimum SM voltage
v_s	output voltage
v_s^*	output voltage reference
V_s	line-to-line rms voltage synthesized by the MMC-STATCOM
$\hat{V}_s$	maximum output voltage
v_{sm}	SM voltage
$\overline{v}_{sm}$	average voltage of all SM voltages
v_{sm}^*	SM voltage reference
v_{sm}^{Σ}	sum of capacitor voltages
v_u	upper arm voltage
v_z	internal voltage
v_z^*	internal voltage reference
W_{conv}	required energy storage per MVA
W_T	total energy storage
W_{Δ}	energy difference between the arms
W_{Σ}	total energy between the arms
W_{Σ}^*	total energy reference
X_a	arm reactance
X_f	grid reactance
$x_{eq,pu}$	maximum per unit value of the output reactance
X_{eq}	equivalent output impedance
Z_{c-h}	case-to-heatsink thermal impedance
Z_{h-w}	heatsink-to-water cooling thermal impedance

$Z_{j-c,foster}$	junction-to-case Foster thermal impedance
Z_{w-a}	water cooling-to-ambient thermal impedance
β	phase displacement between the carrier waveforms in the upper and lower arms
Δi_z	peak-to-peak circulating current ripple
Δv_{dc}	dc-link voltage ripple
Δv_{cl}^{Σ}	sum of capacitor voltage ripples
Δv_{sm}	difference between SM reference voltage instantaneous SM voltage
ΔV_g	grid voltage variation
$\Delta T_{j,c}$	junction and case variation of temperature
Δt_{xi}	time ranges
Δx_{eq}	output reactance variation
λ	modulation gain
λ_f	failure rate
λ_1	failure dependence on the blocking voltage
λ_2	failure dependence on the junction temperature
λ_3	failure dependence on the altitude
λ_h	thermal conductivity
ρ_h	heatsink material density
ϕ	displacement angle of the output current
$\theta_{[1,2]}$	angles of zero crossing of the upper arm current
$\theta_{u,n}$	angular displacements of the upper carrier waveforms
$\theta_{l,n}$	angular displacements of the lower carrier waveforms
ω_n	angular fundamental frequency
ω_s	angular sampling frequency

Superscripts

$*$	reference value
$'$	equivalent static value

Subscripts

a	phase a
b	phase b
c	phase c
u	upper arm
l	lower arm

Contents

1 Introduction

1.1 Context and Relevance

The distribution and transmission systems are complex structures. These systems supply a huge variety of loads, most of them nonlinear or variable, such as motors, electric arc furnaces and loads interfaced by power electronic devices. Moreover, high penetration of solar and wind power plants into the electrical power system is observed. These factors can lead to many issues such as: grid voltage disturbances, voltage instabilities, reactive power, harmonic resonances, among others, which affect the power system overall efficiency (Sharifabadi et al., 2016). Nevertheless, the main objectives of these systems are to supply electric energy to end users with high power quality and reliability, minimizing energy losses and respecting the grid operator standards (Téllez et al., 2018).

Reactive power compensation is one of the well-recognized ancillary services which contributes to the reduction of energy losses, along with other benefits, such as load power factor correction, increasing of the operational capacity of lines and grid devices and improvement of the voltage profile, all of them subject to different operating restrictions (Téllez et al., 2018).

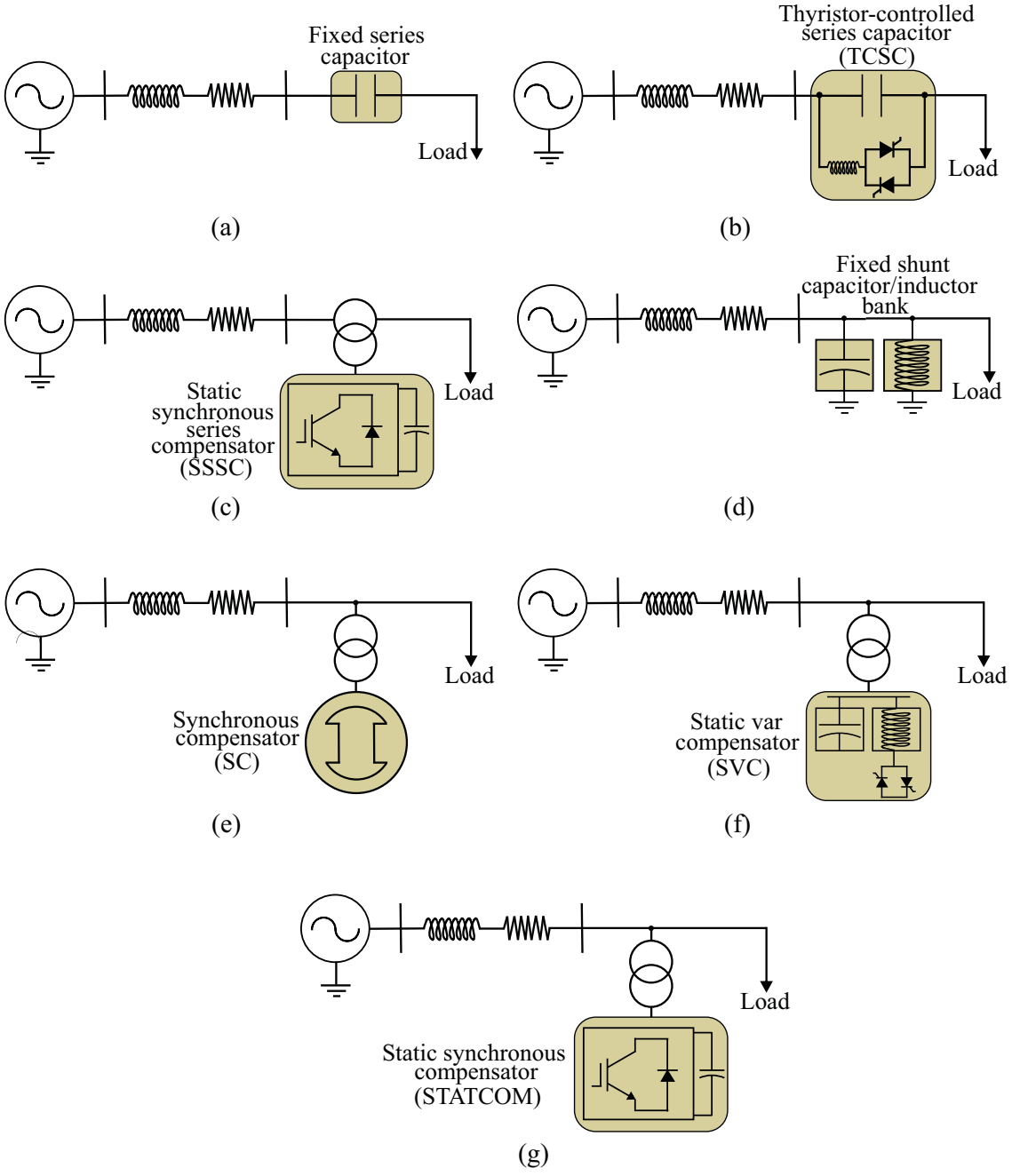
The reactive power compensators can be classified into two categories (Mondal; Chakrabarti; Sengupta, 2014):

- Series compensators: these devices inject voltage in series with the line. They are normally employed to control the longitudinal behavior of the line.
- Shunt compensators: these devices inject current into the system at the point of connection. They are normally employed for voltage control.

The simplest series compensation systems are based on the connection of capacitors in series with the line, as illustrated in Fig. 1 (a). This reactive power solution approach allows increasing the transient stability limit, improving the voltage profile of the system and reducing power losses. However, this configuration cannot change the amount of compensated reactive power (Dixon et al., 2005).

In order to control the compensation, the thyristor-controlled series capacitor (TCSC) was introduced, as illustrated in Fig. 1 (b). The first three-phase TCSC was developed by ABB and installed in 1992 at Kayenta substation in Arizona (Acharya; Sode-Yome; Nadarajah, 2005). Nevertheless, the compensated reactive power is a function of the current flowing through the circuit, which is a drawback of this approach.

Figure 1 – Reactive power compensators: (a) fixed series capacitors; (b) thyristor-controlled series capacitor – TCSC; (c) static synchronous series compensator – SSSC; (d) fixed shunt capacitor/inductor bank; (e) synchronous compensator – SC; (f) static var compensator – SVC; (g) static synchronous compensator – STATCOM.



Source: Elaborated by the author.

Another solution is a configuration based on the series-connected voltage source converter (VSC): the static synchronous series compensator (SSSC). This configuration is shown in Fig. 1 (c). The SSSC injects a voltage with controllable magnitude and phase at the line frequency. Moreover, this solution is capable of handling power flow control, improving transient stability margin and transient damping. The main advantage of SSSC

over a TCSC is that the impedance of the transmission system is unaffected by SSSC and hence resonance problems are avoided (Gandoman et al., 2018).

However, the series compensators have an inherent problem during faults. Their structure must be designed to support the fault currents if compensation is required in such events. Otherwise, a bypass structure must be employed. In this context, the shunt compensation structures present clear advantages, and thus, they are more popular (Dixon et al., 2005).

Similarly to series compensation, the simplest shunt compensation systems are based on the connection of fixed capacitor or inductor banks in shunt with the line, as illustrated in Fig. 1 (d). Despite their simplicity and lower cost, these solutions cannot change the amount of reactive power, which is inefficient when the reactive power varies over a wide range (Dixon et al., 2005).

In the 1920s, synchronous compensators (SCs) were introduced. The SC is illustrated in Fig. 1 (e). Functionally, an SC is simply a synchronous machine connected to the power system which can control reactive power. Nevertheless, synchronous compensators require substantial foundations and a significant amount of starting and protective equipment. Moreover, this technology contributes to short-circuit currents and has higher losses and costs when compared with other reactive power compensation technologies. Nevertheless, the SCs are still widely employed due to the additional capacity to provide inertia, which is important in frequency regulation (Dixon et al., 2005; Igbinovia et al., 2015). Other technologies would require additional energy storage to provide the same support in frequency regulation.

In the 1970s, the static var compensator (SVC) was introduced. The first SVC was installed in Nebraska-USA by General Electric in 1974 (Okeke; Zaher, 2013). The SVC configuration is illustrated in Fig. 1 (f). This configuration is capable to perform lagging and leading reactive power controlling specific parameters of the electrical power system. This capability is achieved by controlling the switching timing of the thyristor. The SVCs are employed to improve the transient stability, damp power swings and reduce system losses by using reactive power control (Gandoman et al., 2018). Nevertheless, the SVC generates low-order harmonic currents on the grid by the switching operation of the thyristor, which requires a large number of passive filters (Dixon et al., 2005; Igbinovia et al., 2015).

In advance of the SVC and based on VSC, the static synchronous compensator (STATCOM) was introduced. The early STATCOMs employed gate turn-off thyristors (GTOs). Modern STATCOMs are based on insulated gate bipolar transistors (IGBTs) or integrated gate-commutated thyristors (IGCTs). The STATCOM is illustrated in Fig. 1 (g). The first STATCOM was installed at Inuyama substation in Japan by Mitsubishi Electric Power Products in 1991 (Acharya; Sode-Yome; Nadarajah, 2005). According to Hingorani,

Gyugyi and El-Hawary (2000), the thyristor-based structures (e.g. SVC) are preferred in installations with high power ratings (in the range of hundreds of Mvar). Nevertheless, the STATCOM presents several advantages, such as fast response time, less space requirement, higher operational flexibility and excellent dynamic characteristics under various operating conditions (Singh et al., 2009; Pereira; Ferreira; Barbosa, 2014; Igbinovia et al., 2015).

Table 1 shows a benchmarking of shunt reactive power compensation technologies (Neutz, 2013). As observed, the fixed shunt capacitor/inductor bank is the cheapest one. Nevertheless, its other features are inferior to those of other technologies. The SC presents interesting features of speed response, repeated operation possible, power control and inertia. Nevertheless, this technology presents high operation costs, due to its lower efficiency, and high time to maintenance in case of failure. On the other hand, the SVC is cheaper, however, it lacks inertia. Finally, STATCOM presents interesting features in terms of operation. Although STATCOMs are more expensive than the other systems, the technical benefits of this technology and recent advances in power converters technology are slowly leading to the use of STATCOM topologies similar to the modernization process observed in high-voltage direct current (HVDC) systems (Behrouzian; Bongiorno, 2017).

Table 1 – Benchmarking of shunt reactive power compensation technologies. *Adapted from:* Neutz (2013).

Technology	Speed of Response	Repeated operation possible	Power Control	Inertia (active power)	Cost CAPEX[1] /OPEX[2]
Fixed shunt capacitor/inductor bank	Slow	Discharge time and wear of switchgear	Fixed steps	No	Low
SC	Fast	Continuous	Continuous	Yes	High OPEX, bad MTTR[3], permanent losses
SVC	Fast	Continuous	Continuous	No	Cheaper than STATCOM for large systems
STATCOM	Fast	Continuous	Continuous	Possible with added energy storage	High CAPEX if no hybrid solution

[1]CAPEX is the capital expenditure and it is related to converter cost: capacitors, magnetic devices, semiconductor devices, controllers, PCBs, cooling system, among others.
[2]OPEX is the operational expenditure and it is mainly associated to the maintenance costs and the costs of the power losses.
[3]The mean time to repair (MTTR) is the time needed to repair a failed hardware module.

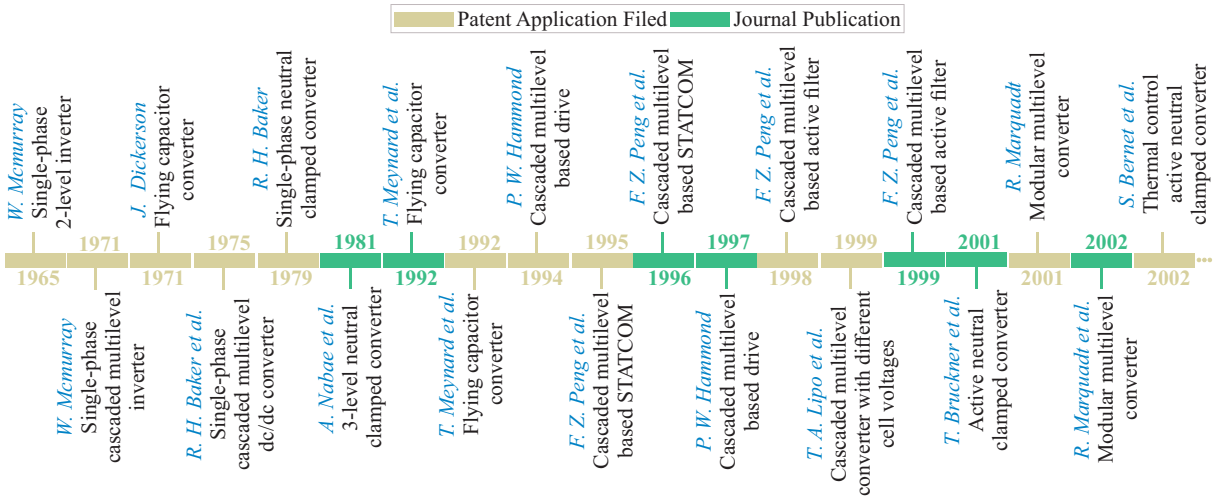
1.2 STATCOM Realization

The major challenge in STATCOM realization is designing a converter topology that must handle high power and high voltages with standard rated semiconductor devices. Indeed, semiconductor devices commercially available are limited in terms of the blocking voltage (up to 6.5 kV for silicon-based devices). For this reason, different STATCOM topologies were developed and commercialized over the years (Fujii; Schwarzer;

De Doncker, 2005; Valdez-Fernández et al., 2013). Moreover, the most recent research efforts in STATCOM realization are targeted at finding efficient and reliable topologies for medium and high voltage systems (Muñoz et al., 2014). Therefore, this section discusses the developments of STATCOM.

Figure 2 summarizes the main scientific contributions, measured in terms of patents and journal papers citation, to the development of power converters employed as STATCOM. These converter topologies are briefly described in the next sections.

Figure 2 – Timeline of the main patents and journal papers related to STATCOM development.



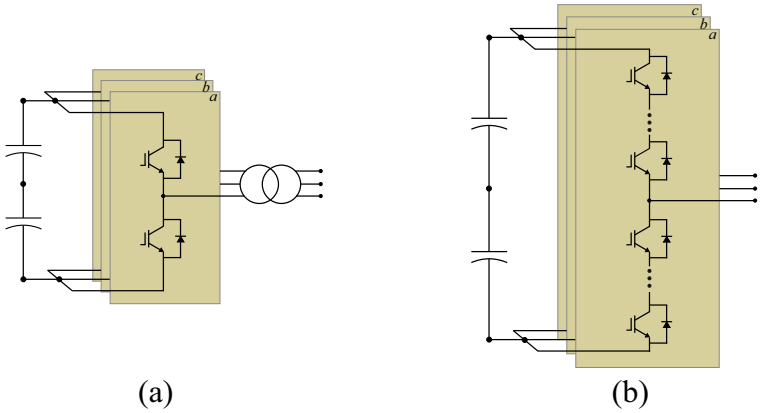
Source: Adapted from Mendonça et al. (2022).

1.2.1 Two-level Converters

The first STATCOMs were implemented by two-level voltage source converters. The two-level converter concept was introduced in the 1960s in a single-phase version (Mcmurray, 1971). The schematic of the three-phase two-level converter with step-up transformer is illustrated in Fig. 3 (a). Since these converters have a limited number of voltage levels, they require relatively high switching frequency to deal with the harmonic distortion requirement. The high switching frequency results in high power losses, which affects the converter efficiency. Furthermore, the high voltage slope (dv/dt) imposes significant stress on the insulation of any equipment connected to the a.c. terminal (Sharifabadi et al., 2016).

Moreover, the voltage capability of these converters is limited due to the available semiconductor devices blocking voltages. In fact, even considering the new silicon carbide (SiC) and gallium nitride (GaN) semiconductor devices, the voltage level of this topology is still limited. In this context, a step-up transformer can be connected to the converter output to allow the connection in medium voltage (MV) (Shukla; Nami, 2015). Nevertheless, the

Figure 3 – Schematic of the three-phase two-level voltage source converter: (a) with step-up transformer; (b) with series connection of semiconductor devices.



Source: Elaborated by the author.

transformer increases the equipment costs, reduces the efficiency and increases the weight and volume (Hagiwara; Akagi, 2009; Fang Zheng Peng et al., 1996).

Another solution that increases the voltage capability and dismisses the step-up transformer is the two-level converter with series connection of semiconductor devices. The schematic of the three-phase two-level converter with series connection of semiconductor devices is shown in Fig. 3 (b). Although this approach results in a higher equivalent blocking voltage, some complex practical issues arise, such as voltage equalization among the semiconductor devices and fault-tolerant operation (Shammas; Withanage; Chamund, 2006). Steady and transient state voltage equalization can be performed by snubber structures. These structures increase the converter switching losses (Shukla; Nami, 2015). To increase the fault tolerance capability, a press-pack can be employed, since these devices present short-circuit failure mode (Ladoux; Serbia; Carroll, 2015). Nevertheless, this technology is commercialized just by a few manufacturers due to some patents (Gunturi; Schneider, 2006; Bijlenga et al., 2004). For these reasons, the series connection becomes costly. Moreover, the inherent drawbacks of two-level converters still persist.

1.2.2 Early Multilevel Converters

An alternative to overcome the limitations of two-level topologies in medium/high-voltage systems is the multilevel converter concept. These converters can employ mature semiconductor technologies to achieve high voltage capability (Leon; Vazquez; Franquelo, 2017). Moreover, the multilevel converters have several advantages over the conventional two-level converters, such as (Shukla; Nami, 2015):

- Lower voltage steps (dv/dt), which reduce stresses in the insulation of any equipment connected at the converter output;

- Higher number of levels can be reached, which results in low harmonic content in the output voltage and current;
- Lower common mode voltage;
- Lower switching frequency can be employed, resulting in higher efficiency;
- Higher power density, since the output filters can be reduced or eliminated in some cases.

On the other hand, multilevel converters have also some disadvantages, such as (Shukla; Nami, 2015):

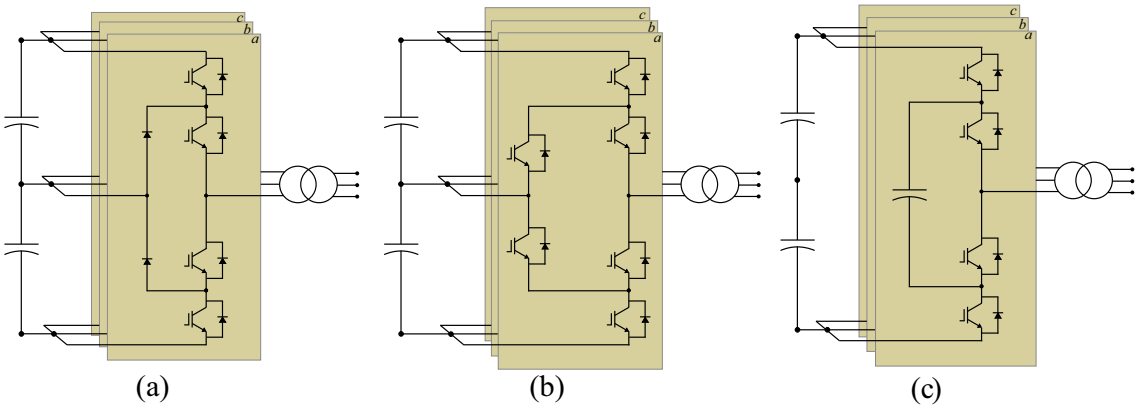
- Higher number of semiconductor devices. As a consequence, a higher number of gate drive circuits are required. This fact may lead to a more expensive and complex system. Nevertheless, part of the cost increase may be offset by the semiconductor devices with lower voltage ratings;
- Higher probability of a system failure due to the higher number of components;
- The increased number of semiconductor devices results in more complicated control;
- Balancing of the capacitors employed as dc voltage sources can be challenging.

Despite these drawbacks, multilevel converters have emerged as the preferred candidates for high-power applications. Furthermore, as the price of power semiconductors and other associated components continue to decrease, the use of multilevel topologies is expected to extend to medium/low power applications as well (Shukla; Nami, 2015).

During the last two decades, several multilevel converter architectures have been introduced (Shukla; Nami, 2015). The most well-known multilevel converters topologies employed in STATCOM applications are: diode clamped multilevel converter (DCMC), active neutral point clamped (ANPC), flying capacitor converter (FC), cascaded H-bridge converter (CHB) and modular multilevel converter (MMC) (Leon; Vazquez; Franquelo, 2017). DCMC, ANPC and FC, considered the early multilevel converters, are discussed in this subsection. CHB and MMC, considered cascaded multilevel converters, are discussed in the next subsection.

The DCMC in a three-level version was introduced by Baker (1979). Furthermore, this converter architecture has been experimentally validated by Nabae, Takahashi and Akagi (1981). The DCMC in the three-level version is commonly known as neutral point clamped (NPC). The schematic of the three-phase NPC is illustrated in Fig. 4 (a). As observed, this converter employs clamping diodes to equalize blocking voltages. Over

Figure 4 – Schematic of the three-phase: (a) NPC converter with a step-up transformer; (b) ANPC converter with a step-up transformer; (c) FC converter with a step-up transformer.



Source: Elaborated by the author.

the years, the NPC was adopted by many manufacturers and was widely employed in medium-voltage electric drives, wind turbines and railway traction systems.

Nevertheless, when more voltage levels are required, the DCMC presents some drawbacks, such as thermal unbalance and mechanical design complexity. These facts limit the number of voltage levels to five or seven in practical applications (Fujii; Schwarzer; De Doncker, 2005; Hagiwara; Akagi, 2009; Sharifabadi et al., 2016). To solve the thermal unbalance of DCMC, the ANPC converter was introduced (Bruckner; Bemet, 2001). The schematic of a three-level ANPC is presented in Fig. 4 (b). As observed, the clamping diodes are replaced by active switches. Consequently, the control of the active switches enables the thermal balance among the converter power switches. For this reason, ANPC converters were applied in several HVDC projects (Sharifabadi et al., 2016).

Another alternative to overcome some of the DCMC drawbacks is the FC converter. The structure of FC is similar to that of the DCMC except that instead of using clamping diodes, the converter uses capacitors in their place (Shukla; Nami, 2015). The FC concept was first introduced in the 1970s by Dickerson and Ottaway (1971). Nevertheless, this topology was practically developed in the 1990s by Meynard and Foch (1992). The schematic of a three-level FC is presented in Fig. 4 (c). In this topology, the additional output levels are achieved through capacitors. When an adequate modulation strategy is employed, the clamping capacitors are automatically balanced and this converter can achieve equalization of losses (Fujii; Schwarzer; De Doncker, 2005; Leon; Vazquez; Franquelo, 2017).

Nevertheless, when more voltage levels are required, voltages at the flying capacitors differ. Thus, capacitors with different ratings must be employed. Consequently, the mechanical design complexity of FC also increases. These facts limit practical applications to low levels in medium voltage systems (Sharifabadi et al., 2016; Leon; Vazquez; Franquelo, 2017).

1.2.3 Cascaded Multilevel Converters

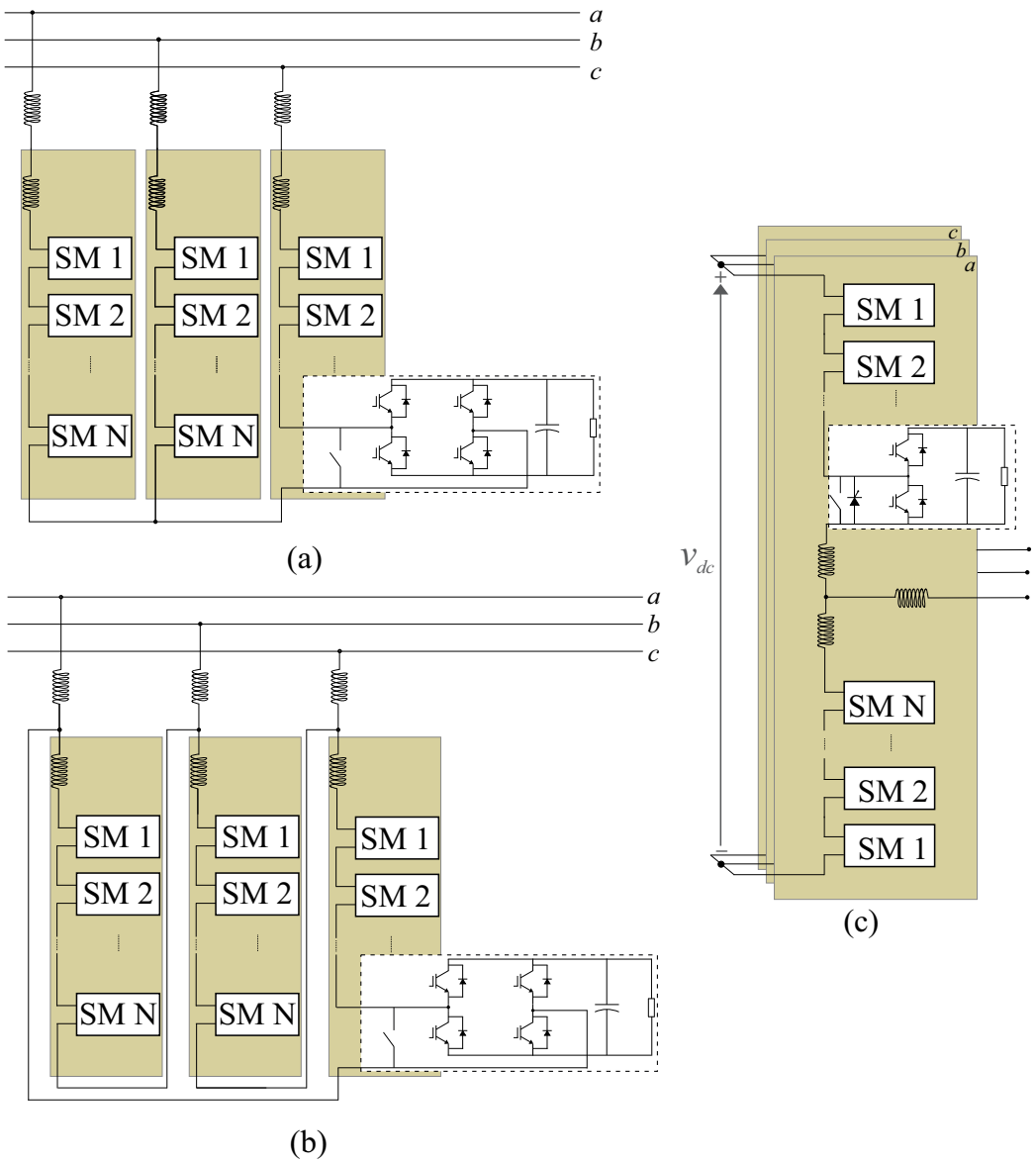
Cascaded multilevel converters are an attractive solution to solve the limitations found in the other multilevel topologies previously discussed. These converters are based on the cascaded connections of submodules (SMs), also called cells, to build up the output voltage. Moreover, the cascaded multilevel converters have several advantages, such as: a higher number of voltage levels that can be reached, since no clamping components are necessary; low switching frequency can be employed, which results in high efficiency; design flexibility, since the voltage rating can be increased by installing more SMs; and redundancy.

The CHB is formed by the series connections of H-bridge SMs, also called full-bridge (FB). The three-phase star and delta-connected CHB topologies — Y-CHB and Δ-CHB, respectively — are illustrated in Fig. 5 (a)-(b). The CHB was introduced in the 1970s for single-phase systems by Mcmurray (1971) and Baker and Bannister (1975). A three-phase CHB based on a star-connected cascaded multilevel converter for variable-speed drives was proposed by Hammond (1994). Usually, the CHB requires one isolated dc source for each SM. Nevertheless, the CHB-STATCOM in star-connected version, which employs only capacitors in the SMs, was proposed by Fang Zheng Peng et al. (1996). Additionally, Fang Zheng Peng et al. (1996) also proposed a three-phase delta-connected CHB-STATCOM.

On the other hand, the MMC is a relatively recent technology that was proposed by Marquardt (2001) and first commercialized in the Transbay cable project in 2010 (Teeuwsen, 2011). Nowadays, this technology has emerged as an attractive solution in medium- and high-voltage STATCOM applications (Pereira et al., 2011; Dekka et al., 2017). Similar to CHB, this converter is formed by the series connections of SMs. As well as in traditional two-level converters, the MMC topology presents a dc-link, while maintaining the important benefits of cascaded multilevel converters. These features have made the MMC attractive and commercial success for HVDC systems. The three-phase MMC topology with half-bridge SMs is illustrated in Fig. 5 (c). Although the first patented MMC presents half-bridge (HB) SMs (Marquardt, 2001), other SM configurations were developed and evaluated over the years (Konstantinou et al., 2015). However, only MMC with HB-SM is considered in this work.

In terms of constructive characteristics, the Y-CHB is the cheapest (Akagi, 2011). Nevertheless, this topology lacks circulating current. For this reason, the capacitor voltage balancing is based on zero-sequence voltage injection. Consequently, Y-CHB is suitable for STATCOM application only when positive sequence currents are injected. However, the ability to control the negative sequence reactive current (necessary for flicker or unbalance compensation) is limited by the voltage rating of the converter, since it can require the injection of a zero sequence voltage equal to the phase voltage (Behrouzian; Bongiorno; De La Parra, 2013).

Figure 5 – Schematic of the three-phase: (a) Y-CHB; (b) Δ-CHB; (c) MMC.



Source: Elaborated by the author.

The second in implementation costs is the Δ-CHB (Akagi, 2011). In addition, this topology presents a circulating current with one degree of freedom, which corresponds to the zero sequence current. Therefore, the capacitor voltage balancing can be performed by the circulating current control, which provides power exchange among the clusters. Consequently, this topology is suitable for STATCOMs employed in flicker compensation, in which positive and negative sequence current compensations are necessary. Nevertheless, this topology has limitations during unbalanced voltage conditions. Indeed, since the circulating current presents only one degree of freedom, the Δ-CHB cannot perform the capacitor voltage balancing when the positive and negative sequence components of the point of common coupling voltage are equal (Behrouzian; Bongiorno; De La Parra, 2013). Under such conditions, the Δ-CHB protection system will trip the converter.

Furthermore, it is noteworthy that the condition of singularity for the Δ-CHB topology is less likely to occur in practice than the condition for Y-CHB, which contributes to the commercial success of Δ-CHB in STATCOM applications. Indeed, the increase of the converter current rating is easier to implement than the increase of the voltage and insulation rating (Cupertino, 2019).

On the other hand, the MMC topology is free from the singularities of CHB topologies. Therefore, despite the MMC topology being more expensive, this topology presents a superior performance in unbalanced conditions, in addition to the advantages of the cascaded multilevel converters (Cupertino, 2019). Therefore, the MMC topology is employed in this work.

Finally, in order to visualize the STATCOM configurations available in the market, Tab. 2 provides a summary of the STATCOM products offered by major manufacturers.

Table 2 – Overview of some STATCOMs commercially available.

Trade Mark	Converter Configuration	ac Voltage Grid	Power Range
VArPro^{TM} (ABB)	Two-level VSC + Transformer	480 V to HV[1]	0.05 - 32 Mvar
PCS 100^{TM} (ABB)	Two-level VSC + Transformer	480 V	0.1 - 4.8 Mvar
PCS 6000^{TM} (ABB)	Three-level VSC (NPC) + Transformer	10 kV to 230 kV	14 - 38 Mvar
SVC Light^{TM} (ABB)	Δ-CHB	69 kV	±640 Mvar
GE-STATCOM^{TM} (GE)	Δ-CHB	132 kV	±100 Mvar
SVC Plus^{TM} (Siemens)	Δ-CHB	HV[1]	±300 Mvar

[1]High Voltage. The manufacturer do not specify the maximum voltage level.

1.3 Modulation Schemes

The modulation strategy defines switching times of the converter power switches. The modulation schemes purpose is to achieve an output voltage that, in average, follows the voltage reference waveform. However, in addition to the desired low-frequency voltage reference, the switching process also produces undesirable higher-order harmonics (Franquelo et al., 2008). Modulation of multilevel converters is also one of the most important focus of researchers since the power losses and the output waveforms quality are strongly dependent on the way to determine the gating signals of the power devices (Leon; Vazquez; Franquelo, 2017). Under such conditions, several modulation schemes have been proposed to multilevel converters.

Specifically for MMC, the energy is no longer stored on its dc-side bus. Instead, the energy is stored in the capacitors placed inside the SM. Due to the converter nature, the currents flow directly through the SMs capacitors and this situation causes voltage

ripple. Consequently, depending on the modulation strategy and its switching frequency, the voltage in the capacitors tends to diverge over time. Thus, the voltage of the capacitors must be balanced to achieve a proper converter operation. This goal is achieved by control of the SMs voltages. Therefore, while for NPC, FC and CHB solutions, the carrier-based pulse-width modulation techniques are used to shape their output voltages and to balance the energy storage of their floating capacitors, in the MMC this is done in more stages (António-Ferreira; Collados-Rodríguez; Gomis-Bellmunt, 2018).

Currently, the most widely used modulation strategies of MMCs can be categorized as multiple-carrier-based modulation, staircase waveform modulation, and space vector modulation (Deng et al., 2020).

The multiple-carrier-based modulation is usually a high-frequency modulation strategy that relies on the application of multiple triangular or saw-tooth carriers stacked symmetrically in the vertical direction or displaced with fixed phase-shift in the horizontal direction named carrier-disposition pulse-width modulation (CD-PWM) or phase-shift carrier pulse-width modulation (PSC-PWM), respectively. As the SMs per arm work in the PWM mode under this condition and the output equivalent switching frequency is high, the multiple carrier-based modulation strategy is suitable for MMC applications with a small number of SMs. The disadvantage of the CD-PWM method is the unbalanced distribution of capacitor voltage fluctuation among SMs. This causes large circulating currents and total harmonic distortion (THD) on the ac side. On the other hand, PSC-PWM produces the natural balancing of SM capacitor voltages as the switching states are similar among all SMs and good output waveform quality is achieved (Deng et al., 2020).

The staircase waveform modulation of MMCs is a kind of low-frequency modulation strategy represented by the nearest-level control (NLC) modulation and the selective harmonic elimination (SHE-PWM) modulation. The NLC modulation is realized by selecting the voltage level nearest to the desired reference' waveform. Compared with the modulation strategies based on multiple carriers, the equivalent switching frequency of the NLC modulation strategy is relatively low, and thus, it is widely used in MMC-based HVDC applications, where hundreds of SMs are employed per arm. Compared with the NLC, the SHE modulation strategy is operated by calculating the switching angles to eliminate specific low-order harmonic components in the output voltage of the MMC. However, the calculation complexity increases drastically with the increase in the voltage levels (Deng et al., 2020).

The modulation schemes based on the space vector method present an important characteristic of reducing the switching losses of semiconductors. However, the space vector methods have limitations when increasing the levels of the converters. For instance, for a cascaded multilevel converter with a number of SMs greater than 20, the space vector schemes are quite complex to implement (Dekka et al., 2017).

Thus, several modulation schemes with different features are defined in the literature. Among these strategies, modulation schemes with fixed and variable switching frequencies are observed, such as PSC-PWM and NLC, respectively. For this reason, the minimum SM voltage control proposed in this work is evaluated with PSC-PWM and NLC.

1.4 STATCOM Trends

Currently, the research efforts on STATCOM have focused on cascaded multilevel converters for medium and high-voltage systems. These researches are motivated by some factors such as the requirements of modern grid codes, system reliability and cost reduction. This section discusses these factors.

1.4.1 Modern Grid Codes Requirements

In addition to controlling positive sequence into the grid, modern grid codes for renewable energy power plants require negative sequence support during voltage sags. As an example, in Germany, the technical requirement for STATCOM connection in the high voltage system imposes positive and negative sequence current injection during unbalanced faults (VDE, 2015). Therefore, the STATCOMs must have these two sequence injection capability (Wijnhoven et al., 2014).

As discussed in Section 1.2.3, Y-CHB and Δ-CHB topologies present a singular operation point during unbalanced conditions (Behrouzian; Bongiorno, 2017; Cupertino, 2019). The converter can be disconnected from the electrical grid if the system reaches this singularity. Nevertheless, the MMC topology can overcome the singularities of CHB topologies. Therefore, recent publications indicate MMC as the most suitable for STATCOMs which are submitted to unbalanced voltage conditions (Cupertino, 2019).

1.4.2 Reliability Requirements

Cascaded converters are composed of a high number of components. Combining a large number of devices can compromise the converter reliability. In this context, the most fragile components must be identified to improve the reliability of this converter. Yang et al. (2011) and Falck et al. (2018) observed that semiconductor devices and capacitors are the converter most susceptible devices. Indeed, 50% of responses to the questionnaire survey of Yang et al. (2011) indicate semiconductor power devices and capacitors as the most fragile components. For this reason, understanding the nature of why and how power electronic products fail is required.

The component failure could be divided into three periods: early failure period, due to manufacturing defects; constant failure period in the useful life of the device; and aging

failure period, due to component degradation processes (wear-out failure) (Richardeau; Pham, 2013; Tu; Yang; Wang, 2019).

In order to increase the converter reliability, the literature suggests the use of redundant SMs to maintain the system in operation, in case of failure in part of the SMs (Farias et al., 2018; Mendonça et al., 2020b; Júnior et al., 2020). For wear-out failure, optimizing the design of components and the use of control algorithms can improve the system reliability and components lifetime (Wang; Liserre; Blaabjerg, 2013).

For the HVDC application, Liu et al. (2016) and Zhang et al. (2017b) calculate the static lifetime (LT) of the semiconductor devices, without presenting the system-level reliability analyses. On the other hand, Zhang et al. (2017a) present the system-level reliability only for semiconductor devices, without including the capacitors in the analyses. More broadly, Xu et al. (2019) and Zhang et al. (2020) consider capacitors and semiconductor devices in their analyses and evaluate the system-level reliability. Nevertheless, these references consider only a specific converter design and wear-out failure of bondwire junctions.

For the STATCOM application, Farias et al. (2017) evaluate the static lifetime of the semiconductor devices. Sousa et al. (2018) and Farias et al. (2020) also include the system-level reliability analysis. Moreover, Sousa et al. (2018) evaluate the modulation strategies reliability effect considering a specific MMC-STATCOM design. Gherard et al. (2020) present a methodology for designing and performing cost-optimization of MMC-based energy storage and static synchronous compensators. Although reliability analyses are included, the focus of this work is on the battery energy storage system and a single modulation strategy is considered. Farias et al. (2020) introduce a reliability-oriented design methodology, in which semiconductor devices with different blocking voltage and forward current capabilities are considered. However, the analyses are performed disregarding the wear-out of the capacitor and only a modulation strategy is considered. Besides, modulation strategies can require different energy storage requirements (Hahn et al., 2018) and, thus, affect the converter design in terms of SM capacitance.

In the long-term lifetime computation, a rainflow counting algorithm is usually employed for the thermal cycling classification. The rainflow was first created for fatigue stress/strain computation in mechanical applications (Chung et al., 2015). For this reason, the heating time information is unavailable in the output of the rainflow function. Most of the works employing rainflow for the lifetime computation of semiconductor devices consider the heating time as half of the cycle time given by this function. This approach is based on the principle that heating and cooling time are equal, which is not always true. Nevertheless, the heating time affects the fatigue computation in power device lifetime estimation (Antonopoulos et al., 2020).

Therefore, this work analyzes the role of modulation strategies and semiconductor

devices blocking voltage on the lifetime of a MMC-STATCOM to perform a complete evaluation of the proposal. Besides, the effect of semiconductor devices and capacitors is considered. Moreover, a modified rainflow that computes the effective heating time is considered in the lifetime computation.

1.4.3 Cost Reduction

The converter cost is directly related to the capital expenditure (CAPEX) and operational expenditure (OPEX). CAPEX is mainly related to the converter component costs: capacitors, magnetic devices, semiconductor devices, controllers, printed circuit boards, cooling systems, among others (Siddique et al., 2016). Therefore, efforts are made to ensure CAPEX reduction in the initial phase of the converter design. Indeed, some approaches aim to reduce the number of components, such as capacitors, sensors, switches and their drive circuits.

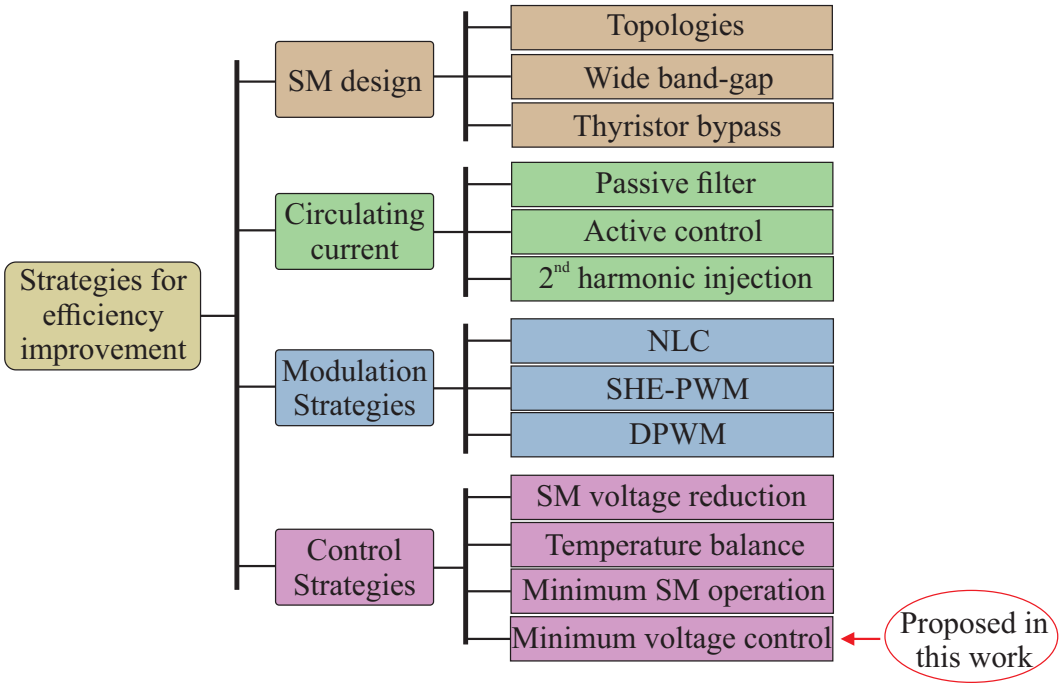
For instance, the design of the MMC operating with third harmonic voltage injection can reduce the SM capacitances and the number of SMs required in the converter (Ilves et al., 2014). Consequently, the number of sensors is reduced which is helpful in the cost saving of the system. Moreover, Farivar, Agelidis and Hredzak (2014) propose a capacitor voltage estimation for multilevel converters where dc voltage sensors are replaced by a single sensor at the ac-side. Silva, Vieira and Rech (2018) also propose the sensor reduction addressed for other cascaded converters through capacitor voltage observers. Prabaharan and Palanisamy (2017) compare the requirement of total components for different cascaded multilevel converters to achieve the same voltage level. Saif et al. (2018) show that for medium voltage three-phase Y-CHB based STATCOM, a larger number of levels in the converter can be employed aiming to reduce the semiconductor costs.

On the other hand, OPEX is related to the converter power losses, maintenance and faulty device replacement (Alvarez et al., 2016; Tu; Yang; Wang, 2019). Since STATCOMs are hot-standby devices, the converter efficiency and non-scheduled maintenance are factors that affect the benefit-cost ratio. These factors drive research that aims to increase the converter reliability and efficiency, which leads to a reduction in OPEX.

Many researches present solutions to increase the efficiency of converters for STATCOM applications. As discussed by Mendonça et al. (2020a), the strategies for losses reduction can be classified into four groups: modulation schemes, SM design, circulating current and control strategies. These groups are shown in Fig. 6.

Over the years, many SM configurations were developed for cascaded topologies (Konstantinou et al., 2015). Most of these configurations focus on power losses reduction and fault tolerance improvement. The hybrid solution with half-bridge and full-bridge SMs was already been discussed as a dc fault-tolerant solution with minimal power losses (Lin

Figure 6 – Overview of the proposed strategies for losses reduction.



Source: Adapted from Mendonça et al. (2020a).

et al., 2016). Moreover, the use of wide band-gap devices has been discussed due to the significant improvement in the efficiency of the converter when high switching frequencies are employed (Peftitsis et al., 2012). In addition, topologies with a bypass branch formed by thyristors or diodes in series are used in MMC topologies to reduce power losses resulting from obtaining dc fault tolerance (Judge et al., 2019).

Regarding the circulating current researches, passive and active methods were proposed to reduce current stress, and consequently, power losses (Tu; Xu; Xu, 2011; Jacobson et al., 2010; Li et al., 2018). Moreover, the losses optimization by injection of second-order harmonic into the arm current of the MMC topology has been proposed (Yang et al., 2018). As mentioned before, the Y-CHB topology lacks circulating current. Therefore, these strategies are inapplicable to this topology.

Modulation scheme approaches are usually related to reducing converter switching losses. Nearest-level control, selective harmonic elimination modulation and discontinuous modulation (DPWM) are some of the strategies proposed for efficiency improvement (Hassanpoor; Norrga; Nami, 2015; Moranchel et al., 2016; Picas et al., 2015). Although the modulation schemes are related to the converter software, these approaches can affect the SM design. For instance, NLC improves SM efficiency. However, this modulation scheme requires higher SM capacitance (Hahn et al., 2018).

Regarding the control strategies, Farias et al. (2018) proposes the reduction of voltage in each SM with redundant SMs. This strategy also reduces the power losses in the

SM components. Furthermore, a converter temperature balance is presented as a solution to reduce the conduction and switching losses of the converter (Sangwongwanich et al., 2016). Moreover, the use of the own SM bypass structures to reduce power losses based on the minimum SM control operation principle was proposed (Mendonça et al., 2020a). These strategies can be employed in both MMC and CHB topologies. In addition, Mendonça et al. (2020a) proposes a minimum SM operation control to reduce power losses. The main principle of this strategy is to bypass SM from the MMC, according to the reactive power reference.

As observed, the majority of strategies for power losses reduction require hardware modification. Nevertheless, strategies without hardware modification requirements can be interesting to already installed systems. Moreover, most of these works disregard the SM voltage impact on the SM capacitor lifetime.

Therefore, this work proposes a novel control strategy that can also be applied to these systems: minimum SM voltage control. This strategy is based on an adaptive dc-side voltage technique which controls the SM voltage reference according to the minimum voltage required in each converter operation condition. Consequently, the losses and stress on SM components can be reduced, improving reliability.

1.5 Purpose and Contributions

The STATCOMs present interesting operation features. As discussed in previous sections, the most recent research efforts in STATCOMs aim to improve the efficiency and reliability of these converters. In addition, according to the modern grid codes requirements, the STATCOM must have positive and negative sequence injection capabilities. In this context, MMC topology is the most interesting cascaded topology for STATCOM application.

This work proposes a novel control strategy based on a variable dc-side voltage technique that controls the SM voltage reference according to the minimum voltage required in each converter operation condition. Consequently, the stress on SM components can be reduced, improving reliability and reducing losses.

In addition, a huge variety of modulation strategies can be employed in MMC-STATCOM. Among these strategies, modulation schemes with fixed or variable switching frequencies can be found. For this reason, the control strategy proposed is evaluated with two distinct modulation strategies: PSC-PWM, with fixed switching frequency, and NLC, with variable switching frequency.

Based on the general purpose, the following topics are approached in this work:

1. *Control tuning of MMC-STATCOM*: this topic proposes a control tuning methodology

to compute the gain of the controllers for an MMC-based STATCOM. The control strategy adopted in this work is composed of four main objectives: global energy control, output current control, circulating current control and capacitor voltage balancing control.

2. *Design of MMC-STATCOM*: this topic proposes eight different designs, considering the same rated power and grid voltage. Nevertheless, the designs consider four different semiconductor blocking voltages, leading to different numbers of SMs. Moreover, for each semiconductor blocking voltage is computed the MMC-STATCOM design with two different modulation strategies (PSC-PWM and NLC). The objective of these case studies is to evaluate the proposal of this work with different SM numbers and modulation strategies with fixed and variable switching frequencies. Besides, the design is focused on providing fair conditions for the reliability analysis.

3. *Minimum SM voltage control and losses reduction*: this topic proposes a variables dc-side voltage control strategy applied to an MMC-STATCOM. The proposed technique aims to improve the converter reliability and reduce the losses by controlling the SM voltage reference according to the minimum voltage required in each STATCOM operation condition. In this topic, the losses reduction is validated by modeling the power losses of an MMC-STATCOM.

4. *Minimum SM voltage control and reliability improvement*: this topic proposes the validation of minimum voltage control in reliability improvement. The wear-out failure methodology is presented as a figure of merit for reliability evaluation. Moreover, a modified rainflow that computes the effective heating time is introduced. Eight MMC-STATCOM case studies with different semiconductor blocking voltages and modulation strategies with fixed and variable switching frequencies are considered.

5. *Experimental validation*: this topic proposes the experimental validation of the control tuning methodology and minimum SM voltage control in an MMC-STATCOM setup. For this purpose, initially, a full-bridge submodule for cascaded topologies was developed in cooperation with the research group GESEP-UFV. Nevertheless, due to the opportunity to perform a guest Ph.D. period at Aalborg University, Denmark, the controls and minimum SM voltage control were implemented and validated in an MMC experimental setup in cooperation with the research group CROSBAT.

1.6 Organization of the Ph.D Thesis

This Ph.D thesis is organized in 5 chapters, as follows:

- Chapter 1 presents the motivations and objectives.

- Chapter 2 describes the modeling, control and design of the MMC-STATCOM. Besides, the converter topology, control strategy and components design are introduced. The control tuning proposal is also presented.
- Chapter 3 introduces the minimum SM voltage control concept. The minimum SM voltage control potential of power losses reduction and experimental validation is also presented.
- Chapter 4 presents the methodology of the wear-out prediction procedure for semiconductor devices and capacitors. Moreover, the reliability improvement of minimum SM voltage control is evaluated.
- Finally, Chapter 5 presents the conclusions and the future developments of this work.

1.7 List of Publications

The results produced in this work originated the following papers.

1.7.1 Published Journal Papers

- R.O. de Sousa, A. F. Cupertino, L. M. F. Morais, H. A. Pereira, "Minimum voltage control for reliability improvement in modular multilevel cascade converters-based STATCOM". Microelectronics Reliability, ISSN 0026-2714, Volume 110, 2020.
- R.O. de Sousa, A. F. Cupertino, L. M. F. Morais, H. A. Pereira, "Wear-Out Failure Analysis of Modular Multilevel Cascade Converters-based STATCOM: The Role of Modulation Strategy and IGBT Blocking Voltage". Microelectronics Reliability, ISSN 0026-2714, Volume 128, 2022.

1.7.2 Published Book Chapter

- D. C. Mendonça, R. O. de Sousa, J. V. M. Farias, H. A. Pereira and S. I. Seleme Jr, A. F. Cupertino, "Multilevel Converter for Static Synchronous Compensators: State-of-art, Applications and Trends". Power Electronics for Green Energy Conversion (eds M.S. Bhaskar, N. Gupta, S. Padmanaban, J.B. Holm-Nielsen and U. Subramaniam), Wiley, 2022.

1.7.3 Submitted Journal Papers (under review)

- R.O. de Sousa, A. F. Cupertino, J. H. D. G. Pinto, L. M. F. Morais, H. A. Pereira and R. Teodorescu, "Control Tuning of Modular Multilevel Converters-based STATCOM". IEEE Transactions on Power Delivery.

- R.O. de Sousa, A. F. Cupertino, L. M. F. Morais, H. A. Pereira and R. Teodorescu, "Experimental validation and reliability analyses of minimum voltage control in modular multilevel converter-based STATCOM". IEEE Transactions on Industrial Electronics.

1.7.4 Published in Journal Papers: In cooperation with the research group

- J. V. G.França, J. H. D. G. Pinto, D. C. Mendonça, J. V. M. Faria, R. O. de Sousa, H. A. Pereira; S. I. Seleme Jr., A. F. Cupertino, "Development of a test platform for electronic power converters". Revista Eletrônica de Potência, 2022.

1.7.5 Published Conference Papers: In cooperation with the research group

- R. O. de Sousa, W. C. S. Amorim, D. C. Mendonça, A. F. Cupertino, L. M. F. Morais and H. A. Pereira, "Thermal Stress Evaluation of a Multifunctional Modular Multilevel Converter – STATCOM Operating as Active Filter". 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 2019, pp. 1-6.

- R. O. de Sousa, A. Kulkarni, M. Hansen, J. Midtgaard, R. Teodorescu, "Wireless control of Smart Battery Systems". 2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG 2022), Kiel, Germany, 2022.

1.7.6 Accepted for Publication Journal Papers: In cooperation with the research group

- R. O. de Sousa, J. V. M. Farias, A. F. Cupertino and H. A. Pereira, "Modulation Strategy Impact on the Energy Storage Requirements of Modular Multilevel Converter Based STATCOM". Journal of Control, Automation and Electrical Systems, 2022.

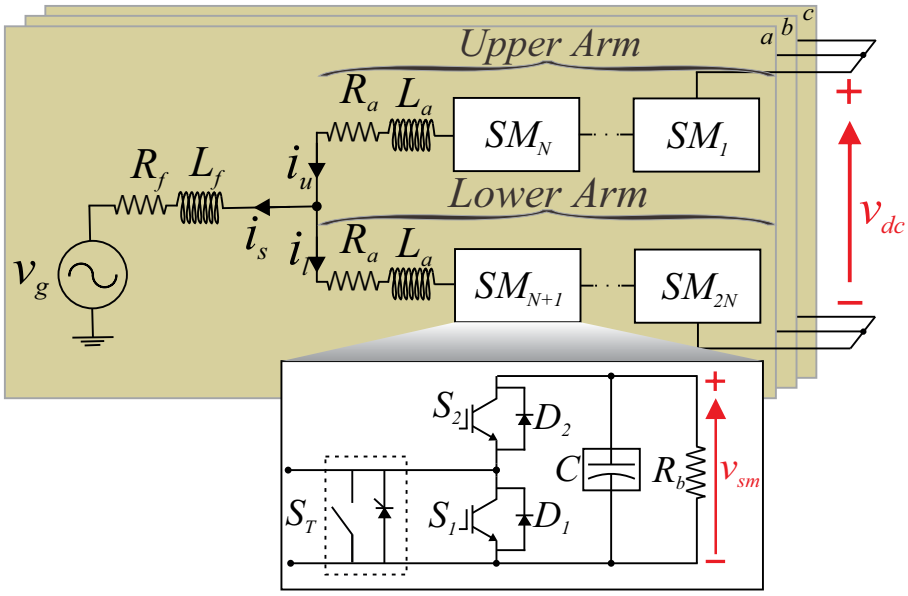
2 Modeling, Control and Design

This chapter describes the modeling, control and design of the MMC-STATCOM. First of all, the converter topology and basic dynamic equations are introduced. Then, the control strategies, control tuning and modulation strategies are presented. In addition, the dc-side voltage and components design considerations are presented. Lastly, the control tuning and design are evaluated through simulation and experimental analyses.

2.1 Topology

The MMC-STATCOM is illustrated in Fig. 7. This topology is composed of N SMs per arm and each SM contains four semiconductor devices (S_1, S_2, D_1 and D_2) and capacitance C. R_b is the bleed resistor to perform the discharge of the SM capacitors when the converter shuts down. Generally, a switch S_T in parallel with the SM is used to bypass it in case of failures (Gemmell et al., 2008). The arm inductance is represented by L_a, which reduces the high-order harmonics in the circulating current and limits the fault currents (Harnefors et al., 2013). R_a is the resistance of the arm inductors. The converter is connected to the grid through a three-phase isolation transformer with inductance L_f and resistance R_f. Moreover, i_u and i_l are the upper and lower arm currents, respectively. Finally, v_g is the grid voltage and i_s is the output current of the MMC-STATCOM. v_{sm} and v_{dc} are the SM and dc-side voltages, respectively.

Figure 7 – Schematic of the MMC-STATCOM.

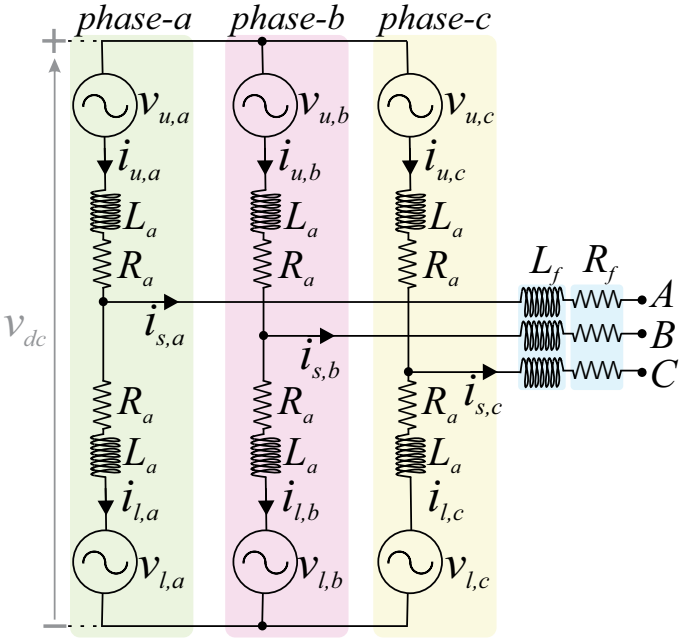


Source: Elaborated by the author.

2.2 MMC Basic Operating Principles

The mathematical modeling presented in this section intends to describe the MMC-STATCOM dynamics. Moreover, the MMC modeling considers perfectly balanced SM capacitor voltages and neglects the switching harmonics. Thus, the arm-average model of an MMC-STATCOM, illustrated in Fig. 8, is considered. In this figure, the arm voltages are represented by voltage sources.

Figure 8 – Arm-average model of an MMC-STATCOM.



Source: Elaborated by the author.

Since the topology presents no dc-side current, the sum of upper and lower arm currents must be zero (Sharifabadi et al., 2016):

$$\sum_{n=1}^{3} i_{u,n} = \sum_{n=1}^{3} i_{l,n} = 0, \tag{2.1}$$

where n is the phase a, b or c, $i_{u,n}$ is the upper arm current of *phase-n* and $i_{l,n}$ is lower arm current of *phase-n*.

The output currents can be calculated as follows (Harnefors et al., 2013):

$$i_{s,n} = i_{u,n} - i_{l,n}. \tag{2.2}$$

where n is the phase a, b or c, $i_{s,n}$ is the output current of *phase-n*. The circulating current is given by:

$$i_{z,n} = \frac{i_{u,n} + i_{l,n}}{2}. \tag{2.3}$$

where n is the phase a, b or c, $i_{z,n}$ is the circulating current of *phase-n*. The arm currents can be written as follows (Sharifabadi et al., 2016):

$$\begin{cases} i_{u,n} = \frac{i_{s,n}}{2} + i_{z,n}, \\ i_{l,n} = -\frac{i_{s,n}}{2} + i_{z,n}. \end{cases} \tag{2.4}$$

Considering Eq. (2.1) and Eq. (2.4), the sum of the phase circulating currents is given by:

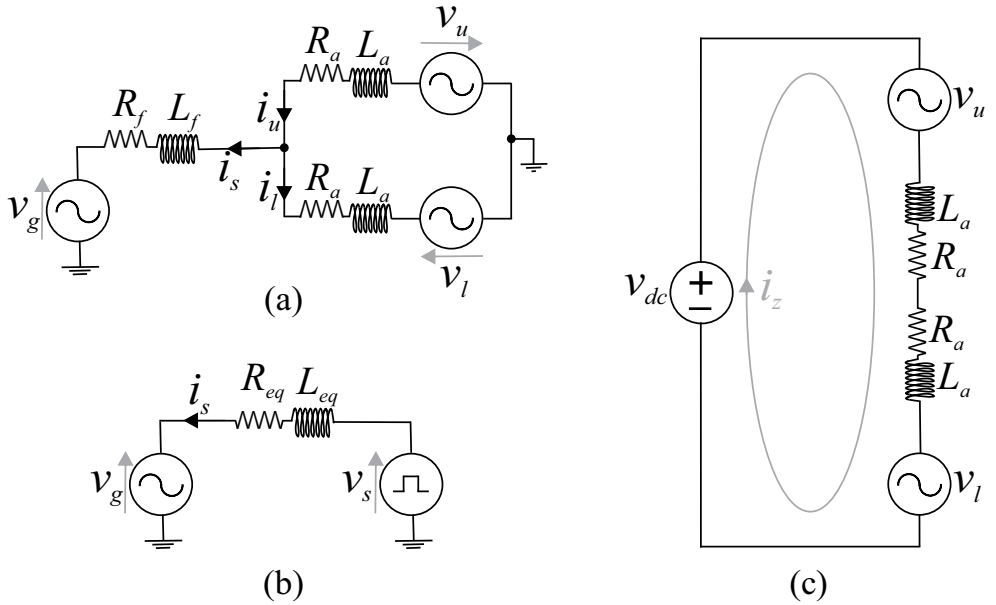
$$\sum_{n=1}^{3} i_{z,n} = 0, \tag{2.5}$$

where n is the phase a, b or c.

2.2.1 Dynamic Modeling

The single-phase equivalent circuit that describes the behavior of the output current per phase is shown in Fig. 9 (a).

Figure 9 – Single-phase equivalent circuit defining (a) the output current; (b) the MMC output voltage; and (c) the circulating current.



Source: Elaborated by the author.

Based on Millman's theorem [1] (Millman, 1940), the following relationship is obtained:

$$v_g = v_s - \left(\frac{L_a}{2} + L_f\right)\frac{di_s}{dt} - \left(\frac{R_a}{2} + R_f\right)i_s, \tag{2.6}$$

[1] According to (Millman, 1940), the association of voltage sources connected in parallel can be reduced to just one equivalent source. The same conclusion can be obtained through Thevenin's theorem.

where v_s is the output voltage of the converter which drives the output current. The equivalent inductance and resistance are $L_{eq} = L_a/2+L_f$ and $R_{eq} = R_a/2+R_f$, respectively. Fig. 9 (b) shows a simplified circuit of the MMC connected to the grid. The output voltage can be expressed by:

$$v_s = \frac{1}{2}\left(-v_u + v_l\right). \tag{2.7}$$

Figure 9 (c) illustrates the equivalent circuit that describes the behavior of the circulating current per phase. The following relationship is obtained:

$$\frac{v_{dc}}{2} - v_z = L_a\frac{di_z}{dt} + R_a i_z, \tag{2.8}$$

where v_z is the internal voltage per phase, which is given by:

$$v_z = \frac{1}{2}\left(v_u + v_l\right). \tag{2.9}$$

2.2.2 Instantaneous Power

The instantaneous active power of each arm is:

$$\begin{cases} p_u = v_u i_u, \\ p_l = v_l i_l. \end{cases} \tag{2.10}$$

The upper and lower arm voltages can be obtained through Eq. (2.9) and Eq. (2.7), as follows:

$$\begin{cases} v_u = v_z - v_s, \\ v_l = v_z + v_s. \end{cases} \tag{2.11}$$

Substituting Eq. (2.11) and Eq. (2.4) into Eq.(2.10), yields:

$$\begin{cases} p_u = v_z\frac{i_s}{2} - v_s\frac{i_s}{2} + v_z i_z - v_s i_z, \\ p_l = -v_z\frac{i_s}{2} - v_s\frac{i_s}{2} + v_z i_z + v_s i_z. \end{cases} \tag{2.12}$$

For sake of simplification, $v_z \approx \frac{v_{dc}}{2}$ is considered, i.e., R_a is neglected and steady-state conditions are assumed (Sharifabadi et al., 2016). Thus, Eq. (2.12) can be rewritten as follows:

$$\begin{cases} p_u \approx \frac{v_{dc}}{2}\frac{i_s}{2} - v_s\frac{i_s}{2} + \frac{v_{dc}}{2} i_z - v_s i_z, \\ p_l \approx -\frac{v_{dc}}{2}\frac{i_s}{2} - v_s\frac{i_s}{2} + \frac{v_{dc}}{2} i_z + v_s i_z. \end{cases} \tag{2.13}$$

Each power term in Eq. (2.13) has a different physical meaning. Different colors are employed in Eq. (2.13) to highlight these terms. The following conclusions can be stated:

1. The term $\frac{v_{dc}}{2}\frac{i_s}{2}$ represents the fundamental frequency oscillating power. This product results in a fundamental frequency ripple in the SM capacitor voltage. Moreover, this term presents opposite signals in the lower and upper arms. Therefore, this power oscillation is not observed at the converter ac terminals.

2. The term $v_s\frac{i_s}{2}$ represents the average value and the second-harmonic power oscillation. Considering v_s and i_s sinusoidal waves, the average value represents the active power transferred from the SMs to the grid. This value must be null in the STATCOM application. The oscillating component represents the second-harmonic ripple in the SM capacitor voltage.

3. The parcels containing the circulating current, i_z, are related to energy exchange among phases and between arms. As previously presented in Eq. (2.5), the circulating current of a particular phase can affect the others. Indeed:

$$i_{z,c} = -i_{z,a} - i_{z,b}. \tag{2.14}$$

   Thus, the term $\frac{v_{dc}}{2}i_z$ indicates that an average value in this circulating current component can perform the energy exchange among the converter phases. Indeed, the sum of the power transferred among the three phases must be zero.

4. The term $v_s i_z$ indicates that a fundamental frequency circulating current leads to a non-zero instantaneous power in the arm. Moreover, these terms present opposite signals in the upper and lower arms. Therefore, a fundamental frequency circulating current can exchange energy between the upper and lower arms.

The three-phase instantaneous active power of the converter is calculated by the sum of the instantaneous active power of all arms, as follows:

$$p_{3n} = p_{u,a} + p_{l,a} + p_{u,b} + p_{l,b} + p_{u,c} + p_{l,c}. \tag{2.15}$$

Considering Eq.(2.13) for each arm, the three-phase instantaneous active power is given by:

$$p_{3n} = v_{dc}(i_{z,a} + i_{z,b} + i_{z,c}) - v_{s,a}i_{s,a} - v_{s,b}i_{s,b} - v_{s,c}i_{s,c}. \tag{2.16}$$

Replacing Eq. (2.5) in Eq. (2.16), the following is obtained:

$$p_{3n} = -v_{s,a}i_{s,a} - v_{s,b}i_{s,b} - v_{s,c}i_{s,c}. \tag{2.17}$$

Therefore, p_{3n} can present an average value and a second-harmonic power oscillation. Under balanced conditions, the second-order oscillations cancel each other. Thus, only the average power component remains in p_{3n}, as expected for three-phase converters. In an MMC-STATCOM, the average power component in p_{3n} is controlled to provide the converter losses and keep constant the converter energy storage.

2.3 Control Strategy

The control objectives of a typical MMC-STATCOM are based on the control of the global energy of the converter, control of the power required to supply the grid and internal losses, control of the circulating current and balancing of the capacitor voltages.

The power is controlled through output current control. This control loop is the main controller of the converter. If a two-level converter was considered, the output voltage reference, which is determined by the output current controller, could be forwarded directly to the pulse width modulator to produce the gate signals. Nevertheless, the higher complexity of the MMC-STATCOM requires another control stage: the internal control. This control stage is composed of the circulating current control and of the sum of the capacitor voltages. The normalized output signals of these controls are the insertion indexes, which go to the modulation and submodule balancing stage (Sharifabadi et al., 2016).

The internal control must ensure that the sum of the capacitor voltages converge to their desired common mean value, v_{dc}. This can be called voltage control. The core of this control is the selection of the insertion indexes (Sharifabadi et al., 2016). To compute the insertion indexes of the converter, the inserted voltages must be normalized. The inserted voltages in upper and lower arms can be approximated by (Sharifabadi et al., 2016; Hagiwara; Maeda; Akagi, 2011):

$$\begin{cases} v_u = v_z^* - v_s^*, \\ v_l = v_z^* + v_s^*, \end{cases} \tag{2.18}$$

where v_z^* and v_s^* are the internal voltage reference and the output voltage reference, respectively.

The normalization of the inserted voltages is what differs the voltage control schemes. The most popular schemes are: direct voltage control, closed-loop voltage control and open-loop voltage control.

In the direct voltage control, the normalization of the insertion indexes is performed by the sum of the SM voltage references, Nv_{sm}^*. Accordingly:

$$n_u = \frac{v_z^* - v_s^*}{Nv_{sm}^*}, \tag{2.19}$$

$$n_l = \frac{v_z^* + v_s^*}{N v_{sm}^*}. \tag{2.20}$$

The direct voltage control inherently gives an asymptotically stable system (Harnefors et al., 2013). This means that the arm voltages reach the reference value without requiring an energy balancing control (Mendonça, 2021). Moreover, this scheme has low computational complexity. Nevertheless, parasitic components appear in the output and internal voltages. This effect can be suppressed by the output and circulating current controllers (Sharifabadi et al., 2016).

In the closed-loop voltage control, the normalization of the insertion indexes is performed by the measured sum of the capacitor voltages (Antonopoulos; Angquist; Nee, 2009). Accordingly:

$$n_u = \frac{v_z^* - v_s^*}{v_{cu}^\Sigma}, \tag{2.21}$$

$$n_l = \frac{v_z^* + v_s^*}{v_{cl}^\Sigma}, \tag{2.22}$$

where v_{cu}^Σ and v_{cl}^Σ are the measured sum of the capacitor voltages of the upper and lower arm, respectively. The parasitic voltage components are absent in this control scheme. However, an energy balancing control is required to obtain an asymptotically stable system (Sharifabadi et al., 2016).

In the open-loop voltage control, the normalization of the insertion indexes is performed by the estimation of the sum of the capacitor voltages (Angquist et al., 2011). Accordingly:

$$n_u = \frac{v_z^* - v_s^*}{\tilde{v}_{cu}^\Sigma}, \tag{2.23}$$

$$n_l = \frac{v_z^* + v_s^*}{\tilde{v}_{cl}^\Sigma}, \tag{2.24}$$

where $\tilde{v}_{cu}^\Sigma$ and $\tilde{v}_{cl}^\Sigma$ are the estimation of the sum of the capacitor voltages of the upper and lower arm, respectively. This scheme is asymptotically stable (Antonopoulos et al., 2014). Moreover, none or just small parasitic voltage components appear (Sharifabadi et al., 2016).

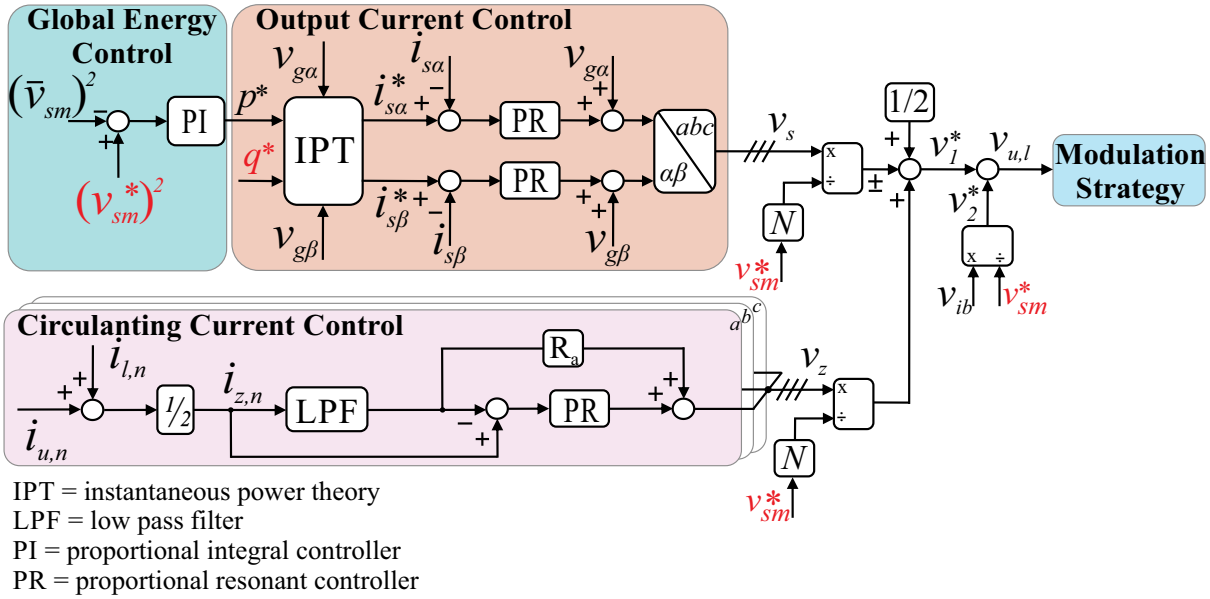
The circulating current control is intimately related to the voltage control. Thus, the circulating current controller must be adapted to suit the voltage control scheme chosen (Sharifabadi et al., 2016). Among the schemes presented, the simplest is the direct

voltage control, which dispenses energy balancing control and ripple estimation. Therefore, direct voltage control is considered in this work.

The control strategy employed is illustrated in Fig. 10. The output current control is responsible for the reactive power exchanged with the grid. This control is implemented in a stationary reference frame ($\alpha\beta$). Additionally, the active power reference of the output current control is generated by the global energy control. This control is responsible to supply converter internal losses. This external loop is inspired by the approach of Pereira et al. (2015) and controls the square of the average voltage ($\overline{v}_{sm}$) of all SM voltages ($v_{sm,i}$). The average voltage is given as follows:

$$\overline{v}_{sm} = \frac{1}{6N} \sum_{i=1}^{6N} v_{sm,i}. \tag{2.25}$$

Figure 10 – Control strategy for MMC-STATCOM: global energy control, output current control and circulating current control.



Source: Elaborated by the author.

The SM voltage reference is important to avoid overmodulation. This reference is given by (Fujii; Schwarzer; De Doncker, 2005):

$$v_{sm}^{*} = \frac{v_{dc}}{N}. \tag{2.26}$$

The global energy control employs a proportional-integral (PI) controller to obtain the active power reference (p^{*}) that needs to flow into the converter. The active and reactive power references (p^{*} and q^{*}) and the stationary components of the grid voltage ($v_{g\alpha}$ and $v_{g\beta}$) are employed to compute the output current references by instantaneous power theory (IPT) (Akagi; Watanabe; Aredes, 2017), as follows:

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \frac{1}{v^2_{g\alpha} + v^2_{g\beta}} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} p^* \\ q^* \end{bmatrix}. \tag{2.27}$$

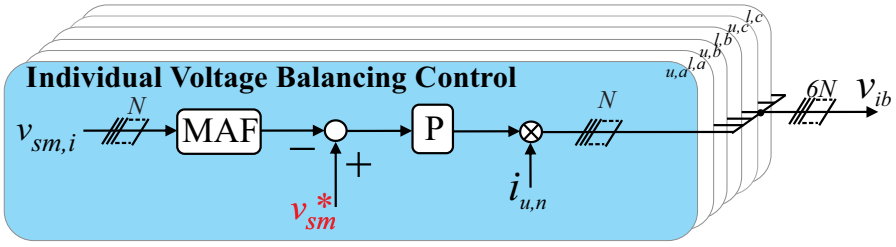
In order to track the current reference, two proportional-resonant (PR) controllers tuned to the fundamental frequency are used in the output current control. The PR output is added to the stationary components of the grid voltage.

The circulating current control composes the internal control of MMC-STATCOM. The circulating current control is responsible for reducing the harmonic content in the circulating current to damp the converter dynamic response (Harnefors et al., 2013; Moon et al., 2013). This control is implemented per phase. Moreover, a Butterworth second-order filter (LPF) is employed to remove the dc component of i_z (Harnefors et al., 2013). The PR controller is added to this control to compensate for the second-order harmonic component that appears in the circulating current (Xu et al., 2016).

2.3.1 Modulation Strategies and Balancing Control

Due to the different features of modulation schemes, two popular modulation strategies are analyzed: PSC-PWM, with fixed switching frequency, and NLC, with variable switching frequency. Moreover, the MMC-STATCOM requires voltage balancing control. For NLC, the cell tolerance band (CTB) algorithm is employed to perform the voltage balancing control for this strategy. For PSC-PWM, the individual voltage balancing control, illustrated in Fig. 11, is employed (Akagi; Inoue; Yoshii, 2007). This control is responsible to maintain the capacitor voltages following the reference v^*_{sm}. For this purpose, a moving average filter (MAF) is employed in $v_{sm,i}$ to attenuate the capacitor voltage ripple and to improve the individual balancing performance (Sasongko et al., 2016). In addition, a proportional controller is employed. Moreover, the controller output is multiplied by the arm current to identify the direction and amplitude of the current (Maharjan; Inoue; Akagi, 2008).

Figure 11 – Individual voltage balancing control.



MAF = moving average filter

Source: Elaborated by the author.

Finally, the normalized reference signals per phase are given by:

$$v_{u,n} = \frac{v_{ib}^*}{v_{sm}^*} + \frac{v_z^*}{N v_{sm}^*} - \frac{v_s^*}{N v_{sm}^*} + \frac{1}{2},$$
$$v_{l,n} = \frac{v_{ib}^*}{v_{sm}^*} + \frac{v_z^*}{N v_{sm}^*} + \frac{v_s^*}{N v_{sm}^*} + \frac{1}{2}, \tag{2.28}$$

where v_{ib}, v_z^* and v_s^* are the output references of individual voltage balancing control, circulating current control and output current control, respectively. Moreover, v_z^*, v_s^* and v_{ib}^* are given in volts. v_{ib}^* is null when NLC is considered.

The schematic of the PSC-PWM strategy is shown in Fig. 12. For PSC-PWM, the MMC SMs are controlled independently, each one by independent carriers (Debnath et al., 2015). The N arm carriers are equally phase-shifted inside half period with a phase displacement between upper and lower arms. The angular displacement of the carriers is calculated as follows:

$$\begin{cases} \theta_{u,n} = \pi \left(\frac{n-1}{N}\right), \\ \theta_{l,n} = \theta_{u,n} + \beta, \end{cases} \tag{2.29}$$

where $n = 1, 2, ..., N$. The angle β indicates the phase displacement between the carrier waveforms in the upper and lower arms. Regarding this displacement, two different modulation strategies can be chosen in terms of the desired harmonic performance (Ilves et al., 2015). The first one is $(N + 1)$-level modulation, where the displacement between the upper and lower arm is given by:

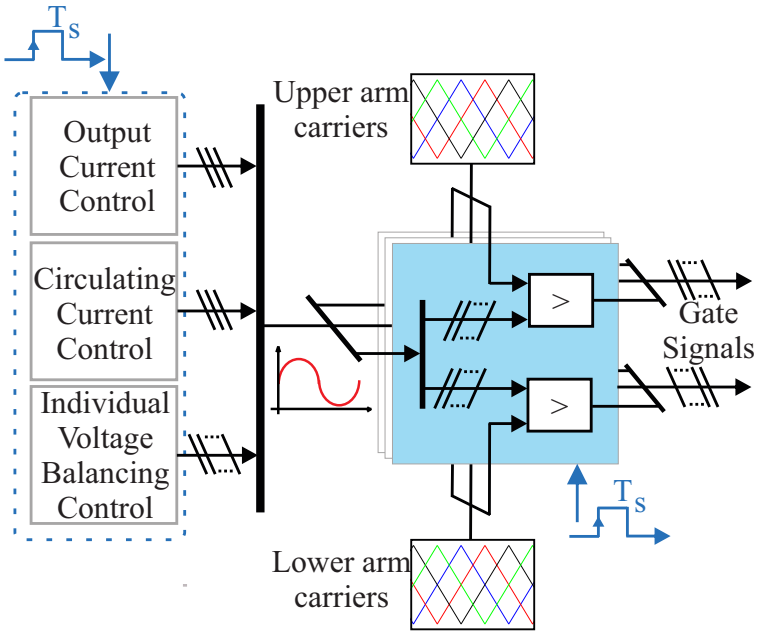
$$\beta = \pi. \tag{2.30}$$

The second method is the $(2N + 1)$-level modulation, where the displacement between the upper and lower arm is given by:

$$\begin{cases} \beta = 0 \quad \text{, if N is odd ,} \\ \beta = \frac{\pi}{N} \quad \text{, if N is even.} \end{cases} \tag{2.31}$$

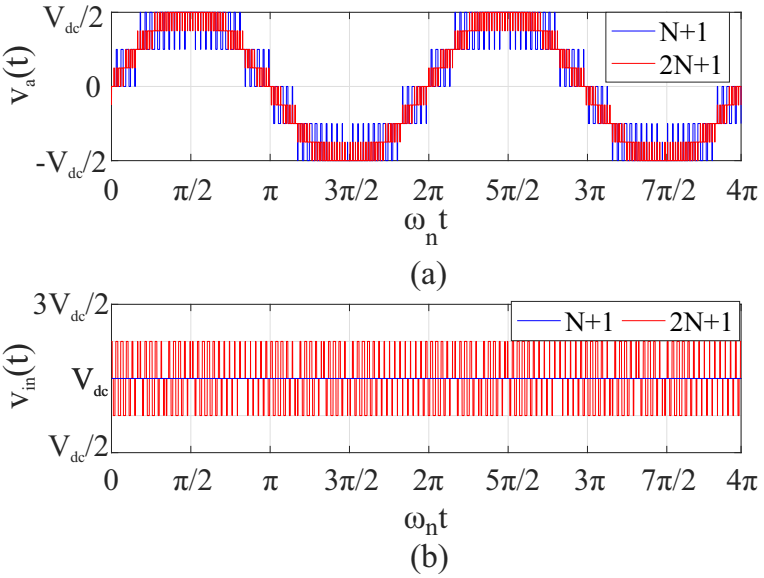
Figure 13 presents a comparison between $(N + 1)$- and $(2N + 1)$-level modulation methods considering 4 SMs per arm and a switching frequency of 900 Hz. As observed in Fig. 13 (a), the MMC output voltage has more levels in the $(2N+1)$-level modulation. This fact provides to the $(2N + 1)$-level modulation a superior performance in terms of power quality at the ac side. On the other hand, the adding of these levels in the $(2N + 1)$-level modulation, results in a ripple in the MMC internal voltage, as illustrated in Fig. 13 (b). Nevertheless, in STATCOM applications the ac side power quality is preferred. Thus, the $(2N + 1)$-level modulation is employed.

Figure 12 – Schematic of PSC-PWM strategy.



Source: Elaborated by the author.

Figure 13 – Comparison of $(N+1)$ and $(2N+1)$ level phase-shifted modulation schemes: (a) MMC output voltage; (b) MMC internal voltage. *Operating Conditions: 4 SMs per arm, switching frequency of 900 Hz.*



Source: Adapted from Sousa (2019)

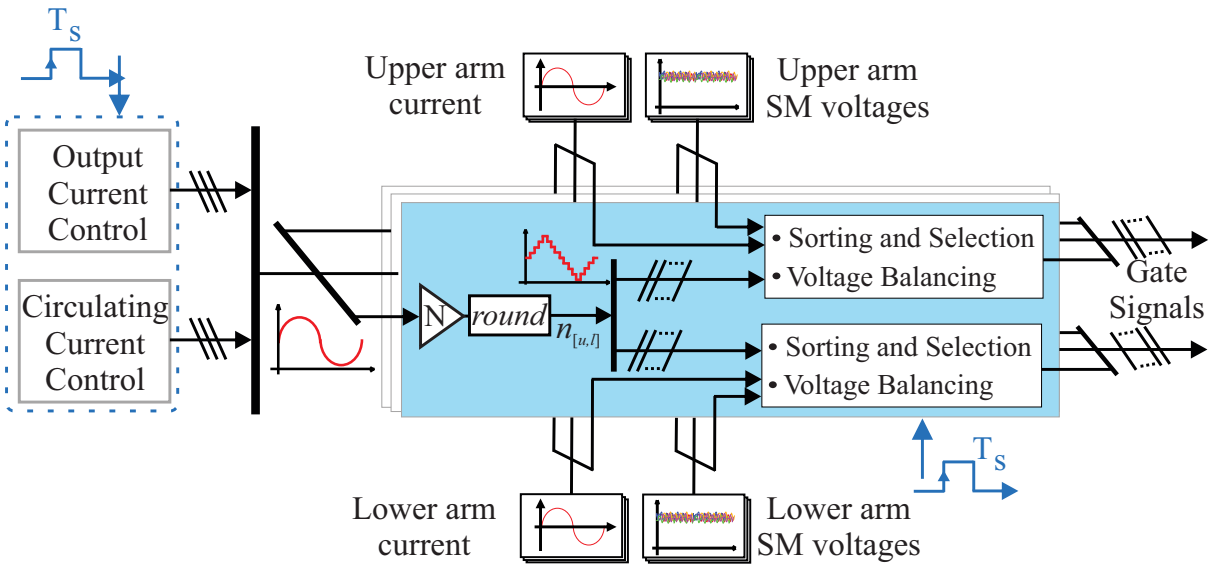
Additionally, the switching pattern of the SMs is generated by comparing the normalized reference signals from the controls with the phase-shifted triangular carrier waves (Debnath et al., 2015).

The schematic of the NLC strategy is shown in Fig. 14. For NLC, the normalized signal from the grid and circulating current controls ($v_{[u,l]}$) are multiplied by the SM number.

Subsequently, the nearest available level is achieved by applying the round function, which approximates the continuous argument to the closest integer (Sharifabadi et al., 2016), as follows:

$$n_{[u,l]} = round(Nv_{[u,l]}), \tag{2.32}$$

Figure 14 – Schematic of NLC strategy.



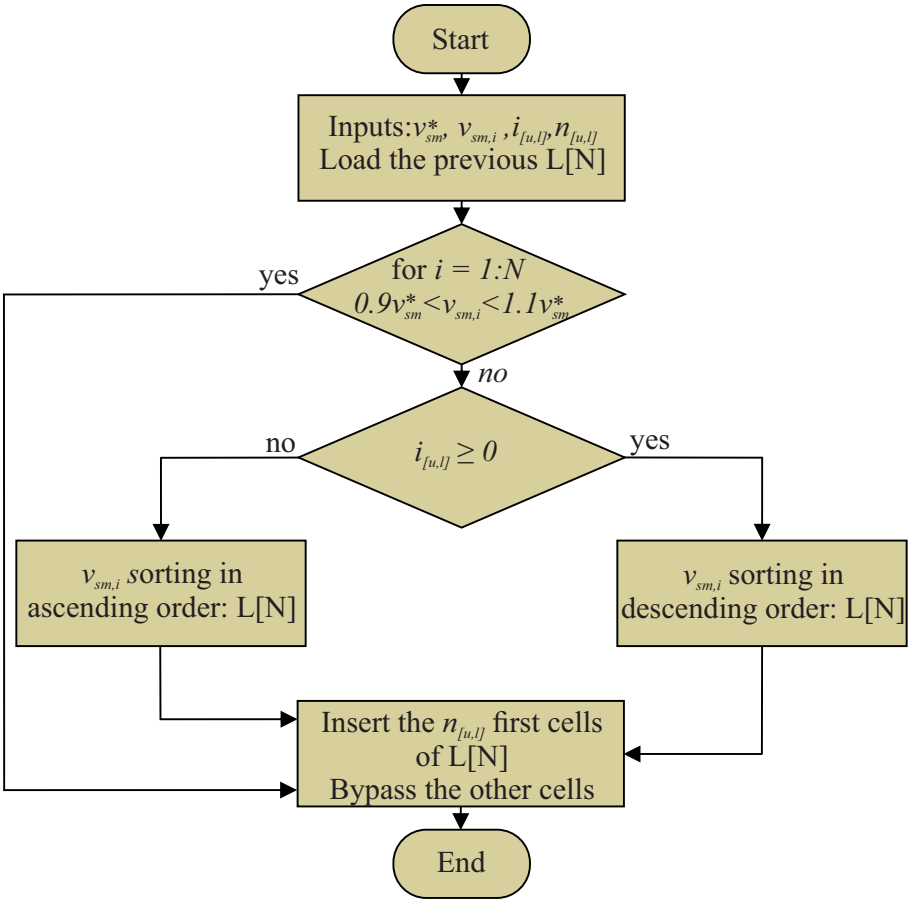
Source: Elaborated by the author.

Thus, the reference becomes a staircase waveform, and the challenge remains in the fact that the lower levels will be used longer than the higher ones, potentially leading to capacitor voltage unbalance. Therefore, NLC is unsuitable for directly assigning the SM to be inserted and bypassed. Instead, it requires a sorting and selection algorithm to ensure individual balancing, which in this case is the CTB algorithm (Sharifabadi et al., 2016). The flowchart of the CTB algorithm is illustrated in Fig. 15.

As observed in Fig. 15, the rounded signal $n_{[u,l]}$, the instantaneous SM voltages $v_{sm,i}$ and the arm current $i_{[u,l]}$ are sent to the CTB algorithm. This algorithm monitors the voltage of each individual capacitor and performs the sorting action at the time that any capacitor voltage violates the voltage boundaries previously stipulated (i.e. v_{mim} and v_{max}). Thus, by utilizing the total available voltage range of each capacitor, this method minimizes the number of switching events for the sake of balancing (Sharifabadi et al., 2016). This work employs 10 % voltage tolerance, i.e. $v_{mim} = 0.9v^*_{sm}$ and $v_{max} = 1.1v^*_{sm}$.

The sorting action produces a list of SMs ($L[N]$). The CTB considers the arm current direction to perform this action. If the arm current is positive, the SM voltages are sorted in descending order. Otherwise, they are sorted in ascending order. Finally, the $n_{[u,l]}$ first SMs of the list are inserted and the others are bypassed.

Figure 15 – Flowchart of CTB algorithm.



Source: Adapted from Sharifabadi et al. (2016).

2.3.2 Switching and Sampling Frequencies

Switching and sampling frequencies are important issues in MMC applications (Sharifabadi et al., 2016; Siddique et al., 2016). The switching frequency (f_{sw}) directly affects the converter efficiency and the capacitor voltage balancing (Cupertino et al., 2018). On the other hand, the sampling frequency (f_s) is the frequency at which the control loops are processed and the modulator updates the gate signals (Siddique et al., 2016). Therefore, this frequency has an important impact on the bandwidth of the current controllers.

For PSC-PWM, Sasongko et al. (2016) demonstrates that interesting values for f_{sw} should support the digital low-pass filter design, such as a moving-average filter. This filter is responsible for eliminating the a.c. component included in the SM capacitor voltages, which works as a disturbance in the current control system. According to the switching frequency employed, the moving-average filter must eliminate the first- and second-order supply frequency components, as well as the capacitor switching components.

If all a.c. component are given by integer multiples of f_n, the moving window time (T_{ma}) can be set as $1/f_n$. Consequently, if only the first- and second-order components of the SM capacitor voltages are considered, this value would be enough. Moreover, according

to Sasongko et al. (2016), if $f_{sw} > 4f_n$, the switching components can be neglected. Thus, $T_{ma} = 1/f_n$ is sufficient for $f_{sw} > 4f_n$. On the other hand, if $f_{sw} \leq 4f_n$ the capacitor switching components must also be eliminated by the moving-average filter. Under this condition, the moving window time must be set as $T_{ma} = f'_n/f_n$, where f'_n is obtained from the irreducible fraction of the switching frequency f_{sw} with respect to the grid frequency f_n, denoted by f'_{sw}/f'_n[1] (Sasongko et al., 2016).

Furthermore, according to reference (Ilves et al., 2015), the switching frequencies integer multiple of the grid frequency may cause instability in the capacitor voltage balancing. Therefore, the switching frequency of PSC-PWM is given as follows:

$$f_{sw} = Kf_n, \tag{2.33}$$

where K is a non-integer number.

PSC-PWM has N carriers per arm. Therefore, there are $2N$ carriers in a period of the grid voltage. Consequently, the sampling frequency has to be fast enough to take all switching moments of the $2N$ carriers. Therefore, the sampling frequency of PSC-PWM is given as follows:

$$f_s = 2Nf_{sw} = 2NKf_n. \tag{2.34}$$

Eq. (2.34) also represents the effective output switching frequency (f_{ef}) of MMC-STATCOM when PSC-PWM modulation is considered (Marzoughi; Burgos; Boroyevich, 2019), i.e., $f_{ef} = f_s$ for PSC-PWM. Moreover, this work employs the same effective output frequency for all PSC-PWM case studies.

Regarding the NLC frequencies, the switching frequency is not fixed, since the switching events occur only when it is necessary (level change or SM exchange process to reach capacitor balancing) (Sousa et al., 2018). Consequently, NLC presents variable effective output switching frequency.

Although switching and effective output frequency cannot be computed for NLC, the sampling frequency requires attention. Considering the unit modulation index amplitude, in order to keep the total harmonic distortion (THD) low, the sampling frequency must fulfill the following requirement (Siddique et al., 2016):

$$f_s > f_2 = \pi N f_n. \tag{2.35}$$

By replacing f_s in Eq. (2.35) by the sampling frequency of PSC-PWM, the following is obtained:

[1] For example, when $f_{sw} = 210$ Hz and $f_n = 60$ Hz, $f'_{sw}/f'_n = 7/2 = 3.5$. Therefore, $f'_{sw} = 7$ and $f'_n = 2$. Thereby, $T_{ma} = 2/f_n$.

$$2NKf_n > f_2 = \pi N f_n \Rightarrow K > \frac{\pi}{2} \approx 1.57. \tag{2.36}$$

Thus, since $K > 3$ is considered, the same sampling frequency can be adopted for both modulation strategies (Eq. (2.34)) regardless of the number of SMs.

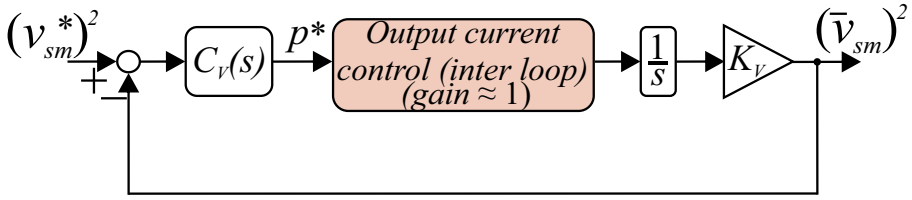
2.4 Control Tuning

The MMC-STATCOM controllers have the purpose of controlling the active and reactive power exchange with the grid, the circulating current and the voltage balancing among SM capacitors. Therefore, the strategies to define these controllers are discussed.

2.4.1 Global Energy Control

The plant transfer function can be obtained by neglecting the converter losses and assuming an even distribution of the energy among the converter SM capacitors. The block diagram of the global energy control is illustrated in Fig. 16.

Figure 16 – Block diagram of the global energy control.



Source: Elaborated by the author.

The behavior of the SM capacitor voltage can be represented by the total energy storage:

$$W_T = \sum_{i=1}^{6N} \frac{1}{2} C v_{sm,i}^2 = 3CNv_{sm}^2. \tag{2.37}$$

The time derivative of Eq. (2.37) represents the instantaneous power in the terminals of the capacitors. Thus, the square of the SM capacitor voltage can be expressed by:

$$Y(s) = Y(0) + \frac{p}{3CNs}, \tag{2.38}$$

where p is the active power to maintain the capacitive energy storage.

Therefore, the following transfer function is obtained:

$$\frac{Y(s)}{\hat{I}_s(s)} = \frac{K_V}{s}, \tag{2.39}$$

where K_V is given by:

$$K_V = \frac{1}{3CN}. \tag{2.40}$$

Moreover, $C_V(s)$ is a PI controller, given by:

$$C_V(s) = k_{p,v} + \frac{k_{i,v}}{s}, \tag{2.41}$$

where $k_{p,v}$ and $k_{i,v}$ are the proportional and integral gains, respectively.

Considering the ideal inner loop (output current control loop) and neglecting the MAF in the measuring procedure, the outer open-loop is obtained by:

$$G_V(s) = \left(k_{p,v} + \frac{k_{i,v}}{s}\right)\left(\frac{1}{3CN}\right)\left(\frac{1}{s}\right). \tag{2.42}$$

The tuning of the controllers is carried out by the pole allocation method. According to the methodology discussed in (Sousa, 2011), the gains for the poles of the transfer function in closed-loop to be real and allocated in the left semiplane, can be obtained as follows:

$$\begin{cases} k_{p,v} = \frac{2\pi(f_{v1}+f_{v2})}{K_V}, \\ k_{i,v} = \frac{4\pi^2 f_{v1} f_{v2}}{K_V}, \end{cases} \tag{2.43}$$

where f_{v1} and f_{v2} are the poles of the closed-loop transfer function. Typically, these poles are separated by a decade and the value of the largest of them must be allocated, at least, one decade below the cutoff frequency of the current grid. This guarantees the proper operation of the cascade control (Cupertino, 2015).

2.4.2 Output Current Control

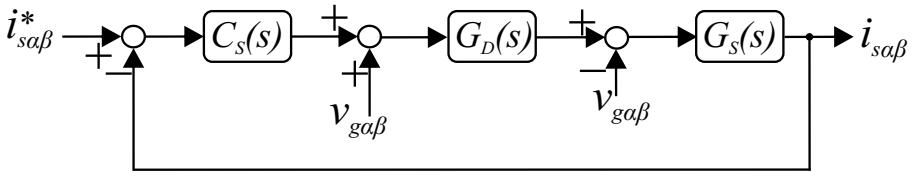
The block diagram of the output current control is shown in Fig. 17. In addition, $C_S(s)$ is the PR controller, given by:

$$C_S(s) = k_{p,s} + \frac{k_{r,s}}{s^2 + \omega_n^2}, \tag{2.44}$$

where $k_{p,s}$ is the proportional gain and $k_{r,s}$ is the resonant gain of the controller output current that is tuned to the fundamental frequency.

The effect of the implementation delay and the zero-order hold can be represented by the following transfer function (Yao et al., 2017):

Figure 17 – Block diagram of the output current control.



Source: Elaborated by the author.

$$G_D(s) = \frac{1 - e^{-T_s}}{T_s s} e^{-T_s} \approx \frac{1}{1.5T_s s + 1}, \tag{2.45}$$

where $T_s = \frac{1}{f_s}$ is the sampling time. The total delay in the control loop is $T_d = 1.5Ts$, which is commonly used in the literature for the control loop stability analysis (Yao et al., 2017).

The plant transfer function of output current $G_S(s)$ can be represented by:

$$G_S(s) = \frac{1}{sL_{eq} + R_{eq}}, \tag{2.46}$$

where $L_{eq} = \frac{L_a}{2} + L_f$ and $R_{eq} = \frac{R_a}{2} + R_f$ are the equivalent inductance and resistance.

Following the methodology discussed in (Sharifabadi et al., 2016), the objective is to maximize the current control bandwidth. Thus, the PR gains can be obtained by:

$$\begin{cases} k_{p,s} = 2\pi f_{c,s} L_{eq}, \\ k_{r,s} = 2\pi f_{h,s} k_{p,s}, \end{cases} \tag{2.47}$$

where $f_{c,s}$ is the desired closed-loop-system bandwidth and $f_{h,s}$ is resonant part bandwidth.

Since the total time delay is not generally negligible, there is an upper limit for $f_{c,s}$ that must be observed for the closed-loop system to remain stable with large enough margins. An useful rule of thumb is:

$$f_{c,s} \leq \frac{f_s}{10}. \tag{2.48}$$

Moreover, $f_{h,s}$ should comply with the following conditions:

$$\begin{cases} f_{h,s} \ll f_{c,s}, \\ f_{h,s} \leq f_n. \end{cases} \tag{2.49}$$

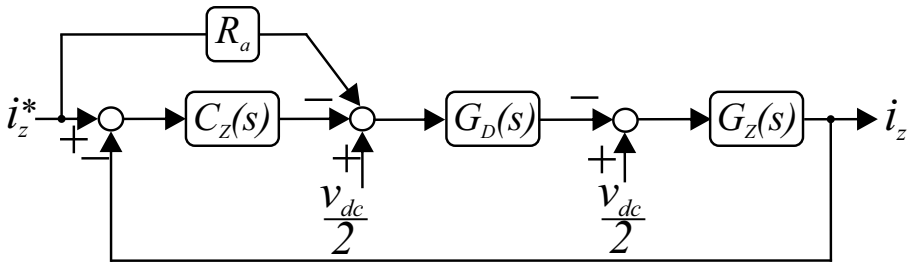
2.4.3 Circulating Current Control

The block diagram of the circulating current control is shown in Fig. 18. Moreover, $C_Z(s)$ is the PR controller, given by:

$$C_Z(s) = k_{p,z} + \frac{k_{r,z}}{s^2 + (2\omega_n)^2} + \frac{k_{r,z}}{s^2 + (4\omega_n)^2}, \tag{2.50}$$

where $k_{p,z}$ is the proportional gain and $k_{r,z}$ is the resonant gain of the controller output current that is tuned to the second- and fourth-order harmonic frequencies.

Figure 18 – Block diagram of the circulating current control.



Source: Elaborated by the author.

The plant transfer function $G_Z(s)$ of circulating current can be represented by:

$$G_Z(s) = \frac{1}{sL_a + R_a}. \tag{2.51}$$

The PR gains are obtained analogously to the gains of the inter loop of output current control. Therefore, following the methodology discussed in (Sharifabadi et al., 2016), the PR gains can be obtained by:

$$\begin{cases} k_{p,z} = 2\pi f_{c,z} L_a, \\ k_{r,z} = 2\pi f_{h,z} k_{p,z}, \end{cases} \tag{2.52}$$

where $f_{c,z}$ is the desired closed-loop-system bandwidth and $f_{h,z}$ is resonant part bandwidth. $f_{c,z}$ and $f_{h,z}$ conditions are:

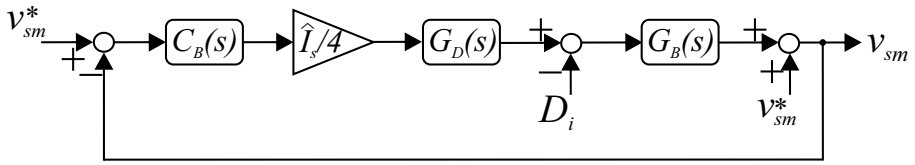
$$\begin{cases} f_{c,z} \leq \frac{f_s}{10}, \\ f_{h,z} \ll f_{c,z}, \\ f_{h,z} \leq f_n. \end{cases} \tag{2.53}$$

2.4.4 Individual Voltage Balancing Control

The block diagram of the individual voltage balancing control is presented in Fig. 19. The block diagram considers the upper arm of phase a.

The aim is to keep each of the three dc voltages in an arm equal to the dc mean voltage of the corresponding arm. The difference between the voltage reference and the dc voltage of the ith converter SM ($v_{sm,i}$) is given by (Maharjan; Inoue; Akagi, 2008):

Figure 19 – Block diagram of arm-balancing control.



Source: Elaborated by the author.

$$\Delta v_{sm,i} = v^*_{sm} - v_{sm,i}. \tag{2.54}$$

The compensating voltage to minimize $\Delta v_{sm,i}$ can be expressed as (Maharjan; Inoue; Akagi, 2008):

$$v_{ib} = k_{p,b} \Delta v_{sm,i} \sin(\omega_n t). \tag{2.55}$$

Equation (2.55) means that the individual balancing controller has a proportional gain of $k_{p,b}$:

$$C_B = k_{p,b}. \tag{2.56}$$

The plant transfer function $G_B(s)$ can be represented by:

$$G_B(s) = \frac{1}{sCv^*_{sm}}. \tag{2.57}$$

The upper arm current can be expressed by:

$$i_u = \frac{\hat{I}_s}{2} \sin(\omega_n t). \tag{2.58}$$

The active power for dc-voltage balancing of the i-th converter SM can be written as:

$$p_{ib} = v_{ib} i_u - D_i, \tag{2.59}$$

where D_i represents the losses or disturbance in the i-th converter SM. Replacing Eq. (2.55) and (2.58) into Eq. (2.59), the follow equation is obtained:

$$p_{ib} = \frac{k_{p,b} \Delta v_{sm,i} \hat{I}_s}{4} (1 - \cos(2\omega_n t)) - D_i. \tag{2.60}$$

Thus, $\Delta v_{sm,i}$ can be expressed by:

$$\Delta v_{sm,i} \approx -\frac{1}{C}\int \frac{p_{ib}}{v^*_{sm}}dt. \tag{2.61}$$

The closed-loop transfer function is given by:

$$\frac{\Delta V_{sm,i}(s)}{D_i(s)} = \frac{1}{sCv^*_{sm} + k_{p,b}.\frac{\hat{I}_s}{4}} \tag{2.62}$$

The closed-loop poles must be located in the left semiplane for the system to be stable (Cupertino, 2015). Thus, the proportional gain can be calculated as follows:

$$k_{p,b} = \frac{8\pi f_{c,b} C v^*_{sm}}{\hat{I}_s}, \tag{2.63}$$

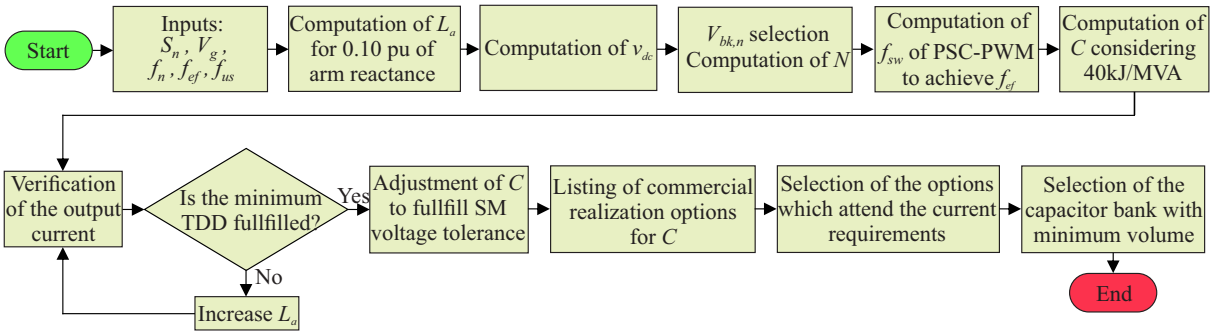
where $f_{c,b}$ is the location of the closed-loop pole. $f_{c,b}$ conditions are:

$$\begin{cases} f_{c,b} \ll f_{c,s}, \\ f_{c,b} \ll f_{c,z}. \end{cases} \tag{2.64}$$

2.5 Design

Figure 20 presents the design flowchart of the MMC-STATCOM components for the simulation cases. This work considers different IGBT blocking voltages ($V_{bk,n}$) employed to perform a three-phase MMC-STATCOM with common rated power (S_n), output voltage (V_g), grid frequency (f_n) and effective output frequency (f_{ef}). The design procedure is defined to comply with grid standards and to provide a similar utilization factor (f_{us}) of the IGBT blocking voltage.

Figure 20 – Design flowchart of the MMC-STATCOM components.



Source: Elaborated by the author.

The utilization factor determines the voltage rating of SM semiconductor devices. If the rating is too close to the operating voltage, the risk of failure will be large, adversely affecting equipment availability. If the voltage rating is chosen with excessive safety margins,

overall efficiency and performance will suffer since higher rated devices require thicker silicon which generates higher losses (ABB, 2013a).

A failure rate model that describes failures due to cosmic rays can be used to help define the utilization factor. This mathematical model covers the three most important influences (blocking voltage, junction temperature, and altitude) and is given by (ABB, 2019):

$$\lambda_f(v_{dc}, T_j, h) = \underbrace{C_3 \exp\left(\frac{C_2}{C_1 - V_{bk,o}}\right)}_{\lambda_1} \times \underbrace{\exp\left(\frac{25 - T_j}{47.6}\right)}_{\lambda_2} \times \underbrace{\exp\left(\frac{1 - (1 - \frac{h}{44300})^{5.26}}{0.143}\right)}_{\lambda_3}. \tag{2.65}$$

where $V_{bk,o}$ is the maximum operational dc blocking voltage in a semiconductor device, T_j is junction temperature in degrees Celsius and h is the altitude in meters above sea level. The model delivers failure rates in FIT, i.e. number of failures within 10^9 element hours. The model parameters C_1, C_2, and C_3 are characteristic values of the individual semiconductor devices which have no physical meaning.

The failure rate model consists of three multiplicands:

- λ_1: dependence on the blocking voltage at nominal conditions, i.e. 25°C and sea level;
- λ_2: dependence on the junction temperature. Term equals unity if $T_j = 25$°C;
- λ_3: dependence on the altitude (h in meters above sea level). Term equals unity if $h = 0$, i.e. sea level.

Considering 25°C and sea level, the maximum dc voltage for a specified failure rate $V_{bk,o}$ can be isolated in Eq. (2.65) as follow:

$$V_{bk,o} = C_1 - \frac{C_2}{\ln\left(\frac{\lambda_f}{C_3}\right)}. \tag{2.66}$$

This work considered the failure rate of $\lambda_f = 100$ FIT, where FIT is the failure in time. Subsequently, $V_{bk,o}$ is used to find the maximum utilization factor of each IGBT module as follows:

$$f_{us,max} = \frac{V_{bk,o}}{V_{bk,n}}, \tag{2.67}$$

Since different IGBT modules are considered in this work, a single f_{us} is selected to comply with all cases and respect the $f_{us,max}$ of each one.

The dc-side voltage can be approximated by (Fujii; Schwarzer; De Doncker, 2005; Cupertino et al., 2018):

$$v_{dc} = \frac{2\sqrt{2}}{\sqrt{3}(1-\Delta v_{dc})}\frac{V_s}{\lambda m_{max}}, \tag{2.68}$$

where V_s is the minimum line-to-line voltage (rms), Δv_{dc} is the dc-side voltage ripple, λ is the modulation gain and m_{max} is the maximum modulation index given by (Fujii; Schwarzer; De Doncker, 2005):

$$m_{max} = \left(\frac{1}{f_{sw}} - 2T_{ds}\right) f_{sw}, \tag{2.69}$$

where T_{ds} is the minimum on-time and dead time of the semiconductor devices. Considering the modulation with the injection of 1/6 of the third harmonic, $\lambda = 1.15$. Moreover, the line-to-line rms voltage synthesized by the MMC-STATCOM is given by (Fujii; Schwarzer; De Doncker, 2005):

$$V_s = (1+\Delta V_g)\left[1 + x_{eq,pu}\,(1+\Delta x_{eq})\right] V_g, \tag{2.70}$$

where V_g is the line-to-line rms grid voltage, ΔV_g is the grid voltage variation, $x_{eq,pu}$ is the per unit value of the output reactance and Δx_{eq} is the output reactance variation.

The number of SMs per arm is given by (Cupertino et al., 2018):

$$N = \frac{v_{dc}}{f_{us} V_{bk,n}}. \tag{2.71}$$

The switching frequency of the case studies with PSC-PWM is defined to obtain the same effective output frequency in all cases. The switching frequency to obtain this f_{ef} is computed for each PSC-PWM by Eq. (2.34). NLC presents variable switching and effective output frequencies.

The arm inductance limits fault currents and improves the circulating current characteristic (Qingrui Tu et al., 2010). Moreover, for the voltage level and the application considered in this work, arm inductors are typically dry-type air-core reactors. Thus, decoupled inductors are considered (Sharifabadi et al., 2016). The arm inductor also performs output current filtering. The per unit (pu) arm inductance values for grid-connected converters are typically limited between 0.05 and 0.15 pu (Sharifabadi et al., 2016). This work employs 0.10 pu of arm inductance. For each case study, it is verified if the grid current total demand distortion (TDD) is lower than 5 %, as recommended by international standards (IEEE, 2014). Finally, the typical arm inductor X/R ratio of 40 is employed in all cases.

The SM capacitance is given by (Cupertino et al., 2018):

$$C = \frac{2NW_{conv}S_n}{6v_{dc}^2}, \tag{2.72}$$

where W_{conv} is the required energy storage per MVA and S_n is the rated power. Cupertino et al. (2018) and Ilves et al. (2014) evaluated the energy storage requirement for a MMC, considering the SM capacitor voltage ripple of 10%, perfectly balanced and close to the average voltage. Under such conditions, the energy storage requirement is 40 kJ/MVA. This energy storage is usually sufficient in cases with PSC-PWM. Nevertheless, individual SM capacitor voltages for a given arm can have a spreading, which depends on the modulation strategy employed. Furthermore, the NLC and PSC-PWM require different SM capacitance (Hahn et al., 2018). Thus, the SM capacitance of each case study with NLC is adjusted to fulfill the voltage ripple of 10%. Subsequently, the SM capacitances are approximated to commercial values. The capacitors are selected to comply with the range of current and the design with minimum volume is selected. The range of currents considered is between 0.25 pu and 0.75 pu of ac output current amplitude (Sousa, 2014).

2.6 Case Studies

2.6.1 Simulation Cases

The case studies are based on simulations implemented in the PLECS environment. The common parameters considered in the MMC-STATCOM case studies are given in Tab. 3. An MMC-STATCOM of 17 MVA rated power, connected to a 60 Hz network with a line voltage of 13.8 kV at the point of common coupling is considered in all case studies. The sampling frequency of 8.4 kHz is considered for all cases.

Table 3 – Common Parameters of Design. *Remark: pu means per unit at rated power and voltage.*

Parameter	Value
dc-side voltage (v_{dc})	21.61 kV
Rated power (S_n)	17 MVA
Line-to-line rms grid voltage (V_g)	13.8 kV
Grid frequency (f_n)	60 Hz
Effective output frequency (f_{ef})	8.4 kHz
Transformer inductance (L_f)	1.5 mH (0.05 pu)
Transformer resistance (R_f)	0.032 Ω (0.003 pu)
Transformer X/R ratio	18
Arm inductance (L_a)	2.97 mH (0.10 pu)
Arm resistance (R_a)	0.028 Ω (0.002 pu)
Arm X/R ratio	40
Utilization factor (f_{us})	60%

Four semiconductor blocking voltages are considered to evaluate the converter with different numbers of SMs: 1.7 kV, 3.3 kV, 4.5 kV and 6.5 kV. Moreover, commercially available ABB HiPak IGBTs modules with a rated current close to 800 A are selected. The IGBT module part numbers are shown in Tab. 4. Besides, for each blocking voltage, it is considered case studies with the modulation strategies PSC-PWM and NLC. The name of each case study and their respective parameters are shown in Tab. 4.

Table 5 presents the characteristic parameters for each ABB HiPak IGBTs module (i.e. C_1, C_2, and C_3) employed (ABB, 2019). Considering these parameters, Eq. (2.66) and Eq. (2.67), the maximum continuous dc blocking voltage $V_{bk,o}$ and utilization factor $f_{us,max}$ are computed. $V_{bk,o}$ and $f_{us,max}$ are presented in Table 5 for each IGBTs module employed. As observed, the maximum recommended nominal voltage for semiconductor devices is below 60.12% of $V_{bk,n}$. Therefore, $f_{us} = 60\%$ is considered in this work.

Table 4 – Parameters of each simulation case study.

Case	C_{N17}	C_{P17}	C_{N33}	C_{P33}	C_{N45}	C_{P45}	C_{N65}	C_{P65}
Modulation Strategy	NLC	PSC	NLC	PSC	NLC	PSC	NLC	PSC
Number of SMs per arm (N)	21		11		8		6	
IGBT module blocking voltage ($V_{bk,n}$)	1.7 kV		3.3 kV		4.5 kV		6.5 kV	
IGBT module part number	5SND0800M170100		5SNA0800N330100		5SNA0800J450300		5SNA0750G650300	
Switching frequency (f_{sw})	-	200 Hz	-	381.82 Hz	-	525 Hz	-	700 Hz
SM capacitance (C)	14.07 mF	14.07 mF	6.25 mF	5.56 mF	4.94 mF	4.18 mF	3.42 mF	2.99 mF
Capacitors per SM	7	7	9	8	13	11	16	14
Volume of the SM capacitor bank	3.5 dm^2	3.5 dm^2	4.5 dm^2	4.0 dm^2	6.5 dm^2	5.5 dm^2	8.0 dm^2	7.0 dm^2
Capacitor selected	2010μF/1.3kV-60A		695μF/2.2kV-60A		380μF/3kV-60A		855μF/2kV-60A	
Capacitor part number	E50.S34-205NT1		E50.S34-694NT0		E50.S34-384NT0		E50.S34-864NT0	
Equivalent series resistance (R_s)	1 mΩ		1.3 mΩ		1.1 mΩ		1.4 mΩ	
Capacitor thermal resistance (R_{th})	0.9 K/W		0.9 K/W		0.9 K/W		0.9 K/W	
Nominal SM voltage	1.029 kV		1.965 kV		2.701 kV		3.601 kV	

Table 5 – Blocking voltage ratings for individual IGBT Module.

$V_{bk,n}$ (kV)	Part num.	C_1	C_2	C_3	$V_{bk,o}$ (kV)	$f_{us,max}$ (%)
1.7	5SND0800M170100	983	914	3.03×10^6	1.072	63.03
3.3	5SNA0800N330100	1784	2211	9.40×10^5	2.026	61.38
4.5	5SNA0800J450300	2279	7222	7.53×10^6	2.922	64.94
6.5	5SNA0750G650300	2567	18525	1.00×10^8	3.907	60.12

In this chapter, the dc-side voltage is computed by Eq. (2.68), neglecting the voltage and output reactance variations. Moreover, the conservative approach of dc-side voltage is considered to comply with all operational conditions and all case studies. Thus, v_{dc} is computed considering $V_{bk,n} = 6.5$ kV and $f_{sw} = 700$ Hz. Indeed, since the same f_{ef} is considered, the lowest value of m_{max} (0.9979) and, consequently, highest v_{dc} is found for $V_{bk,n} = 6.5$ kV. Therefore, v_{dc} is 21.61 kV for all cases.

Regarding the arm inductance L_a, 0.10 pu of arm inductance is considered, i.e., 2.97 mH (base values: 17MVA and 13.8 kV). The arm resistance R_a is computed considering the typical arm inductor X/R ratio of 40, thus, 0.028 Ω is employed.

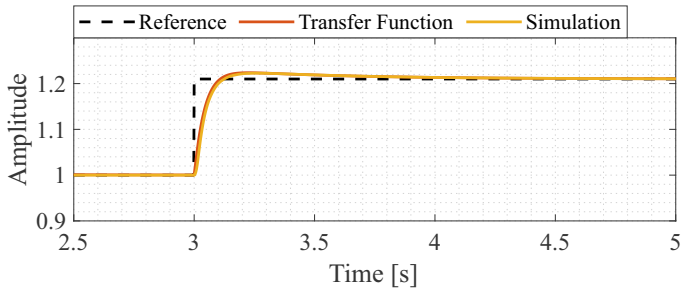
The SM capacitances are computed with Eq. (2.72) and adjusted to fulfill the voltage ripple of 10%. Subsequently, the SM capacitances have to be approximated to commercial values. The realization of the SM capacitance is based on Electronicon Film Capacitors. The total SM capacitance, capacitor selected, the volume of the capacitor bank and the number of capacitors are presented in Tab. 4. For 1.7 kV, 3.3 kV and 4.5 kV blocking voltages, only capacitors in parallel are employed. For 6.5 kV blocking voltage, strings of two capacitors in series are connected in parallel.

Following the considerations of Section 2.4, the controllers of the MMC-STATCOM are adjusted to guarantee the proper operation of each control loop, simultaneously. Besides, the parameters of Tab. 3 and Tab. 4 are employed. The sampling frequency of $f_s = 8.4$ kHz is considered for all cases.

The pole frequencies of the global energy controller are set to $f_{v1} = 3$ Hz and $f_{v2} = 0.3$ Hz. Fig. 21 presents the step response of the closed-loop transfer function and the MMC-STATCOM simulation considering the case study C_{P17} of Tab. 4. The MMC-STATCOM simulation was performed in PLECS environment, in which a system-level simulation with the electrical components, controllers and delay of measurements are considered. As observed, in Fig. 21, the step happens at 3 s. Moreover, the transfer function and MMC-STATCOM simulation present similar responses. Both responses to the step present an overshoot. Besides, the global energy control needs approximately 1.5 s to reach the reference.

For the output current and circulating current controllers, the frequencies are set at the condition limits, as follows:

Figure 21 – Step response of global energy controller. *Remark: Simulation considering case study C_{P17}.*



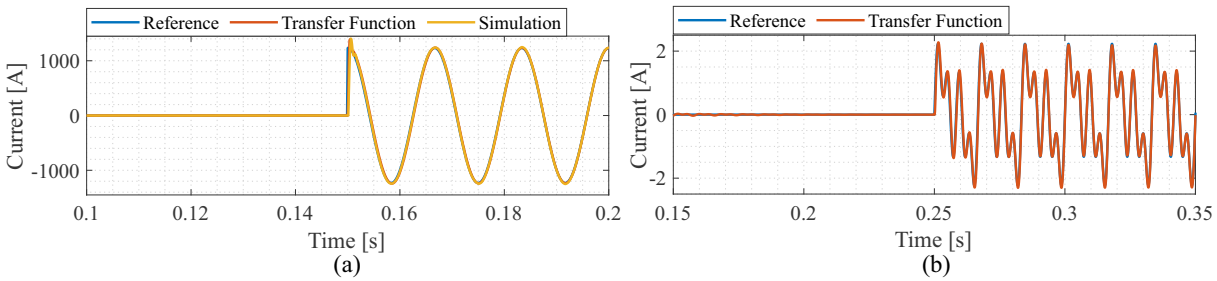
Source: Elaborated by the author.

$$\begin{cases} f_{c,s} = \frac{f_s}{10}, \\ f_{h,s} = f_n. \end{cases} \tag{2.73}$$

The performance of the output current controller is evaluated by tracking a sinusoidal reference in a stationary frame ($\alpha\beta$), as shown in Fig. 22 (a). Until 0.15 s the reference is zero. After 0.15 s a unit reference is given. As observed, the transfer function and the MMC-STATCOM simulation reach the reference almost instantly.

The performance of the circulating current controller tracking a sinusoidal reference is evaluated, as shown in Fig. 22 (b). Until 0.25 s the reference is zero. After 0.25 s a reference that presents the fundamental, second- and fourth-order harmonic components with unity amplitudes and phase 0 is followed. As observed, the controller allows the circulating current to follow the reference as desired.

Figure 22 – (a) Output current controller response. (b) Circulating current controller response.



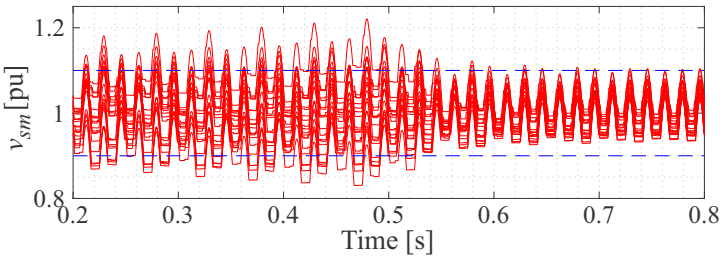
Source: Elaborated by the author.

Finally, the frequencies of the individual balancing control are defined to comply with the closed-loop-system bandwidth lower than all other controllers. Thus, the frequency is given by:

$$f_{c,b} = \frac{f_s}{10^6}. \tag{2.74}$$

The performance of the individual balancing controller in SM voltages is evaluated, as shown in Fig. 23. A simulation considering case study C_{P17} and rated leading reactive power ($q = 1$ pu) is considered. Until 0.5 s the MMC-STATCOM works without the individual voltage balancing controller. After 0.5 s individual balancing controller is activated. The dashed lines indicate the 10% tolerance of voltage ripple. As observed in Fig. 23, the SM voltages reach the steady state in approximately 0.1 s. Besides, the 10% tolerance of voltage ripple is respected with the controller.

Figure 23 – Effect of individual voltage balancing controller in SM voltages. *Remark: Simulation considering case study C_{P17} and rated leading reactive power ($q = 1$ pu).*



Source: Elaborated by the author.

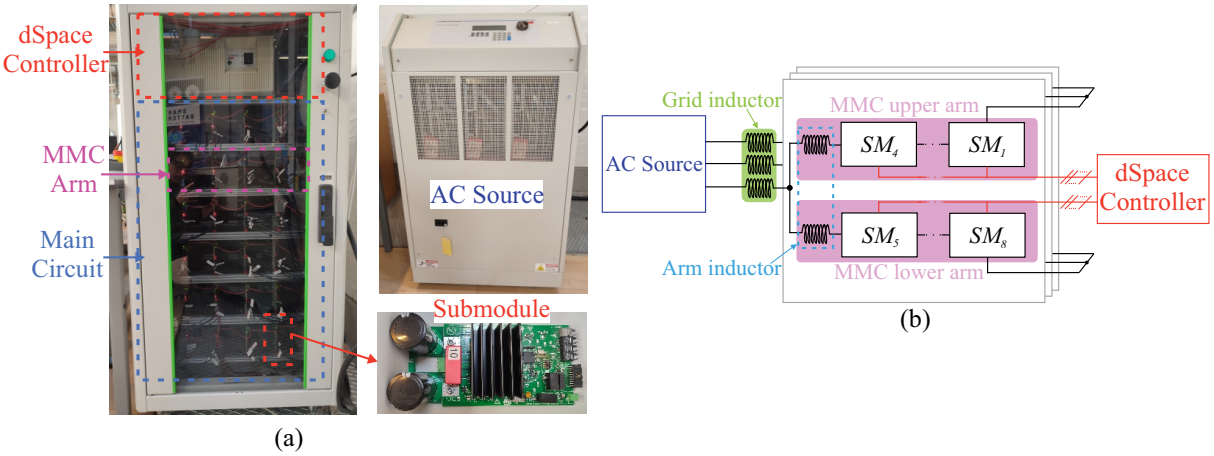
2.6.2 Experimental Setup

The control dynamic behavior is verified in the laboratory MMC-STATCOM setup shown in Fig. 24. The experimental MMC setup is a prototype with three phase half-bridge configuration. The main parameters of the experimental platform are presented in Tab. 6. The digital controller is based on the dSPACE real-time control platform model DS1006. The measurement is achieved by DS4004 board. Each submodule is a half-bridge submodule with hardware protection (overcurrent and overvoltage protection). A rate limiter of 0.1 pu/ms is employed in the reference of reactive power in the controller to avoid the protection being activated during the experimental tests.

Table 6 – MMC-STATCOM setup parameters.

Parameter	Value
Number of SMs per arm (N)	4
dc-side voltage (v_{dc})	229.82 V
Rated power (S_n)	1 kVA
Grid voltage amplitude (phase-to-neutral) ($\hat{V}_g$)	83 V
Grid frequency (f_n)	60 Hz
Switching frequency (f_{sw})	1050 Hz
Sampling frequency (f_s)	8.4 kHz
Grid inductance (L_f)	1.8 mH (0.05 pu)
Arm inductance (L_a)	10 mH (0.10 pu)
SM capacitance (C)	2000 μF
IGBT module part number	PSS15S92F6-AG

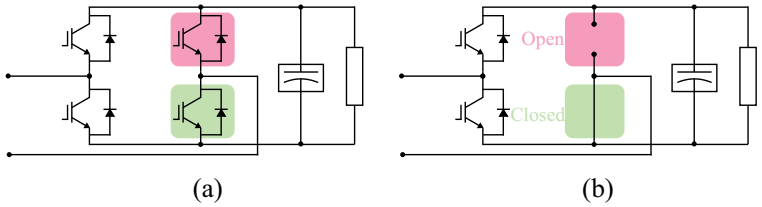
Figure 24 – (a) MMC-STATCOM experimental setup; (b) schematic of the experimental setup.



Source: Elaborated by the author.

The submodules of the setup are able to perform cascaded topologies with full-bridge or half-bridge SMs. For this reason, the experimental setup is composed of full-bridge submodules. Thus, the SMs can operate in full-bridge or half-bridge mode, as illustrated in Fig. 25 (a) and (b), respectively. Since SM in half-bridge configuration is employed in this work, the second leg of the full-bridge has an IGBT that is always blocking and another that is always conducting, as illustrated in Fig. 25 (b). The IGBT that is always conducting inserts a voltage drop in the SM circuit.

Figure 25 – MMC-STATCOM setup submodule in: (a) full-bridge mode; (b) half-bridge mode.



Source: Elaborated by the author.

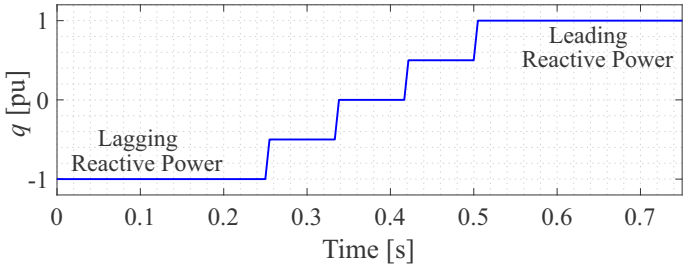
The dc-side voltage is computed by Eq. (2.68), considering the parameters of Tab. 6 and neglecting the voltage and output reactance variations. Moreover, the voltage margin of 12 V per SM is added to compensate for the voltage drops that happen in the circuit, such as in the semiconductor devices, inductors, dead time and solders of components and cables.

2.7 Dynamic Response

2.7.1 Simulation Results

This section presents the MMC-STATCOM dynamic response. Simulations in PLECS environment are performed to demonstrate the dynamic behavior of the MMC-STATCOM. This demonstration is performed considering the cases of blocking voltage 1.7 kV (C_{P17} and C_{N17}). The reactive power profile considered is presented in Fig. 26.

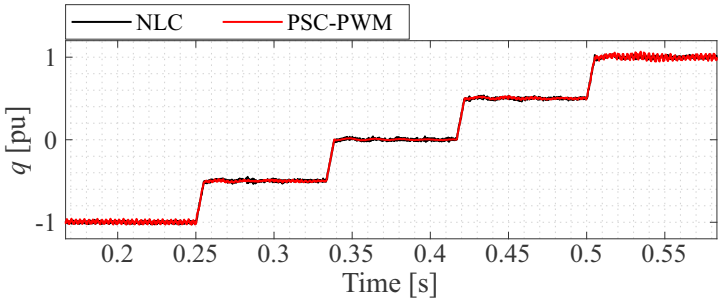
Figure 26 – Dynamic profile of reactive power employed in the simulations. *Remark: The reactive power exchange during the transients happens at 0.1 pu/ms.*



Source: Elaborated by the author.

Figure 27 presents the instantaneous reactive power synthesized by the MMC-STATCOM. The reactive power is computed with instantaneous power theory. For both modulation strategies, the reactive power response follows the reactive power profile. In addition, PSC-PWM presents higher oscillations than NLC when the converter is performing rated lagging and leading reactive power.

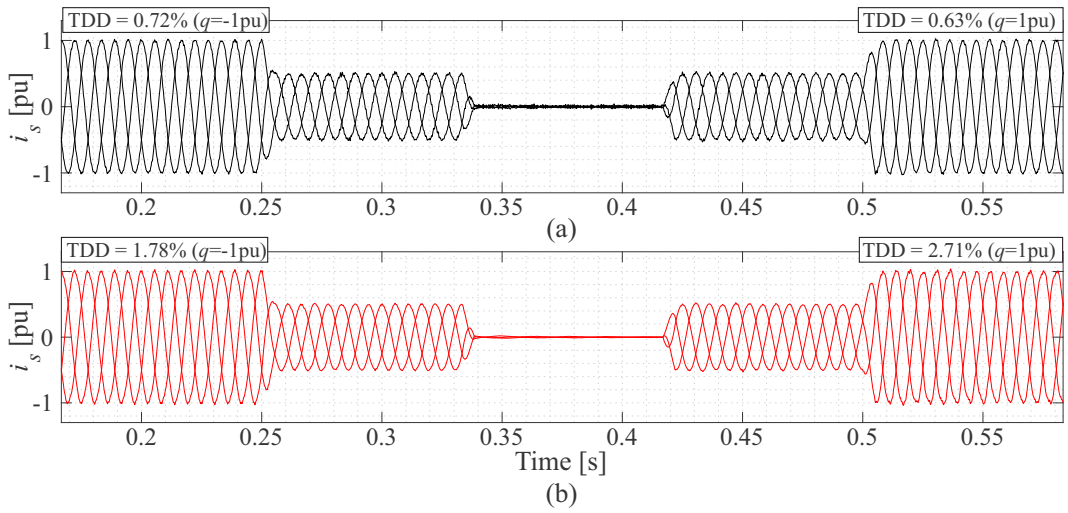
Figure 27 – Instantaneous reactive power synthesized by the MMC-STATCOM.



Source: Elaborated by the author.

Figure 28 shows the output current. As observed, the output current follows the reactive power profile for both modulation strategies. Moreover, the TDD when the converter is performing rated lagging and leading reactive power is presented. Both modulation strategies fulfill the TDD limit of 5% recommended by IEEE standard (IEEE, 2014). Furthermore, NLC presents lower values than PSC-PWM in both operational conditions.

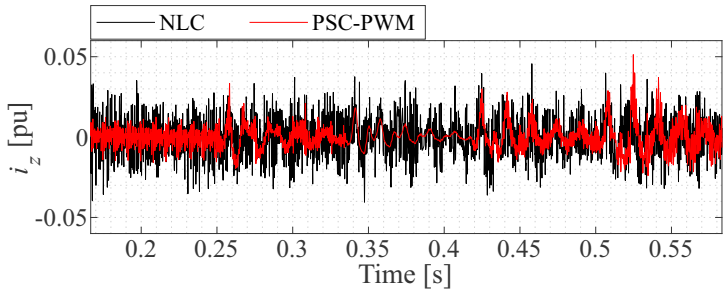
Figure 28 – Output current synthesized by the MMC-STATCOM with: (a) NLC; (b) PSC-PWM. *Remark: Considering the base current of 1005.8 A.*



Source: Elaborated by the author.

In terms of circulating current, the dynamic responses are presented in Fig. 29. In accordance with previous results, PSC-PWM presents lower oscillations than NLC.

Figure 29 – Dynamic behavior of the circulating current of phase A. *Remark: Considering the base current of 1005.8 A.*

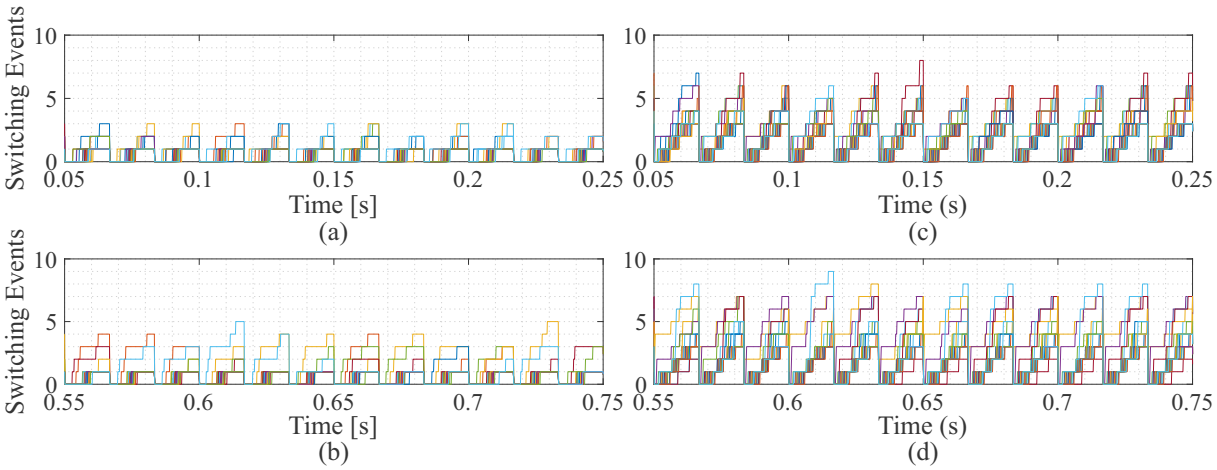


Source: Elaborated by the author.

Figure 30 presents the number of switching events per cycle when the converter is in lagging and leading rated reactive power with both modulation strategies. As observed, the number of switching events varies among the cycles even for PSC-PWM due to the fact of its carrier frequency (200 Hz) is a interharmonic of the grid frequency. Furthermore, NLC presents lower number of switching events than PSC-PWM in both operational conditions. This facts indicates lower effective switching frequency with NLC.

Figure 31 presents the SM capacitor voltages. The dashed lines indicate the 10% tolerance of voltage ripple. As observed in Fig. 31, the capacitor ripple follows the reactive power operation. In addition, for both strategies, there is an inversion in the shape of capacitor voltages when the converter provides reactive power to when the converter performs lagging reactive power. As observed, NLC presents higher spreading in the 10%

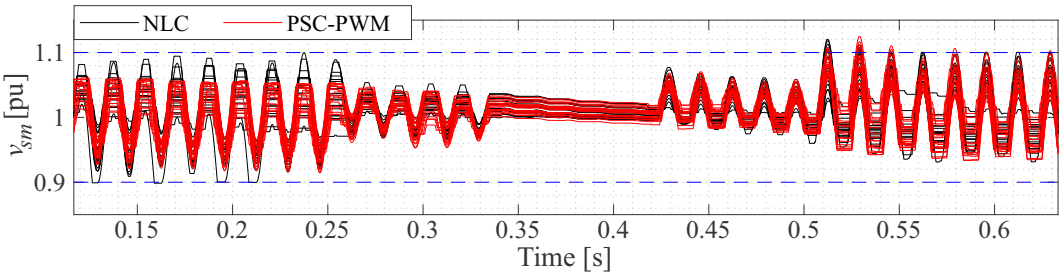
Figure 30 – Number of switching events per cycle when the converter is performing: (a) lagging rated reactive power with NLC; (b) leading rated reactive power with NLC; (c) lagging rated reactive power with PSC-PWM; (d) leading rated reactive power with PSC-PWM.



Source: Elaborated by the author.

range of voltage ripple than PSC-PWM. This characteristic is intrinsic of the sorting and selection algorithm.

Figure 31 – Capacitor voltage dynamics on the upper arm of phase A.



Source: Elaborated by the author.

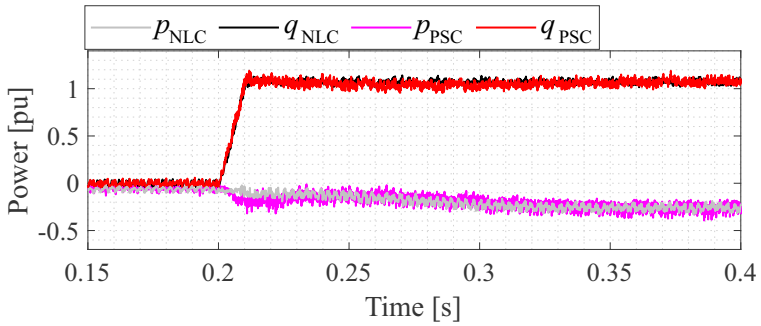
2.7.2 Experimental Results

To validate the MMC-STATCOM control behavior during the transient, the converter is started with null reactive power and the reactive power reference is changed to $q = 1$ pu (leading) in 0.2 s. Since a rate limiter of 0.1 pu/ms is employed in the reference of reactive power, the transient is performed in 10 ms.

Figure 32 presents the active (p) and reactive (q) power with both modulation strategies. As observed, both approaches achieve 0 to 1 pu in 10 ms. A small overshoot is observed during the transient period for both cases.

Figure 33 presents the output current and TDD for both modulation strategies. As observed, the current presents a sinusoidal shape and TDD around 2% for both cases. In

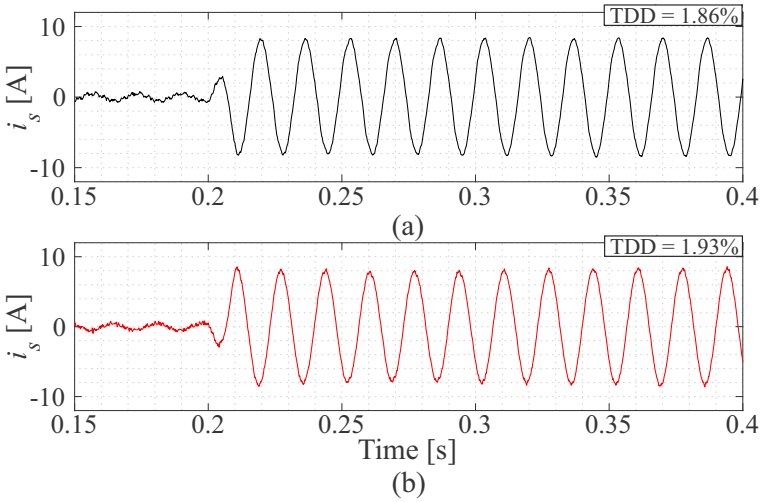
Figure 32 – Experimental response of active (p) and reactive (q) power for NLC and PSC-PWM.



Source: Elaborated by the author.

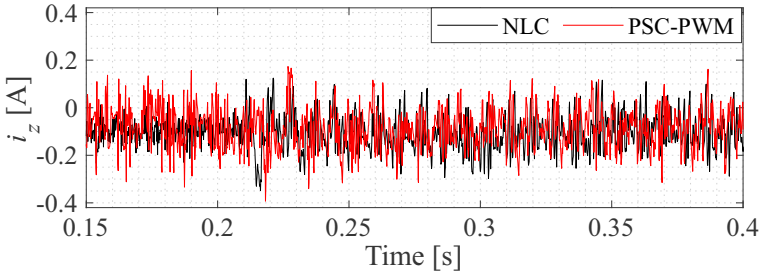
addition, Fig. 34 shows the circulating current for both modulation strategies. As observed, these currents are controlled and their maximum amplitude is lower than 0.5 A for both cases.

Figure 33 – Experimental response of output current synthesized by the MMC-STATCOM with: (a) NLC; (b) PSC- PWM.



Source: Elaborated by the author.

Figure 34 – Experimental response of circulating current for NLC and PSC-PWM.

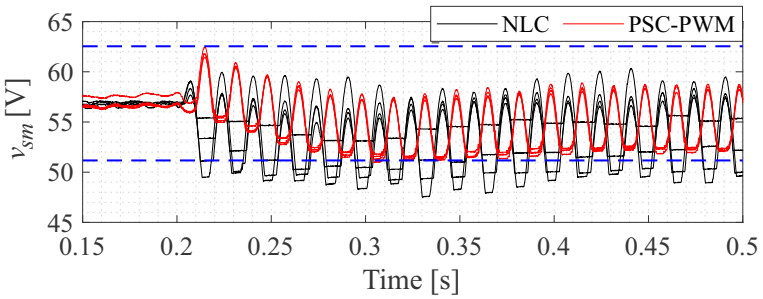


Source: Elaborated by the author.

Figure 35 presents the SM capacitor voltages in one arm for both modulation

strategies. As observed, the transient of the voltages is slower due to the capacitor having to charge to achieve rated operational condition. For PSC-PWM, the arm SM capacitor voltages respect the 10% voltage tolerance (51.7 V to 57.45 V) and have lower spreading among themselves. For NLC, the SM capacitor voltages have a bigger spread and exceed the lower limit of the 10% voltage tolerance.

Figure 35 – Experimental response of SM capacitor voltages on the upper arm of phase B for NLC and PSC-PWM.



Source: Elaborated by the author.

2.8 Chapter Conclusions

In this chapter, the topology, modeling, control strategy and design of MMC-STATCOM were presented. In addition, different MMC-STATCOM designs were computed. The designs considered four different IGBT blocking voltages and two modulation strategies (PSC-PWM and NLC). The specificities of each modulation strategy in terms of control and design were considered and presented.

The dynamic response of the converter was demonstrated by a medium voltage simulation for the cases employing 1.7 kV blocking voltage with both modulation strategies. In addition, the control dynamic behavior was experimentally validated in an MMC setup platform. The results show that the power response follows the reference, besides, supplies the internal losses of the converter. The 10% ripple tolerance of the SM voltages is respected in the steady state for both modulation strategies. Moreover, the 5% TDD limit recommended by IEEE standard is fulfilled. These results demonstrate the effectiveness of the controls employed. In the next chapter, the SM minimum voltage control strategy is presented.

3 Minimum SM Voltage Control

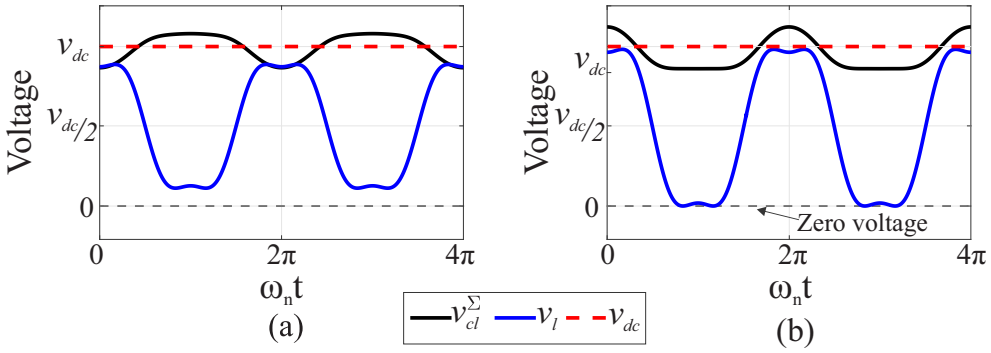
This chapter introduces the main contribution of this work: the minimum SM voltage control (MVC). The potential of working with lower submodule voltage during operational conditions below nominal power is presented. In addition, the MVC is computed for the case studies proposed in Chapter 2. Finally, the converter dynamic behavior with this technique is evaluated through simulation and experimental analyses.

3.1 Limits of Linear Modulation Region

The dc-side voltage is an important parameter to avoid overmodulation (Fujii; Schwarzer; De Doncker, 2005). Moreover, the methodology proposed by Cupertino et al. (2018) and presented in Chapter 2 is defined as a conservative approach. Indeed, this methodology computes the voltage synthesized by the converter without considering the output current displacement angle and amplitude, which leads to a maximum value of V_s (Mendonça, 2021). Thus, the approach of Mendonça et al. (2020a) is considered in this chapter. In this approach, the minimum dc-side voltage design is computed considering the limits of the modulator linear region ($0 \leq n_l \leq 1$).

Figure 36 (a) and (b) illustrate the waveforms for lower arm inserted voltages (v_l) and the sum of capacitor voltages of the lower arm (v_{cl}^{Σ}) in the limit of the modulator linear region when the converter performs lagging and leading reactive power, respectively. When the converter performs lagging reactive power, the inserted voltage is limited by v_{cl}^{Σ}. On the other hand, a gap between the inserted voltage v_l and the sum of capacitor voltages v_{cl}^{Σ} is observed when the converter performs leading reactive power. Thus, lower dc-side voltage is required when the converter performs leading reactive power.

Figure 36 – Inserted voltage of lower arm and sum of capacitor voltages when the converter performs: (a) lagging reactive power; (b) leading reactive power.



Source: Adapted from Sousa et al. (2020).

Moreover, as expressed in Eq. (2.18), the inserted voltage v_l is related to the output voltage. Therefore, different from traditional two-level converters, MMC has a non-negligible voltage ripple that limits the maximum output voltage, $\hat{V}_s$ (Sharifabadi et al., 2016). In addition, the voltage drop of the converter inductances also impacts these limits. This will be discussed later in this chapter.

Considering the symmetry among the converter arms, only the lower arm of one phase is analyzed. It is assumed that the error in the sum of capacitor voltages estimation is negligible. Moreover, by neglecting the harmonics in the circulating current, the internal voltage reference is given by (Sharifabadi et al., 2016):

$$v_z^* \approx \frac{v_{dc}}{2}. \tag{3.1}$$

Moreover, 1/6 of third harmonic voltage injection is considered to extend the region of linear operation of the converter. Considering that positive sequence reactive power is controlled at the grid point of common coupling, the output voltage reference is given by:

$$v_s^* = \hat{V}_s \cos(\omega_n t) - \frac{\hat{V}_s}{6} \cos(3\omega_n t), \tag{3.2}$$

where ω_n is the grid frequency in rad/s. The converter output current is given by:

$$i_s = \hat{I}_s \cos(\omega_n t - \phi), \tag{3.3}$$

where $\hat{I}_s$ is the output current amplitude and ϕ is the displacement angle of the output current. The estimation of the sum of the capacitor voltages presented in (2.18) is given by:

$$\tilde{v}_{cl}^{\Sigma} = v_{dc} + \Delta v_{cl}^{\Sigma}, \tag{3.4}$$

where Δv_{cl}^{Σ} is the sum of capacitor voltage ripples, given by (Mendonça et al., 2020a):

$$\Delta v_{cl}^{\Sigma} = \frac{N}{2Cv_{dc}} (\Delta W_{\Sigma} - \Delta W_{\Delta}) \tag{3.5}$$

where ΔW_{Σ} and ΔW_{Δ} are given by (Mendonça et al., 2020a):

$$\Delta W_{\Sigma} = -\frac{\hat{V}_s \hat{I}_s}{4\omega_n} \sin(2\omega_n t - \phi) + \frac{\hat{V}_s \hat{I}_s}{24\omega_n} \sin(2\omega_n t + \phi) + \frac{\hat{V}_s \hat{I}_s}{48\omega_n} \sin(4\omega_n t - \phi) \tag{3.6}$$

$$\Delta W_{\Delta} = -\frac{v_{dc} \hat{I}_s}{2\omega_n} \sin(\omega_n t - \phi) - \frac{2\hat{V}_s i_z}{\omega_n} \sin(\omega_n t) + \frac{\hat{V}_s i_z}{9\omega_n} \sin(3\omega_n t) \tag{3.7}$$

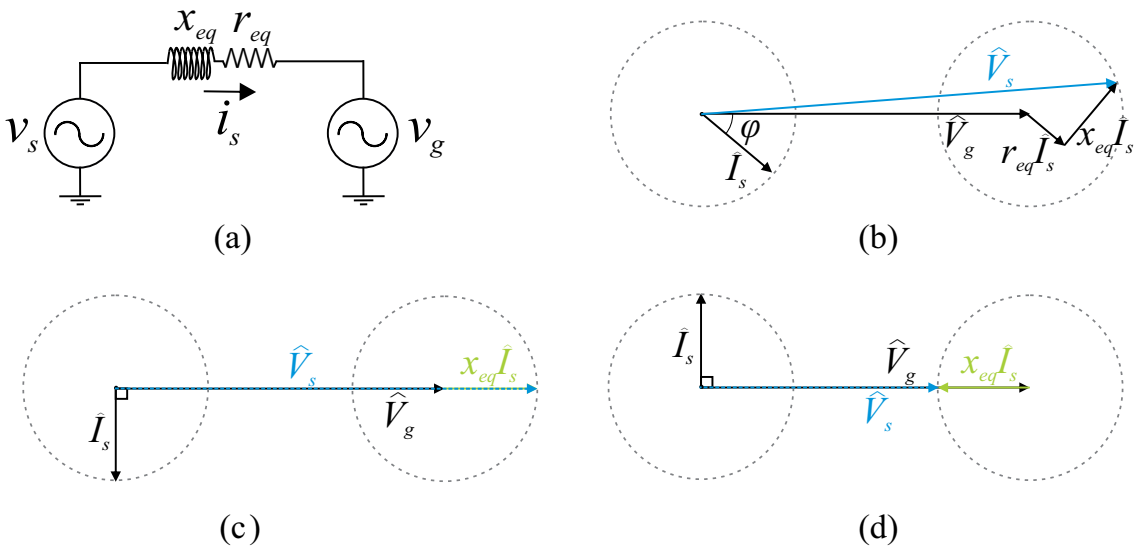
Moreover, i_z is given by (Mendonça et al., 2020a):

$$i_z = \frac{\hat{V}_s \hat{I}_s \cos(\phi)}{2v_{dc}} \tag{3.8}$$

The MMC-STATCOM average model and the phasor diagram are illustrated in Fig. 37 (a) and (b), respectively. As observed, $\hat{V}_s$ is a function of the output current displacement angle of the converter (ϕ). By neglecting the arm resistance r_{eq}, the output voltage required for grid-connected applications when the converter injects current ($\hat{I}_s$) can be computed by inspection of Fig. 37 (b), as follows (Mendonça et al., 2020a):

$$\hat{V}_s = \sqrt{\left[\hat{V}_g\left(1 + \Delta V_g\right) + x_{eq}\hat{I}_s \sin(\phi)\right]^2 + \left[x_{eq}\hat{I}_s \cos(\phi)\right]^2}. \tag{3.9}$$

Figure 37 – MMC-STATCOM: (a) average model; (b) generic phasor diagram; (c) phasor diagram for leading reactive power operation; (d) phasor diagram for lagging reactive power operation.



Source: Elaborated by the author.

Figure 37 (c) and (d) presents the phasor diagrams for leading reactive power ($\phi = 90^o$) and lagging reactive power ($\phi = -90^o$) operations neglecting the arm resistance ($r_{eq} = 0$). As observed, these conditions represent the maximum and minimum requirement of $\hat{V}_s$.

By replacing Eq. (3.1), (3.2) and (3.4) into Eq. (2.19) and (2.20):

$$n_l = \frac{\frac{v_{dc}}{2} + \hat{V}_s \cos(\omega_n t) - \frac{\hat{V}_s}{6}\cos(3\omega_n t)}{v_{dc} + \frac{N}{2Cv_{dc}}(\Delta W_\Sigma - \Delta W_\Delta)}. \tag{3.10}$$

Considering Eq. (3.6)-(3.10) and the maximum insertion index (i.e. $n_l = 1$), the reachable output voltage limited by the sum of capacitor voltages is the maximum and a third-degree polynomial of v_{dc} is obtained (Mendonça et al., 2020a):

$$v_{dc,r}^3 + dv_{dc,r}^2 + ev_{dc,r} + f = 0, \tag{3.11}$$

where d, e and f are given by:

$$d = -\frac{N\hat{I}_s}{2\omega_n C}\sin(\frac{\pi}{6} - \phi) - \sqrt{3}\hat{V}_s, \tag{3.12}$$

$$e = -\frac{N\hat{V}_s\hat{I}_s}{4\omega_n C}\sin(\frac{\pi}{3} - \phi) + \frac{N\hat{V}_s\hat{I}_s}{24\omega_n C}\sin(\frac{\pi}{3} + \phi) + \frac{N\hat{V}_s\hat{I}_s}{48\omega_n C}\sin(\frac{2\pi}{3} - \phi), \tag{3.13}$$

$$f = \frac{4N\hat{V}_s^{\,2}\hat{I}_s\cos(\phi)}{9\omega_n C}. \tag{3.14}$$

From the polynomial equation (Eq. (3.11)), the roots are computed to obtain the minimum dc-side voltage.

In the region where n_l is limited by the zero voltage (i.e. $n_l = 0$), the MMC behavior is similar to that of two-level converters, and the minimum dc-side is given by (Cupertino et al., 2020):

$$v_{dc,0} = \sqrt{3}\hat{V}_s. \tag{3.15}$$

As observed in Eq. (3.15), the minimum dc-side voltage is the same expected for two-level converters with non-negligible dc-side voltage ripple.

Furthermore, the minimum dc-side voltage for operation in the linear region is given by the maximum value between $v_{dc,0}$ and the polynomial roots of Eq. (3.11) ($v_{dc,r}$) (Cupertino et al., 2020):

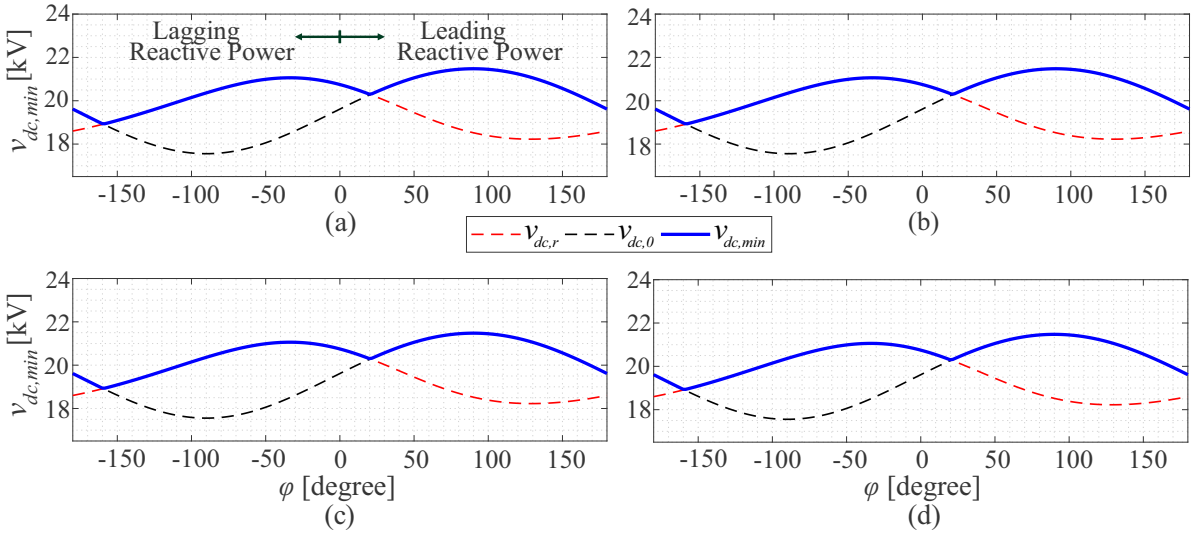
$$v_{dc,min} = \max(v_{dc,0}, v_{dc,r}). \tag{3.16}$$

The coefficients of Eq. (3.11) are a function of the SM capacitance. As observed in Eq. (2.72), the capacitance is also a function of the dc-side voltage. Thus, the capacitance or the dc-side voltage must be defined to initiate the analyses. In this work, the capacitance is computed considering the conservative dc-side voltage design (Eq. (2.68) and (2.70)). Moreover, 40 kJ/MVA of energy storage requirement is employed. Since this energy storage

requirement is considered, the same minimum dc-side voltage is computed for designs that differ only by the modulation strategy and SM capacitance.

Therefore, the minimum dc-side voltage can be computed by Eq. (3.16) for the different semiconductor blocking voltages, as shown in Fig. 38. The parameters of Tab. 3 and Tab. 4 are considered. As observed, the required dc-side voltage varies according to the output current displacement angle. Moreover, since the same equivalent inductance is considered for all cases, similar values of minimum dc-side voltage are found for the case studies.

Figure 38 – Minimum dc-side voltage for operation in the linear region of the modulator as a function of the operating angle of the output current (ϕ) for cases with blocking voltage: (a) 1.7 kV; (b) 3.3 kV; (c) 4.5 kV; (d) 6.5 kV. *Considerations: Parameters of Tab. 3 and 4 and SM capacitance considering 40 kJ/MVA of energy storage requirement.*



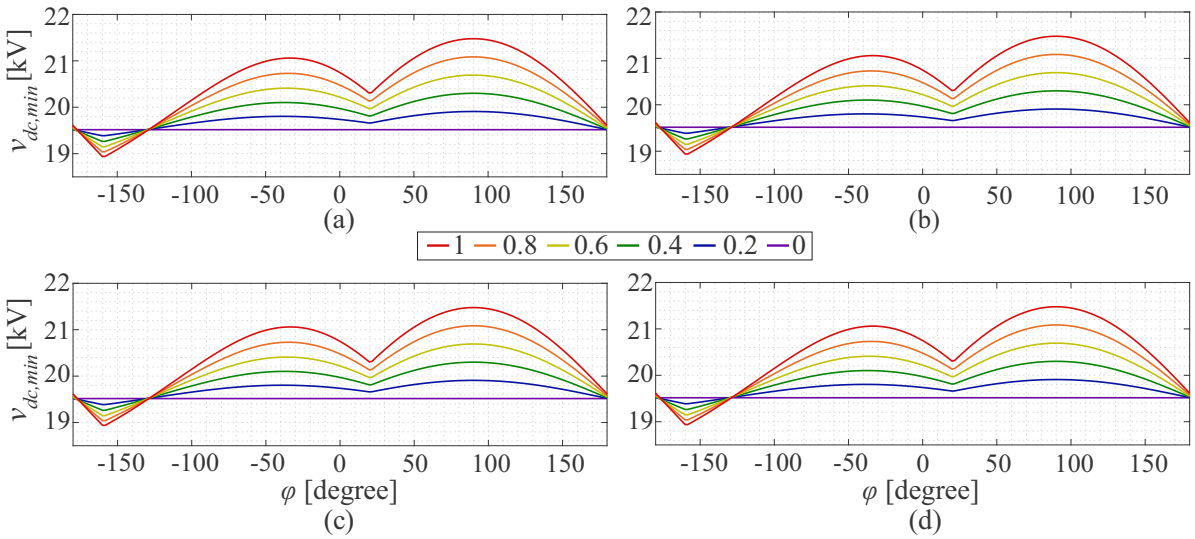
Source: Elaborated by the author.

The minimum dc-side voltage is also a function of output current amplitude. Fig. 39 presents $v_{dc,min}$ curves considering 0 up to 1 pu of nominal output current amplitude (I_{sn}) for all case studies. As observed for each case, the converter requires lower $v_{dc,min}$ for lower output current amplitude (lower operational conditions). This dependence is explored in the next section.

3.2 MVC Strategy

As discussed in the last section and observed in Fig. 39, the minimum dc-side voltage is a function of the displacement angle and amplitude of the output current. Consequently, when the converter STATCOM application is considered, the $v_{dc,min}$ is a function of reactive power (q). Indeed, the module of the reactive power is proportional to

Figure 39 – Minimum dc-side voltage as a function of the operating angle and peak of the output current for cases with blocking voltage: (a) 1.7 kV; (b) 3.3 kV; (c) 4.5 kV; (d) 6.5 kV. *Considerations: Parameters of Tab. 3 and 4 and SM capacitance considering 40 kJ/MVA of energy storage requirement.*



Source: Elaborated by the author.

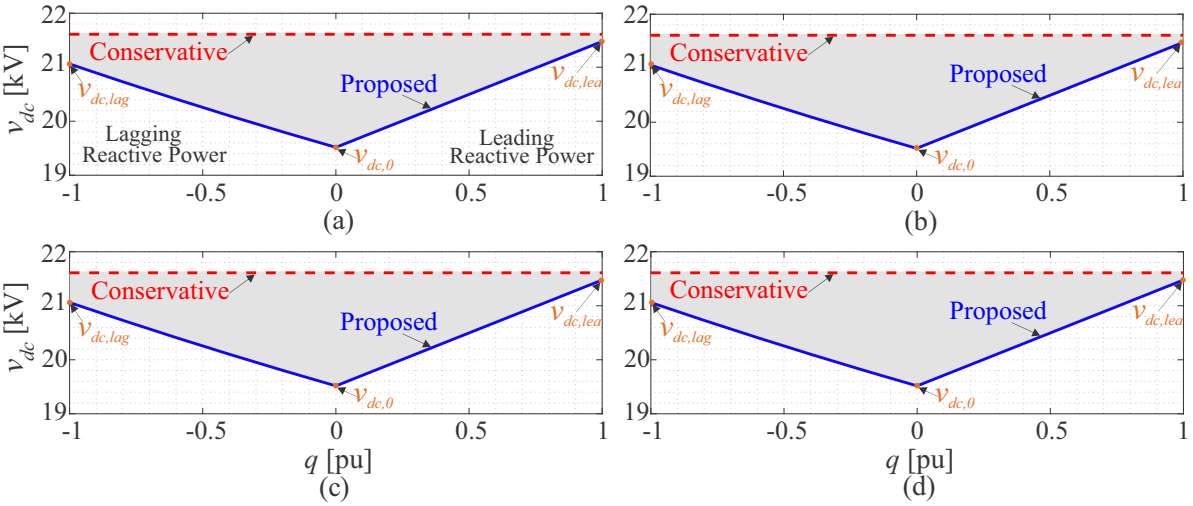
the output current amplitude and its characteristic (lagging or leading) is related to the displacement angle.

Thus, the $v_{dc,min}$ for MMC-STATCOM is found at ±90 degrees of each curve of Fig. 39. Nevertheless, the converter needs to make up for internal losses in practical applications. For this reason, the maximum $v_{dc,min}$ in lagging ($\phi < 0$) and leading ($\phi > 0$) output current is considered for each current amplitude. Following these considerations, Fig. 40 shows the $v_{dc,min}$ for each case study as a function of the MMC-STATCOM operation. The voltages $v_{dc,lag}$, $v_{dc,lea}$ and $v_{dc,0}$ are the minimum dc-side voltage at rated lagging reactive power, rated leading reactive power and hot standby operation, respectively.

The conservative dc-side voltage computed in Chapter 2 is highlighted in Fig. 40. As observed, for all case studies the minimum dc-side voltage (proposed v_{dc}) is lower than conservative v_{dc}. In addition, the proposed v_{dc} is similar among the cases.

Given these considerations, the MVC strategy is proposed. The potential MVC consists in controlling the MMC-STATCOM according to the dc-side voltage based on the proposed curves of Fig. 40. Indeed, since the SM voltage reference v_{sm}^{*} is proportional to dc-side voltage, as defined in Eq. (2.26), the SM voltages are maintained at the minimum for each operational condition. Consequently, the voltage on the SM components is lower than in the conservative design.

Figure 40 – Minimum dc-side voltage as a function of the reactive power operation for: (a) 1.7 kV; (b) 3.3 kV; (c) 4.5 kV; (d) 6.5 kV. *Considerations: Parameters of Tab. 3 and 4 and SM capacitance considering 40 kJ/MVA of energy storage requirement.*



Source: Elaborated by the author.

3.3 Potential of Losses Reduction

A physics-inspired empirical model of the IGBT power module can be used to investigate the potential of reducing losses of MVC. For this purpose, the average and rms currents in each semiconductor device are very useful to estimate the conduction and switching losses of the MMC-STATCOM.

3.3.1 Current Stress

The mathematical model is based on the following assumptions:

- The ripple of the capacitor voltage is not considered;
- The high-frequency component present in the currents is negligible;
- Delays and non-idealities present in the modulation process are negligible;
- The losses are evenly distributed among the converter SMs.

Considering these assumptions and replacing Eq. (3.1), (3.2) and (3.4) into Eq. (2.19) and (2.20), the insertion index is given :

$$n_u = \frac{\frac{v_{dc}}{2} - \hat{V}_s \cos(\omega_n t) + \frac{\hat{V}_s}{6} \cos(3\omega_n t)}{v_{dc}}. \tag{3.17}$$

Considering the relationship:

$$\hat{V}_s = m\frac{v_{dc}}{2}, \tag{3.18}$$

where m is the maximum modulation index. By replacing Eq. (3.18) into Eq. (3.17), the insertion index can be represented by:

$$n_u = \frac{1}{2} - \frac{m}{2}\cos(\omega_n t) + \frac{m}{12}\cos(3\omega_n t). \tag{3.19}$$

To keep the converter losses and the rms arm currents at a minimum, i_z should be pure dc, i.e. $i_z = \frac{i_{dc}}{3}$ (Sharifabadi et al., 2016). Since STATCOM operation is considered, $i_{dc} = 0$, thus, $i_z = 0$. Following this assumption and replacing Eq. (3.3) into Eq. (2.4):

$$i_u = \frac{\hat{I}_s}{2}\cos(\omega_n t). \tag{3.20}$$

The average current in the semiconductor devices is given by (Mendonça et al., 2022):

$$i_{SD,avg} = \frac{1}{2\pi}\int_{\theta_1}^{\theta_2} n_u \times i_u d\omega t, \tag{3.21}$$

where $\theta_1 = \pi$ rad and $\theta_2 = 2\pi$ rad are the angles that define the zero crossing of the upper arm current. The rms current of the semiconductor devices is given by (Mendonça et al., 2022):

$$i_{SD,rms} = \sqrt{\frac{1}{2\pi}\int_{\theta_1}^{\theta_2} n_u \times i_u^2 d\omega t}, \tag{3.22}$$

Solving Eq. (3.21) and (3.22), the average and rms currents are obtained (Mendonça et al., 2022):

$$\begin{cases} i_{SD,avg} = \frac{\hat{I}_s}{4\pi}, \\ i_{SD,rms} = \frac{\hat{I}_s}{4\sqrt{2}}. \end{cases} \tag{3.23}$$

As observed in Eq. (3.23), the average and rms currents are independent of the modulation index for MMC-STATCOM.

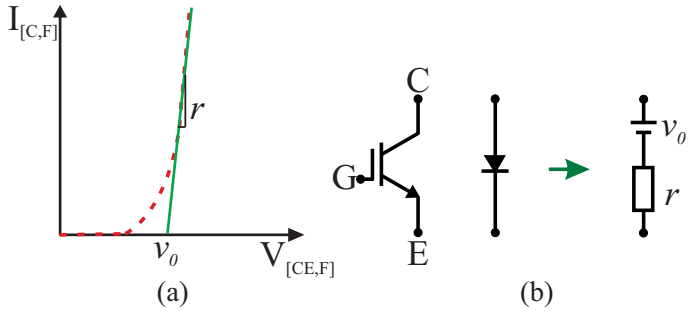
3.3.2 Power Losses

The average conduction losses are given by the integration of forward losses. These losses can be expressed by (Baliga, 2008):

$$P_{cd,SD} = v_0 \times i_{SD,avg} + r \times i_{SD,rms}^2, \tag{3.24}$$

where v_0 and r are the forward characteristics represented in Fig. 41.

Figure 41 – Approximation of an IGBT (or diode) forward characteristic by v_0 and r.



Source: Adapted from Huber and Kolar (2017).

The arm current flows through a semiconductor device per SM at any instant in time. Considering PSC-PWM modulation, diodes and IGBTs present, approximately, the same average and rms currents. Therefore, the MMC-STATCOM conduction losses are given by:

$$P_{cd,T} = 12N(P_{cd,IGBT} + P_{cd,diode}). \tag{3.25}$$

The switching energy of an IGBT is the sum of all turn-on and turn-off energies. For diodes, the turn-on energy can be disregarded and only the recovery energy counts. Moreover, the dc voltage over the semiconductor devices can vary in different applications. Thus, the dependence of the switching energy on the dc voltage needs to be considered (ABB, 2009). In this work, the dc voltage over the IGBT and diodes is approximated to the SM voltage reference.

The average switching losses are given by the integration of switching energies (Baliga, 2008). Moreover, the switching losses during half a grid period can be estimated based on the SM average current, as (ABB, 2009):

$$P_{sw,SD} = f_{sw} \times K_{sw} \times (A_{sw} + B_{sw} i_{SD,avg} + C_{sw} i^2_{SD,avg}) \frac{v^*_{sm}}{V_{bk,n}}, \tag{3.26}$$

where $A_{sw,}$, B_{sw} and C_{sw} are parameters related to the IGBT module that can be fitted from empirical data. K_{sw} represents the blocking voltage dependence of the switching energies. Note that three individual K_{sw} exist for turn-off, turn-on and diode recovery losses, i. e., K_{on}, K_{off} and K_{rec}. Finally, the MMC-STATCOM switching losses are given by:

$$P_{sw,T} = 12N(P_{sw,IGBT} + P_{sw,diode}). \tag{3.27}$$

3.3.3 MVC and Power Losses

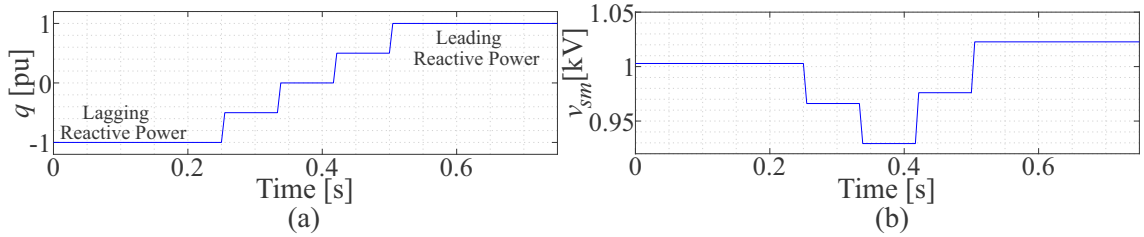
The MVC is a variable dc-side voltage control strategy that directly affects the SM voltage and, consequently, the dc voltage over the SM. As observed in Eq. (3.24)-(3.25), the operating voltage of the SM is unrelated to the conduction losses. Therefore, the conduction losses are not affected by this strategy. On the other hand, Eq. (3.26) demonstrates that the switching losses are proportional to the SM voltage.

Consequently, MVC directly affects the switching losses of SM semiconductor devices. Moreover, the semiconductor device losses affect the thermal cycling of these components, which affects their lifetime (Antonopoulos et al., 2020), as will be discussed in the next chapter. Regarding the SM capacitors, the lifetime of these components is directly affected by the voltage imposed on them (Electronicon, 2014). Therefore, the MVC strategy has the potential to reduce the converter losses, by reducing switching losses, and to improve the lifetime of SM components, resulting in higher MMC-STATCOM reliability at system-level. The grey area of Fig. 40 represents the region of switching losses reduction and lifetime extension when MVC is employed.

3.4 Simulation Analyses

This section presents the MMC-STATCOM dynamic response employing MVC. Simulations in PLECS environment are performed to demonstrate the dynamic behavior of the MMC-STATCOM. This demonstration is performed considering the case studies of blocking voltage 1.7 kV (C_{P17} and C_{N17}). The reactive power profile considered is presented in Fig. 42 (a). Moreover, the SM voltage reference profile considering MVC is shown in Fig. 42 (b).

Figure 42 – Dynamic profile of: (a) reactive power; (b) SM voltage reference with MVC. *Remark: The reactive power exchange during the transients happens at 0.1 pu/ms.*

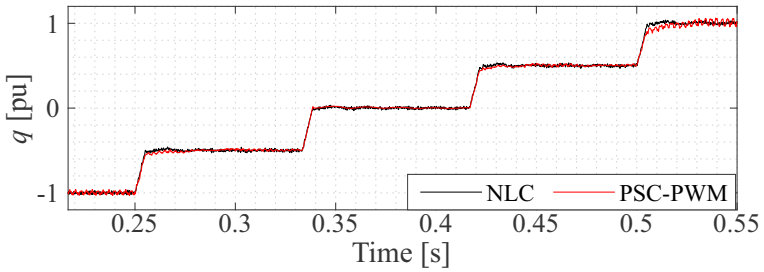


Source: Elaborated by the author.

Figure 43 shows the reactive power performed by the MMC-STATCOM. The behavior of reactive power is similar to response without MVC. In fact, for both modulation strategies, the reactive power response follows the reactive power profile. In addition,

PSC-PWM presents higher oscillations than NLC in rated reactive power operation. Besides, PSC-PWM presents a slower reactive power response than NLC.

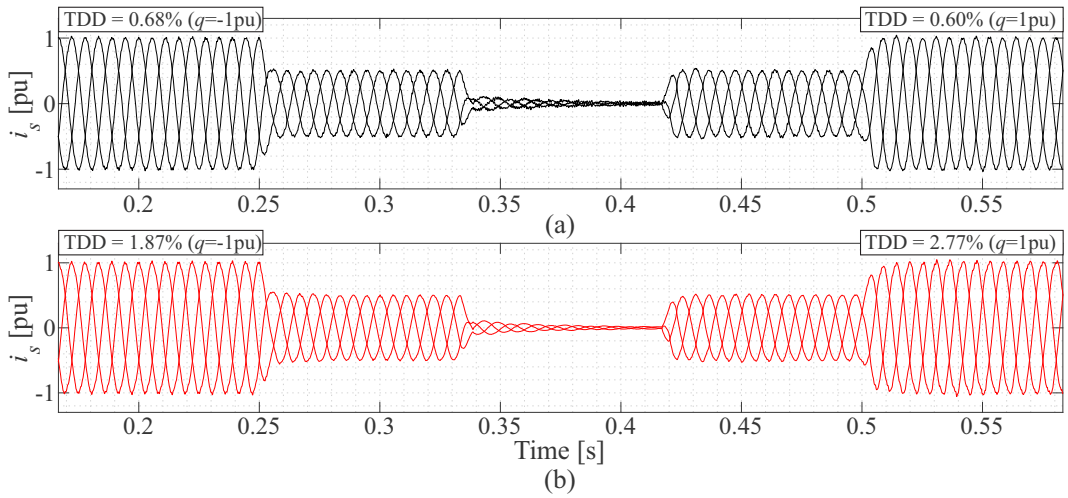
Figure 43 – Instantaneous reactive power synthesized by the MMC-STATCOM.



Source: Elaborated by the author.

Figure 44 shows the output current. As observed in Fig. 44 (a) and (b), for both modulation strategies, the output current follows the reactive power profile. In addition, Fig. 44 shows the output current TDD when the converter performs rated lagging and leading reactive power. Moreover, NLC presents lower values of TDD than PSC-PWM for both operational conditions. However, both cases fulfill IEEE TDD standards.

Figure 44 – Output current synthesized by the MMC-STATCOM with: (a) NLC; (b) PSC-PWM. *Remark: Considering the base current of 1005.8 A.*

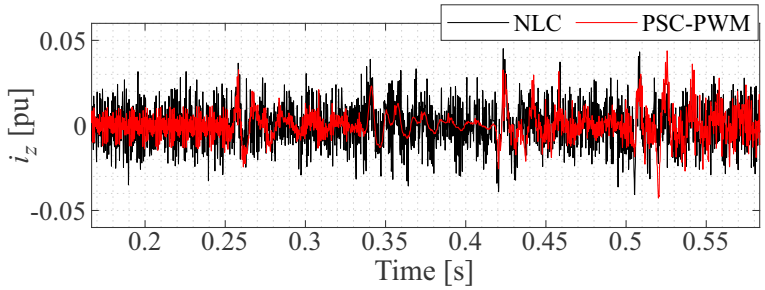


Source: Elaborated by the author.

In terms of circulating current, the dynamic responses are presented in Fig. 45. As observed, PSC-PWM presents similar oscillations to the NLC when the converter is performing rated lagging and leading reactive power. In the other conditions, NLC presents higher oscillations than PSC-PWM.

Fig. 46 demonstrates the effect of the MVC in the SM capacitor voltages for both modulation strategies. As observed, the SM voltages follow the references of reactive power and SM voltage of Fig. 42. Furthermore, the SM voltage averages are lower when

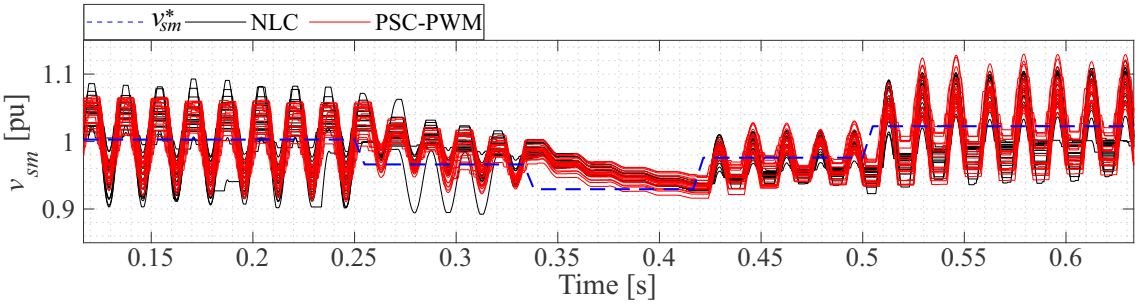
Figure 45 – Dynamic behavior of the circulating current of phase A. *Remark: Considering the base current of 1005.8 A.*



Source: Elaborated by the author.

the converter performs lagging reactive power than when the converter performs leading reactive power for these case studies.

Figure 46 – Capacitor voltage dynamics on the upper arm of phase A.



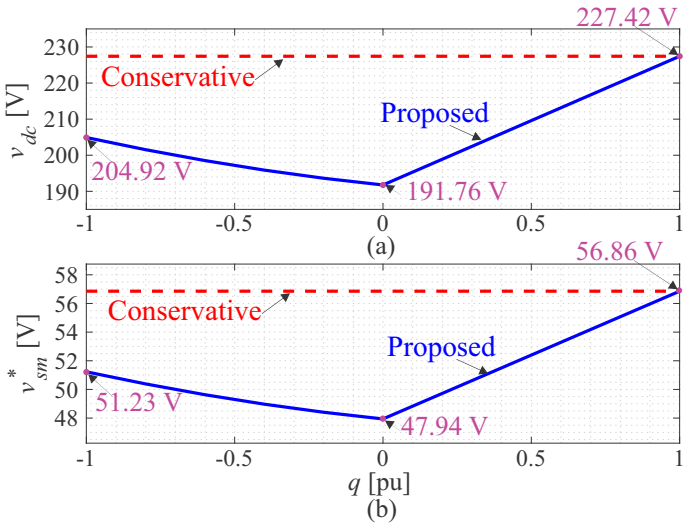
Source: Elaborated by the author.

3.5 Experimental Validation

The minimum SM voltage control is verified in the laboratory MMC-STATCOM setup presented in subsection 2.6.2. Fig. 47 (a) presents the minimum dc-side voltage for MMC-STATCOM setup for conservative and MVC approaches. Moreover, Fig. 47 (b) shows the SM voltage reference considered in the controllers as a function of the reactive power operation. For conservative and MVC approaches, the voltage margin of 12 V per SM is added to compensate for the voltage drops of the circuit. As observed, v_{dc} and v^*_{sm} computed with MVC are lower than the conservative approach in all operational conditions.

As observed in Fig. 47, the most critical operational condition related to the MVC technique is when the converter is operating with null reactive power ($q = 0$ pu) and the grid requires its full capacity of lagging or leading reactive power ($q = \pm 1$ pu). To evaluate these scenarios, two tests are performed:

Figure 47 – For each operational condition: (a) minimum dc-side voltage; (b) SM voltage reference.



Source: Elaborated by the author.

1. Leading operation: the converter is started with null reactive power and the reactive power reference is changed to 1 pu in 0.2 s.

2. Lagging operation: the converter is also started with null reactive power and the reactive power reference is changed to - 1 pu in 0.2 s.

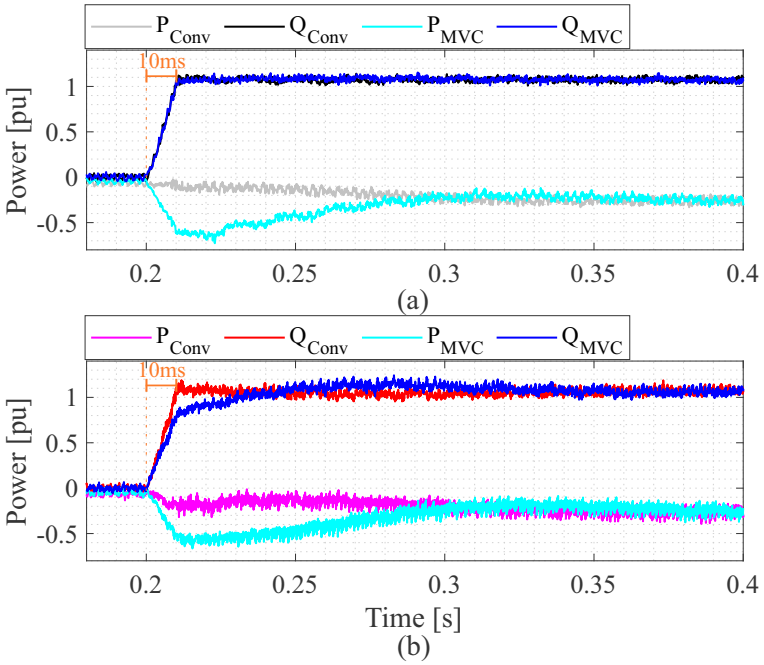
A rate limiter of 0.1 pu/ms is employed in the reference of reactive power in the controller to avoid protection activation during the experimental tests. The results of these tests are presented in the next subsections.

3.5.1 Leading Operation

Figure 48 (a) and (b) present the active and reactive power with conservative and MVC approaches for NLC and PSC-PWM, respectively. As observed in Fig. 48 (a) for NLC, both approaches achieve 1 pu of reactive power in 10 ms. On the other hand, for PSC-PWM the reactive power takes 40 ms to achieve 1 pu with MVC and 10 ms with the conservative approach (see Fig. 48 (b)). This slower response is also observed in the SM capacitor voltages (see Fig. 51 (b)). This behavior suggests that the individual voltage balancing control used with PSC-PWM could be having a response insufficiently fast with MVC.

Regarding the active power, for both modulation strategies with MVC, a higher overshoot during the transient period than with the conservative approach is observed. This overshoot with MVC occurs due to the fact that the capacitors require more energy to change from 0 pu to 1 pu of reactive power. Indeed, with the conservative approach, the SM average voltage (approximately v^*_{sm}) is 56.86 V for both operational conditions, while

Figure 48 – Experimental response of active (P) and reactive (Q) power with Conservative (Cons) and MVC approaches for: (a) NLC; (b) PSC-PWM.



Source: Elaborated by the author.

with MVC this value changes from 47.94 V to 56.86 V (see Fig. 47 (b)). Furthermore, the current presents a sinusoidal shape and TDD around 2% for all cases. Moreover, the TDD is lower for PSC-PWM and higher for NLC with MVC than the conservative approach.

Figure 50 (a) and (b) show the circulating current with conservative and MVC approaches for NLC and PSC-PWM, respectively. As observed for both approaches, these currents are controlled and their maximum amplitude is lower than 0.5 A for both cases.

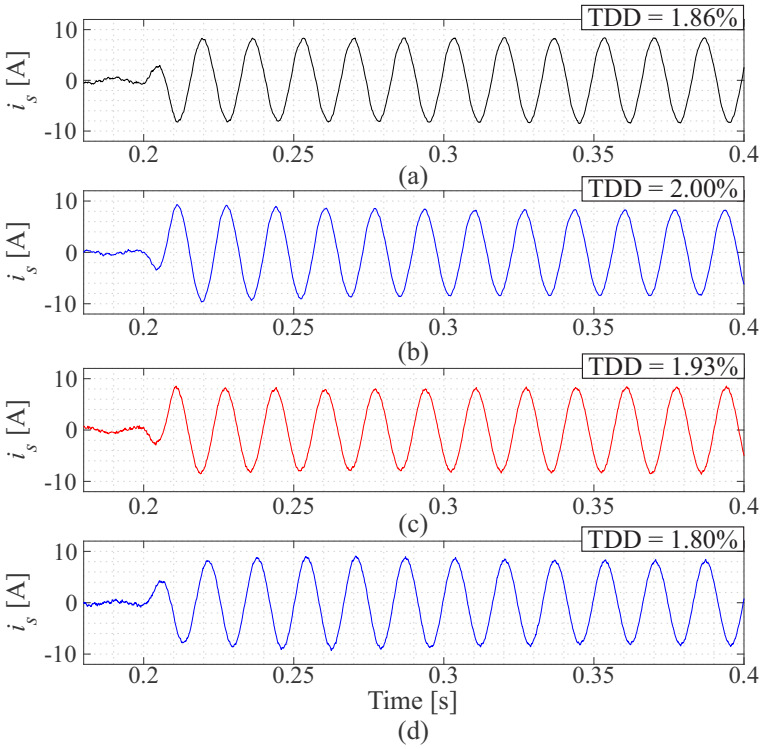
Figure 51 (a) and (b) present the SM capacitor voltages in one arm with conservative and MVC approaches for NLC and PSC-PWM, respectively. As observed, the SM voltages follow the SM voltage reference of Fig. 47 (b). In addition, the transient of the voltages is slower with MVC due to the capacitor requiring more energy to achieve rated operational condition with this technique. Moreover, the SM capacitor voltages respect the superior limit of the 10% voltage tolerance for both modulation strategies with MVC.

Figure 52 presents the inserted voltage (v_u) and the sum of capacitor voltages (v_{cl}^{Σ}) for both modulation strategies and control approaches. As observed, the limits of the linear region are respected in all cases. Therefore, no overmodulation is observed.

3.5.2 Lagging Operation

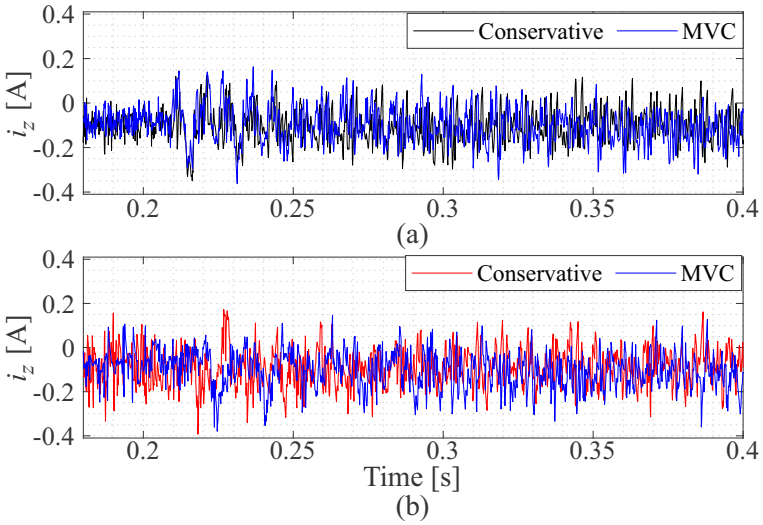
Figure 53 (a) and (b) present the active and reactive power with conservative and MVC approaches for NLC and PSC-PWM, respectively. As observed in Fig. 53 (a) for

Figure 49 – Experimental response of output current: (a) conservative approach with NLC; (b) MVC with NLC; (c) conservative approach with PSC-PWM; (d) MVC with PSC-PWM.



Source: Elaborated by the author.

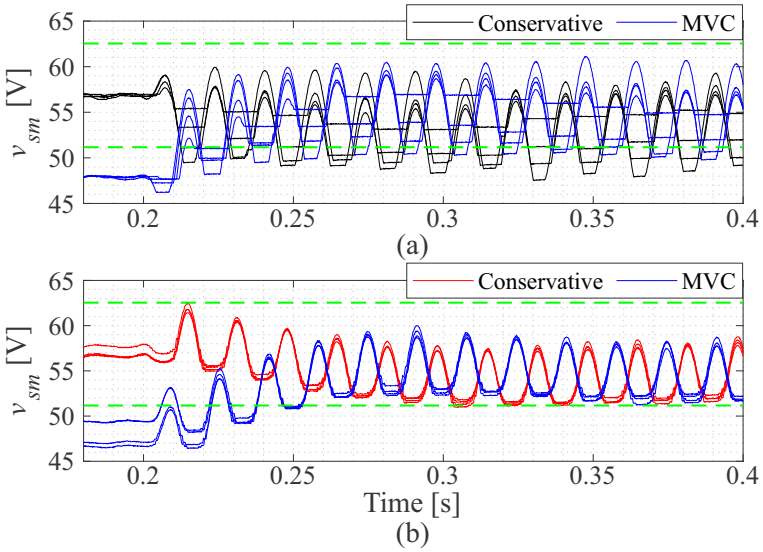
Figure 50 – Experimental response of circulating current with the conservative approach and MVC for: (a) NLC; (b) PSC-PWM.



Source: Elaborated by the author.

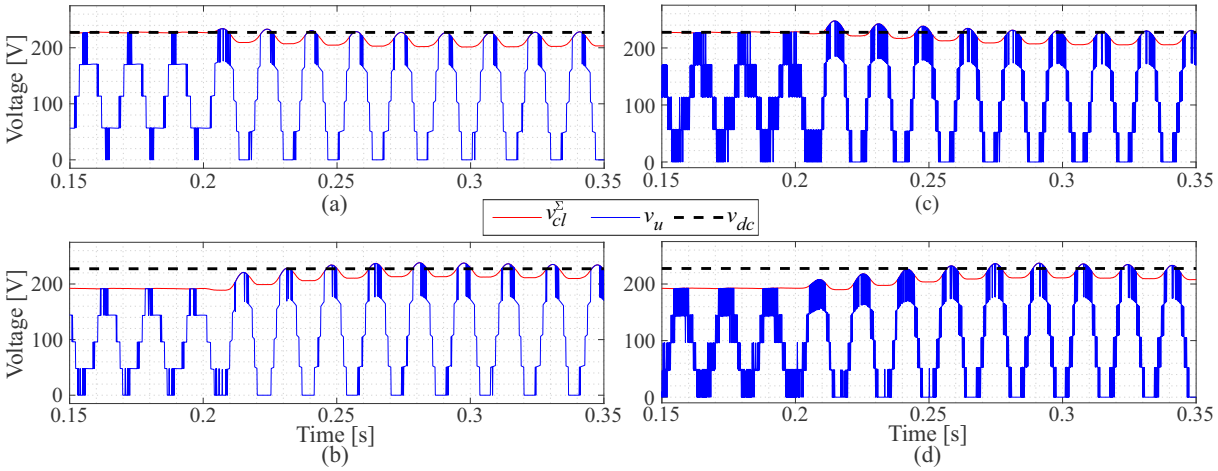
NLC, both approaches achieve -1 pu of reactive power in 10 ms. On the other hand, for PSC-PWM the reactive power takes 80 ms to achieve -1 pu with both approaches (see Fig. 53 (b)).

Figure 51 – Experimental response of SM capacitor voltages on the upper arm of phase B with the conservative approach and MVC for: (a) NLC; (b) PSC-PWM.



Source: Elaborated by the author.

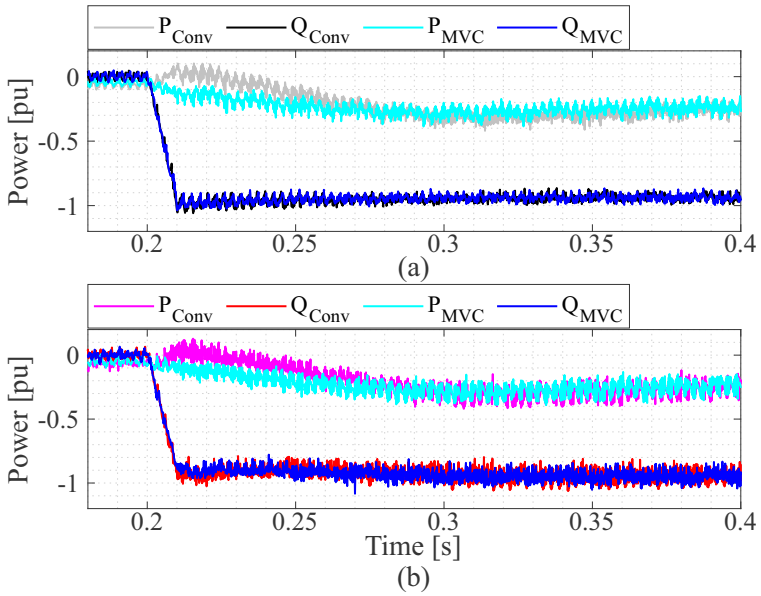
Figure 52 – Experimental response of inserted voltage and sum of capacitor voltages on the upper arm of phase B for: (a) NLC with conservative approach; (b) NLC with MVC; (c) PSC-PWM with conservative approach; (d) PSC-PWM with MVC.



Source: Elaborated by the author.

Regarding the active power, for both modulation strategies with MVC, a higher overshoot during the transient period than with the conservative approach is observed. Also, the active power takes around 100 ms to achieve a steady state. The higher overshoot also appears in the grid and circulating currents, as shown in Fig. 54. As discussed in the last subsection, this overshoot occurs due to the fact that, with MVC, the capacitors require more energy to change from 0 pu to -1 pu of reactive power. Indeed, with the conservative approach the SM average voltage (approximately v_{sm}^{*}) is 56.86 V for both operational conditions, while with MVC this value changes from 47.94 V to 51.23 V (see

Figure 53 – Experimental response of active (P) and reactive (Q) power with Conservative (Cons) and MVC approaches for: (a) NLC; (b) PSC-PWM.



Source: Elaborated by the author.

Fig. 47 (b)). Furthermore, the current presents a sinusoidal shape and TDD around 2% for all cases. Moreover, the TDD is higher with MVC for NLC and lower with MVC for PSC-PWM.

Figure 55 (a) and (b) show the circulating current with conservative and MVC approaches for NLC and PSC-PWM, respectively. As observed for both approaches, these currents are controlled and their maximum amplitude is lower than 0.5 A for both cases.

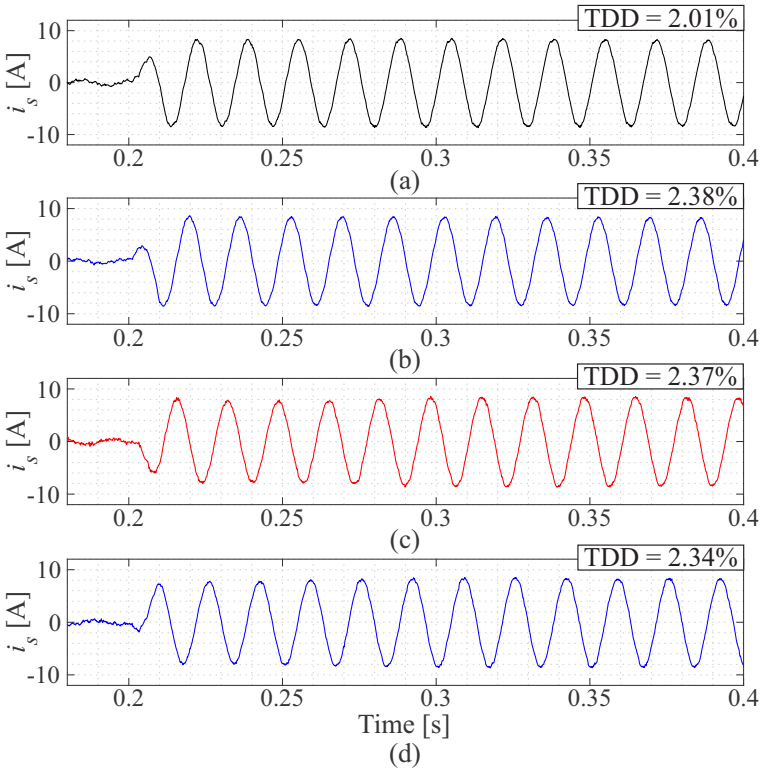
Figure 56 (a) and (b) present the SM capacitor voltages in one arm with conservative and MVC approaches for NLC and PSC-PWM, respectively. As observed, the SM voltages follow the SM voltage reference of Fig. 47 (b). In addition, the transient of the voltages is slower with MVC due to the capacitor requiring more energy to achieve rated operational condition with this technique. Moreover, the SM capacitor voltages respect the superior limit of the 10% voltage tolerance for both modulation strategies with MVC.

Figure 57 presents the inserted voltage (v_u) and the sum of capacitor voltages (v_{cl}^{Σ}) for both modulation strategies and control approaches. As observed, the limits of the linear region are respected in all cases. Therefore, no overmodulation is observed.

3.6 Chapter Conclusions

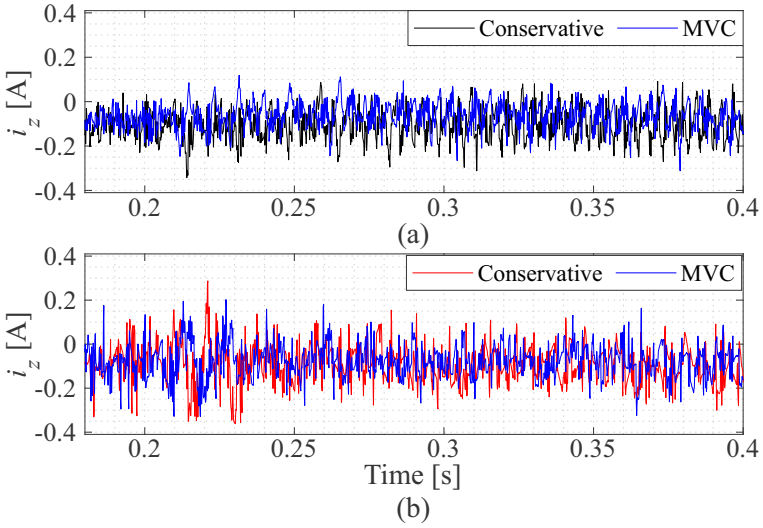
This chapter presented the minimum SM voltage control strategy. The discussion of this strategy considered two modulation schemes: PSC-PWM and NLC. Moreover, designs

Figure 54 – Experimental response of output current: (a) conservative approach with NLC; (b) MVC with NLC; (c) conservative approach with PSC-PWM; (d) MVC with PSC-PWM.



Source: Elaborated by the author.

Figure 55 – Experimental response of circulating current with the conservative approach and MVC: (a) NLC; (b) PSC-PWM.

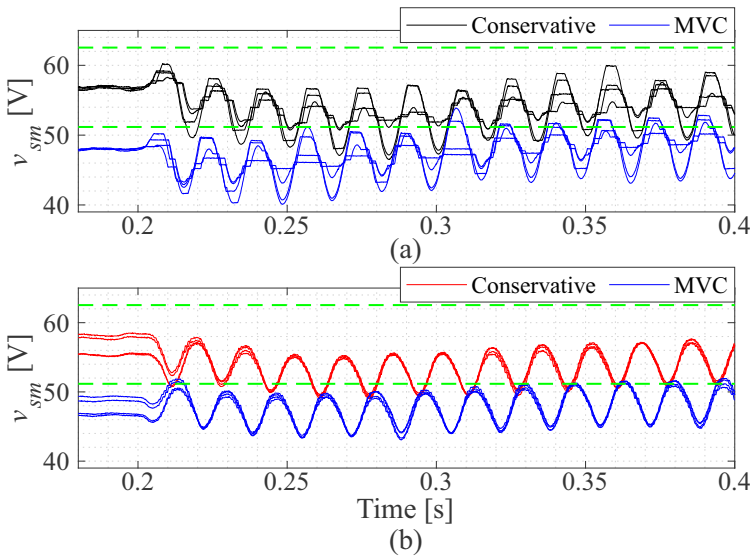


Source: Elaborated by the author.

with four different blocking voltages are considered in simulation analyses. The MVC dynamic behavior was experimentally validated in the MMC setup platform.

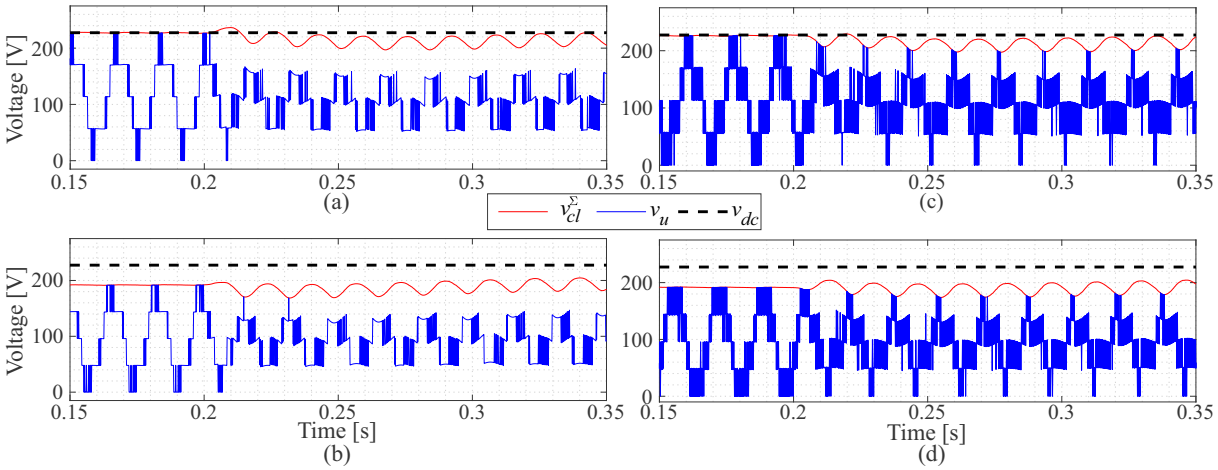
In addition, the potential for reduction of losses was analyzed through modeling of

Figure 56 – Experimental response of SM capacitor voltages on the upper arm of phase B with the conservative approach and MVC for: (a) NLC; (b) PSC-PWM.



Source: Elaborated by the author.

Figure 57 – Experimental response of inserted voltage and sum of capacitor voltages on the upper arm of phase B for: (a) NLC with conservative approach; (b) NLC with MVC; (c) PSC-PWM with conservative approach; (d) PSC-PWM with MVC.



Source: Elaborated by the author.

the power losses of an MMC-STATCOM. The MVC strategy demonstrated the potential to improve the converter efficiency, by reducing switching losses, and improving the lifetime of the SM components, resulting in higher MMC-STATCOM reliability at system-level.

The dynamic response of the MMC-STATCOM with MVC has been demonstrated through simulations for the cases employing 1.7 kV blocking voltage and both modulation strategies. In addition, the MVC dynamic behavior was experimentally validated in the

MMC setup platform. The 10% ripple tolerance of the SM voltages in steady state is respected for both modulation strategies. Moreover, the 5% TDD limit recommended by IEEE standard is met. In addition, the average SM voltage is lower when the converter employs the MVC approach. Additionally, the average SM voltage is lower when the converter performs lagging reactive power than when the converter performs leading reactive power. Moreover, the experimental results demonstrated a slower power response with MVC than with the conservative approach.

Therefore, the analyses of this chapter demonstrate the effectiveness of MVC and its effect on power losses and capacitor voltage.

4 Wear-Out Prediction

This chapter aims to discuss the effect of minimum SM voltage control on the reliability and losses of an MMC-STATCOM. For this purpose, the wear-out failure methodology is introduced as a figure of merit for reliability evaluation. The methodology is focused on semiconductor devices and capacitors. Moreover, the case studies presented in Chapter 2 are considered. The analyses are based on simulations implemented in the PLECS and MATLAB/Simulink environment. Besides, analyses comparing the MVC strategy and the conservative approach of Cupertino et al. (2018) are performed.

4.1 Introduction

Reliable operation over the designed lifetime is essential for any power electronics system, mainly because the dependability of power electronics is becoming a prerequisite for system safety in several applications. Indeed, the failure of a single power electronic component causes downtime and maintenance costs (Wang; Liserre; Blaabjerg, 2013; Falck et al., 2018).

Power electronic systems include a large number of fragile elements, semiconductors, capacitors, magnetics, controllers, sensors and auxiliary devices (Falck et al., 2018). Thus, since the MMC-STATCOM topology can have hundreds/thousands of components, reliability concerns are present in the converter design (Alharbi; Bhattacharya; Yousefpoor, 2017).

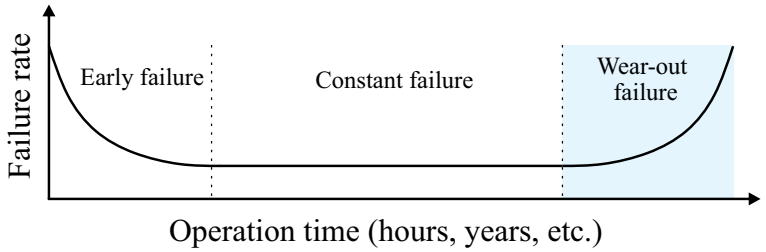
The reliability evaluation is divided into three periods of failure (Lienig; Bruemmer, 2017):

- Early failure: also known as infant mortality failure, occurs during the early life of a product due to manufacturing defects that escape detection.
- Constant failure: also known as random failure, occur during the useful life of the device. The failure in this period is unpredictable and unforeseeable due to the statistical superimposition of a number of independent factors. The failure rate is constant during this period of intrinsic fails.
- Wear-out failure: also known as aging failure, occur at the end of the service life caused by degradation processes of the component during the use of the device.

Figure 58 presents the classic bathtub failure curve with the component failure periods. As observed, the failure rate increases exponentially in the wear-out failure period

due to the cumulative damage (Lienig; Bruemmer, 2017).

Figure 58 – Bathtub failure curve divided into three periods.



Source: Elaborated by the author.

The design of the converter must ensure its operation without any wear-out failures and unplanned maintenance stops. Moreover, the wear-out failure can be predicted at a certain level, if the degradation mechanism is known. For this reason, this work analyzes the wear-out failure period.

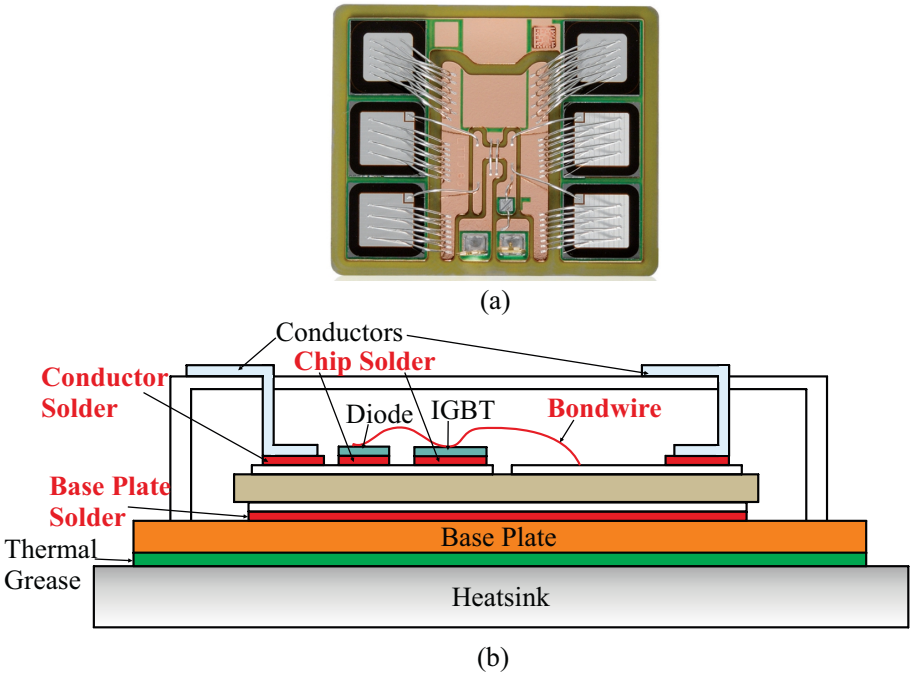
Several works propose methodologies to estimate the lifetime of components considering wear-out failure period (Falck et al., 2018). Since semiconductor devices and capacitors are most likely to fail, the majority of these works focus on them. In addition, temperature is one of the main stress factors. For this reason, thermal models are usually employed in lifetime evaluation procedures.

For semiconductor devices, the stress factors are related to the junction and case temperature. These temperatures are proportional to the internal losses and, consequently, thermal cycling. Besides, semiconductor devices are formed by different materials, as illustrated for an IGBT module in Fig. 59. Thus, the thermomechanical stress produced by thermal cycling results in the degradation of the solders and bondwires. Furthermore, the most critical joints of an IGBT module are bondwire, base plate solder, conductor solder and chip solder, as shown in Fig. 59.

The hotspot temperature and the operational voltage are the stress factors in the wear-out failure of capacitors. The hotspot is the internal point of the capacitor where the temperature reaches the maximum value. Moreover, the Metallized Polypropylene Film Capacitors, illustrated in Fig. 60, are usually employed at high voltage levels. In this capacitor technology, the thermal stress produces chemical degradation of the film, leading to component failure (Wang; Blaabjerg, 2014).

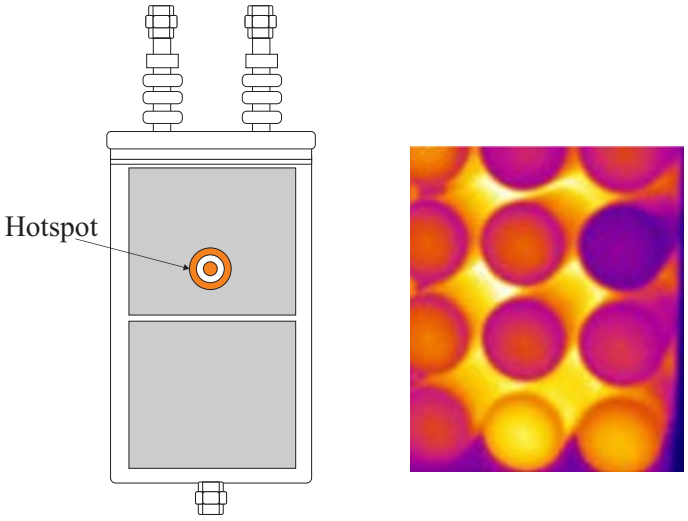
Based on this information, this chapter performs reliability analyses, focusing on the wear-out failure period, with the purpose to evaluate the impact of MVC with different modulation strategies and IGBT blocking voltages on the lifetime of an MMC-STATCOM.

Figure 59 – (a) ABB's IGBT module opened; (b) Schematic of an IGBT module.



Source: Adapted from ABB (2019) and ABB (2014).

Figure 60 – (a) Schematic of a film capacitor; (b) Thermal image of a capacitor bank.



Source: Adapted from Electronicon (2014).

4.2 Semiconductor Devices

The long-term lifetime evaluation flowchart of semiconductor devices is shown in Fig. 61. The flowchart presents the main steps of the wear-out failure computation: power losses look-up table acquisition, thermal model, peak and valleys, rainflow, heating time computation, lifetime model and Miner's rule. These steps are discussed in this section.

4.2.1 Power Losses Look-up Tables

In order to compute the semiconductor devices losses for each operational condition, the power losses of the devices are obtained from look-up tables based on the datasheet curves, as follows:

- The conduction losses of the diodes were obtained employing the curves of dc forward current as a function of the forward voltage;
- The switching losses of the diodes were obtained from the curves of switching losses as a function of the dc forward current;
- The conduction losses of the IGBTs were obtained employing the curves of dc collector current as a function of the collector-emitter voltage;
- The switching losses of the IGBTs were obtained from the curves of switching losses as a function of the dc collector current.

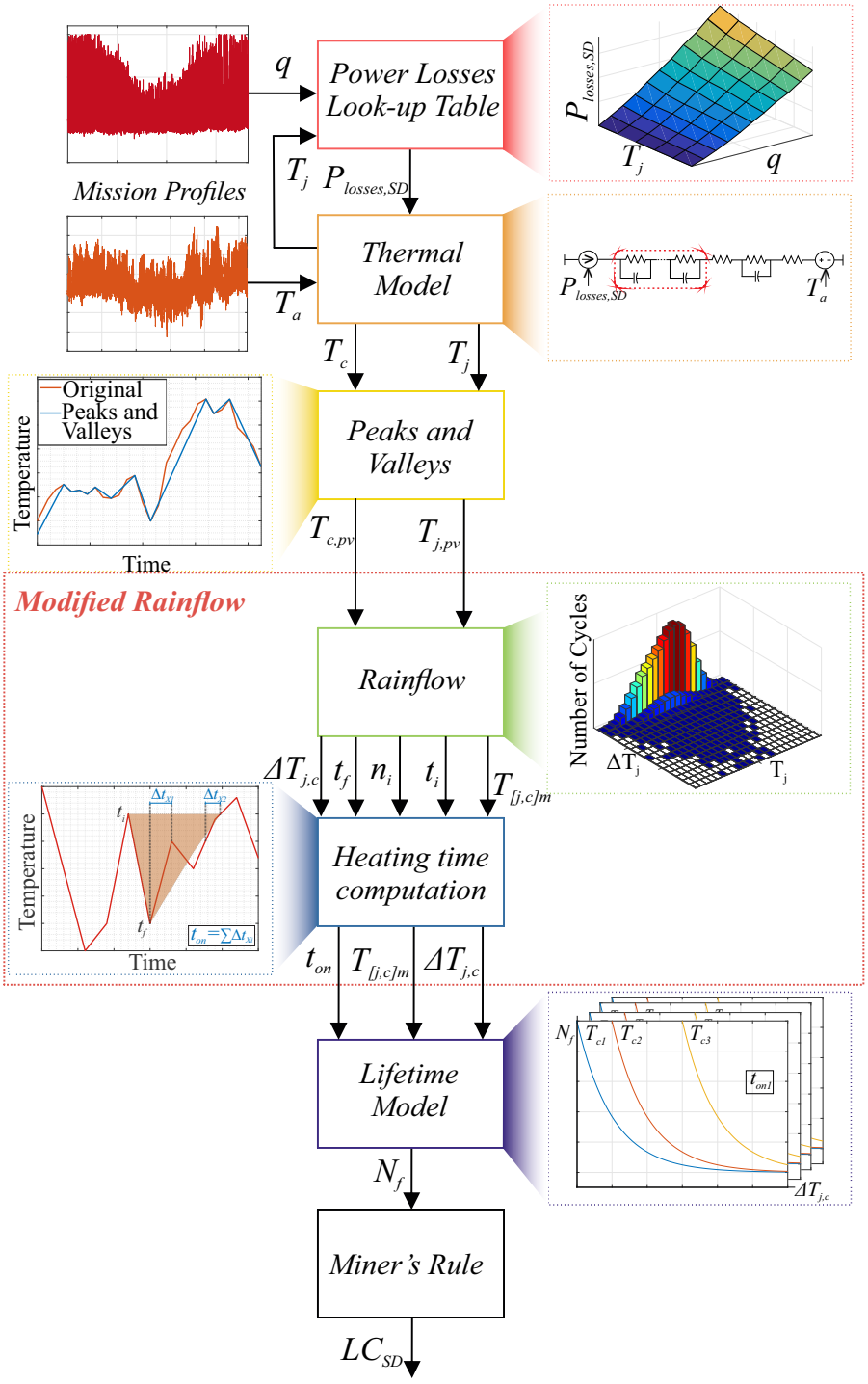
Additionally, an important feature is the power losses dependence of the temperature. In fact, the information mentioned above for the temperatures of 25°C, 125°C and 150°C are obtained in the datasheet contents. Fig. 62 (a)-(d) presents the curves at a junction temperature of 25°C for the four ABB HiPak IGBT Module considered in this work. The gate resistances considered in switching energies curves of Fig. 62 (a)-(b) are shown in Tab. 7.

Table 7 – Gate resistances considered in switching energies curves.

Blocking voltage	1.7 kV	3.3 kV	4.5 kV	6.5 kV
Turn-on IGBT switching energy curve	1.2 Ω	2.2 Ω	2.2 Ω	2.7 Ω
Turn-off IGBT switching energy curve	1.8 Ω	2.2 Ω	2.2 Ω	15 Ω
Diode reverse recovery curve	1.2 Ω	2.2 Ω	2.2 Ω	2.7 Ω

By employing the look-up tables based on the datasheet curves and simulations of the MMC-STATCOM in PLECS environment, a new look-up table is generated. For this purpose, a number of simulations are repeatedly performed in the range of reactive power of -1 pu to 1 pu and the range of junction temperature of 0°C to 150°C. The look-up table produced by PLECS simulations is employed in the wear-out failure procedure, which is represented in Fig. 61. As observed, the annual mission profiles of reactive power (q) and ambient temperature (T_a) are employed with the look-up table and thermal model to obtain the annual mission profile of power losses. These losses are used in the thermal model that follows.

Figure 61 – Lifetime evaluation flowchart of semiconductor devices.

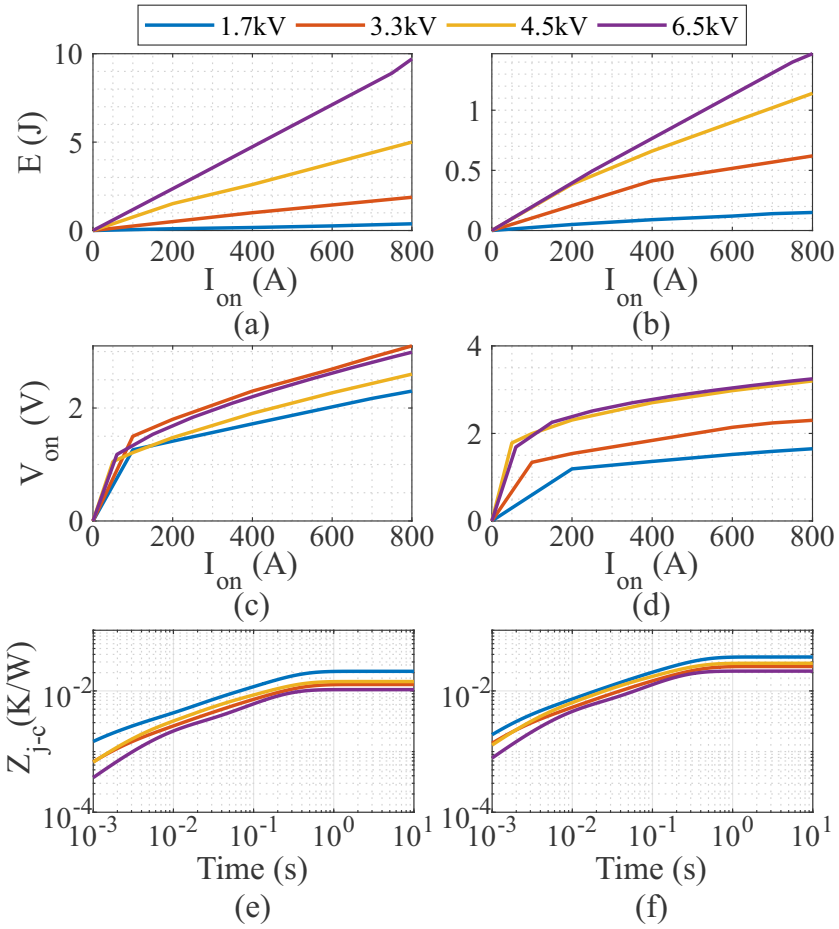


Source: Elaborated by the author.

4.2.2 Thermal Model

The thermal model is based on a partial-fraction circuit, also known as the Foster Model (Infineon, 2020). This model is employed to estimate the junction temperature (T_j) and case temperature (T_c), as illustrated in Fig. 63. The Foster model parameters are based on mathematical fitting of the measured/simulated temperature curves. Each

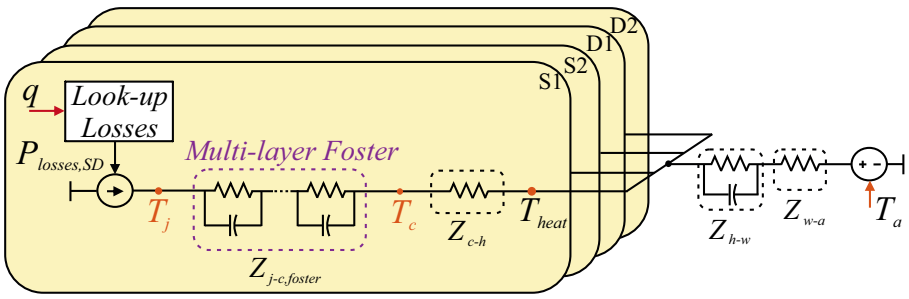
Figure 62 – Power devices curves extracted from datasheets: (a) IGBT switching energies per pulse; (b) Diode reverse recovery characteristic; (c) IGBT on-state characteristics; (d) Diode forward characteristics; (e) IGBT transient thermal impedance; (f) Diode transient thermal impedance.



Source: Elaborated by the author.

RC parameter in the Foster network represents no physical meaning. Moreover, the junction-to-case transient thermal impedances ($Z_{j-c,foster}$) are usually specified based on a Foster model in the datasheets (Infineon, 2020). The datasheet junction-to-case transient thermal impedances are shown in Fig. 62 (e)-(f).

Figure 63 – Thermal model based on Foster model.



Source: Elaborated by the author.

The literature discusses that the Foster model may show inaccuracy to estimate the thermal behaviors when extending the Foster network with external cooling conditions like thermal grease and heatsink. Nevertheless, this issue occurs only when a short-time regime is considered. Since this work performs long-time analyses, in which mission profiles with a sample time of five minutes are employed, the short-time regime issues of this model will not be a problem. Indeed, the thermal behaviors are already in a steady state at this sample time (ABB, 2013b; Xu et al., 2020).

This work considers a water-cooled heatsink per submodule. The heatsink model proposed by Asimakopoulos et al. (2015) for power converters is employed. This model considers a uniform temperature profile throughout the power devices base plate and heatsink volume. The heatsink geometry has a simple rectangular cross-section, and it is approximated by a simple orthogonal brick (Asimakopoulos et al., 2015; Júnior et al., 2019). In such conditions, the heatsink parameters can be computed by:

$$R_{h-w} = \frac{d_h}{\lambda_h A_h}, \tag{4.1}$$

$$C_{h-w} = c_h \rho_h d_h A_h, \tag{4.2}$$

where d_h is the heatsink thickness, λ_h is the thermal conductivity of the heat sink material, A_h is the heatsink surface area, c_h is the specific heat capacity and ρ_h is the material density. Since each SM has one module with two IGBT, the heatsink surface area is considered as having twice the IGBT module area. In addition, this work considers an aluminum heatsink. The common parameters of aluminum heatsinks are shown in Tab. 8. The heatsink surface areas are presented in Tab. 9.

Table 8 – Parameters of the water-cooled heatsink (Asimakopoulos et al., 2015).

Parameter	Value
d_h	3 cm
λ_h	238 W/(m°C)
c_h	900 J/(kg°C)
ρ_h	2700 kg/m^3

Additionally, it is necessary to calculate the thermal resistance representing the water cooling system in order to improve the heat exchange from the heatsink to the ambient. This resistance can be calculated by (Asimakopoulos et al., 2015):

$$R_{w-a} = \frac{1}{h_c A_h}, \tag{4.3}$$

where h_c is the water flow convection coefficient which can range from 50 to 2500 W/(m^{2}K), depending on the speed and type of water flow, temperature-dependent properties, and

pressure (Júnior et al., 2019). In this work, the necessary value of h_c was determined through thermal simulations, which were performed in order to keep the case temperatures lower than 80°C. This temperature limitation is considered to avoid the extrapolation of the superior limits of the lifetime model employed (Neutz, 2013). Consequently, this will result in a lifetime extension of the power modules, as will be further discussed. For each IGBT Module case, the same heatsink design for PSC-PWM modulation at rated conditions is assumed for NLC. The computed water-cooled heatsink thermal impedances are presented in Tab. 9.

Table 9 – Specific parameters and thermal impedances of the water-cooled heatsink.

V_{bk} (kV)	1.7	3.3	4.5	6.5
A_h (m^2)	0.0364	0.0364	0.0364	0.0532
h_c ($W/(m^2K)$)	380	850	1950	3700
R_{h-w} (°C/W)	0.0035	0.0035	0.0035	0.0024
C_{h-w} (kJ/°C)	2.65	2.65	2.65	3.88
R_{w-a} (K/kW)	72.3	32.3	14.1	5.1

4.2.3 Modified Rainflow

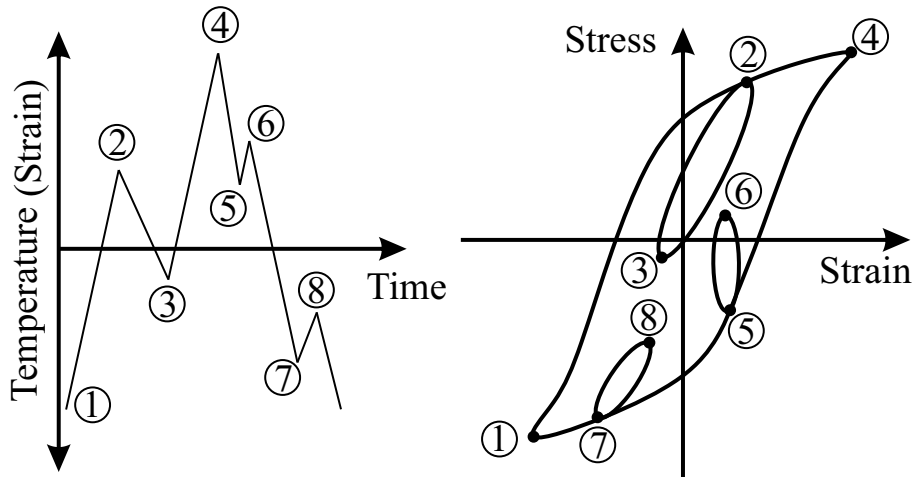
Due to the difference in thermo-mechanical properties of the adjacent components connected by solder, a shear force acts across the solders interconnecting layer and produces simultaneous bending and stretching of the whole assembly (Chung et al., 2015). Analyzing the deformation mechanisms of the solder joint layer, the shear stress-strain response of the solder joint to periodical thermal cycling has the shape of a hysteresis loop (Hall, 1984). The accumulation of damage in the solder material is reflected by the area enclosed by the hysteresis loop (Chung et al., 2015).

A hysteresis loop describes the complex stress-strain history of the solder layer exposed to repetitive cyclic loading, and the shape of the hysteresis can be explained by the behavioral model of solder material. The minimum and maximum shear stress and strain values of the hysteresis loop correspond to the extreme values of the temperature cycle (Chung et al., 2015).

Furthermore, at different stress levels and temperatures, the solder material experiences different physical deformations that gradually contribute to damage accumulation and finally to the failure of the solder interconnection. Consequently, the stress-strain plot can be employed as a tool for the lifetime estimation of solder joints in electronic devices (Chung et al., 2015). A generic time domain data and its corresponding stress-strain hysteresis loop are presented in Fig. 64.

To compute the hysteresis loop a counting algorithm is required. In this work, a rainflow counting algorithm is employed. However, only the extreme points (peaks and valleys) of the temperatures T_j and T_c are desired to compute these loops. Therefore, before

Figure 64 – Time domain data and its corresponding stress-strain hysteresis loop.



Source: Adapted from: Samavatian, Iman-Eini and Avenas (2018)

rainflow, the profile data is transformed to data with only peak and valley information (GopiReddy et al., 2015). Finally, the rainflow counting algorithm can compute the hysteresis loop as described in Infineon (2019).

As previously discussed, the rainflow was first created for fatigue stress/ strain force computation in mechanical applications. In these applications, the resulting fatigue is unaffected by the period of time that a stress/strain force is applied. On the other hand, the heating time affects the fatigue computation in power device lifetime estimation (Antonopoulos et al., 2020). Nevertheless, the heating time is not computed by conventional rainflow.

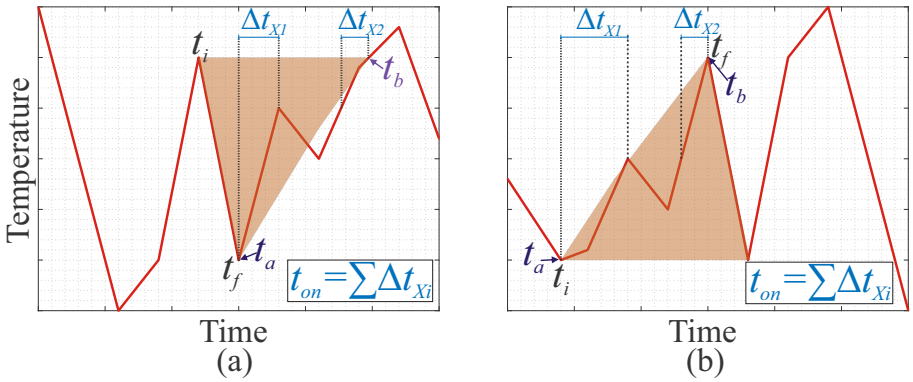
Although works that employ the MATLAB rainflow code written by Nieslony (2003) consider the heating time as half of the cycle time given by this function, this approach is based on the principle that heating and cooling time are equal, which can be an untruth. Indeed, the rainflow algorithm only computes time in the extreme points of temperature: initial cycle (t_i) and final cycle (t_f). Nieslony function considers the cycle time as double of this range of time.

Following the previous assumptions and considering the discussions of Antonopoulos et al. (2020), a modified rainflow function is created to compute the effective heating time from the original temperature profile data. Thus, the modified rainflow is a contribution of this work.

The modified rainflow function uses the conventional rainflow and adds steps in the procedure to compute the effective heating time and filter the semi-cycles. In this function, t_i and t_f are employed to locate the cycle in the original data and to verify the cycle direction. Depending of t_i and t_f respective temperature, T_i and T_f, the cycle is classified in ascending, if $T_i < T_f$, or descending, if $T_i > T_f$. The procedure is illustrated

in Fig. 65 for both conditions. As observed, this verification defines the first t_a and last t_b points of heating time computation. Subsequently, the time ranges (Δt_{Xi}), at which the temperature increases are computed and added, resulting in the effective heating time.

Figure 65 – Example of heating time (t_{on}) computation for: (a) ascending cycle; (b) descending cycle.



Source: Elaborated by the author.

4.2.4 Lifetime Model

The regular data series with constant average values ($T_{[j,c]m}$), peak ($\Delta T_{j,c}$), heating time (t_{on}) obtained from rainflow and effective heating time computation is the input information of the lifetime model.

In this work, the number of cycles to failure (N_f) is calculated using look-up tables provided by Application Note of ABB for Hi-Pak power modules (ABB, 2014). This application note employs Weibull distribution. In addition, the results of this distribution are used to determine the B_{10} lifetime which is described as the number of cycles in which 10% of the modules of a population fail. Moreover, the lifetime models in the application note are based on the Coffin-Manson law and fatigue of the joints due to plastic deformation (ABB, 2014). Furthermore, the application note presents B_{10} lifetime for four critical joints of the IGBT module: bondwire, base plate solder, conductor solder, and chip solder (ABB, 2014).

The chip, base plate and conductor solders are dependent of the cycle period. In this context, for the model of chip solder, T_{jm}, ΔT_j and t_{on} are employed. For the base plate and conductor solders, T_{cm}, ΔT_c and t_{on} are employed. In addition, the lifetime of the base plate and conductor solders are described by the same model (ABB, 2014).

On the other hand, the model of the bondwire is independent of the cycle period. This model assumes that the immediate plastic deformation leads to fatigue instead of time-dependent creep. For this reason, T_{jm}, ΔT_j are employed in this model (ABB, 2014).

The LT models provided by ABB (2014) have a superior limit of 16 hours when longer cycles are considered. Thus, it is assumed that the viscoplastic deformation saturates when cycles higher than 16 hours are observed (Infineon, 2019).

Subsequently, with the N_f values of each model, the Life Consumptions (LCs) of the semiconductor devices are calculated separately for each model by using the Miner's rule (Mine, 1945), as follows:

$$LC_{SD} = \sum_i \frac{n_i}{N_{f,i}}, \tag{4.4}$$

where LC_{SD} is LC for each semiconductor device in the SM (S_1, S_2, D_1 or D_2), n_i is the i^{th} number of cycles obtained from the rainflow algorithm and $N_{f,i}$ is the i^{th} number of cycles to failure.

4.3 SM Capacitors

The capacitor lifetime evaluation flowchart is shown in Fig. 66. The flowchart presents the main steps of the capacitor wear-out failure computation: power losses look-up table acquisition, thermal model, lifetime model and Miner's rule. These steps are discussed in this section.

4.3.1 Power Losses Look-up Table and Thermal Model

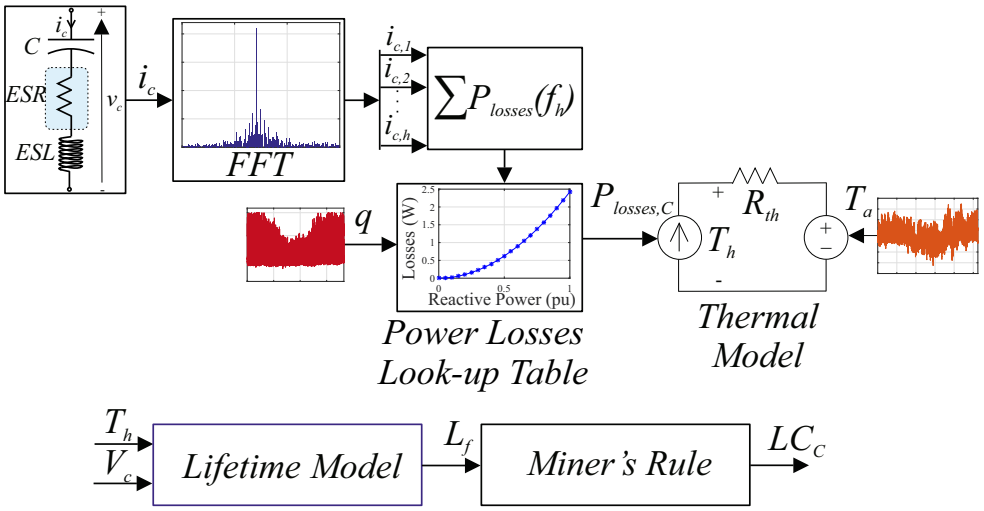
The capacitor can be modeled as an ideal capacitor (C) in series with an equivalent series resistor (ESR) and an equivalent series inductor (ESL). ESR models power dissipation. In addition, ESR is frequency-dependent and can be calculated as follows (Electronicon, 2014; Yang et al., 2014):

$$ESR(f_i) = R_s + \frac{\tan(\delta_0)}{2\pi f_i \times C_N}, \tag{4.5}$$

where R_s is the sum of the internal ohmic resistances, f_i is the frequency, $\tan(\delta_0)$ is the dielectric dissipation factor and C_N is the nominal capacitance of the selected capacitor. According to the datasheet, $tan(\delta_0) = 2 \times 10^{-4}$ (Electronicon, 2014). The other parameters are given for each case in Tab. 4 of Chapter 2.

In order to obtain the power losses look-up table of the capacitors, simulations of the MMC-STATCOM in PLECS environment are performed. These simulations are performed, repeatedly, for the range of reactive power of -1 pu to 1 pu, in which the capacitor current is measured.

Figure 66 – Lifetime evaluation flowchart of the capacitor.



Source: Elaborated by the author.

Due to ESR frequency dependency, the fast Fourier transform (FFT) is applied in the capacitor current. Subsequently, the power losses can be calculated, for each operational condition, by (Electronicon, 2014; Yang et al., 2014):

$$P_{losses,C} = \sum_{i=1}^{H} I_{c,i}^2 \times ESR(f_i), \tag{4.6}$$

where $I_{c,i}$ is the amplitude of the capacitor current for the frequency f_i and H represents the Hth harmonic order of the capacitor current. The capacitor current is sampled at the sampling frequency f_s in a period of 2 s, with a frequency resolution of 0.5 Hz. The capacitor power losses look-up table is obtained by applying Eq. (4.6). As observed in Fig. 66, the annual mission profiles of reactive power and ambient temperature are employed with the look-up table and thermal model to obtain the annual mission profile of power losses.

The hotspot temperature (T_h) of the capacitor is given by (Yang et al., 2014):

$$T_h = P_{losses,C} R_{th} + T_a, \tag{4.7}$$

where R_{th} is the thermal resistance of the capacitor given in the datasheet and presented in Tab. 4 for each design.

4.3.2 Lifetime Model

According to Electronicon (2014), the lifetime model of the capacitor is given by:

$$L_{c,f} = L_0 \times \left(\frac{V_c}{V_{c,r}}\right)^{-n} \times 2^{\left(\frac{T_{h,r}-T_h}{7k}\right)} \tag{4.8}$$

where $L_{c,f}$ is the time-to-failure, $L_0 = 100{,}000$ hours is the rated lifetime, $V_{c,r}$ and $T_{h,r} = 70°C$ are the rated values of the capacitor voltage and hotspot temperature obtained in the datasheet. In addition, V_c and T_h are the capacitor voltage and hotspot temperature in which the capacitor is operating. The parameters of the capacitor lifetime model, $n = 8.8529$ and $k = 0.9895$, are obtained from the datasheet (Electronicon, 2014).

The capacitor LC is also calculated by using the Miner's rule, as follows:

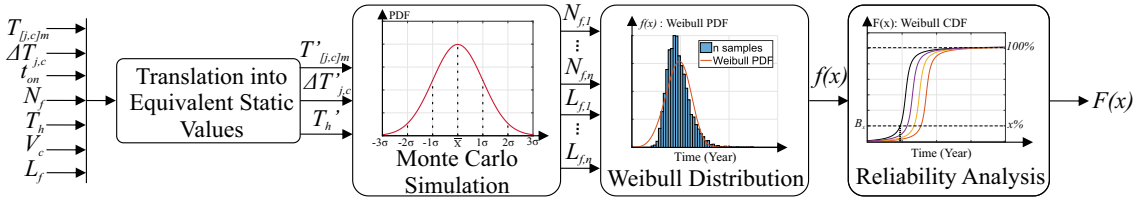
$$LC_C = \sum_i \frac{l_i}{L_{c,f,i}}, \tag{4.9}$$

where LC_C is LC for each capacitor, l_i is the operating time, according to the mission profile resolution and $L_{c,f,i}$ is the time-to-failure calculated from Eq. (4.8).

4.4 Monte Carlo-based Reliability Evaluation

The lifetime evaluation methodologies previously presented consider an ideal case of fixed time-to-failure in which all components fail at the same time. However, this consideration is not realistic. Indeed, the lifetime models presented may vary due to the manufacturing process, mission profile and lifetime model parameters (Sangwongwanich et al., 2018). Monte Carlo simulation is employed to approximate practical applications. This method introduces parameter variations into the lifetime model (Reigosa et al., 2016). The Monte Carlo analysis flowchart is shown in Fig. 67.

Figure 67 – Monte Carlo Analysis flowchart.



Source: Elaborated by the author.

Firstly, the Monte Carlo analysis demands the conversion of the dynamic parameters ($T_{[j,c]m}$, $\Delta T_{j,c}$ and T_h) into equivalent static values ($T'_{[j,c]m}$, $\Delta T'_{j,c}$ and T'_h) which result in the same lifetime, when applied on the lifetime model (Reigosa et al., 2016).

Monte Carlo simulation employs normal distribution which requires the definition of the maximum variation expected in the lifetime model parameters. For semiconductor devices, a sensitivity test is carried out to define this variation. The test considers the

proportion of the difference between typical and maximum values of collector-emitter (for IGBT) and forward (for diode) voltages presented in the datasheet. Thereafter, the proportion of difference and the on-state typical curves (Fig. 62 (c)-(d)) is employed to compute the on-state maximum curves. Subsequently, the on-state maximum curves are employed in the lifetime procedure and the maximum damage is computed. Finally, the dynamic parameters of this case are converted into equivalent static values and the maximum variation is computed. As noted, the sensitivity test is related to the conduction losses, which is similar in cases with the same blocking voltage and different modulation strategies. Therefore, the sensitivity test is carried out for the NLC case of each blocking voltage. The maximum variation of each blocking voltage is presented in Tab. 10.

Table 10 – Sensitivity test.

Parameter	Join	1.7 kV	3.3 kV	4.5 kV	6.5 kV
$T'_{[j,c]m}$	BPCS	1.81%	1.14%	0.14%	0.71%
	CS	1.98%	1.31%	0.13%	1.08%
	BW	1.98%	1.31%	0.13%	1.08%
$\Delta T'_{j,c}$	BPCS	3.95%	3.87%	3.03%	6.85%
	CS	3.31%	2.71%	2.82%	5.61%
	BW	2.36%	2.13%	1.99%	2.47%

For capacitor lifetime model the standard deviation of 5% is applied in T'_h, n, k, L_0 and V_c.

Monte Carlo simulation with a population of 10,000 samples is carried out for each component using the lifetime models. The lifetime yield for each sample is obtained from the simulation and fitted with the Weibull distribution ($f(x)$), which is the probability density function (PDF) given by (Sangwongwanich et al., 2018):

$$f(x) = \frac{\beta}{\eta^\beta} x^{\beta-1} exp\left[-\left(\frac{x}{\eta}\right)^\beta\right] \tag{4.10}$$

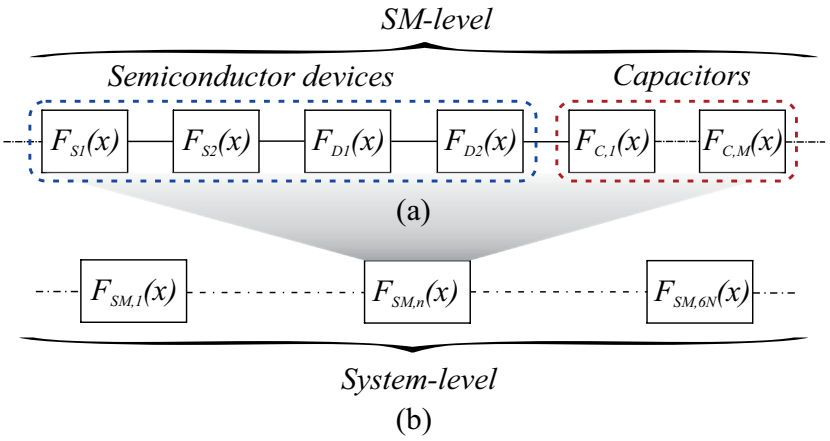
where x is the operation time, β is the shape parameter and η is the scale parameter.

From lifetime distribution, it is also obtained the component unreliability function ($F(x)$), which is a cumulative density function (CDF). $F(x)$ represents the proportion of failure population as a function of time and is given by (Sangwongwanich et al., 2018):

$$F(x) = \int_0^x f(x)dx \tag{4.11}$$

The unreliability functions are combined, separately for each critical structure of the SM components (i.e. base plate and conductor solders, bondwire, chip solder and capacitors). The unreliability block diagrams of SM and system-level are shown in Fig. 68. Moreover, the unreliability of each critical structure can be calculated, at system-level, as follows:

Figure 68 – Unreliability block diagram of: (a) SM-level; (b) system level.



Source: Elaborated by the author.

$$F_f(x) = 1 - \prod_{n=1}^{6N} (1 - F_{f,sm,n}(x)) \tag{4.12}$$

where f is BPCS, BW, CS, or C. $F_{f,sm,n}(x)$ is the critical structure unreliability at SM-level, given by:

$$F_{f,sm}(x) = 1 - \prod_{i=1}^{I} (1 - F_{f,i}(x)) \tag{4.13}$$

where $F_{f,i}(x)$ is the structure unreliability function of each component in the SM, which for semiconductor devices is S_1, S_2, D_1 or D_2, and for SM capacitor bank represents each capacitor.

Finally, combining all critical structure unreliabilities, the MMC-STATCOM system-level is calculated as follows:

$$F_{MMC}(x) = 1 - \prod_{f=1}^{4} (1 - F_f(x)) \tag{4.14}$$

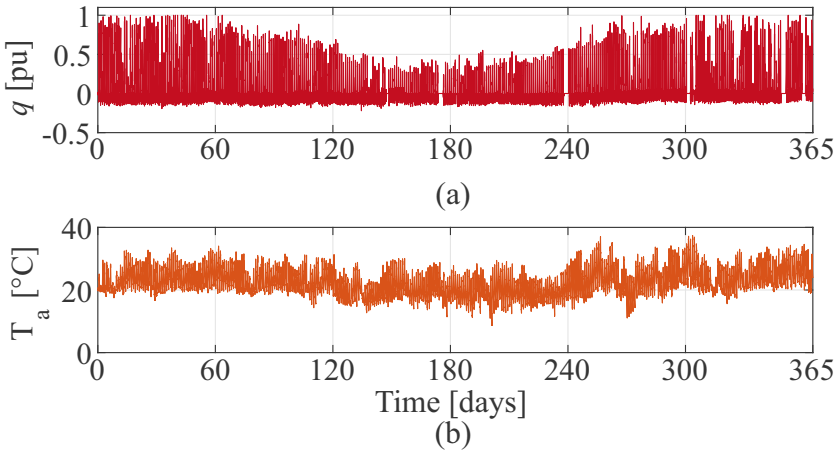
where i is each structure.

4.5 Losses and Wear-out with MVC

This section presents implementation and analyses based on the reliability methodologies previously discussed. The results are based on simulations implemented in the PLECS and MATLAB/Simulink environment, considering parameters of Tab. 3 and Tab. 4. Besides, analyses comparing MVC strategy and conservative dc-side voltage for the eight case studies are performed. Fig. 69 shows the mission profiles of reactive power and

ambient temperature employed in the analyses. These profiles are based on measurements in Southeastern Brazil over a year with a data sampling time of 5 minutes.

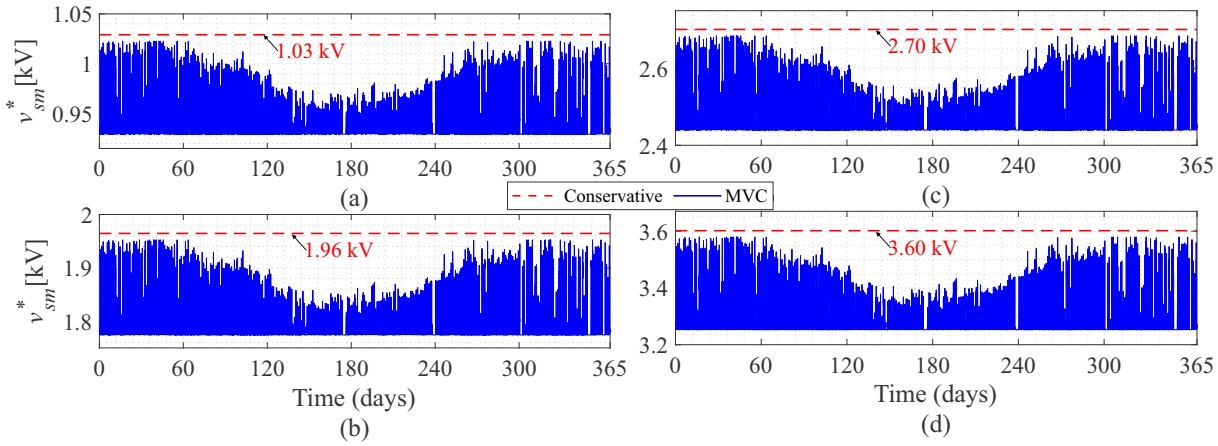
Figure 69 – Mission profiles: (a) reactive power (S_b = 17 MVar); (b) ambient temperature.



Source: Elaborated by the author.

The annual profile of SM voltage reference with MVC is obtained considering the reactive power mission profile. The SM voltage reference profiles are shown in Fig. 70 for each blocking voltage considered. As observed, v^*_{sm} with MVC is lower than with the conservative approach during the whole year. Thus, the SMs operate with lower voltage when MVC is applied during the entire year.

Figure 70 – Annual mission profile of SM voltage reference for V_{bk} of: (a) 1.7 kV; (b) 3.3 kV; (c) 4.5 kV; (d) 6.5 kV.

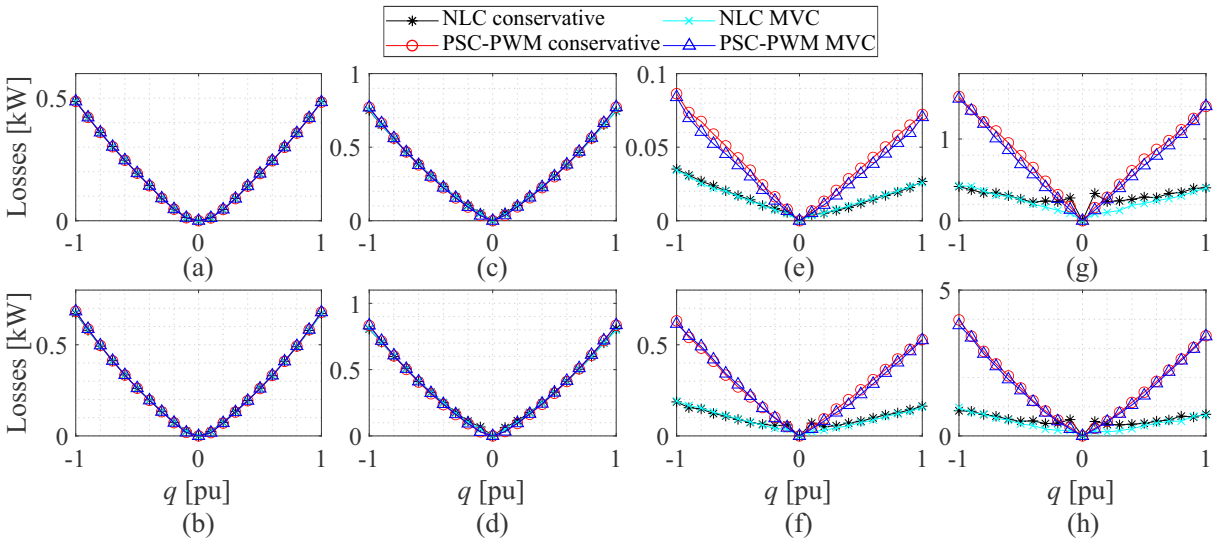


Source: Elaborated by the author.

Figure 71 presents semiconductor device losses per SM at an ambient temperature of 25°C. The losses are presented for all case studies employing conservative and MVC approaches. Fig. 71 (a)-(d) present the conduction losses and Fig. 71 (e)-(f) the switching losses. The conduction and switching losses behavior are in accordance with the datasheet curves presented in Fig. 62 (a)-(d). For each blocking voltage, the conduction losses of

both modulation strategies are similar. Nevertheless, switching losses are higher with PSC-PWM. Moreover, the losses increase according to the blocking voltage, in which 6.5 kV presents the highest losses for both modulation strategies. Thus, cases with NLC and lower $V_{bk,n}$ present lower semiconductor device losses per SM. Regarding MVC, the effect on conduction losses is negligible for all cases. Additionally, cases with PSC-PWM and higher blocking voltage are more affected due to the higher switching frequency.

Figure 71 – Semiconductor devices losses per SM: (a) conduction losses for $V_{bk,n} = 1.7$ kV; (b) conduction losses for $V_{bk,n} = 3.3$ kV; (c) conduction losses for $V_{bk,n} = 4.5$ kV; (d) conduction losses for $V_{bk,n} = 6.5$ kV; (e) switching losses for $V_{bk,n} = 1.7$ kV; (f) switching losses for $V_{bk,n} = 3.3$ kV; (g) switching losses for $V_{bk,n} = 4.5$ kV; (h) switching losses for $V_{bk,n} = 6.5$ kV.

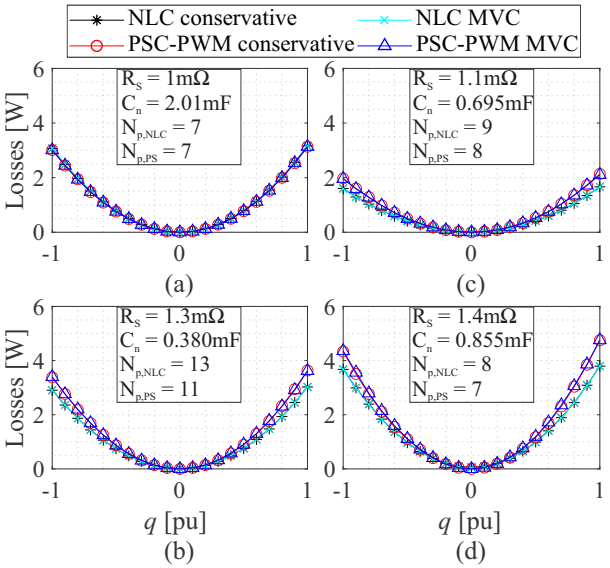


Source: Elaborated by the author.

Figure 72 presents the capacitor losses employing conservative and MVC approaches. The losses are presented for all case studies. Cases with PSC-PWM present higher losses than with NLC, except for 1.7 kV. Indeed, cases with PSC-PWM have a lower number of capacitors in parallel and, thus, a higher current flowing through each capacitor, increasing its thermal stress. Cases C_{P17} and C_{N17} have the same number of capacitors per SM. Consequently, the same current is conducted through each capacitor in parallel (approximately). C_{P65} presents higher capacitor losses. The case C_{N65} is also the most stressed when NLC is employed. Moreover, MVC does not affect capacitor losses. This is expected, since the model of capacitor losses (Eq. (4.6)) considered is unattached to the SM voltage.

Figure 73 and Fig. 74 present the annual profile of the case temperature of diode D1 and hotspot temperature of an SM capacitor, respectively. Their average temperature is indicated by the dashed line. Diode D1 is the most stressed in C_{P17} and it is chosen to compare the other cases. Moreover, the temperatures are presented for both modulation strategies employing conservative and MVC approaches for the extreme blocking voltage

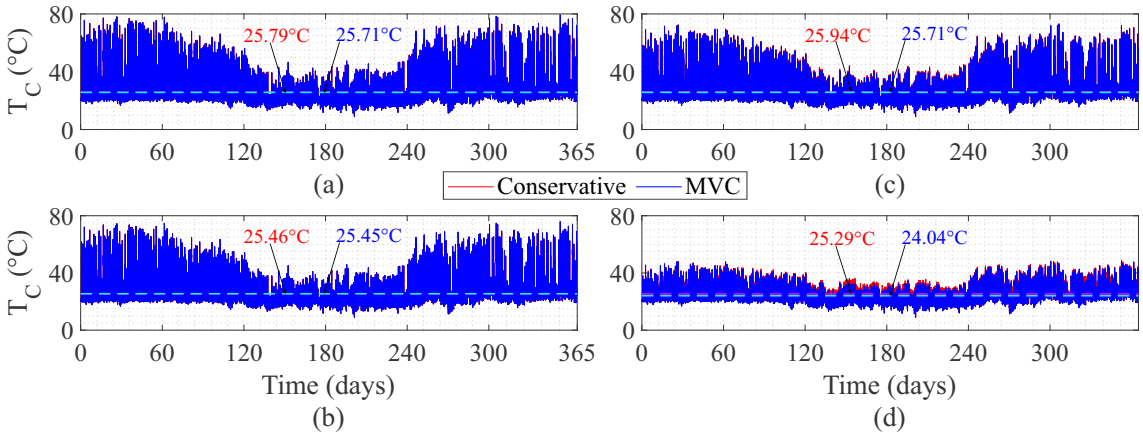
Figure 72 – Individual capacitor losses with blocking voltage: (a) 1.7 kV; (b) 3.3 kV; (c) 4.5 kV; (d) 6.5 kV. *Remark: $N_{p,NLC}$ $N_{p,PS}$ are the number of capacitors per SM in parallel arrangements for NLC and PSC-PWM, respectively.*



Source: Elaborated by the author.

cases (1.7 kV and 6.5 kV). As observed, the MVC effect on the capacitor thermal stress (hotspot temperature) is negligible for all cases. On the other hand, this technique decreases the thermal stress on semiconductor devices. Indeed, since the temperatures are directly related to the power losses, this result is agreeing with the operational losses previously presented.

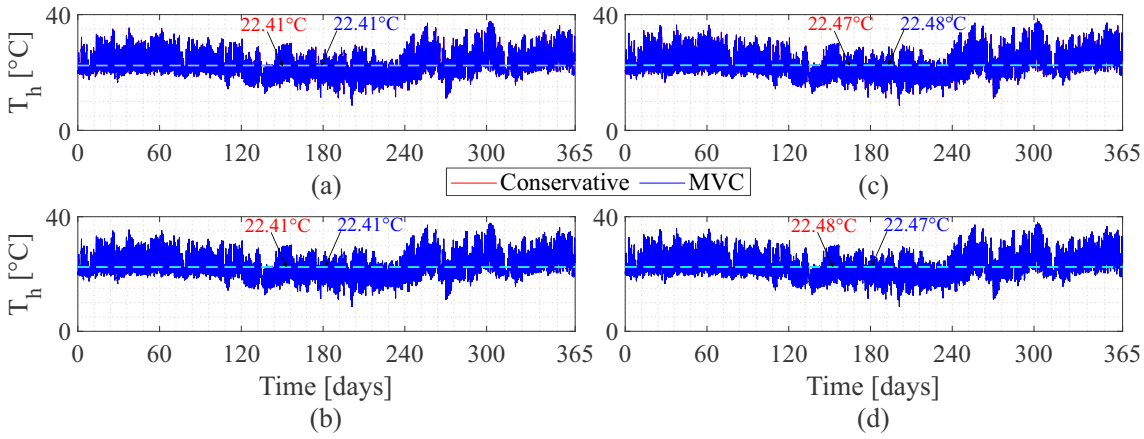
Figure 73 – Case temperature of diode D1: (a) $V_{bk} = 1.7$ kV and PSC-PWM; (b) $V_{bk} = 1.7$ kV and NLC; (c) $V_{bk} = 6.5$ kV and PSC-PWM; (d) $V_{bk} = 6.5$ kV and NLC.



Source: Elaborated by the author.

Figure 75 (a)-(c) presents the annual profiles average and maximum variation ($\Delta T_{C,max}$) of case temperature of diode D1, the average hotspot temperature for all case studies. The average and the maximum variation of case temperature are higher in cases with PSC-PWM than with NLC, independently of blocking voltage. Both average and

Figure 74 – Hotspot temperature: (a) $V_{bk} = 1.7$ kV and PSC-PWM; (b) $V_{bk} = 1.7$ kV and NLC; (c) $V_{bk} = 6.5$ kV and PSC-PWM; (d) $V_{bk} = 6.5$ kV and NLC.



Source: Elaborated by the author.

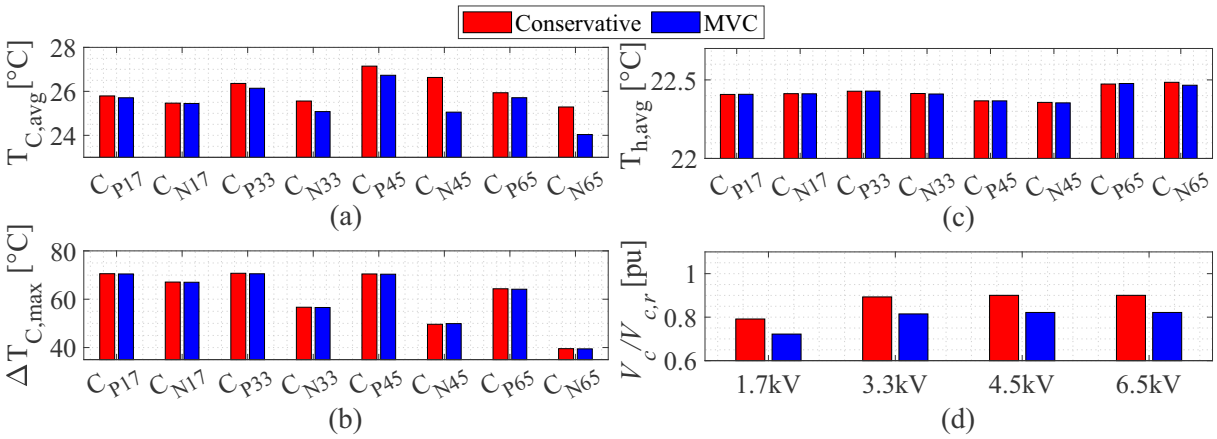
maximum variation of case temperature have an effect on lifetime evaluation since they constitute the thermal cycle. The average and maximum variation of temperature are directly related to the inputs of the semiconductor device lifetime models. As observed in Fig. 75 (a), MVC decreases the average case temperature for all cases. Besides, cases with higher $V_{bk,n}$ are more affected. On the other hand, no significant impact in $\Delta T_{C,max}$ and the average hotspot temperature with MVC is observed in Fig. 75 (b)-(c).

Figure 75 (d) presents the average SM voltage stress ($\frac{V_c}{V_{c,r}}$) for blocking voltages and control approaches. For MVC and conservative approaches, $V_c = v^*_{sm}$ is considered. Thus, a fixed value and the average of the SM voltage annual profile (see Fig. 70) are considered for conservative and MVC approaches, respectively. As observed, 4.5 kV and 6.5 kV presents the highest voltage stress, while 1.7 kV presents the lowers voltage stress with both control approaches. Moreover, MVC decreases the SM voltage stress for all cases.

The semiconductor devices static life consumptions obtained from the lifetime models and Miner's rule are shown in Fig. 76 and Fig. 77, for PSC-PWM and NLC, respectively. Fig. 76 (a)-(c) and Fig. 77 (a)-(c) present the LC of base plate and conductor solder (BPCS), chip solder (CS) and bondwire (BW), respectively. As observed, the highest values of LC are found for base plate and conductors solders. Furthermore, the LCs for BPCS are highlighted in these figures. The LC results follow the maximum temperature variation pattern. This result demonstrated the damage is more sensitive to the maximum temperature variation. Furthermore, the MVC decreases LC for all case studies.

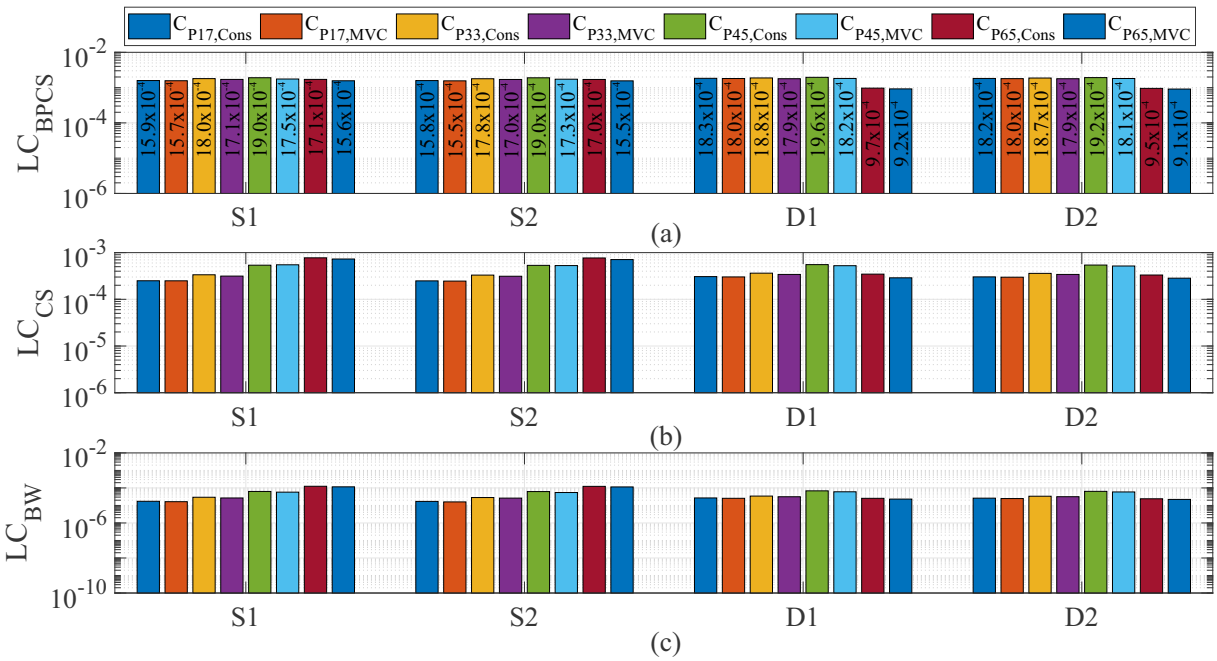
Figure 78 presents the capacitor static life consumptions. Cases with the blocking voltage of 1.7 kV have lower static damage. Moreover, PSC-PWM cases have higher LC than NLC and the blocking voltage of 6.5 kV has the highest static damage. This result demonstrates that the voltage stress on the capacitor is more relevant than their thermal stress damage contribution when the capacitor wear-out is evaluated. In addition, T_h

Figure 75 – Annual profiles: (a) average case temperature of diode D1; (b) maximum variation $\Delta T_{C,max}$; (c) average hotspot temperature; (d) average SM voltage stress ($\frac{V_c}{V_{c,r}}$).



Source: Elaborated by the author.

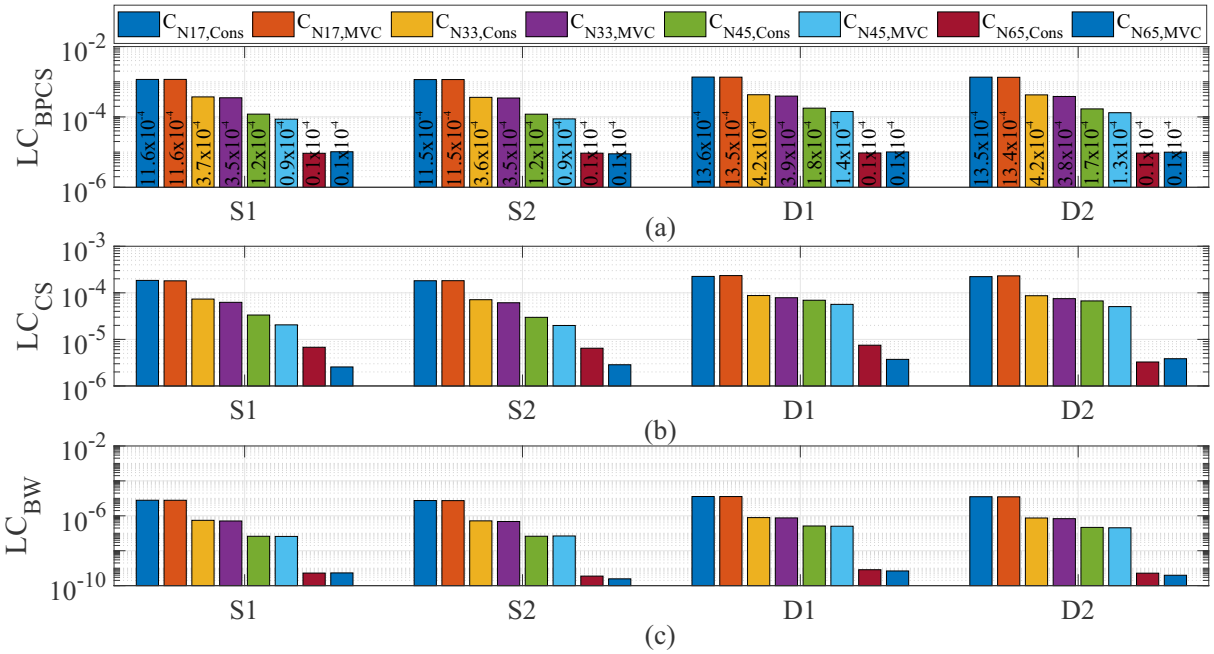
Figure 76 – PSC-PWM semiconductor device static damages of: (a) base plate and conductor solders – BPCS; (b) chip solder – CS; (c) bondwire – BW. (Semi-logarithmic scale).



Source: Elaborated by the author.

demonstrates relevance in the other cases with identical average voltage stress (4.5 kV and 6.5 kV), in which LC follows the same pattern of average T_h. Moreover, cases with MVC present lower LC than those with the conservative approach for both modulation strategies. In fact, the capacitor LC decreases around 53% with MVC. It must be highlighted that even though the MVC effect in hotspot temperature is negligible, the capacitor damage is lower with MVC due to the voltage stress reduction of MVC. Thus, the MVC operation

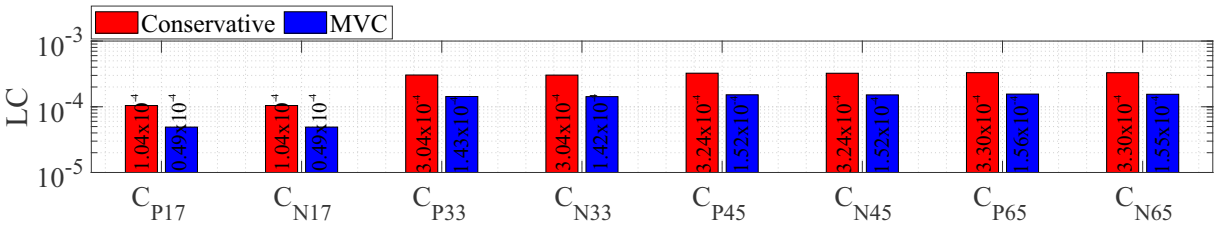
Figure 77 – NLC semiconductor device static damages of: (a) base plate and conductor solders – BPCS; (b) chip solder – CS; (c) bondwire – BW. (Semi-logarithmic scale).



Source: Elaborated by the author.

with lower voltages has a higher effect on the capacitor LC for all case studies.

Figure 78 – Individual SM capacitor static life consumption.

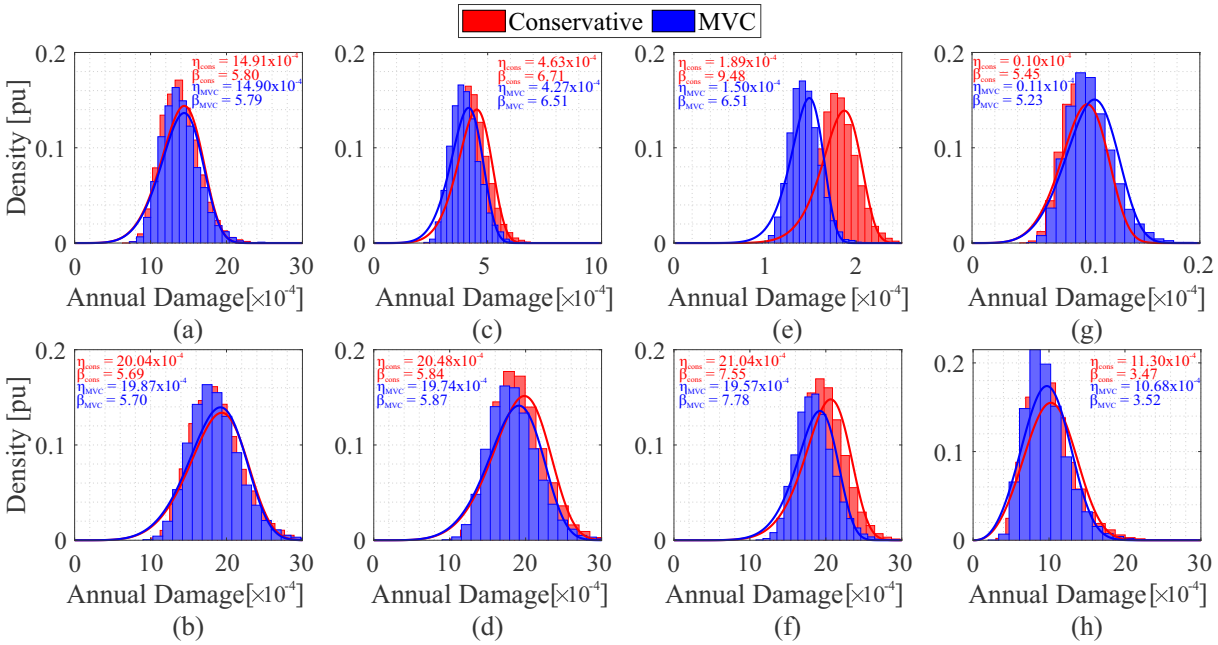


Source: Elaborated by the author.

Figure 79 presents the histogram of Monte Carlo simulations and PDF curves of BPCS of the diode D1. The PDF curves are computed by Eq. (4.10). As observed in Fig. 79, NLC presents lower damage than PSC-PWM in most of the histogram distribution, in which higher blocking voltages present lower damage. For all cases, the average value of the histogram distribution (η) is lower for MVC than for the conservative approach, with exception of case C_{N65}. Nevertheless, the difference, in this case, is relatively small. Moreover, for all case studies part of the distributions with MVC and conservative approach are intercepting each other. Indeed, since some bins of MVC conflict with some of the conservative approach, there is a small probability of the conservative approach have the same or lower annual damage than MVC.

Figure 80 presents the histogram of Monte Carlo simulations and PDF curves of

Figure 79 – Monte Carlo simulations of BPCS of the diode D1 with MVC and conservative approach for case: (a) C_{N17}; (b) C_{P17}; (c) C_{N33}; (d) C_{P33}; (e) C_{N45}; (f) C_{P45}; (g) C_{N65}; (h) C_{P65}.



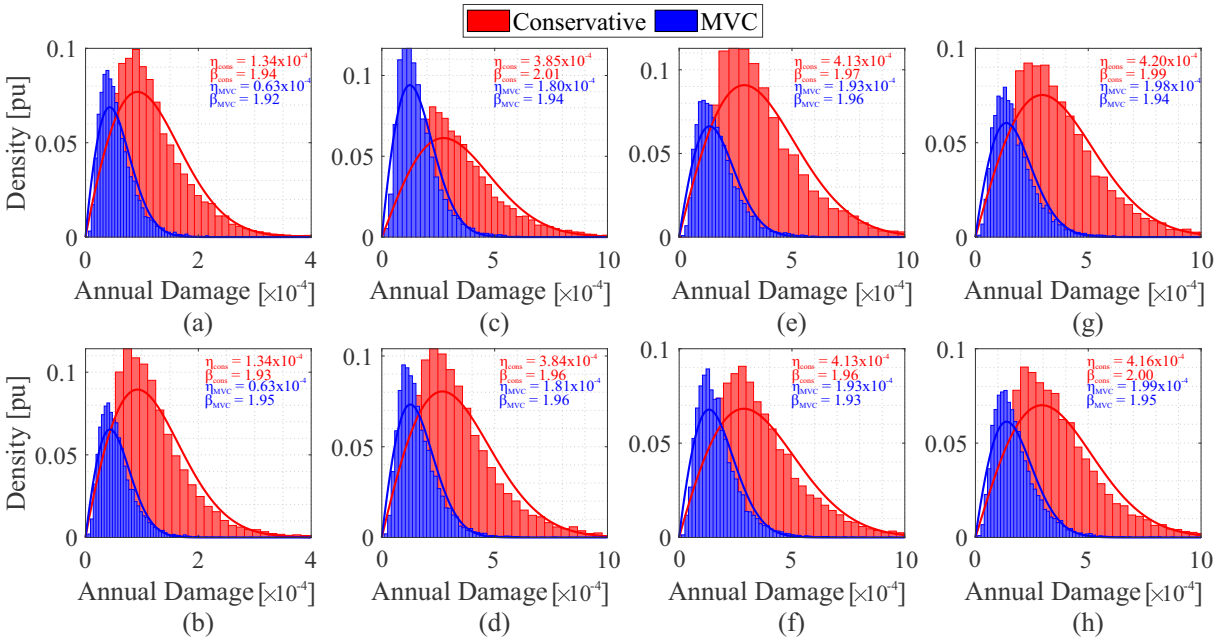
Source: Elaborated by the author.

the capacitors. The PDF curves are computed by Eq. (4.10). Cases with the blocking voltage of 1.7 kV present the average value of the histogram distribution (η). Moreover, for all cases, the average value of the histogram distribution (η) is lower for MVC than for the conservative approach. Moreover, for all case studies part of the distributions with MVC and conservative approach are intercepting each other. Indeed, since some bins of MVC conflict with some of the conservative approach, there is a small probability of the conservative approach have the same or lower annual damage than MVC. Nevertheless, these interceptions occur with less frequency than for semiconductor devices (see Fig. 79).

Figure 81 exhibits the unreliability at system-level in the first 30 years which includes all semiconductor critical joints and capacitors. This figure has also highlighted the unreliability in 20 years (F_{20}). As observed, 4.5 kV and 6.5 kV cases present the highest unreliabilities in this range. Furthermore, MVC has lower unreliability than the conservative approach in this range for all cases.

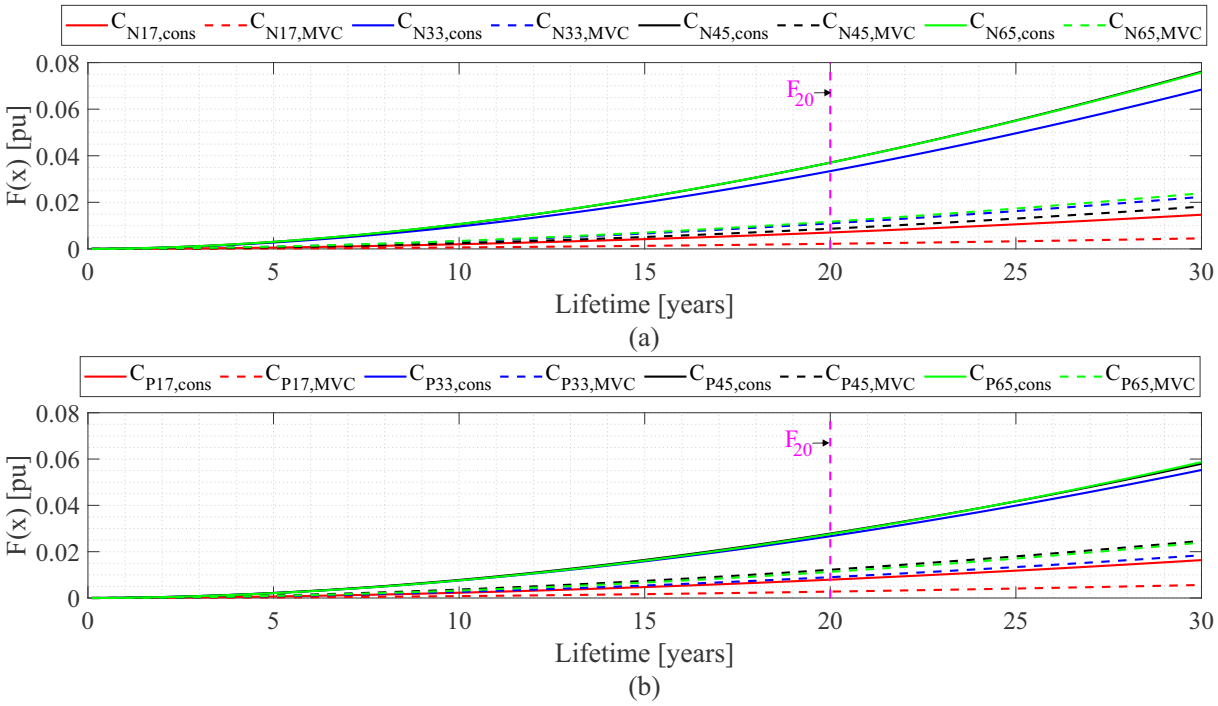
Figure 82 shows the MMC-STATCOM annual energy losses, normalized according to the total annual energy losses (159.61 MWh) of case C_{P65} with the conservative approach. Losses of arm inductors, capacitors and semiconductor devices were considered. As observed, the arm inductor and capacitor losses are similar for all cases with MVC and conservative approaches. Furthermore, cases with the same semiconductor blocking voltage have similar conduction losses for both modulation strategies with MVC and conservative approaches. Besides, the conduction losses decrease with the blocking voltage. Thus, the arm inductor,

Figure 80 – Monte Carlo simulations of the capacitors with MVC and conservative approach for case: (a) C_{N17}; (b) C_{P17}; (c) C_{N33}; (d) C_{P33}; (e) C_{N45}; (f) C_{P45}; (g) C_{N65}; (h) C_{P65}.



Source: Elaborated by the author.

Figure 81 – MMC-STATCOM unreliability function at system-level with MVC and conservative approach for: (a) NLC cases; (b) PSC-PWM cases.

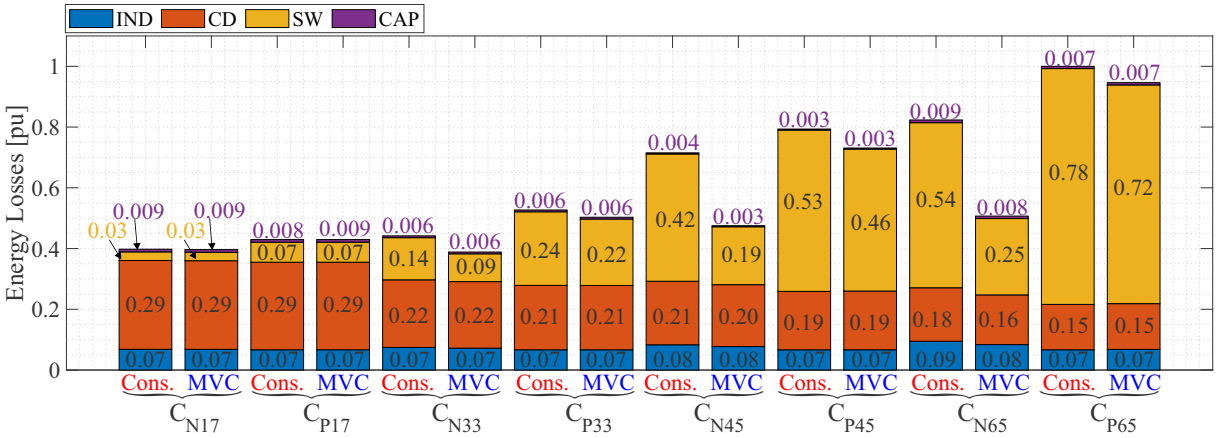


Source: Elaborated by the author.

capacitor and conduction losses are unaffected by MVC. Furthermore, the switching losses increase with the semiconductor blocking voltage. Moreover, the reduction of switching

losses with MVC increases with the blocking voltage and is more expressive for NLC. The total losses increase according to the blocking voltage, in which MVC losses reduction is more expressive for higher blocking voltages and NLC.

Figure 82 – MMC-STATCOM annual energy losses. (*Remark: IND = inductor losses; CD = conduction losses; SW = switching losses; CAP = capacitor losses. Base value of energy losses 128.49 MWh.*)



Source: Elaborated by the author.

Finally, Fig. 83 presents the MMC-STATCOM F_{20} (unreliability in 20 years) and annual energy losses map considering MVC and conservative approaches. Cases with NLC have lower energy losses than PSC-PWM when the same blocking voltage is considered. As observed in Fig. 83, MVC decreases the energy losses of all cases. This result is expected since MVC directly affects switching losses.

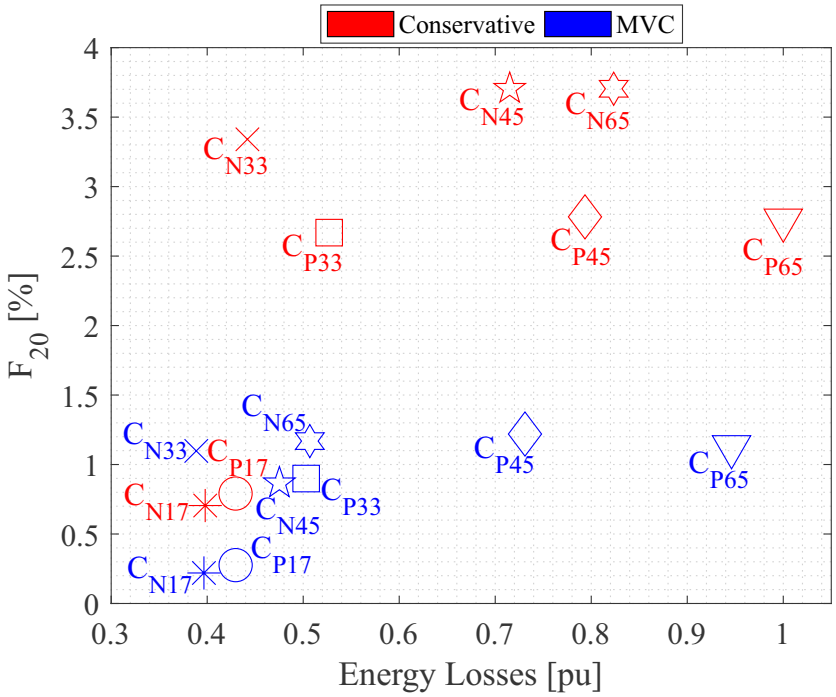
Regarding the F_{20}, MVC decreases unreliability for all cases. Moreover, the MVC approximates the F_{20} of cases with the same blocking voltage and different modulation strategies. The MVC has a higher impact on F_{20} of NLC than PSC-PWM. This is explained by the superior number of capacitors per SM required by the NLC, which are the most affected SM components.

As observed in Fig. 83, this result demonstrates that the relationship between energy losses and unreliability is not straightforward. Moreover, cases of 4.5 kV and 6.5 kV are the most affected by MVC due to their higher energy losses and unreliability with the conservative approach. On the other hand, cases with a blocking voltage of 1.7 kV, C_{P17} (*) and C_{N17} (O), are better positioned in the map, closer to the origin, in which C_{N17} is the most interesting among the cases when MVC is applied.

4.6 Chapter Conclusions

This chapter presented the wear-out procedure and evaluated the minimum SM voltage control effect on wear-out failure and losses of an MMC-STATCOM. The wear-out

Figure 83 – F_{20} and annual energy losses map.(*Remark: the base value of annual energy losses is 128.49 MWh*)



Source: Elaborated by the author.

procedure is focused on the semiconductor devices and capacitors. The semiconductor reliability was evaluated independently for all critical joints. A modified rainflown algorithm was introduced. The analyses were performed with two modulation strategies: PSC-PWM and NLC. Moreover, four different semiconductor blocking voltages were considered: 1.7 kV, 3.3 kV, 4.5 kV and 6.5 kV.

The results demonstrate that the MVC reduces around 53% the wear-out of the capacitors in all case studies. Moreover, MVC decreases the semiconductor devices wear-out in all case studies employing both modulation strategies. MVC approximates the reliability of cases with the same blocking voltage and different modulation strategies and reduces the losses of all cases. Moreover, MVC makes NLC and PSC-PWM reach a similar level of reliability for the blocking voltage. Therefore, the cases with NLC become more interesting due to the lower losses. Among the semiconductor blocking voltages analyzed, 1.7 kV is the most indicated.

Finally, the proposed technique reduces the losses and increases the reliability of the converter with both modulation strategies and different blocking voltages. Furthermore, no hardware modification is required to implement the proposed strategy. For this reason, it can be stated that the MVC has the potential to improve MMC-STATCOM operational costs and reliability.

5 Summary and Research Perspectives

MMC-STATCOMs have important challenges related to the expensive implementation cost of these converters. The previous chapters introduced and evaluated a proposal of a variable dc-side voltage, minimum SM voltage control. The objective of this strategy is the MMC-STATCOM losses reduction and reliability improvement to reduce operational costs. This chapter summarizes the main conclusions and contributions of this Ph.D. thesis and the possible future developments.

5.1 Conclusions

This work proposed a novel control strategy based on a variable dc-side voltage technique: minimum SM voltage control. The proposed technique aims to improve the converter reliability and reduce the losses by controlling the SM voltage reference according to the minimum voltage required on each MMC-STATCOM operational condition. For this purpose, two modulation strategies were employed: PSC-PWM, with a fixed switching frequency, and NLC, with a variable switching frequency. To evaluate the converter with different numbers of SMs, four different semiconductor blocking voltages were considered: 1.7 kV, 3.3 kV, 4.5 kV and 6.5 kV. A control tuning and design methodology of MMC-STATCOM was proposed. Moreover, a wear-out prediction methodology was presented as a figure of merit for reliability evaluation, in which a modified rainflown algorithm was introduced. The conclusions of this work can be divided into three categories:

- MMC-STATCOM design and control methodology;
- MVC potential and dynamic response;
- Losses and Wear-out with MVC.

5.1.1 MMC-STATCOM design and control (Chapter 2)

- Different modulation strategies (e.g. PSC-PWM and NLC) can require different capacitor energy storage requirements to fulfill the same voltage ripple tolerance. This fact affects the SM capacitor bank design.
- Case studies with a higher number of SMs (lower blocking voltages) require a lower number of capacitors in the SM capacitor bank to fulfill the energy storage requirement.

- The design and control tuning proposed demonstrated operational effectiveness. Indeed, the simulation and experimental results showed satisfactory dynamic responses for all case studies and the experimental setup.

5.1.2 MVC potential and dynamic response (Chapter 3)

- The mathematical modeling of the power losses of an MMC-STATCOM demonstrated the potential of losses reduction of MVC. In fact, MVC improves the converter efficiency by reducing switching losses, which are proportional to the SM voltage reference.
- MVC demonstrated operational effectiveness. Indeed, the simulation results showed satisfactory dynamic responses for all case studies with conservative and MVC approaches. Nevertheless, the experimental results demonstrated a slower power response with MVC than with the conservative approach.

5.1.3 Losses and Wear-out with MVC (Chapter 4)

- MVC reduced the losses and increased reliability of the converter in all case studies.
- MVC reduced around 53% the wear-out of the capacitors in all case studies.
- MVC reduced the semiconductor devices wear-out with modulation strategies of fixed (i.g. PSC-PWM) and variable (e.g. NLC) switching frequencies.
- For both control approaches (MVC and conservative), the relationship between energy losses and reliability is not straightforward among the case studies.
- Considering the conservative approach case studies with a higher number of SMs and a lower number of capacitors per SM demonstrated a better trade-off between energy losses and unreliability. When MVC is employed, a higher number of SMs is still the most interesting solution. Moreover, the different number of capacitors per SM (energy storage requirement) required for different modulation strategies has a low effect on the system-level reliability.
- MVC approximates the reliability of cases with the same number of SMs and different modulation strategies. Therefore, energy losses are the determining factor for choosing the best design and modulation strategy. In this work, cases with NLC become more interesting due to the lower losses.

5.2 Research Perspectives

Although many aspects were studied and documented in the present Ph.D thesis, other aspects of the proposal can be explored in future developments of this work. From the author's point of view, the following topics can be approached in further works:

- Improvement of the minimum SM voltage control by considering unbalanced grid voltage and current. The extension of this strategy for unbalanced conditions requires an update of the mathematical modeling of the limits of linear modulation region to guarantee negative voltage and current compensation;
- Evaluation of the minimum SM voltage control application combined with redundancy strategies. In this analysis, the constant failure rate region can be included in the reliability evaluation. Additionally, the effect of redundancy strategy and the computation of the correct redundancy factor can be approached;
- Extension of the minimum SM voltage control strategy for MMCs with other types of submodules, such as hybrid MMC and full bridge MMC. The implementation for other multilevel converters can also be explored;
- Evaluation of the minimum SM voltage control for other MMC applications, such as active power filters. The multifunctional operation of the MMC-based STATCOMs with this strategy can also be explored.

As observed, the possibilities for future developments are many. The author really expects this research project to have continuity after the present Ph.D thesis.

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Biography

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