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SELECTIVE OUTPUT IMPEDANCE-BASED DOUBLE PI LOOP CONTROL STRATEGY FOR SINGLE-PHASE GRID-CONNECTED INVERTERS

Master's Thesis presented to the Graduate Program in Electrical Engineering of the Federal University of Minas Gerais in partial fulfillment of the requirements for the degree of Master in Electrical Engineering.

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"Selective Output Impedance-based Double Pi Loop Control Strategy For Single-phase Grid-connected Inverters"

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Resumo

Nas últimas décadas, avanços significativos foram obtidos em relação aos sistemas de eletrônica de potência, permitindo o desenvolvimento de fontes de energia renováveis como a solar fotovoltaica (FV), eólica, entre outras, cujo uso tem crescido significativamente. Essas fontes, principalmente a solar fotovoltaica, têm uma característica descentralizada, sendo usualmente implementadas em pequenos Geradores Distribuídos (GDs), que são instalados próximos a centros de carga ou na própria unidade consumidora e conectados diretamente a redes de baixa tensão.

No Brasil, desde 2012, quando Agência Nacional de Energia Elétrica (ANEEL) regulamentou a geração distribuída, a potência instalada desses geradores aumentou exponencialmente. Apesar da representatividade dessa modalidade de geração ainda ser pequena frente ao Sistema Interligado Nacional (SIN), entende-se que o seu atual estágio de desenvolvimento e disseminação é ideal para a realização de pesquisas e trabalhos nessa área, pois o seu desenvolvimento traz novos desafios técnicos e regulatórios. O trabalho aqui apresentado expõe contribuições nesse sentido, colaborando com os avanços tecnológicos que permitem o desenvolvimento de sistemas de gerações distribuídos mais eficientes e robustos.

Este trabalho propõe um esquema de controle de potência para inversores de potência monofásicos conectados à rede baseado no uso de controladores PI implementados em coordenadas naturais (abc). O seu comportamento físico e modelo matemático são apresentados e analisados detalhadamente e a impedância de saída do conversor é derivada analiticamente para avaliar a sua capacidade de rejeição a perturbações. Os resultados mostram que o esquema proposto é efetivamente capaz de rejeitar as perturbações causadas pela tensão da rede, obtendo baixos valores de THD da corrente injetada, mesmo com significativa distorção harmônica da tensão.

Adicionalmente, o Conversor Duplo, que consiste na associação em paralelo de dois conversores controlados em corrente, é também apresentado como um estudo de caso. A análise dessa configuração objetiva auxiliar na avaliação dos modelos matemáticos derivados e da estratégia proposta para controle de potência.

Abstract

Over the last decades, significant advancements were made on power electronic systems. This allowed the development of Renewable Energy Sources, such as Solar Photovoltaic (PV), Wind and many others, that have been remarkably growing in the last years. These sources, especially solar PV, are characterized by their decentralized characteristic, being usually implemented in small Distributed Generators (DGs) installed near to or in consumer centers and connected directly to low-voltage networks.

In Brazil, since 2012, when the electrical energy regulating agency allowed the connection of DGs to the distribution grid, their installed capacity has increased exponentially. Although their total installed capacity is still not a significant part of the Brazilian National Interconnected System, their current state of development demands intense study as they bring new technical and regulatory challenges. The work carried herein presents contributions in that sense, collaborating with technological advancements that allow the development of more efficient and robust distributed generation systems.

This work proposes a power control strategy for single-phase Current-Driven Grid-Connected Converters based on the use of natural frame PI controllers. Its physical behaviour and mathematical model are presented in detail and the inverter output impedance is analytically derived to analyze the disturbance rejection capability of the system. The results show that the proposed scheme is capable of effectively rejecting disturbances originating from the grid voltage, achieving low current THD lower even with highly distorted grid voltage.

The concept of the Double Converter Configuration, which consists in the parallel association of two current-driven converters, is also presented as a case study. The analysis of this configuration also helps the evaluation of the derived mathematical models and the proposed power control strategy.

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Chapter 1

Introduction

The 20th century saw a revolution unlike any other in human history. Across all areas of knowledge, huge advancements were achieved and new technologies were developed, allowing an era of unmatched development and growth. As a consequence, human population grew sharply, from around 2.5 billion in 1950 to 7.7 billion in 2019 [1] and, consequently, a proportional increase in resource extraction, consumer goods production and energy generation was necessary. In spite of the technological advancements, which allowed the development of new power sources, the bulk of the energy demand continued to be supplied by fossil fuels, such as oil, coal and gas. Until 2017, these sources accounted for roughly 80% of the world energy supply, including transportation, as illustrated in Figure 1.1 [2]. However, their use has enormous drawbacks. In the 1970s, for example, the petroleum crisis showed that the world was too reliant on a scarce and non-renewable source of energy and, with that, there came severe economic, social and geopolitical consequences. Although petroleum production continued to rise in the following decades, as technological advancements allowed its extraction in ever increasing depths and less accessible places, its production is still dominated by a few countries, making it susceptible to political interference, causing great uncertainty and leading to volatility in price, which greatly impacts the world economy.

In this context, over the last decades, power electronic systems started to mature and their cost decreased significantly. Consequently, it found ever increasing areas of application, such as industry, transportation and power systems, enabling an increase in productivity and energy savings [3]. Its advance also allowed the development of Renewable Energy Sources (RES), such as Solar Photovoltaic (PV), Wind and many others that now present a viable alternative to the use of fossil fuels, bringing strategic, technical, environmental and social benefits. Economically, renewables also present advantages, since their cost of operation is low, as they have no need for fuel, and

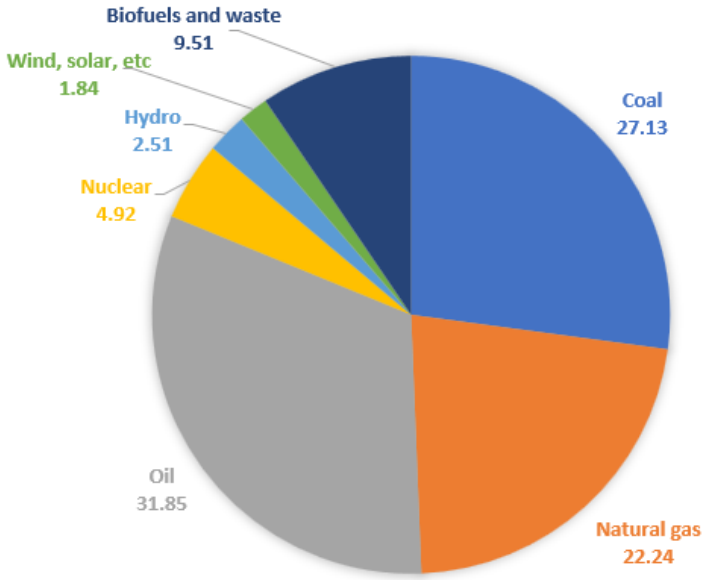

Figure 1.1. World energy consumption by source in 2017 [2]

can be placed next to or in the consumer centers, reducing the distribution distance and minimizing system losses. Additionally, as most countries are highly dependent on fossil fuels, many governments choose to hand out subsidies to their use. The latest estimation of the International Monetary Fund (IMF) showed that, in 2015, these subsidies amounted US$4.7 trillion globally, accounting for a total of 6.3% of the global Gross Domestic Product (GDP) [4]. This number was expected to grow to US$ 5.2 trillion in 2017. Increasing the use of RES may be a way of reducing such costs.

In the early years of the 21st century, the growth of renewable energy was remarkable, especially with solar and wind generation quickly rising in installed capacity. Academic interest on this subject also grew and a substantial amount of research was produced regarding the use, construction and efficiency improvement of these systems. Recent years also saw an increase in the awareness over the impact that human activity and energy consumption has over the environment. As the world population is expected to continue grow until the end of the century [1], there is great concern about sustainability. In that sense, it is expected that power electronics will play an even more important role in the following decades, as it can help pave the path for a more sustainable development.

In Brazil, as in the rest of the world, the energy consumption is still supplied mostly by fossil fuels, although the electricity generation is mostly reliant on renewable sources. Brazil has a country-wide interconnected electrical system, in which hydroelectric power accounts for 68% of the total installed capacity. Wind, solar and other renewable sources account for an extra 18%, thermonuclear for 1% and fossil fuel

powered thermoelectric for the remaining 13% [5]. In the last decades, however, the expansion of hydroelectric power has been limited, since the sites with most potential for the construction of new power plants are located mainly in the northern region, far from the biggest cities and consumer centers. Social and environmental issues are also a major drawback for its expansion, as these sites are located in the Amazon forest region. Additionally, in recent years, severe droughts affected Brazil, lowering the reservoirs to critical levels and forcing the system operator to scale back their use, at the cost of an increase in generation from thermoelectric fossil-fuel powered plants.

Considering all these issues, it is evident that the current model, in which electricity is generated in centralized locations and distributed over long distances, has reached a saturation point. Therefore, a solution to increase electricity generation in a more sustainable way must be found. Today, the alternative that shows greater viability is the Distributed Generation (DG), which can be defined as *"an electric power source connected directly to the distribution network or on the customer side of the meter"* [6]. This model has as its main benefits the use of clean and renewable power sources, lower environmental impact, sustainability and possibility of electrical matrix diversification. It also reduces the burden placed on centralized power plants as well as the losses and loading in transmission and distribution lines, which allows utilities to postpone investment in expanding their infrastructure. Additionally, as such generators are usually based in power electronics, they allow the implementation of several ancillary functions which help to increase the system efficiency and power quality.

The motivation for this work comes from the laid out background. The necessity for fast change in the energy supply scenario has brought great interest in distributed generation and driven an accelerated development of the sector. In Brazil, since 2012, when the electrical energy regulating agency allowed the connection of DGs to the distribution grid, their installed capacity has reached 2.2 GW, with only solar PV amounting to 2 GW [7]. Although this value is still negligible compared to the entirety of the Brazilian electrical system, its current state of development demands intense study as this new generation model brings new technical and regulatory challenges that must be addressed and discussed to provide a theoretical basis that can be used to solve future problems that may arise when the DG achieves more significant penetration levels. To accomplish that, Current-Driven Grid-Connected converters, responsible for interfacing sources like solar PV and wind to the grid, must be able to operate not only as power sources, but as active components of the electrical grid, helping on the mitigation of disturbances and contributing for the improvement of its security, reliability and energy quality. The work carried herein presents contributions in that sense, collaborating with technological advancements that allow the development of

more efficient and robust distributed generation systems.

Finally, the concept of the Double Converter Configuration is also presented herein. This configuration consists in the parallel association of two current-driven converters and is chosen as a case study to evaluate an alternative of assuring the compliance of older grid-connected inverters, that operate with unity power factor and do not implement ancillary functions, with newer standards and requirements. In this case, instead of replacing the existing converter, the connection of a supplementary unit is proposed to retrofit the old one and assure the correct operation of the system. The analysis of this configuration also helps the evaluation of the derived mathematical models and proposed power control strategy.

1.1 Grid-Connected Converter Control

Renewable power sources are usually interfaced with the electrical grid through power converters, usually implemented as Grid-Feeding Inverters [8], in which the system has a current source characteristic with high output impedance. The basic function of these converters is regulating the power flow to the grid, but they must also comply with operation standards, such as the IEEE Std 1547-2018 [9] or one of many others country specific regulations, that establish requirements for the connection of the Distributed Generators (DGs) to the grid, such as the limitation of the Total Harmonic Distortion (THD) of its output current to certain limits, Volt/VAr control and the implementation of other ancillary functions. These systems must also be robust enough to not be affected by external disturbances, as distortions on the voltage waveform at the connection point of the DG, referred herein as Point of Common Coupling (PCC).

A vast amount of publications is available in the literature proposing and evaluating different control strategies for current-driven grid-connected converters. They can be broadly categorized as linear and non-linear. One of the most common non-linear strategies is the hysteresis control [10], that is easy to implement and has a very fast dynamic, but does not have a fixed switching frequency, which complicates the design of the converter output filter and the overcurrent protection. The Repetitive control [11] is also very common, but is more complex to implement and needs careful tuning to avoid instability. Many other non-linear strategies are also discussed on the literature [12], but such controllers are not the focus of this work. In here, for greater simplicity and fairness of comparison, only linear strategies are analyzed.

The linear control category can be further subdivided into three groups. Assuming that the inverter has an LCL output filter, there are three state variables that can

be individually controlled: the current of the converter-side inductor (i_f), the capacitor voltage (v_o) and of the grid-side inductor current (i_g). Other variables, such as the filter capacitor current (i_c) and inductor voltages (v_f and v_g) are considered auxiliary variables. This is also true for converters with LC filters connected to a grid with inductive characteristics. Therefore, the inverter control strategies can be categorized as [13]: single-loop [14, 15, 16], double-loop [17, 18, 19] and triple-loop control [20, 21, 22].

The single-loop category comprehends the control systems in which only one of the state variables is controlled and, therefore, only three configurations are possible. The capacitor voltage control has limited applications, being mostly used in Uninterruptible Power Supply (UPS) systems [23] and voltage-source-based grid-supporting inverters for Microgrids [8]. Since it does not directly control either of the currents, it does not provide resonance damping nor overcurrent protection. The grid-side current control is widely used in grid-tied inverters because of its ability to regulate the power flow, control harmonic distortion and provide overcurrent protection. However, its control is inherently unstable [24], requiring that additional measures are taken, as the use of passive or active damping methods, increasing the complexity of its implementation, or the use of an external control loop, categorizing a double-loop control system. Finally, there is the converter-side inductor current control. Because of its simplicity, low-cost and inherently stable control system [25, 26], this is the most widely used single-loop strategy. It provides overcurrent protection and power flow regulation, but is not capable of directly controlling the power flow exchange with the grid or regulate grid current harmonic distortion, since the interaction between the grid and the capacitor is not controlled. In general, single-loop control strategies have difficulty in limiting current harmonics and avoiding resonances between the converter and the grid.

The double-loop category comprehends the strategies in which the control of two different variables are cascaded, allowing for the simultaneous regulation of two quantities. Although they do not necessarily need to be both state variables and an auxiliary one may be used, the use of inductor voltages is rarely addressed in the literature [23] and, thus, most double-loop strategies use a combination of the three aforementioned state variables and filter capacitor current. This structure has the benefit of increasing the flexibility of the controller design. As an example, the inherent instability of the grid-side inductor current control can be compensated by adding an inner loop that regulates the capacitor current [18]. The overall performance of the dual-loop configuration is usually superior to the single-loop strategies, but it is still limited regarding the simultaneous implementation of ancillary services, such as Low-Voltage Ride Through (LVRT), seamless transition between grid-tied and islanded operation modes, harmonic rejection and resonance damping [13].

The triple-loop control consists on the cascading of three control loops. The most commonly discussed configurations in the literature are the $i_f - v_o - i_g$ [22] and $i_c - v_o - i_g$ [20], although many others may be implemented. Compared to both single and double-loop, these structures present greater control flexibility and achieve better performance, allowing the implementation of a system that is robust, capable of performing ancillary functions and resilient to external disturbances and parameter variations. A disadvantage is that, to avoid unwanted interaction between two controllers, the cutoff frequency of a loop has to be limited by the inner one. Therefore, the outermost control loop usually has a narrow bandwidth, requiring that measures are taken to improve the system performance, such as the reduction of sampling delays or the use of wide bandwidth controllers on the innermost loop.

Regardless of the category that the chosen strategy falls into, the used controller configurations are usually the same. The most common ones are the Proportional (P), the Proportional-Integral (PI), implemented in stationary or synchronous reference frames, the Proportional-Resonant (PR), Proportional-Integral-Resonant (PI-R) [27, 28], and the Dead-Beat (DB) [14, 13]. For the stationary-frame PI, the most challenging issue is the low gain of the open loop transfer function at higher frequencies, which causes steady-state error when tracking time-varying references. To overcome this limitation, the Park transformation is widely used, since it allows to represent the error signals as DC quantities in the dq-frame, where PI controllers ensure zero steady-state error. Still, it does not allow the elimination of oscillations that appear in the dq quantities under unbalanced grid voltage conditions, requiring the use of two controllers to independently regulate the positive and negative sequence components [8]. Similarly, for harmonic compensation, a reference frame has to be used for each frequency, increasing the computational cost of its implementation. However, in case of single-phase applications, the Park transformation cannot be directly applied, so a quadrature voltage signal has to be synthesized, which is typically done by displacing the measured voltage by a quarter fundamental period. In [29], a simplified method to calculate the dq components is proposed, improving the system dynamics, but the other aforementioned problems remain unaddressed.

PR and PI-R controllers solve the drawbacks of the natural frame PI. Their high gain at selected frequencies enhances the Dynamic Stiffness (DS) [19, 30] of the system, which is a measure of its disturbance rejection capability. These types of controllers provide reasonable results, even in very adverse grid conditions, and can be used for selective harmonic compensation [17]. Their main drawback when compared to the PI is their increased complexity and difficult implementation, especially when the control of multiple harmonic components is required or when the grid frequency oscillates over

a wider range, as is the case in weak power systems, such as off-grid networks.

Finally, there are several works reporting good results with the use of Dead-Beat controllers [13]. This type of controller is relatively simple and capable of regulating harmonic components without the need for several parallel units, which is an advantage over the resonant controllers. Its wide bandwidth also makes it a good choice to be used in the inner control loop of a triple-loop configuration. However, its optimum performance requires an accurate knowledge of the controlled system's parameters, posing an additional requirement with respect to the PI implementations.

This work presents a double-loop control strategy, in which the internal loop regulates the filter inductor current while the external one regulates the power flow and harmonics, and explores commercial solutions widely used for grid-connected converters. Both loops use exclusively PI controllers. Hence, the proposed strategy is simple and easy to implement. It will also be shown that it can compensate for the discussed limitations of the PI controller, achieving a low output current THD even when the grid voltage presents significant harmonic content.

1.2 Objectives

1.2.1 General Objectives

This work aims to study and evaluate the operation and behaviour of control systems and strategies applied to Current-Driven Grid-Connected Converters, widely used for interfacing Renewable Energy Systems to the grid, in the context of their ability to implement ancillary and grid-support functions, allowing the Distributed Generator to operate as an active part of the grid. The advantages and drawbacks of several control strategies commonly addressed in the literature are discussed and a double-loop control system based exclusively on PI regulators is proposed.

1.2.2 Specific Objectives

More specifically, the objectives that this work aims to accomplish are:

1. Development of a digital control strategy for current-driven grid-connected converters that achieves high Dynamic Stiffness;
2. Evaluate the performance of the proposed digital control strategy;
3. Implement the proposed digital control strategy on a commercially available PV inverter to experimentally validate its operation.

1.3 Contributions

The main contributions of this work are listed as follows:

1. Derivation of a mathematical equivalent model for the Current-Driven Grid-Connected and Double Converters;
2. Calculation of the Output Impedance for Grid-Connected and Double Converters;
3. Proposal of a power and harmonics control strategy based on PI regulators;
4. Design and development of the Microgrids Laboratory at the Engineering School of the Federal University of Minas Gerais.

1.4 Text Organization

This text is structured in seven chapters. This first one presents an introduction to the studied topic, the state of the art in control strategies for grid-connected converters, discusses the advantages and drawbacks associated with each one and states the main objectives and contributions brought by this work. Chapter 2 presents the converter configurations studied herein, discusses the basics about their operation, derives their mathematical model and introduces the concept of Dynamic Stiffness.

Chapter 3 is more oriented to the design and practical implementation of the converters. Procedures for sizing its output filter and tuning the current controller are presented. It then concludes with the derivation of the closed-loop transfer function of the current control loop, laying the groundwork for the proposed strategy, which is presented in Chapter 4. This chapter starts by introducing the concept upon which the power control loop is built, showing that the disturbance currents can be compensated by manipulating the current control reference in a specific way. Then, it describes the proposed strategy and explains in detail each one of the algorithms that had to be implemented. It concludes by demonstrating that the use of the power control loop causes an increase in the Dynamic Stiffness of the converter, achieving a similar result to the one obtained by applying resonant controllers to the current control loop. Then, Chapter 5 presents the Microgrids Laboratory that was designed and built at the Engineering School of the Federal University of Minas Gerais as part of this work, which is where the experiments that compose this work were conducted. Chapter 6 shows and discusses the simulation and experimental results and, finally, Chapter 7 presents the conclusions that can be drawn from this work and discusses possible future research.

Chapter 2

System Modelling

This chapter presents the circuit, configuration and functionalities of the converters studied in this work. First, a Current-Driven Grid-Connected Converter will be analyzed. After, a case study, consisting on the parallel association of a supplementary converter to an existing grid-tied inverter will be presented.

The mathematical model of the current control loop is discussed and each one of its components is studied in detail. For now, the behaviour of the systems is analyzed when using a single-loop current control, that is, when there are no outer voltage or power loops regulating the reference signal that is fed to the current control. Finally, the concept of Dynamic Stiffness (DS) is introduced as a figure of merit to quantify the resilience of the control system to external disturbances.

2.1 Grid-Connected Converter

The first system studied herein is a current-driven grid-connected converter composed of a single-phase VSI, as illustrated by Figure 2.1, and operating as a *Grid-feeding inverter* [8], meaning that it is seen by the grid as a controlled current source with a high output impedance. This kind of system is normally used to interface RES, such as PV plants or wind turbines, with the grid,

With the ever increasing installed capacity of RES in the past decades, the interest of researchers in the subject also grew and, with that, several different configurations were proposed to build such a system [31]. These converters are usually composed of multiple stages, being the most common first stage a DC-DC converter, such as a Boost converter, that is used to link the primary energy source to the DC bus. It is usually responsible for making the voltage levels compatible with the system operation and for implementing functions such as Maximum Power Point Tracking (MPPT) for

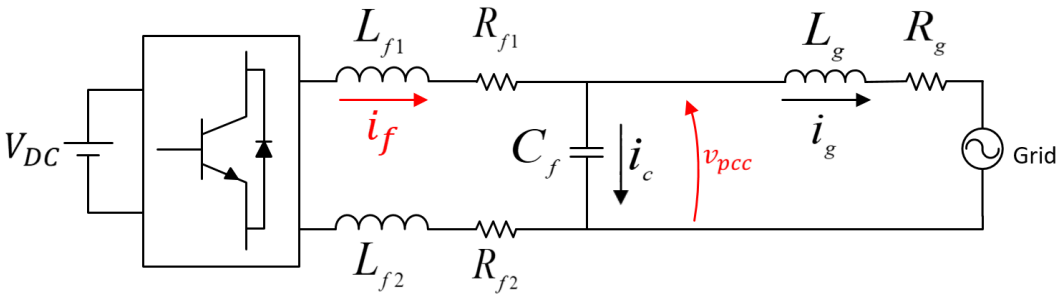

Figure 2.1. Grid-Connected Inverter

PV systems. However, as the focus of this work is the connection between the inverting stage and the utility grid, the primary energy source and the first stage are simplified and represented as an ideal DC voltage source.

In this work, the analyzed configuration is the same one employed by the commercial inverter used on the experimental setup and is one of the most common for small power PV applications. As shown on Figure 2.1, it consists of a transformerless inverter, with an IGBT H-bridge as the inverting stage and an LC circuit in the output for filtering of the switching ripple. The filter inductor is divided into two equal parts (L_{f1} and L_{f2}) and connected to both output terminals of the transistor H-bridge to reduce the circulation of common mode currents through the semiconductors [32, 33]. R_{f1} and R_{f2} are the parasitic Equivalent Series Resistance (ESR) of the inductors. L_g and R_g are the grid inductance and resistance, respectively, and, thus, are not part of the output filter, although this inductance also slightly helps to attenuate the output current harmonics. The filter current, i_f, and the PCC voltage, v_{pcc}, are highlighted as these are the quantities used to implement the current control described in this section and the power control presented in Chapter 4.

2.1.1 Current Control Loop

In Voltage Source Inverters (VSIs), the filter current control is done by regulating the H-bridge output voltage. The difference between this voltage and the grid forces the desired current flow through the filter inductor. The voltage modulation is usually done by using a Pulse Width Modulation (PWM) system to drive the H-bridge switching.

The block diagram of the current control loop is shown in Figure 2.2, where $C_i(s)$ represents the current controller and $G_d(s)$ models the computational delay. C_{pk} is the PWM carrier peak-to-peak amplitude, $DPWM$ is the digital PWM model, $G_{conv}(s) = 2V_{DC}$, where V_{DC} is the DC-link voltage, as shown in Figure 2.1, is the converter Transfer Function (TF) for three-level PWM [34], H_i is the current transducer

gain and v_{pcc} is the voltage at the PCC. Z_f represents the output filter impedance. For frequencies lower than half of its resonance, the filter model may be approximated by a single inductor [35], that is, the current that flows through the capacitor may be disregarded and. Thus, i_f can be considered equal to i_g and the filter impedance can be represented as $Z_f = sL_f + R_f$.

The block in the feedback path represents the sampling of the filter current and indicates that the controller system is digital. The transition back from the digital to the continuous domain is done by the DPWM system. The multiplication and sum by $c_{pk}/2$ are used to ensure that the modulating signal sent to the PWM is between 0 and 1. This was used to make the model compatible with the experimental setup, that will be described in Chapter 5.

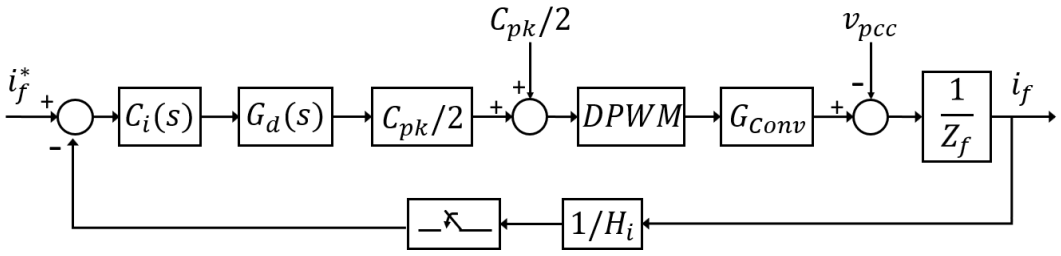

Figure 2.2. Inverter-side current control loop.

2.1.1.1 Computational Delay Model

In analog control systems, the control signal is continuously updated based on the changes of the controlled quantity with minimal time delay between the disturbance in the output and the control action. In digitally controlled systems, however, there is an inherent delay between the sampling of the controlled quantity and the update of the control action due to the Analog-to-Digital Conversion (ADC), to the time spent by the digital processor to perform the calculations that compose the control algorithm and to the time needed to update the PWM duty cycle. In most Digital Signal Processors (DSPs) used to implement the current control in inverter systems, the PWM is synchronized with the modulating signal and its duty cycle is updated to the compare register, where the value used as a reference to the PWM comparator is stored, when the carrier reaches zero and/or its peak value. Hence, it is necessary to consider the effect of sampling and account for its inherent delay when tuning the controller.

The computational delay can be modelled by applying the time translation property of the Laplace Transform that states:

$$\mathcal{L}\{x(t)\} = X(s) \longleftrightarrow \mathcal{L}\{x(t-t_0)\} = e^{-st_0} \cdot X(s) \tag{2.1}$$

This delay can also be expressed in function of the sampling period of the system (T_s), as shown in (2.2), where λ is a constant used to adjust the delay

$$G_d(s) = e^{-s\lambda T_s} \tag{2.2}$$

2.1.1.2 PWM Modelling

In an analog control system, the PWM sampling is natural and does not insert any delays in the current control loop [34]. However, as is the case in almost all modern systems, in this work, a digital controller is used. Herein, it is assumed the use of a symmetrical, uniformly sampled, single-update PWM, with unipolar modulation and triangular carrier [36]. According to [34, 37], it is possible to model the DPWM delay as a *zero-order hold* and thus, the frequency response of this kind of system is as shown in (2.3), where D is the duty cycle.

$$DPWM(s) = \frac{1}{2c_{pk}} \cdot \left(e^{-s(1-D)\frac{T_s}{2}} + e^{-s(1+D)\frac{T_s}{2}}\right) \tag{2.3}$$

Since the switching frequency is usually very high, in the order of dozens of kHz and the sampling frequency is twice this value, it is reasonable to assume that T_s is a very small number and, therefore, it is possible to assume that D is constant during one switching period. Through the use of the Euler identity, (2.3) can be rewritten as:

$$\begin{aligned} DPWM(s) &= \frac{1}{2c_{pk}} \cdot \left(e^{-s\frac{T_s}{2}} \cdot e^{s\frac{DT_s}{2}} + e^{-s\frac{T_s}{2}} \cdot e^{-s\frac{DT_s}{2}}\right) \\ &= \frac{e^{-s\frac{T_s}{2}}}{2c_{pk}} \cdot \begin{pmatrix} \cos(\omega D\frac{T_s}{2}) + j\sin(\omega D\frac{T_s}{2}) + \\ \cos(-\omega D\frac{T_s}{2}) + j\sin(-\omega D\frac{T_s}{2}) \end{pmatrix} \end{aligned} \tag{2.4}$$

To simplify this result, since T_s is very close to zero, the *cosine* terms are considered equal to 1 while the *sine* terms are considered equal to 0, resulting in the expression shown in (2.5).

$$DPWM(s) = \frac{e^{-s\frac{T_s}{2}}}{c_{pk}} \tag{2.5}$$

Linearizing this equation through the Padé approximation, the following result is obtained:

$$DPWM(s) = \frac{1}{c_{pk}} \cdot \frac{1 - s\frac{T_s}{4}}{1 + s\frac{T_s}{4}} \tag{2.6}$$

To simplify the final model, the computational time delay represented by (2.2) is inserted into the PWM model and a single transfer function is derived to model both blocks. To do this, the sampling time in (2.6) has to be increased by λT_s, resulting in (2.7). In most applications, λ is typically either 0.5 or 1 [25]. For practical reasons, the current control used in this work is implemented in a manner that the feedback signal is equal to the average of the last two samples and, consequently, the delay between the measurement and update of the modulation signal is increased. Because of that, the delay between the first sample and the control actuation is equal to one switching period. Therefore, λ is considered equal to one. Consequently, the PWM can be modeled as shown on (2.7)

$$\begin{aligned} DPWM(s) &= \frac{e^{-s(1+2\lambda)\frac{T_s}{2}}}{c_{pk}} \\ DPWM(s) &= \frac{1}{c_{pk}} \cdot \frac{1 - s(1+2\lambda)\frac{T_s}{4}}{1 + s(1+2\lambda)\frac{T_s}{4}} \\ DPWM(s) &= \frac{1}{c_{pk}} \cdot \frac{1 - s\frac{3T_s}{4}}{1 + s\frac{3T_s}{4}} \end{aligned} \tag{2.7}$$

2.1.2 Dynamic Stiffness (Output Impedance)

If a short-circuit is applied to the output of the current-driven converter, the current control loop shown in Figure 2.2 does not have any disturbances because, in that case, v_{pcc} is equal to zero. Although the PI controller has a poor performance in tracking time-varying signals, by simulating the operation of the system in such a configuration, it is seen that, at the fundamental frequency, the PI is still capable of accurately controlling the current, as shown in Figure 2.3. Nonetheless, when the current-driven converter is connected to the grid, the circulation of an unwanted current is observed, even if the current reference signal is set to zero, as shown in Figure 2.4. Therefore, it is possible to conclude that this behaviour is not due only to the poor performance of the PI controller regarding sinusoidal references, but must also be related to the presence of disturbances external to the current control loop.

The resilience of a system to a disturbance is characterized by its Dynamic Stiff-

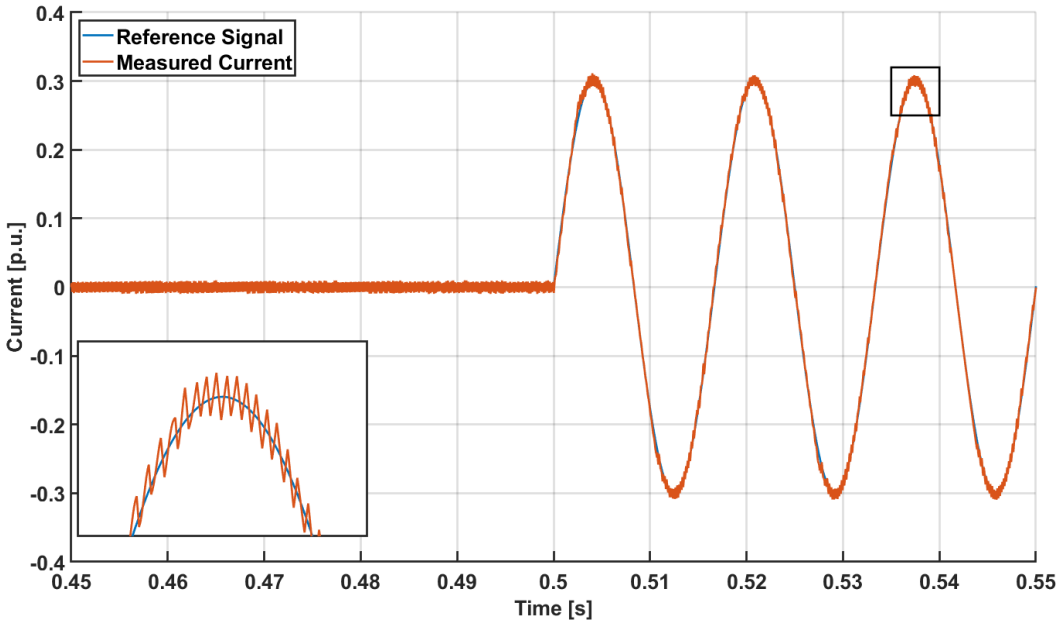

Figure 2.3. Operation of the current control in a short-circuit test with a 60Hz reference.

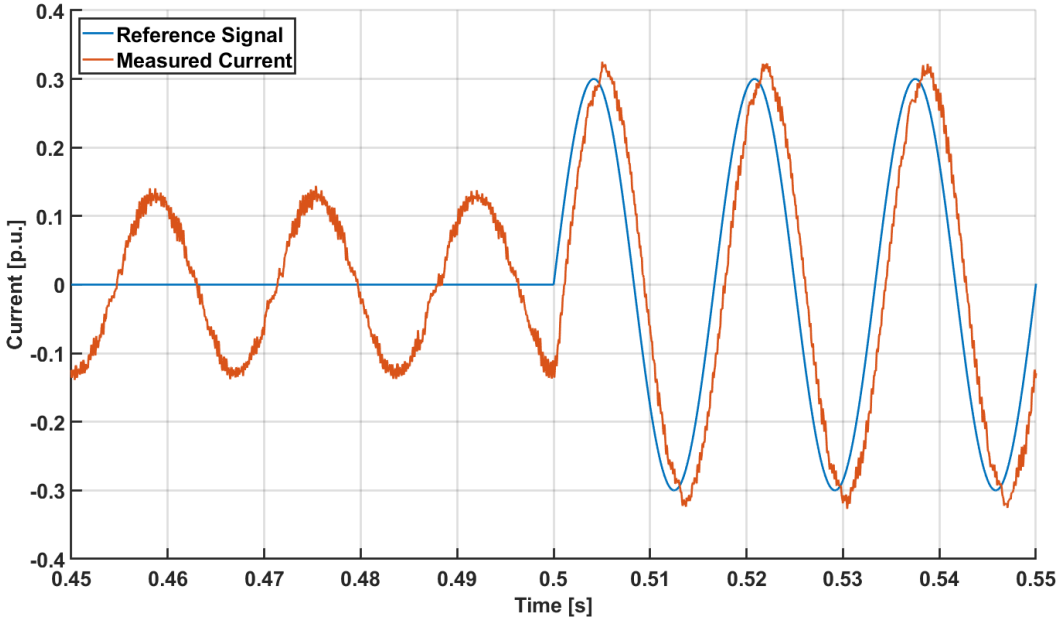

Figure 2.4. Operation of the current control connected to the grid with a 60Hz reference.

ness [19, 30, 38]. This quantity is defined as the capability of a system to reject a disturbance caused by an external source and is quantified as the amplitude of the external disturbance needed to produce a unit variation in the controlled quantity. It may be used to analyze any system but, in the particular case of current-driven grid-connected converters, the two possible external disturbances are the grid voltage and load currents. However, loads connected to the PCC do not significantly affect the performance of current-controlled converters and, therefore, the most important disturbance to be analyzed is the grid voltage. Since the controlled quantities are either the filter or grid currents, the system Dynamic Stiffness is equal to its Output Impedance (Z_{out}) and has unit of Ohms [Ω]. From now on, these two terms are used interchangeably.

The actual output impedance perceived by the grid at the PCC is different from the simple association of the passive filter components. For example, if the the reference is equal to zero, the controller will actively drive the PWM to modulate the output voltage and minimize current flow through the filter inductor and, thus, the current circulation is not determined only by the inductor impedance. Consequently, the computation of this quantity has to also take into account the effect of the current control and, therefore, is very much affected by the type of controller used.

2.1.2.1 Dynamic Stiffness Regarding the Filter Current

The Dynamic Stiffness considering the filter current as the system output is derived from the block diagram in Figure 2.2 as the inverse of the TF between i_f and v_{pcc}. This diagram is redrawn in Figure 2.5 to more clearly show its derivation and the resulting expression is shown in (2.8). For now, to simplify the initial analysis, the PCC voltage is considered as the source of the disturbance. It is straightforward that a higher impedance makes the system less susceptible to voltage disturbances.

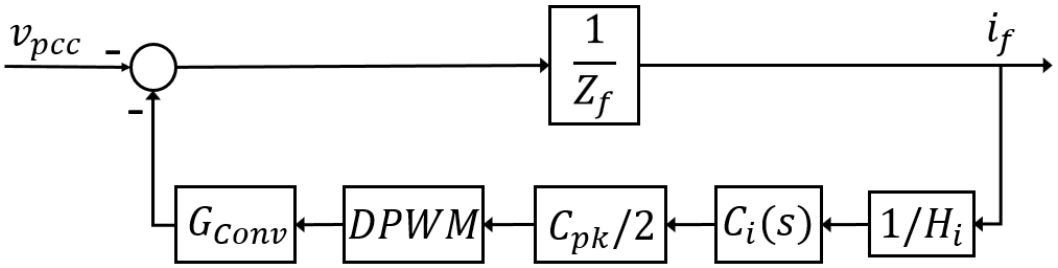

Figure 2.5. Block diagram for determination of the output impedance regarding the filter current and PCC voltage.

$$Z_{i_f}^{v_{pcc}}(s) = \frac{v_{pcc}}{i_f}(s) = -\left(\frac{V_{DC} \cdot DPWM(s) \cdot C_i(s)}{H_i} + Z_f\right) \tag{2.8}$$

This equation shows that the magnitude of $Z_{I_f}^{v_{pcc}}$ is directly proportional to the open-loop gain of the controller TF. This explains why some controller configurations have better disturbance rejection capability. The PI-Resonant, for example, has high gain on selected harmonics that yield high output impedance at those frequencies. The Dynamic Stiffness is also high when Dead-Beat controllers are used, since they have high gain in a wide range of frequencies [13]. As such, the disturbance rejection capability of the current control is high when these controllers are used. PI controllers, however, have poor disturbance rejection capability due to their low gain (lower than 40dB) in medium to high frequencies, leading to poor performance when the inverter is connected to a grid with distorted voltage.

To illustrate this difference, Figure 2.6 shows the comparison between the Output Impedance of a current-driven grid-tied converter when a PI or PI-Resonant controllers are used. The fundamental grid frequency (60 Hz), third and fifth harmonics are highlighted. It can be seen that, for the PI controller, the impedance drops when the frequency increases, yielding a low value in the range between 180-900Hz. Since the most significant power system voltage harmonics are usually located in this range (3^{rd} to 15^{th} harmonics), this deteriorates the inverter performance. In higher frequencies,

however, the impedance magnitude rises again due to the natural behaviour of the filter inductor. In contrast, as expected, for the PI-R controller, the output impedance has high-gain peaks on the selected frequencies. Consequently, perturbation currents imposed by these harmonics of the grid voltage are low.

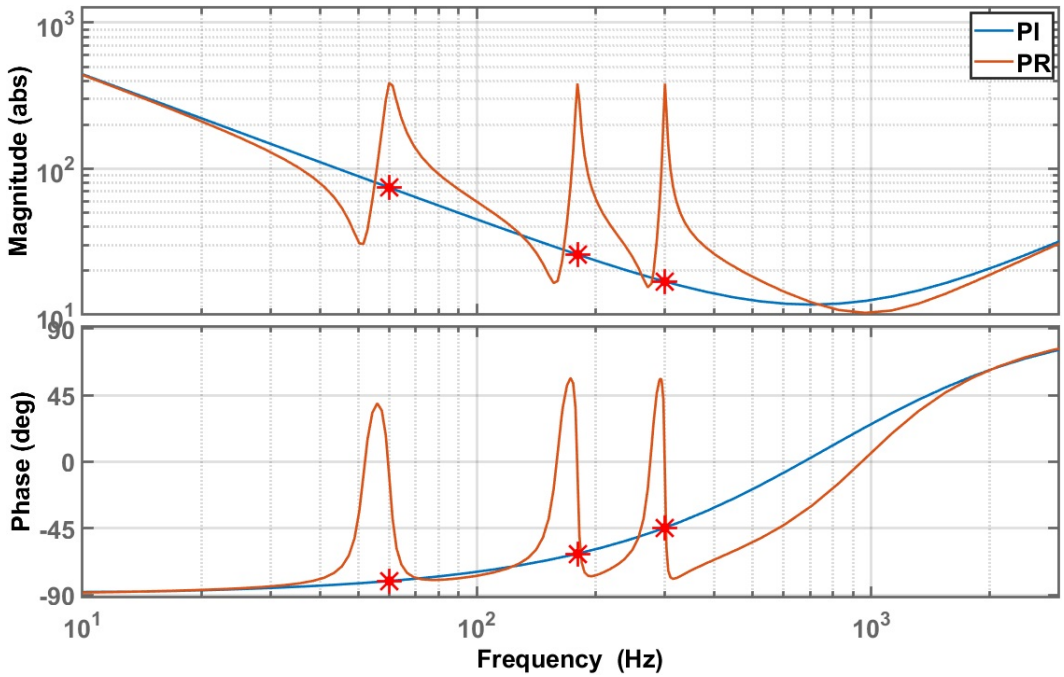

Figure 2.6. Example of Dynamic Stiffness for a current-driven grid-connected inverter for PI and PR current controllers.

An analogous approach may be derived to obtain the Output Impedance regarding the grid voltage ($Z_{i_f}^{v_g}$). This quantity is not as practical, since its derivation depends on the value of the grid impedance, which is not always known nor easy to determine. However, it may be useful for configurations such as the one used on the experimental setup built for this work, where an isolation transformer is connected to the system output. In this case, the grid impedance may be reasonably approximated by the transformer leakage inductance and wire resistance.

If the diagram of Figure 2.5 is redrawn to include the relationship between the filter current and the voltages from the grid and the Point of Common Coupling, the result shown on Figure 2.7 is obtained. In this figure, $Z_{i_f}^{v_{pcc}}$ is the output impedance derived in (2.8), Z_g is the grid impedance and Z_c is the filter capacitor impedance. The manipulation of this diagram yields an expression relating the grid voltage (v_g) directly to the filter current (i_f), as shown on (2.9).

$$Z_{i_f}^{v_g} = \frac{Z_g \cdot (Z_{i_f}^{v_{pcc}} - Z_c) + Z_c \cdot Z_{i_f}^{v_{pcc}}}{Z_c} \tag{2.9}$$

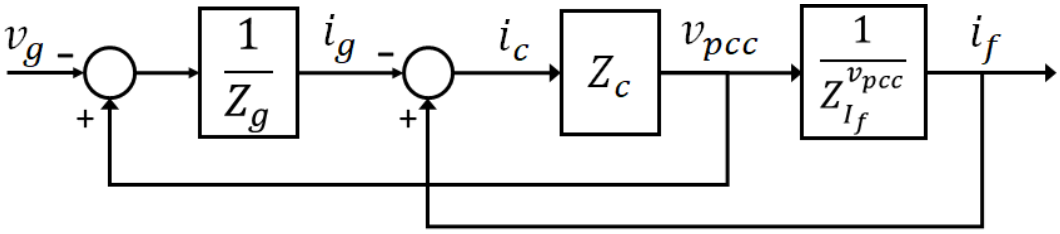

Figure 2.7. Block diagram for the derivation of the output impedance regarding the filter current and grid voltage.

Figure 2.8 shows the difference between the quantities calculated based on (2.8) and (2.9). It is possible to see that, for low frequencies, the impedances are all very similar, because in this range the response is dominated by the controller, since the inductor reactance is small. For higher frequencies, however, the series inductor dominates the response and, thus, the impedances vary significantly. In this region, the magnitude increases faster for the impedance calculated in (2.9), because it considers the grid impedance and, thus, the total equivalent inductance is higher.

Another discerning point between the two forms of calculating the output impedance is the ability to model the interaction between the converter filter and the grid impedance. From Figure 2.8, it is clear that the magnitude of the curve representing $Z_{i_f}^{v_g}$ decreases around 2.5kHz, which is caused by the resonance between the inverter output filter and the grid inductance. This interaction could not be determined when analyzing only the impedance regarding the PCC voltage.

2.1.2.2 Dynamic Stiffness Regarding the Grid Current

The block diagram shown on Figure 2.7 can also be rearranged to illustrate the transfer function between the grid current and voltage. The equation resulting from this derivation is shown in (2.10). This equation may be interpreted as the parallel association of the inverter output impedance and the filter capacitor, summed to the grid impedance. Both negative signs, outside the parenthesis and in the fraction denominator, are due to the conventional current direction. In this work, the positive direction of the output filter current is adopted as being going out from the converter and into the grid, while the positive direction of the capacitor current is flowing into the capacitor, as shown on Figure 2.1. However, if the position of the current sensor is inverted, the negative sign is removed. The frequency response associated to this equation is also shown on Figure 2.8.

$$Z_{i_g}^{v_g} = -\left(\frac{Z_{i_f}^{v_{pcc}} \cdot Z_c}{Z_{i_f}^{v_{pcc}} - Z_c} + Z_g\right) \tag{2.10}$$

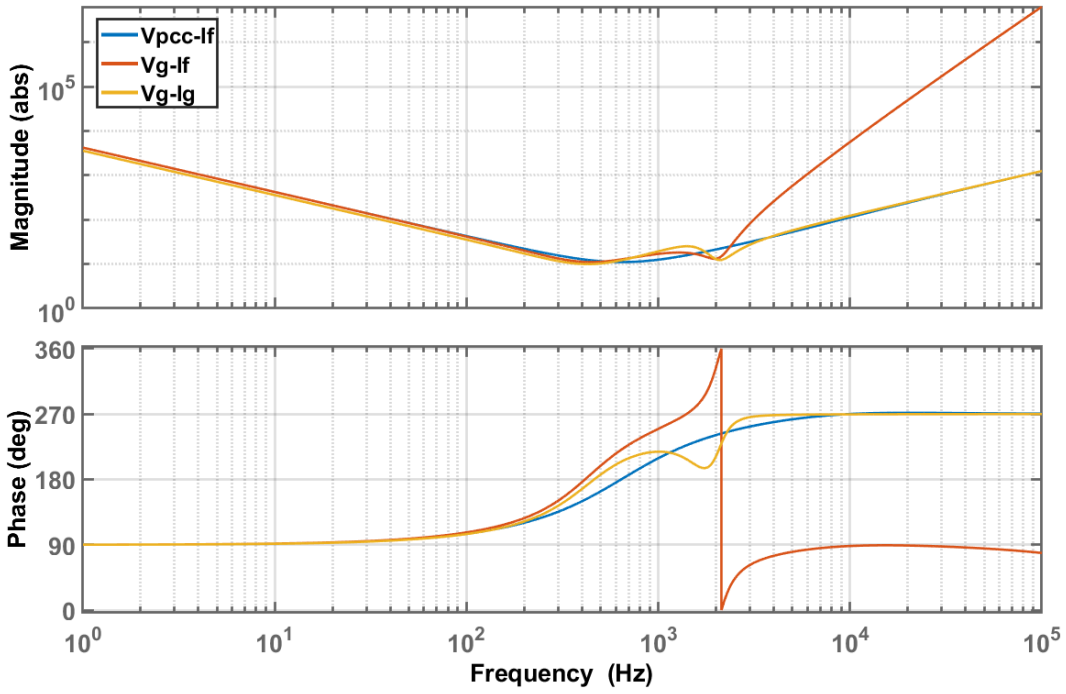

Figure 2.8. Comparison of the Dynamic Stiffness for different perturbations and outputs.

2.2 Double Converter

The second system analyzed in this work is the Double Converter Configuration, which consists in the parallel association of two converters, as shown in Figure 2.9. It validates the current control loop model and the analysis carried in Section 2.1.2 and supports the power control strategy that is proposed in Chapter 4.

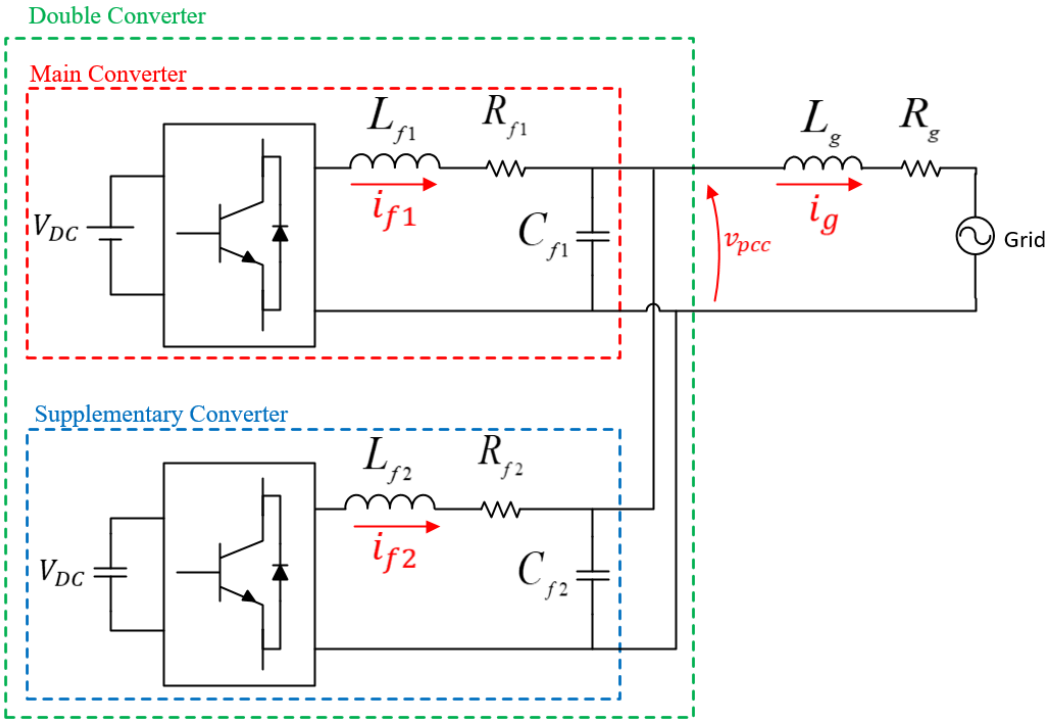

Figure 2.9. Main and supplementary inverters

The main unit is a conventional H-bridge inverter, based on power silicon semiconductors, usually IGBTs, and is responsible for injecting the most part, or the entirety, of the active power generated by the primary source into the grid. It has a relatively slow switching frequency, in the range of 10 kHz to 20 kHz, which is usually the operating range of commercially available grid-tied inverters. For this reason, its current control system has a low bandwidth and, therefore, is slow and cannot accurately control the flow of harmonic currents. Consequently, the main converter is incapable of providing ancillary services, does not comply with more recent interconnection and interoperability recommendation for DGs integration, such as the IEEE Std 1547 [9], and is susceptible to the circulation of disturbance currents if the grid voltage is distorted.

The supplementary converter also has a traditional H-bridge topology, however, its rated power is 25% to 50% of the main unit. It does not necessarily processes active power, but is responsible for the control of reactive power and harmonics. For this

reason, its DC bus does not necessarily needs a primary energy source and may be composed only by capacitors. In this case, however, a DC bus voltage control must be implemented to allow the capacitor charge from the grid side. Additionally, the current control of the supplementary converter must have a higher bandwidth and, therefore, demands a faster operating hardware. Thus, this converter must be based on state-of-the-art technology, such as silicon-carbide or other wide-bandgap semiconductors, as well as powerful digital signal processors, that enable a higher switching frequency, in the order of 100 kHz or more. Since it may not be responsible for injecting active power into the grid, it does not need an energy source and so its DC bus may be constructed using capacitors.

The main motivation for the use of such a configuration, especially in a scenario of ageing RES and increasingly stricter grid codes, is retrofitting old converters that may not be capable of following the growing requirements or comply with the standards for connection of a Distributed Energy Resource (DER) to the utility grid. This may be the case of an old inverter, represented by the main unit, which operates with unity power factor, injecting only active power into the grid. In this case, the update and modernization of the grid codes may render it obsolete, but, instead of replacing the old inverter, a supplemental converter could be connected in parallel to it and, as defined by the IEEE 1547-2018 standard [9], would be used to "*obtain compliance with some or all of the interconnection requirements*". For example, if the output current of the main inverter has a high THD caused by grid disturbances, the supplemental unit could be used to regulate the current that is injected into the grid, reducing its harmonic components to acceptable limits. Additionally, it could be used to regulate the PCC voltage by means of a Volt/VAr function. This is especially useful in situations where a high power converter is connected to a weak grid, causing its terminal voltage to rise when injecting power into the utility system, as is the case in large wind or solar farms installed in remote locations, that are often limited on how much power they can provide to the utility network. This feature could also be useful for small systems. In Brazilian rural areas, for example, the voltage may be supplied by the utility in a split-phase configuration (120/240 V), in which the phase voltage is higher than the usual three-phase systems (127/220 V). It is common for PV inverters installed in these areas to shutdown due to grid overvoltage. If such inverters were built using the Double Converter configuration, the supplemental unit could be used to regulate the PCC voltage magnitude, avoiding such problems.

Another application for the double converter configuration is the cost reduction in converter manufacturing. In traditional IGBT-based converters, the limited switching frequency of the hardware makes it difficult to develop an equipment that complies

with all grid codes and regulations. Therefore, it is necessary to use high-power wide-bandgap semiconductors, which are usually much more expensive and increase the final cost of the equipment. Alternatively, the Double Converter configuration may be used, in which the main unit is based in traditional IGBTs and provides the active power that is to be injected into the grid. The supplemental unit can then be constructed based in low-power wide-bandgap semiconductors with high switching frequency and be responsible for controlling the reactive power and harmonics and implementing the ancillary functions demanded by the grid operator. Therefore, the equipment cost can be reduced.

2.2.1 Current control loop

The current control loop of both the main and supplementary converters is identical to the one described in Section 2.1. However, the PWM modulation used in the Double converter simulations is different than the one used for the grid-connected converter. In this case, an uniformly sampled PWM with double update and triangular carrier is assumed. Therefore, the PWM model is as described in (2.11) [34, 37].

$$DPWM(s) = \frac{1}{2c_{pk}} \left(e^{-sDT_s} + e^{-s(1-D)T_s} \right) \tag{2.11}$$

The simplification of this expression is analogous to (2.3). Applying Euller's identity and assuming that the sampling period is close to zero and the duty cycle, D, is constant during one switching period, it gives:

$$DPWM(s) = \frac{1 + e^{-sT_s}}{2c_{pk}} \tag{2.12}$$

Applying the Padé approximation to this equation and taking the computational delay into account by increasing the sampling time by λT_s, the linear model shown in (2.13) is obtained.

$$DPWM(s) = \frac{1}{c_{pk}} \cdot \frac{1}{1 + s\frac{(1+\lambda)T_s}{2}} \tag{2.13}$$

2.2.2 Dynamic Stiffness (Output Impedance)

The output impedance of each converter regarding the PCC voltage is calculated using by applying the respective parameters into (2.8). Since the converters operate independently and the current controller of the supplementary unit is much faster

than the main one, the two converters are modelled as a parallel association of two impedances, as shown on Figure 2.10.

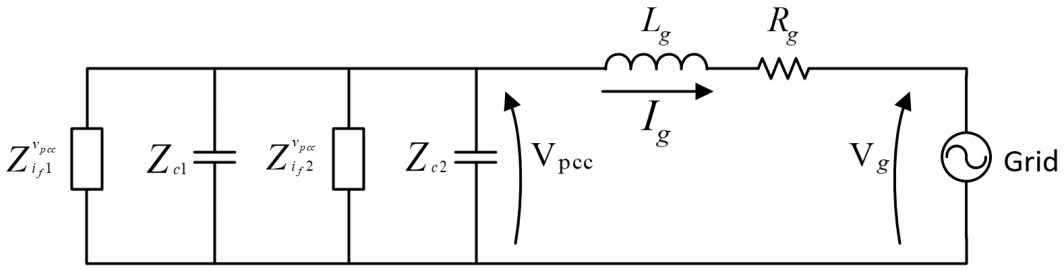

Figure 2.10. Equivalent circuit for calculation of the double converter output impedance.

This circuit may be simplified by considering the parallel association of the output impedance of each converter with its filter capacitor, similarly to (2.10). Once again, the negative sign on the denominator is due to the adopted current flow direction. The resulting circuit is shown on Figure 2.11.

$$Z_{out}^{1} = \frac{Z_{If1}^{v_{pcc}} \cdot Z_{c1}}{Z_{If1}^{v_{pcc}} - Z_{c1}} \qquad Z_{out}^{2} = \frac{Z_{If2}^{v_{pcc}} \cdot Z_{c2}}{Z_{If2}^{v_{pcc}} - Z_{c2}} \tag{2.14}$$

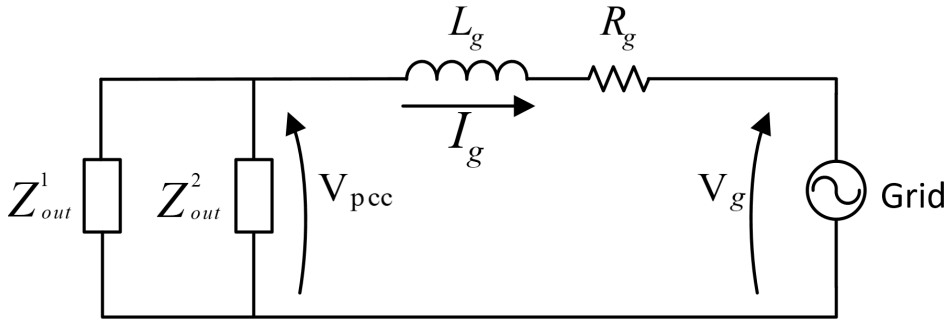

Figure 2.11. Simplified equivalent circuit for calculation of the dual converter output impedance.

Finally, the total impedance seen by the grid is calculated as shown in (2.15).

$$Z_{out}^{double} = -\left(Z_g + \frac{Z_{out}^{1} \cdot Z_{out}^{2}}{Z_{out}^{1} + Z_{out}^{2}}\right) \tag{2.15}$$

The bode plot of the expressions (2.14) and (2.15) is shown in Figure 2.12, from which a few observations can be made. First, it is evident that the output impedance of the supplementary converter is higher than that of the main one. This is due to the higher switching frequency and wider bandwidth of the current controller. Second, it

can be noted that the total output impedance, as seen from the grid, is smaller than the impedance for both converters. This is to be expected, since this is the result of a parallel association. The only region where this is not true is around 8kHz, near the resonance frequency of the main converter, where the grid impedance prevents the total impedance of being too small.

This result apparently suggests that the insertion of a secondary converter actually deteriorates the performance of the system from a grid perspective, since it degrades the total output impedance. However, this is true only if the supplemental converter implements only its inner current control loop. As it is shown on Section 4.2, when the supplementary converter is used to control the power flow to and from the grid, the output impedance is increased at the frequencies of interest, improving the system performance.

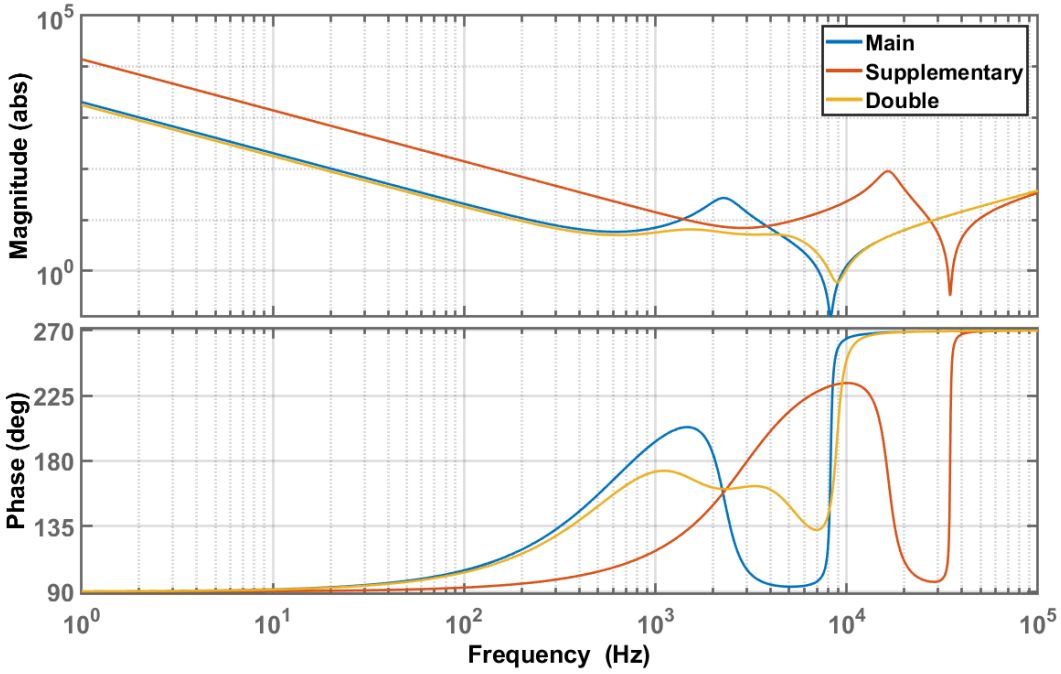

Figure 2.12. Output impedance for the main and supplemental converters and their association.

2.3 Conclusions

This chapter presented the circuit, configuration and functionalities of the converters studied herein and analytical models were developed for the components of the current control loop. The Dynamic Stiffness, a figure of merit used to quantify the system robustness to external disturbances, was introduced and it was shown that, in the case of the grid-tied inverter, it corresponds to its Output Impedance, although it may have other physical meaning when other systems are analyzed. Two different ways of calculating this quantity, regarding the PCC and grid voltages, were studied and it was shown that, although the relation between the PCC voltage and the filter current ($Z_{i_f}^{v_{pcc}}$) is simpler to calculate, it cannot model the resonance between the output filter and the grid. However, the calculation of the output impedance regarding the grid voltage ($Z_{i_f}^{v_g}$) is difficult to accurately determine, as it is dependent of the grid impedance value.

Concerning the double converter, the derived model showed that the supplementary unit has greater resiliency to external disturbances when compared to the main unit. That is expected, since the supplementary has higher switching and sampling frequencies, that allow the implementation of faster control loops. However, it was shown that the simple parallel association of these two converters actually reduce the system Output Impedance as seen from the grid, as is expected from the parallel association of two impedances. Section 4.2 will elaborate on how the supplementary unit can be used to actually improve the performance of the main unit.

It is worth remarking that, during the development of this work, it was noted that the incorrect modelling of the PWM and computational delays severely compromises the model accuracy, the calculation of output impedance and impacts the system performance. Even a difference of a few sampling periods regarding the delay can significantly alter the expected results and, therefore, the correct determination of this model is paramount to the calculation of the correct open-loop current control transfer function and tuning of the controllers.

Chapter 3

Parameter Sizing and System Design

3.1 Grid Model

In this work, the grid is modelled as a Thèvenin equivalent, in which an ideal AC voltage source is in series with an RL impedance branch. The equivalent capacitance is disregarded because, in low-voltage distribution networks, where most distributed generators are connected to, this component is normally negligible. Instead, these networks are characterized by significant resistive and inductive components, with a low X/R ratio [39, 40, 41].

For the grid-connected converter studied herein, the grid impedance is negligible when compared to the coupling transformer impedance, whose determination is shown in Section 5.4.1. For this reason, in the simulations of the grid-connected inverter, the actual grid impedance is disregarded and only the transformer impedance is used. However, in the simulations of the Double converter, the grid resistance and inductance are considered equal to the ones shown in (3.1). Assuming that the Double converter is connected to a 220 Vrms/60 Hz grid, these values result in an X/R ratio of 0.189 and corresponds to a short-circuit power of approximately 400 kVA, as shown in (3.2), characterizing a strong grid.

$$R_g = 120\ m\Omega \qquad L_g = 60\ \mu H \tag{3.1}$$

$$S_{sc} = \frac{V_{\phi\phi}^2}{|Z_g|} = \frac{220^2}{\sqrt{0.12^2 + (2\pi \cdot 60 \cdot 60 \cdot 10^{-6})^2}} = 396.35\ kVA \tag{3.2}$$

3.2 Grid-Connected Converter

3.2.1 Output Filter Sizing

The output filter is an essential part of an inverter system. It is responsible for eliminating the switching ripple from the output current and reducing its harmonic content to adequate levels. It must also have an inductive characteristic to guarantee proper operation of the VSI when connected to the utility grid [35] and may consist on a single inductor or be based on an LC or LCL circuit, depending on the switching frequency, inverter power and other application characteristics.

The sizing of the filter components is a task that must be carefully executed, since there is a trade-off between its ability to block the switching harmonics and its physical size and weight. Large filters block current harmonics more effectively but end up being too heavy and bulky, making them expensive and unfeasible to use in practical applications. High values of inductors and capacitors also interfere with the current control loop bandwidth because they reduce the filter resonance frequency (f_{res}) and limit the range in which the controller can effectively regulate the output. The controller bandwidth must be limited to a value lower than f_{res} to keep its actuation in a region where the filter does not attenuate the output signal. In this work, the filter circuit used on all analysis and simulations of the Grid-Connected Converter is based on the commercial inverter used on the experimental setup, that uses an LC circuit, and, therefore, its parameters were already predetermined and were not designed as part of this work. The inductance values are provided by the manufacturer and confirmed by means of a simple test in which an inductor is connected to a current source with known value and its terminal voltage is measured. The values of the grid-connected converter filter components are shown on Table 3.1.

Table 3.1. Grid-connected inverter output filter parameters

Parameter	Symbol	Value
Inductor	$L_{f1} \mid L_{f2}$	1 mH
Inductor ESR	$R_{f1} \mid R_{f2}$	0.1 Ω
Capacitor	C_f	6.6 μF

3.2.2 Controller Tuning

The modelling of the current control loop components is shown in Section 2.1.1. From that, it is possible to calculate the open-loop transfer function of the system and tune the controller. The tuning strategy varies depending on the type of controller chosen. Herein, due to its simplicity, a PI controller is used. Despite its disadvantages and limitations, as discussed in Chapter 1, it is shown in Chapter 4 that they do not impact the system performance when the proposed control strategy is implemented.

The first step to tune the current controller is determining the output filter resonance frequency. For an LC filter, this calculation is straightforward, as shown by the expression on (3.3).

$$f_{res} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{3.3}$$

As discussed on Section 3.2.1, the parameters used for the grid-connected inverter are based on the commercial inverter used on the experimental setup. Thus, it is necessary to estimate its resonance to determine the maximum controller bandwidth. From the parameters shown on Table 3.1:

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{2mH \cdot 6.6\mu F}}$$

$$f_{res} = 1385Hz \tag{3.4}$$

The bandwidth of the control system is limited by the resonance frequency, since the filter attenuates signals at higher frequencies, limiting the actuation capability of the controller. Thus, the crossover frequency chosen to design the current controller is 1 kHz. There is also a resonance between the filter capacitor and grid inductance, but since the grid inductance is usually unknown, this parameter is not used to tune the controller. Regardless, as the grid inductance is usually much smaller than the one of the output filter, this resonance happens on a higher frequency and does not affect the controller tuning.

Another important parameter to be determined previously to the controller tuning is the *Phase Margin*. It is a measurement of the relative stability of a system and represents the maximum phase delay that can be added to it without causing instability. Consequently, the greater its value, the more stable the system, if a constant gain is assumed [42]. It is also related to the disturbance rejection capability. The lower its value, the lesser the impact of disturbances in the system output. Hence, there is a trade-off between stability and immunity to disturbances. A system designed to have

the best possible transient response will have its output strongly affected by disturbances. Similarly, if the controller is designed to reject all external interference, the system will normally be unstable or have highly oscillating transient response. Thus, the controller design must be iterated until a good compromise is achieved between these two constraints. Herein, the chosen value for the phase margin is 60 degrees. The use of this value is suggested by [43] to guarantee the system stability even if its parameter values vary within a certain range. Having chosen the current controller bandwidth and phase margin, its gains can be calculated. To do this, it is necessary to first obtain the open-loop transfer function of the current loop. From the previous sections, the current loop open-loop TF can be expressed as:

$$G_{OL}^{i}(s) = \frac{DPWM \cdot G_{conv}}{Z_f \cdot H_i}$$

$$G_{OL}^{i}(s) = \frac{1}{c_{pk}} \cdot \frac{2V_{DC}}{(s \cdot L_f + R_f) \cdot H_i} \cdot \frac{1 - s\frac{3T_s}{4}}{1 + s\frac{3T_s}{4}} \tag{3.5}$$

To tune the controller, the method described in [34] is used. The open-loop TF of the current loop, considering the PI controller, is expressed by (3.6).

$$G_{OL}^{i}(s) = \left(\frac{K_{pi} \cdot s + K_{ii}}{s}\right) \cdot \frac{1}{c_{pk}} \cdot \frac{2V_{DC}}{(s \cdot L_f + R_f) \cdot H_i} \cdot \frac{1 - s\frac{3T_s}{4}}{1 + s\frac{3T_s}{4}} \tag{3.6}$$

From this equation, K_{pi} and K_{ii} are determined by imposing the magnitude of the transfer function to be equal to 1 at the crossover frequency and its phase to be equal to the chosen phase margin. Solving the resulting system of equations yields the values shown in (3.7). This result was obtained by considering $c_{pk} = 1$, $V_{DC} = 311V$ and $H_i = 20$. The filter parameters are as shown on Table 3.1.

$$K_{pi} = 0.80 \qquad K_{ii} = 767.65 \tag{3.7}$$

Figure 3.1 compares the Bode Diagram of the open-loop system without and with the controller. It can be seen that the crossover frequency is close to the desired value even before the controller is added, but the phase margin is not. From this figure, it is also clear that the PI increases the DC gain and adjusts the crossover frequency and phase margin to the desired values. Finally, Figure 3.2 shows the dynamics of the closed-loop current control. In this case, its behaviour is reasonably approximated by a DC gain for frequencies to 100 Hz, but for higher frequencies it inserts an amplitude and phase difference in the system.

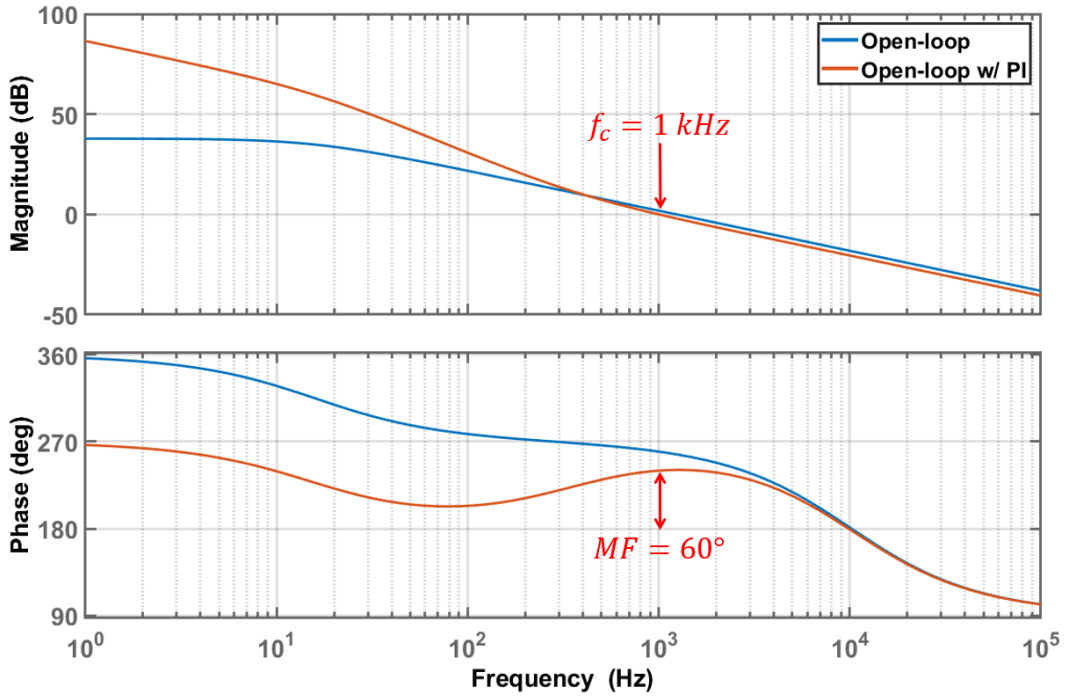

Figure 3.1. Open-loop current control transfer function, $G^i_{OL}(s)$.

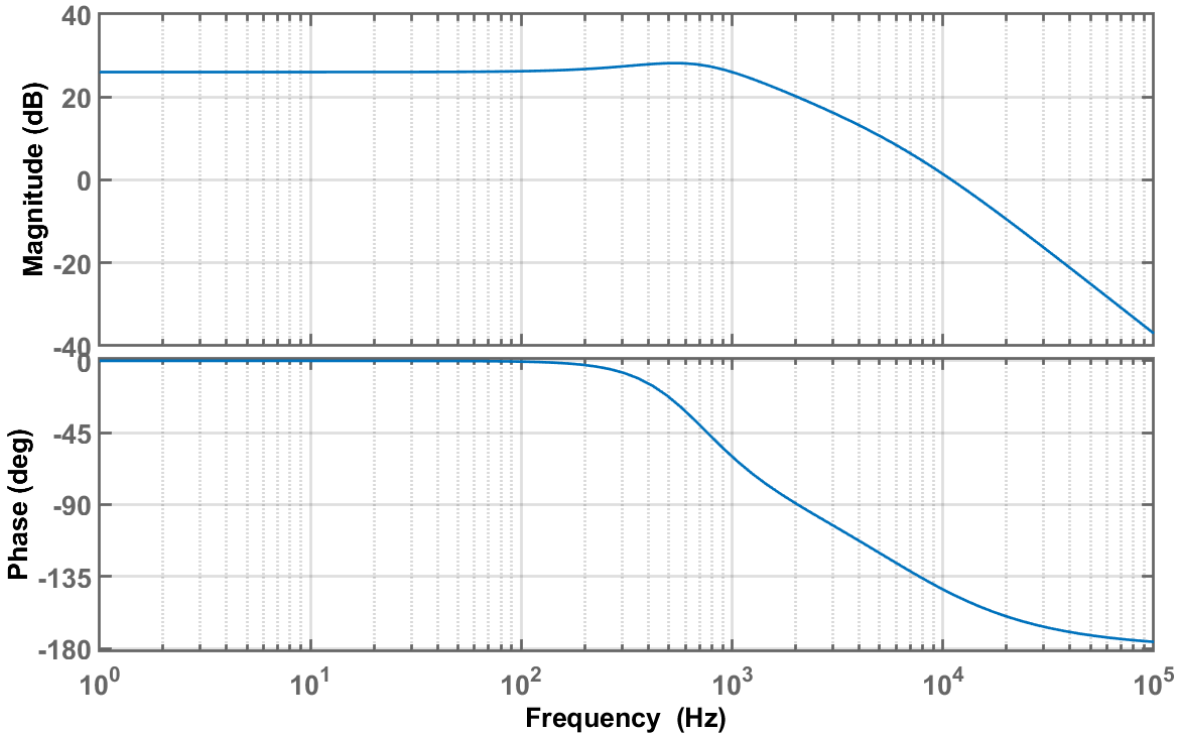

Figure 3.2. Closed-loop transfer function of the current control loop, $G^i_{CL}(s)$.

To evaluate the performance of the system after tuning the controller, two metrics are analyzed: the transient response and the disturbance rejection capability. Regarding the transient, for a grid-connected inverter, the main concern is to avoid high current overshoot, since it may damage its components. Additionally, the settling time must be as low as possible to not compromise the operation of the outer power control loop. These two quantities are related, being a higher overshoot and a lower settling time achieved by reducing the phase margin. Figure 3.3 shows the step response of the system for the chosen crossover frequency and phase margin. For this configuration, an overshoot of 20% and a settling time of about 1.3 ms were obtained.

Finally, the response of the system when subject to disturbances is analyzed by its Dynamic Stiffness, as discussed in Section 2.1.2, by applying (2.8), (2.9) and (2.10). For example, by evaluating $Z_{if}^{v_{pcc}}$ at the fundamental frequency (60 Hz), it is determined that the output impedance for this system when using the calculated controller values is about 70 Ω. This means that a 1.8 A_{rms} current (127 V_{rms}/70 Ω) will flow through the output filter when the system is connected to the grid and the current reference is kept at zero. This value is higher than desired, but due to the limitations of the PI controller, it cannot be reduced further without increasing the overshoot, deteriorating the transient response.

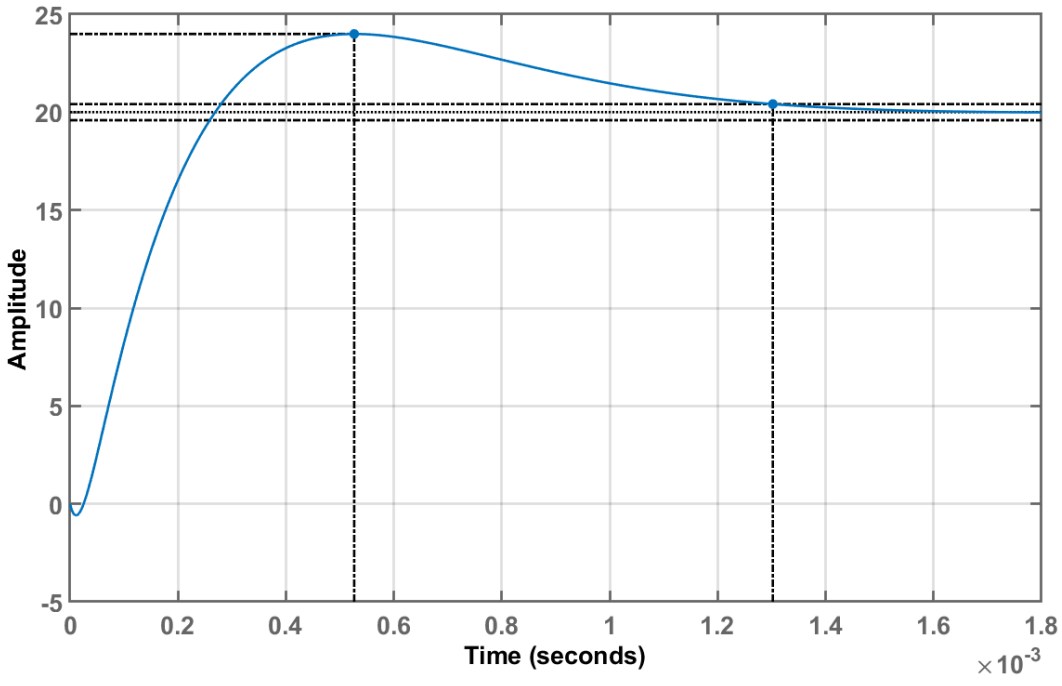

Figure 3.3. Closed loop current control step response.

3.3 Double Converter

The Double Converter Configuration is setup as shown on Figure 2.9. As this section aims to analyze only the current control, it is assumed that both the main converter and supplementary converters do not have any sort of power regulation, being their control system responsible exclusively for regulating its output filter current, with no direct influence on the grid current. Therefore, the two converters operate independently from each other.

3.3.1 Main Converter Output Filter Sizing

Differently from the grid-connected inverter, for the double converter there is not a commercial equipment from which to get the filter parameters. Thus, this section describes the procedure for determining them based on the main electrical characteristics of both converters. For the main converter, these parameters are shown on Table 3.2.

Table 3.2. Main inverter electrical parameters

Parameter	Value
Maximum power	5kVA
Nominal voltage	220V
Output current	22.7A
Switching Frequency	12kHz

From these parameters, it is possible to derive the maximum output current of the main inverter. It is also a good practice to establish a security coefficient to avoid that the output current ever exceeds the maximum allowed value, even during transient conditions. Assuming a security coefficient (K_{sec}) equal to 25%, it gives:

$$I_{max} = \frac{S_{max} \cdot K_{sec}}{V_{nom}}$$

$$I_{max} = \frac{5000VA \cdot 1.25}{220V}$$

$$I_{max} = 28.41A_{RMS} \tag{3.8}$$

Thus, the maximum peak output current is:

$$I_{max}^{pk} = 40.18A_{pk} \tag{3.9}$$

To size the output filter inductor, it is necessary first to establish the maximum allowed ripple, ΔI_{max}. Considering it as 10% of the maximum current, the output

filter inductance may be calculated as shown in (3.10) [44], where V_{dc} is the DC-link voltage, f_{sw} is the inverter switching frequency. $\overline{I}_{max}$ is the maximum parameterized current ripple and, for three-level modulation, it is equal to 0.25.

$$L = \frac{\overline{I}_{max} \cdot V_{dc}}{2 \cdot f_{sw} \cdot \Delta I_{max}}$$

$$L = \frac{0.25 \cdot 400}{2 \cdot 12000 \cdot 4}$$

$$L = 1mH \tag{3.10}$$

As a rule of thumb, the output filter resonance frequency is determined as being equal to one sixth of the switching frequency, since the current loop crossover frequency is at least one decade below f_{res} [34]. Thus:

$$f_{res} = \frac{f_{sw}}{6} = 2kHz \tag{3.11}$$

From (3.10) and (3.11), the filter capacitor is determined:

$$C = \frac{1}{(2\pi \cdot f_{res})^2 \cdot L}$$

$$C = \frac{1}{(2\pi \cdot 2000)^2 \cdot 0.001}$$

$$C = 6.3\mu F \tag{3.12}$$

The value obtained for the filter capacitor in (3.12) is not a standardized commercial value. Thus, the closest one available may be selected in order to keep the resonance frequency as close to the desired value as possible. This can be achieved by using two $3.3\mu F$ capacitors in parallel, to obtain $C = 6.6\mu F$, yielding an output filter resonance frequency of:

$$f_{res} = 1959Hz \tag{3.13}$$

3.3.2 Supplementary Converter Output Filter Sizing

The procedure for sizing the supplementary converter output filter is identical to the one presented for the main converter. However, as shown on Table 3.3, for this converter, the switching frequency is significantly higher and the rated output power is lower. Consequently, the passive components of the filter are largely reduced, as

shown in the following equations. The values of maximum ripple current and security coefficient used are the same as in the previous section.

Table 3.3. Supplementary inverter electrical parameters

Parameter	Value
Maximum power	2.5kVA
Nominal voltage	220V
Output current	11.4A
Switching Frequency	96kHz

$$I_{max}^{pk} = \frac{2500 \cdot 1.25 \cdot \sqrt{2}}{220}$$

$$I_{max}^{pk} = 20.1A_{pk} \tag{3.14}$$

$$L = \frac{0.25 \cdot 400}{2 \cdot 96000 \cdot 2}$$

$$L = 250\mu H = 0.25mH \tag{3.15}$$

Again, the resonance frequency is designed as being one sixth of the switching frequency. Thus:

$$f_{res} = \frac{f_{sw}}{6} = \frac{96kHz}{6} = 16kHz \tag{3.16}$$

Then, the filter capacitor may be determined as:

$$C = \frac{1}{(2\pi \cdot 16000)^2 \cdot 0.25 \cdot 10^{-3}}$$

$$C = 400nF = 0.4\mu F \tag{3.17}$$

Once more, the obtained value for the filter capacitor is not standardized. To approximate the desired value, the use of two capacitors in parallel, each with a capacitance of $0.22\mu F$, was assumed. Thus, the final resonance frequency of the output filter is:

$$f_{res} = 15174Hz \tag{3.18}$$

3.3.3 Controller Tuning

The model of the current control loop for the supplementary converter is the same as for the main converter, shown in Figure 2.2. Therefore, the current controller for both converters is tuned following the procedure described in Section 3.2.2. For the main inverter, the resonance frequency of the filter is approximately 2 kHz and, thus, the chosen crossover frequency was 1 kHz. The phase margin is again chosen as 60 degrees. Therefore, the controller gains for the main converter are:

$$K_{pi}^{main} = 0.61 \qquad K_{ii}^{main} = 1392.0 \tag{3.19}$$

Since the switching and resonance frequency of the supplementary converter are much higher than those of the main unit, the current controller may have a larger bandwidth. Thus, its crossover frequency is chosen as 5 kHz and the phase margin as 60 degrees. Therefore, the gains for the supplemental converter are:

$$K_{pi}^{sup} = 0.37 \qquad K_{ii}^{sup} = 4569.2 \tag{3.20}$$

Figure 3.4 shows the dynamics of the closed-loop current control of both converters. It is clear that the main converter has a narrower bandwidth, as expected, and higher DC gain, due to its higher rated power. Figure 3.5 shows the transient response of the current control loop of both converters. As expected, the control of the supplemental converter is much faster, achieving a settling time of 0.25 ms, while the main converter control needs 1.3 ms to achieve the steady-state. The overshoot is also within acceptable values for both converters, being equal to 17.0% for the main converter and 24.2% for the supplemental. Thus, the transient behaviour of both control loops is adequate and, following the procedure described in Section 3.2.2, the disturbance rejection capability must now be determined to validate the controller tuning results. The value of $Z_{i_f}^{v_{pcc}}$ can be calculated for both the main and supplementary converters by evaluating (2.8) at the fundamental frequency, yielding values of about 30 Ω and 230 Ω, respectively. This shows that, as expected, the supplementary converter is more effective in rejecting disturbances and, therefore, a lower current will flow through its filter when connected to the grid, if compared to the main unit.

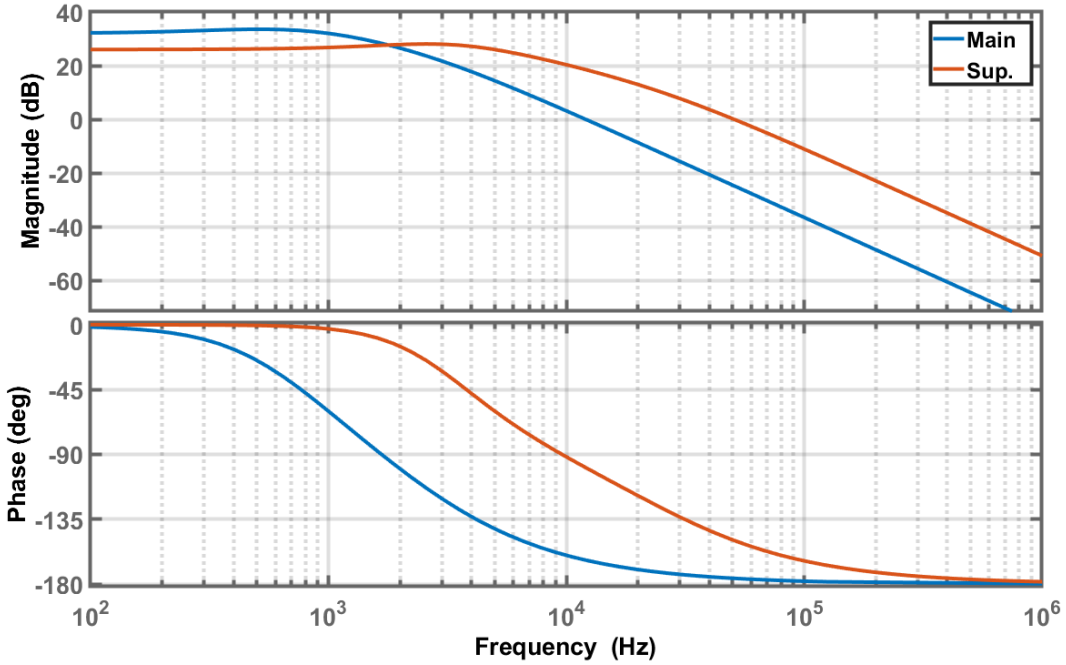

Figure 3.4. Closed-Loop current control dynamics for the main and supplementary converters.

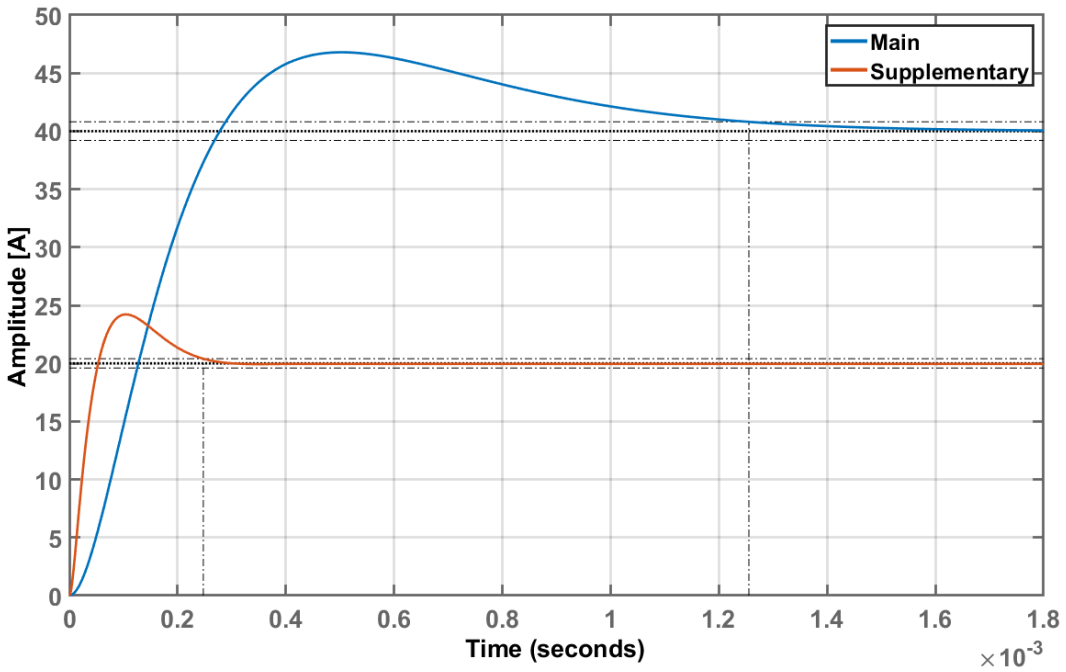

Figure 3.5. Step response of the main and supplemental converters current control.

3.4 Conclusions

This section presented a more detailed description of the parameters that were used in the simulations and experiments developed for this work. The design procedure for sizing the output filter of a current-driven converter was shown.

The PI controllers that regulate the current loop were also tuned for both the grid-connected and Double converters. By using the model derived in Chapter 2 and traditional controller tuning techniques, the K_i and K_p gains were determined and the resulting dynamics of the closed-loop control were analyzed. It was shown that there is a trade-off between the disturbance rejection capability, which is measured by the Dynamic Stiffness, and transient response, quantified in the sense of settling time and overshoot. Therefore, the controller tuning must be carefully carried out to assure that the system is not susceptible to external disturbances nor has a transient response with excessive overshoot or oscillatory behaviour that may damage the most sensitive system components.

Chapter 4

Selective Output Impedance-Based Control

4.1 Grid-Connected Converter

Chapter 2 shows that the use of certain types of controllers may render the system susceptible to disturbances coming from the grid voltage due to its low resulting output impedance, which justifies the use of high gain controllers usually found in the literature, such as the PI-Resonant or Dead-beat, in the current control loop.

This section aims to demonstrate that there is no need to use more complex controllers because, despite its disadvantages, a simple PI may suffice as output current regulator as long as an outer control loop is used to generate an adequate reference, compensating the circulation of unwanted currents terms and improving the disturbance rejection capability of the system. The control strategy proposed herein uses exclusively PI controllers, which make it very robust, simple and easy to implement.

4.1.1 Analytical Disturbance Compensation

The derivation of the output impedance, shown in Figure 2.8, suggests that it may be possible to analytically calculate the magnitude and phase of the disturbance currents. This section demonstrates that this can, in fact, be done and that, by knowing the exact external disturbance the output is subject to, either by measurement or estimation, it can be completely eliminated by using the opposite signal as reference to the current loop. This analysis helps to further understand the behaviour of the current control and introduces the basic operation of the proposed power control loop, which is presented in Section 4.1.2.1

If the value of Z_{out} at the frequency of interest is previously determined, the disturbance current is obtained by measuring the PCC voltage and applying Ohm's law, as shown in (4.1). However, to completely eliminate the perturbation, the reference signal must also account for the dynamics of the closed-loop current control (G^i_{CL}). As can be seen in Figure 3.2, at low frequencies the closed-loop current control can be approximated as an static gain, but at higher frequencies, because of the limitations of the PI controller, there is an attenuation and phase deviation on the system. Thus, the output current significantly differs from the input and, because of that, the reference must be compensated to obtain the desired result. The calculation of the reference signal that should be input to the current control loop to ensure that the output current is free of disturbances is shown in (4.2).

$$I_h(jh\omega_0) = \frac{V_{pcc}(jh\omega_0)}{Z_{out}(jh\omega_0)} \tag{4.1}$$

$$I^*_h(jh\omega_0) = -\frac{V_{pcc}(jh\omega_0)}{G^i_{CL}(jh\omega_0) \cdot Z_{out}(jh\omega_0)} \tag{4.2}$$

Figure 4.1 shows the simulation results for the output filter current (I_f) of a current controlled grid-tied inverter connected to a point with heavily distorted voltage, with 10% of both 3rd and 5th harmonic components. The upper graph shows the current when a reference equal to zero is applied to the input of the current control loop, while the bottom one shows the current for the same grid condition, but using a reference calculated according to (4.2). It shows that the disturbance is completely eliminated, as expected. Another example of the open-loop compensation is illustrated in Figure 4.2, that shows the current reference signal calculated accordingly to (4.2) for a 60 Hz purely sinusoidal grid voltage and fed to the current loop in order to achieve zero current flow through the output filter. It is clear that it yielded a good result, since the filter inductor current is completely free of any disturbances.

The results shown in Figures 4.1 and 4.2 are similar to the obtained when a zero reference is applied to a current control loop implemented with resonant or dead-beat controllers and demonstrate that it is theoretically possible to calculate the exact reference that must be passed to the current control loop to eliminate the disturbances. Therefore, it is possible to devise an external control loop that would be responsible for continuously calculating the current reference, assuring zero disturbance in the output. In the ideal case, its output would be exactly equal to the signal given by (4.2).

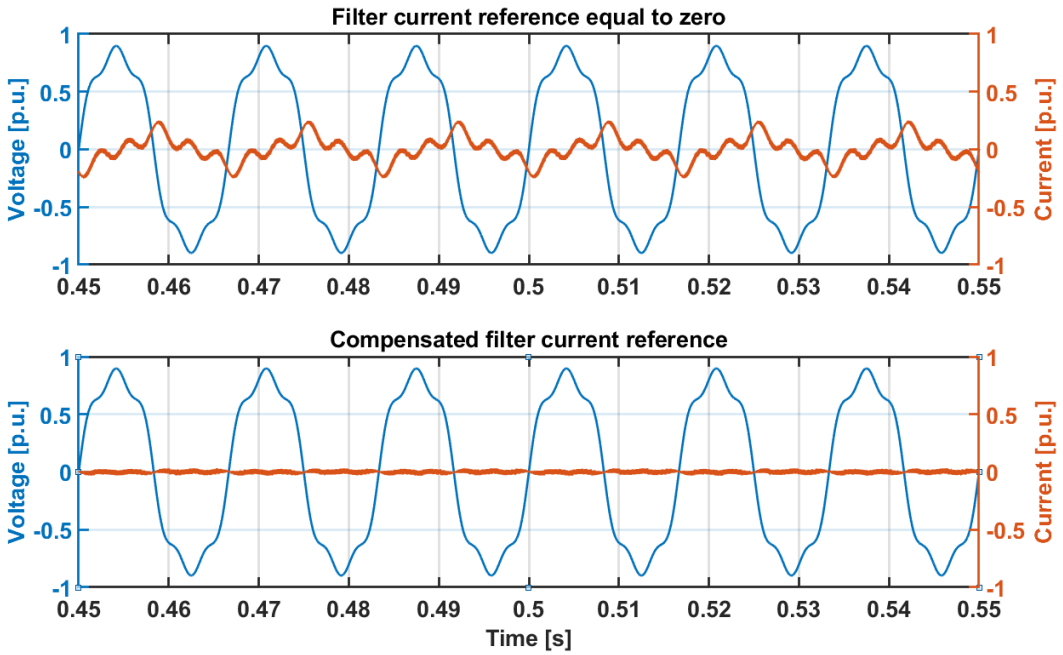

Figure 4.1. Comparison of zero reference and open-loop compensation for the filter current (i_f) control.

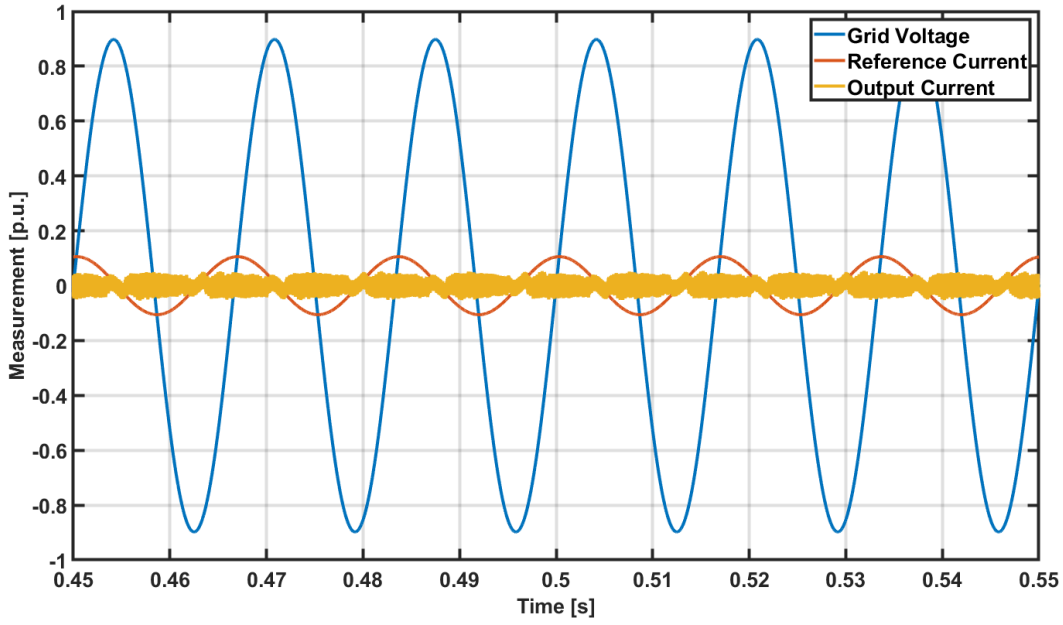

Figure 4.2. Reference current for zero output filter current (i_f).

4.1.2 Power and Harmonics Control

4.1.2.1 Proposed Strategy

As discussed in the last section, the disturbances present on the output current can be compensated by manipulating the current reference. In this section, an external control loop that calculates the correct input to eliminate the perturbations in real-time is proposed. Its configuration is shown on Figure 4.4, where $G_i(s)$ represents the closed-loop current control, whose transfer function and dynamics are represented in (3.6) and Figure 3.2. It is composed of a pair of PI controllers, $C_p(s)$ and $C_q(s)$, which are responsible for regulating the flow of active (P) and reactive (Q) power. The output of each controller is then multiplied by purely sinusoidal signals with frequency equal to the grid voltage fundamental component, x_1 and $\hat{x}_1$, being the first in-phase with the grid voltage and the second phase-shifted by $-90°$. In this work, these signals have unity amplitude and are generated by a Phase-Locked Loop (PLL), normally used in grid-connected converters to synchronize the system with the grid voltage, but for the control of active and reactive power, the measured grid voltage may also be used to implement these signals. In this case, however, the open-loop gain of the system changes, since the grid voltage does not reach 1 p.u. The resulting signals, i_a^* and i_r^*, are then added. Therefore, by controlling the amplitude of these signals, the first pair of PI regulators actively controls the magnitude and phase of the output current fundamental component.

The calculation of active and reactive power is done accordingly to the Conservative Power Theory (CPT) [45, 46], as shown in (4.3), where $\widehat{v}_{pcc}$ is the integral of the PCC voltage without its average value, named voltage homo-integral, calculated as shown in (4.4).

$$P = \frac{1}{T}\int_T v_{pcc} \cdot i_f \; dt \qquad\qquad Q = \frac{1}{T}\int_T \widehat{v}_{pcc} \cdot i_f \; dt \tag{4.3}$$

$$\widehat{v}_{pcc} = \omega \int_0^t v_{pcc} \; d\tau \; - \; \frac{\omega}{T}\int_T \left[\int_0^t v_{pcc} \; d\tau\right] dt \tag{4.4}$$

This strategy may be replicated as many times as needed, according to the application requirements or the number of harmonic components present on the grid voltage, by adding N other controller pairs, being each one responsible for regulating one harmonic frequency. For higher frequencies, x_h and $\hat{x}_h$ are obtained by multiplying the output angle of the PLL by an integer representing the harmonic order and subsequently obtaining its sine or cosine. The harmonic distortion quantities associated to each component, $D_{h\parallel}$ and $D_{h\perp}$, are calculated for each individual frequency and

quantified for the in-phase and quadrature components as shown in (4.5), where $I_{h\parallel}^{pk}$ and $I_{h\perp}^{pk}$ are the peak values of the in-phase and quadrature components of the output filter current.

$$D_{h\parallel} = V_{RMS} \cdot \frac{I_{h\parallel}^{pk}}{\sqrt{2}} \qquad D_{h\perp} = V_{RMS} \cdot \frac{I_{h\perp}^{pk}}{\sqrt{2}} \tag{4.5}$$

Figure 4.3 shows the logic used to calculate all reference and sinusoidal signals, where v_{pcc} and i_f are the measured PCC voltage and filter current. The output signals shown in this figure are then fed to the adequate point on the power control loop, as shown on Figure 4.4.

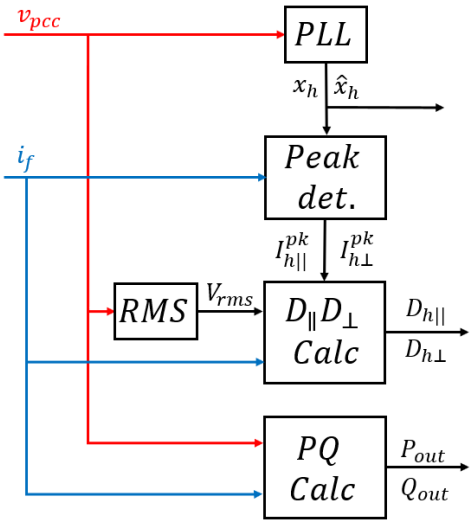

Figure 4.3. Signal generation algorithm.

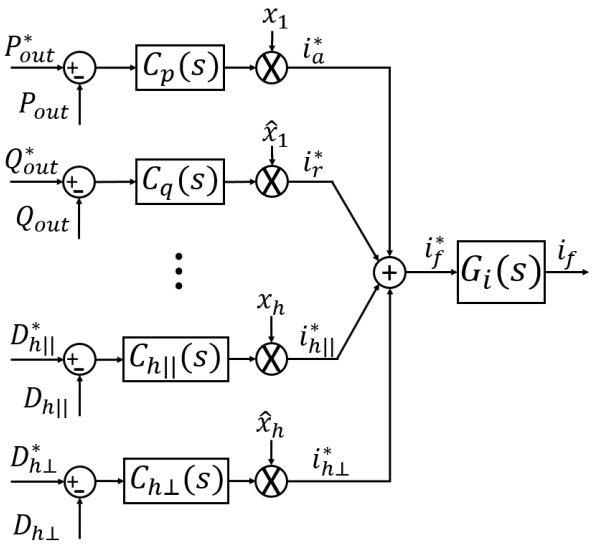

Figure 4.4. Proposed control strategy.

The resulting current reference signal, i_f^*, has the characteristics discussed in Section 4.1.1, being equal to the opposite of the perturbation signal, compensated by the current loop dynamics. To demonstrate this, a simulation is conducted in Simulink in which the analytical reference calculated by means of (4.2) is compared with the current reference generated by the power control loop, with all references set to zero. In this simulation, all parameters are equal to the nominal values used to analytically calculate the current reference signal. The obtained results are shown in Figure 4.5. The box on this figure details the zoom-in-view around 0.5 s. It is seen that both signals are almost identical. Since the values of all parameters are known, the analytical derivation is very accurate. Small deviations are observed and may occur due to computational rounding errors and model inaccuracies. Nevertheless,

their magnitude is so small that they can be considered negligible and, thus, this figure confirms that the power control loop behaves as expected.

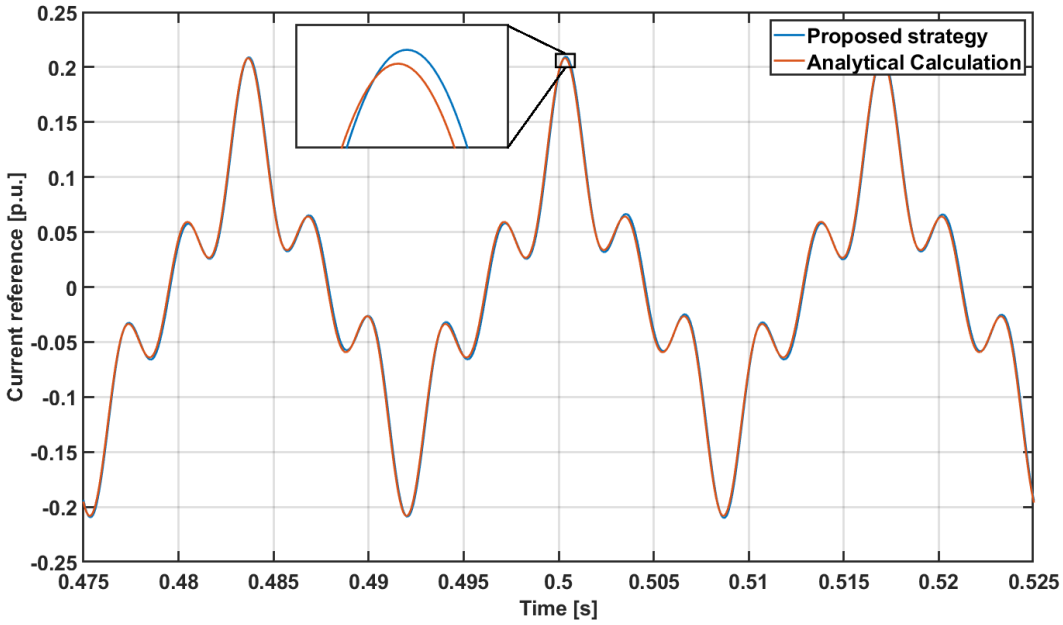

Figure 4.5. Current references generated by the proposed strategy and analytical calculation.

Finally, since only the filter inductor current (i_f) is controlled, reactive power is exchanged between the grid and the filter capacitor and, therefore, a small grid current (i_g) circulates even when the filter current is equal to zero. This can be avoided by previously estimating the capacitor reactance and inserting an offset value in the reactive power control loop reference (Q^*_{out}). In this case, there will be a small reactive flow through the filter inductor, but the grid current will be equal to zero.

4.1.2.2 Current Peak Detection

As shown on the last section, the calculation of the harmonic distortion quantities ($D_{h\parallel}$ and $D_{h\perp}$) depends on the determination of the in-phase and quadrature peak values of the output current. In this work, an algorithm based on the application of a Fourier transform to a single frequency is used to obtain such values. This section describes its operation in detail.

At first, assume that the filter current is composed of a single harmonic frequency, $h\omega$, and has a phase shift of ϕ_h degrees:

$$i_{fh} = I_h^{pk} \sin(h\omega t + \phi_h) \tag{4.6}$$

This waveform can be decomposed into an in-phase and a quadrature components, as shown in (4.7).

$$i_{fh} = I_h^{pk}\big[\sin(h\omega t)\cos(\phi_h) + \cos(h\omega t)\sin(\phi_h)\big]$$

$$i_{fh} = I_h^{pk}\cos(\phi_h)\sin(h\omega t) + I_h^{pk}\sin(\phi_h)\cos(h\omega t)$$

$$i_{fh} = I_{h\parallel}^{pk}\sin(h\omega t) + I_{h\perp}^{pk}\cos(h\omega t) \tag{4.7}$$

If this waveform is multiplied by the in-phase unit signal x_h, it results in (4.8). The average value of this equation is equal to half the peak value of the output current in-phase component.

$$i_{fh}\cdot x_h = I_{h\parallel}^{pk}\sin^2(h\omega t) + I_{h\perp}^{pk}\cos(h\omega t)\sin(h\omega t)$$

$$i_{fh}\cdot x_h = \frac{I_{h\parallel}^{pk}}{2}\big(1-\cos(2h\omega t)\big) + \frac{I_{h\perp}^{pk}}{2}\sin(2h\omega t) \tag{4.8}$$

A similar derivation is done for the multiplication by $\hat{x}_h$. In this case, the average value of the multiplication is half of the peak value of the quadrature component.

$$i_{fh}\cdot \hat{x}_h = I_{h\parallel}^{pk}\sin(h\omega t)\cos(h\omega t) + I_{h\perp}^{pk}\cos^2(h\omega t)$$

$$i_{fh}\cdot \hat{x}_h = \frac{I_{h\parallel}^{pk}}{2}\sin(2h\omega t) + \frac{I_{h\perp}^{pk}}{2}\big(1+\cos(2h\omega t)\big) \tag{4.9}$$

Therefore, the peak values of the in-phase and quadrature components of the output filter current are obtained as shown on Figure 4.6, where LPF is a low-pass filter with cutoff frequency of 15 Hz used to extract the average value of the signals shown in (4.8) and (4.9). Note that the input current is multiplied by two so that the output of the algorithm is exactly the desired peak values.

Even though this analysis was done considering a single harmonic, it is still valid if the filter current is composed of N different frequencies. This is because signals with different frequencies are orthogonal and, thus, the average value of their multiplication is always zero. Thus, the final result is the same:

$$\frac{1}{T}\int_0^T i_f\cdot x_h\,dt = \frac{1}{T}\int_0^T \left[sin(h\omega t)\sum_{k=1}^{N} I_h^{pk} sin(k\omega t+\phi_k)\right] dt$$

$$\frac{1}{T}\int_0^T i_f\cdot x_h\,dt = \frac{I_{h\parallel}^{pk}}{2} \tag{4.10}$$

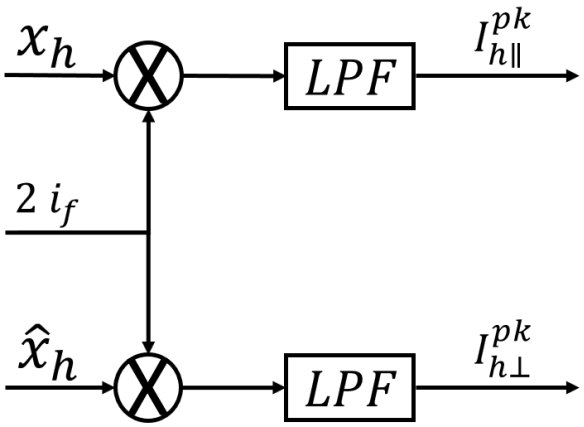

Figure 4.6. Peak detection algorithm.

4.1.2.3 Phase-Locked Loop Controller Tuning

A fundamental part of the strategy presented in this work is the determination of the angle of the grid voltage, that enables the calculation of the in-phase and quadrature signals in all frequencies of interest. The correct determination of these signals depends on the adequate synchronization with the grid voltage. This demands that the PLL is fast, accurate and able to track the grid voltage with minimal error, even under distorted grid conditions. For this reason, it is important that the gains of the PLL PI regulator are correctly determined. Since the sampling frequency is much higher than the frequencies tracked by the PLL, its model can be simplified to the one shown on Figure 4.7 [47], consisting of a PI controller, $C(s)$, in series with integrator and a first-order approximation of the digital delay. The linearization of the moving average filter (MAF) shows that it can be considered as a unit gain. Hence, the open and closed-loop transfer functions of the PLL are as shown on (4.11) and (4.12).

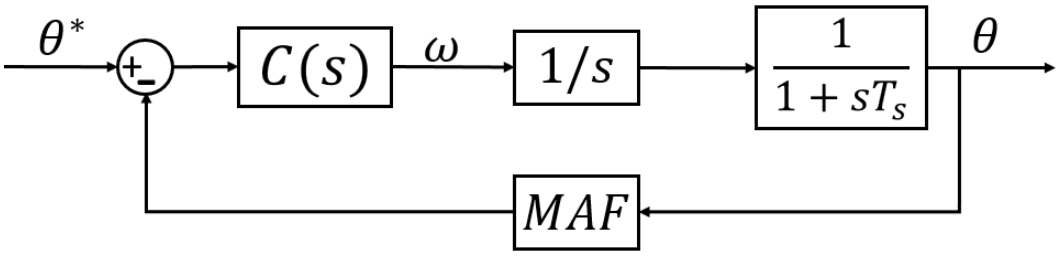

Figure 4.7. Simplified PLL closed-loop model

$$G_{OL}^{PLL}(s) = \frac{s \cdot K_p + K_i}{s} \cdot \frac{1}{s} \cdot \frac{1}{1 + s \cdot T_s} \tag{4.11}$$

$$G_{CL}^{PLL}(s) = \frac{s \cdot K_p + K_i}{s^3 \cdot T_s + s^2 + s \cdot K_p + K_i} \tag{4.12}$$

Considering that the sampling frequency is high, implicating that T_s is small, the third order term can be disregarded without compromising the system performance. Therefore, the closed-loop transfer function assumes the canonical form:

$$G_{CL}^{PLL}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{K_p \cdot s + K_i}{s^2 + K_p \cdot s + K_i} \tag{4.13}$$

Considering a setting time equal to 0.03 ms and a damping ratio of 0.7, the natural frequency of the system is equal to 158.69 *rad/s* and, thus, the controller gains can be determined. The resulting values are shown on (4.14).

$$K_p = 222.16 \qquad K_i = 25,181.22 \tag{4.14}$$

4.1.2.4 Power Controller Tuning

From Figures 4.3 and 4.4 it can be seen that the feedback of the power control loop is done through the power and harmonics (PQD) calculation algorithms and, thus, it can be represented as a single entity as shown on Figure 4.8, where $G_{CL}^{i}(s)$ is the closed-loop transfer function of the current control, H_p is the per-unit base power and MAF represents the moving average filter used to implement (4.3) to (4.5). This figure shows that the power loop is non-linear due to the two signal multiplications. Nonetheless, this section shows that a reasonable approximation can be derived to allow the proper design of the power PI controllers.

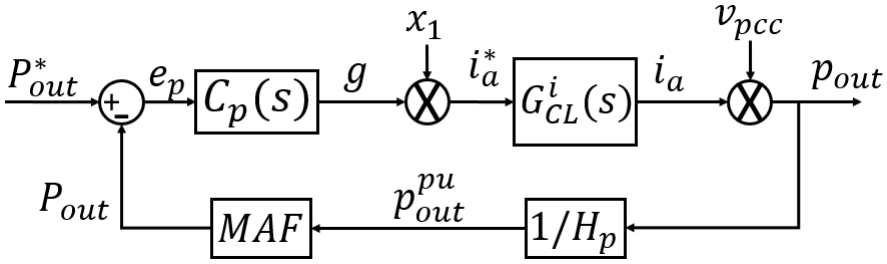

Figure 4.8. Active power control loop

In Figure 4.8, the regulated quantity is the active power (P). However, this structure remains nearly unchanged if a different quantity (Q, $D_{h\|}$ or $D_{h\perp}$) is to be controlled, as only the frequency and phase of signal x_1 have to be changed.

The presence of parallel loops does not interfere with the controller tuning because they regulate quantities that are orthogonal to the active power and, therefore, can be

disregarded. The controller tuning is also independent of the signal frequency, since only the average values are regulated. Thus, the procedure shown in this section can be applied to any of the power control loops. However, it is not necessary to tune the controllers of each loop individually since the dynamic for all of them is identical and, therefore, it is possible to use the same K_p and K_i gains for all loops.

The first simplification regards the MAF. This filter is implemented by a convolution of an input signal with a rectangular window with amplitude $1/T$ in the time domain, as per (4.3). Its Laplace transform is a *sinc* function. Despite being overly complicated to allow the tuning of the controller, the *sinc* function is reasonably approximated by a first-order low-pass filter [48] whose cutoff frequency is equal to 1/4 of the frequency that the MAF is tuned to. Figure 4.9 shows the frequency response of a MAF tuned to 60 Hz and a LPF with cutoff frequency (ω_c) equal to 15 Hz, or 94 *rad/s*. It is clear that the MAF has a narrow bandwidth and, because of that, it is inherently slow.

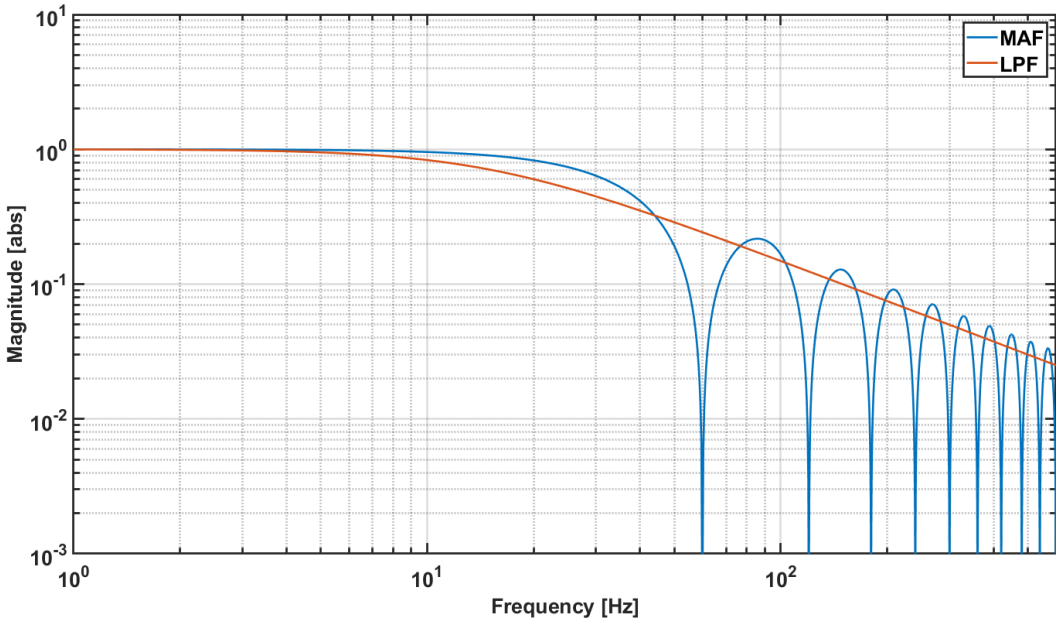

Figure 4.9. Comparison of the MAF and a first-order low-pass filter

As a consequence, it is concluded that the dynamic of the PQD calculation algorithms is dominated by the response of the MAF. Consequently, the dynamics of the power control loops is also slow. This allows a series of other simplifications to be made. First, the closed-loop current control, $G_s(s)$, may be considered equal to its DC gain, H_i. Figure 3.2 shows that this approximation is reasonable for frequencies lower than 100 Hz.

Next, it is necessary to determine the transfer function between the PI output signal, g, and the instantaneous active power, P_{out}. Its exact model cannot easily be obtained, since the time-domain signal multiplications make the system nonlinear, but as the controlled quantity is the average active power, they may be eliminated from the model without loss of generality. The calculation of the instantaneous power is shown in (4.15). This equation shows that the multiplication of the unitary signal, x_1, with the component of the PCC voltage of same frequency yields an average and an oscillating components. Since the oscillating part of the instantaneous power has twice the frequency of the original signal, it is reasonable to assume that the MAF completely rejects this component and only the average value needs to be considered for tuning the controller [49]. This remains valid even if the PCC voltage is distorted, because x_1 is guaranteed to be purely sinusoidal and, therefore, the average value of its multiplication by a signal with different frequency will always be equal to zero.

$$\begin{aligned} p_{out} &= g \cdot x_h \cdot H_i \cdot v_{pcc} \\ &= g \cdot H_i \cdot V_{pk} \cdot sin^2(h\omega_0 t) \\ &= \frac{g \cdot V_{pk} \cdot H_i}{2} \left[1 - cos(2h\omega_0 t)\right] \end{aligned} \tag{4.15}$$

Therefore, the DC gain between the PI output and the average active power is equal to $\frac{V_{pk} \cdot H_i}{2}$ and the loop dynamic is dominated by the LPF. Hence, the open-loop transfer function of the power loop can be determined as in (4.16).

$$G_{OL}^{P,Q,D} = \frac{V_{pk}}{2H_v} \frac{\omega_c}{s + \omega_c} \tag{4.16}$$

From this equation, K_p and K_i are determined using the same procedure described in Section 3.2.2 to tune the current controller. The chosen crossover frequency of the power control loop is equal to 10 Hz and its phase margin is 75 degrees. The resulting gains are shown on (4.17).

$$K_{pp} = 0.86 \qquad K_{ip} = 159.31 \tag{4.17}$$

4.1.3 Output Impedance

As shown in Section 4.1.2.1, the power control loop manipulates the current reference signal for the current control to eliminate the circulation of perturbation currents. This can be understood as an increase in Z_{out} at frequencies in which the PQD loops are implemented. However, the power control loop model derived in Section 4.1.2.4 to tune the PI controllers is simplified and, therefore, cannot be used to demonstrate this effect. In this section, a more complete expression for the current-driven grid-connected converter output impedance is derived, similarly to Section 2.1.2, but considering the presence of the power control loops.

In steady-state conditions, the output of the power PI controller can be considered constant and, by definition, i_a^* is purely sinusoidal. Assuming that the in-phase signal, x_h, is a sine wave, the first multiplication shown in Figure 4.8 is modelled as shown in (4.18). An analogous derivation is done for the reactive power considering the quadrature signal, $\hat{x}_h$, as a cosine wave. The result is shown in (4.19).

$$\frac{i^*_{f,h\parallel}}{g}(s) = \frac{i^*_a}{g}(s) = \frac{sh\omega_0}{s^2 + (h\omega_0)^2} \tag{4.18}$$

$$\frac{i^*_{f,h\perp}}{g}(s) = \frac{i^*_r}{g}(s) = \frac{s^2}{s^2 + (h\omega_0)^2} \tag{4.19}$$

Regarding the second multiplication, the product between i_a^* and the PCC voltage can be handled similarly to (4.16). Since only the average value of the power is of interest, the grid voltage can be treated as being purely sinusoidal despite the presence of harmonic components, as the average value of the product between signals of different frequencies is always equal to zero (i.e., orthogonality principle). Then, the power calculation in the time-domain is represented as a phasor multiplication in the frequency domain and, assuming that the current angle is zero, the average active power is then defined as (4.20). An analogous derivation is done for all other controlled quantities, regardless of the frequency.

$$P_{out} = |I_a|\angle\Theta_a \cdot |v_{pcc}|\angle 0^\circ = |I_a|\angle 0^\circ \cdot |v_{pcc}|\angle 0^\circ$$

$$P_{out} = \frac{I_{a,pk} \cdot V_{pk}}{2} \tag{4.20}$$

Finally, considering the dynamics of the MAF as previously discussed, it is possible to determine the open-loop transfer function of the in-phase and quadrature loops, as in (4.21) and (4.22).

$$G_{OL}^{\parallel}(s) = \frac{V_{pk}(h\omega_0)}{2H_v}\frac{\omega_c}{s+\omega_c}\frac{s}{s^2+(h\omega_0)^2} \tag{4.21}$$

$$G_{OL}^{\perp}(s) = \frac{V_{pk}}{2H_v}\frac{\omega_c}{s+\omega_c}\frac{s^2}{s^2+(h\omega_0)^2} \tag{4.22}$$

It is evident that these equations, due to the *sine* and *cosine* Laplace Transforms, have a similar transfer function structure as the ideal Proportional-Resonant controller. This suggests that the proposed strategy can achieve the same result as a PR controller. In fact, if the diagram shown in Figure 4.8 is redrawn to explicitly show the relationship between the inductor current and the grid voltage when the power control loop is considered, the system shown in Figure 4.10 is obtained. Its transfer function represents the total output impedance of the system and can be calculated as in (4.23), where $F(s) = DPWM(s) \cdot G_{conv} \cdot C_i(s)$. The Bode diagram representation of this equation is shown in Figure 4.11, illustrating the peaks at the 3^{rd} and 5^{th} harmonics. These frequencies were selected because they are commonly present in power systems due to the connection of non-linear loads and, therefore, usually demand compensation.

$$Z_{out}(s) = -\left[Z_f(s) + \frac{F(s)}{H_i}\left(1 + \sum C_{P,Q,D}(s) \cdot G_{OL}^{P,Q,D}(s)\right)\right] \tag{4.23}$$

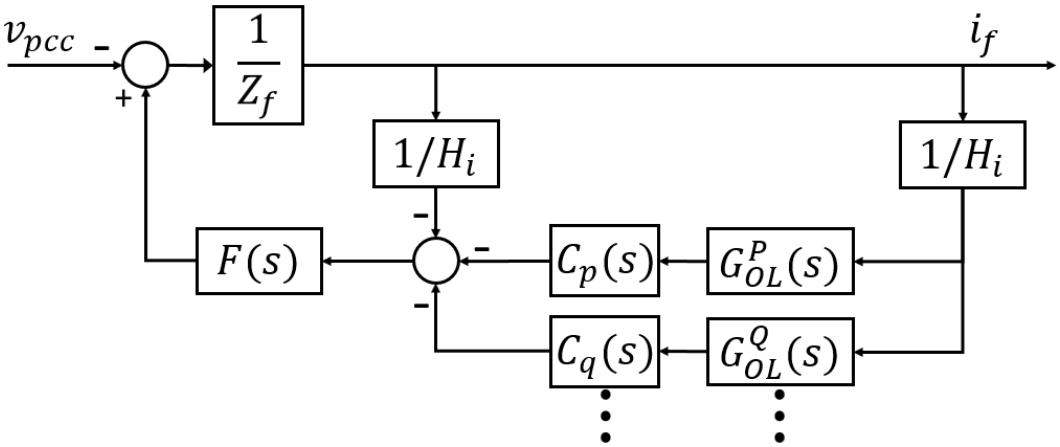

Figure 4.10. Block diagram for the derivation of Z_{out} regarding the filter current and PCC voltage and considering the power control loops

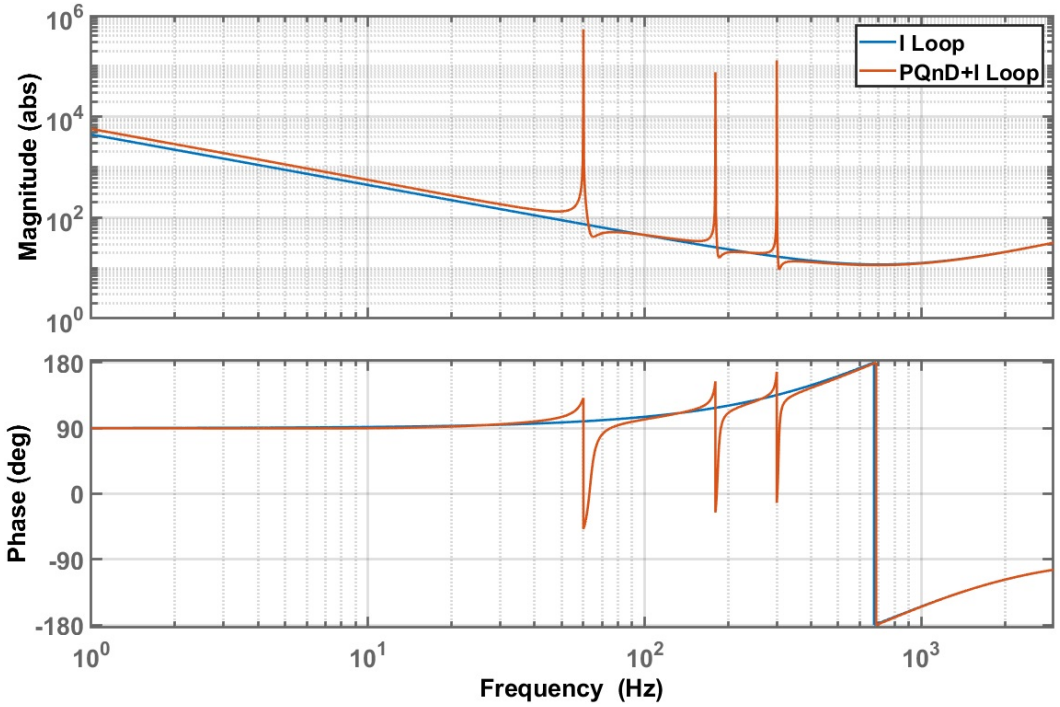

Figure 4.11. Output impedance when applying the power control loops

4.2 Supplementary Converter

The concept of the supplementary converter is introduced in Section 2.2, where its objectives and operation principles were presented. The output filter current control is addressed in Section 3.3. This section analyzes the strategy and the requirements for the implementation of the power and harmonics control.

4.2.1 Power and Harmonics Control

The Double converter configuration, illustrated in Figure 2.9, is composed of a main unit with slow dynamics and poor dynamic stiffness, that injects only active power to the grid and does not provide ancillary functions. Therefore, its power control is composed of a single loop and does not have the multiple controller pairs shown in Figure 4.4. Because of that, it is susceptible to external disturbances.

Therefore, the supplementary converter is proposed to bring such features to the Double Converter system without altering the operation of the main unit. For that, the supplementary unit needs to have a control strategy that can compensate the disturbances that flow to and from the grid caused by the main unit. The proposed strategy is shown on Figures 4.12 and 4.13. As can be seen, it is very similar to the one presented in Section 4.1.2.1, with the exception that the Q and D quantities are calculated based on the grid current (i_g). Thus, the supplementary converter does not directly regulate its own output current, but rather the sum of both converter currents.

Finally, since the supplementary converter must not provide or consume active power, a P control loop based on the filter current (i_f), has to be implemented. This is done to increase the dynamic stiffness of the supplementary converter to the in-phase fundamental harmonic component. However, the loop reference is kept always at zero. For that reason, the supplementary converter must have two current sensors, to monitor i_{f2} and i_g, and an additional voltage sensor, to measure the PCC voltage.

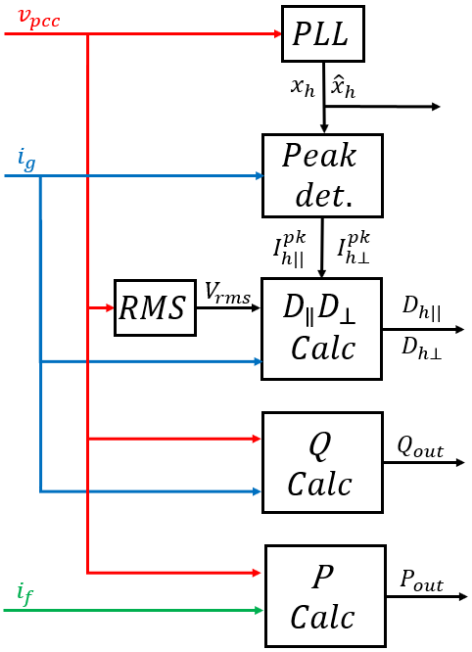

Figure 4.12. Signal generation algorithm for the supplementary converter

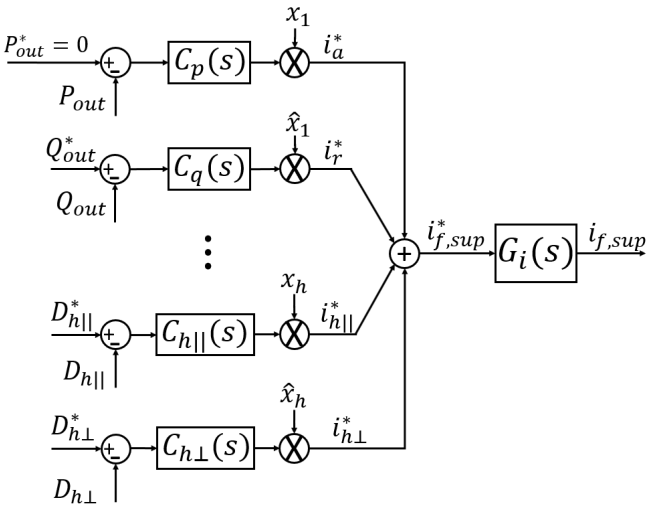

Figure 4.13. Supplementary converter control strategy

4.3 Conclusions

This chapter presented the proposed strategy for power and harmonics control in both grid-connected and supplementary converters. It was shown that its operation consists in manipulating the current reference signal so that it is equal to the disturbance current compensated by the dynamics of the closed-loop current control. The operation of the signal generation algorithm was also explained, detailing the peak detection algorithm and the tuning of the PLL controller gains. Additionally, a procedure to tune the gains of the power controller based on a simplification of the power control loop was presented.

Finally, it was demonstrated that the time-domain multiplication of the power PI controller output by a sinusoidal signal achieves a result similar to the application of a PI-resonant and that the addition of the power control loops has the effect of increasing the Dynamic Stiffness of the converter, which was the desired result. Therefore, it is concluded that the mathematical model derived confirms that the proposed strategy behaves as expected.

Chapter 5

The Microgrid Laboratory

5.1 Presentation

The Microgrids Laboratory is a new facility at the Engineering School of the Federal University of Minas Gerais (UFMG), in Brazil, whose construction was started as part of this work. It has been developed to enable the execution of experiments to validate the strategy presented herein, but also to provide a complete and easy to use setup to other students and professors, helping to increase the quality of the research produced at the university. It will also allow the offer of classes related to renewable energies, PV systems and microgrids to both undergraduate and graduate students. This laboratory has been built in partnership with Brazilian company **PHB Solar**, a manufacturer of grid-connected inverters for photovoltaic power plants, the TESLA laboratory of UFMG, CNPq (420850/2016-3) and FAPEMIG (APQ-02518-16).

5.2 Proposal

The main goal of the laboratory is to study and explore the many possible configurations of a multi-functional distributed generator, collaborating with technological advancements that allow the development of better and more efficient inverter systems. It will be used for the study of grid-connected distributed generators and microgrids. It is expected that several professors and students of the university, in both the Electrical and Electronics Engineering Departments may find its facilities useful for developing their work. The intention is that this laboratory will be expanded, with the addition of new and better equipment, whenever resources are provided both through research projects or partnership with private sector companies.

5.3 Construction

The Microgrids laboratory was set up in the same room that contains the Electrical Machines Drive laboratory. The adaptation of the existing structure was done by the UFMG TESLA laboratory team with the help of UFMG technicians and coordinated by professor Danilo Brandão. To accommodate the new testbenches, the physical structure of the laboratory had to be reorganized and its electrical installations had to be adapted. A new three-phase circuit was added to the laboratory to implement the microgrid to which the inverters and loads are connected. Protection equipment, such as circuit breakers and residual current devices, measurement and monitoring systems were also installed.

5.4 Testbench

Each one of the DG lab testbenches contains a commercial single-phase PV inverter of either PHB-1500-NS or PHB-3000-NS models, whose main electrical inverter parameters are shown in Tables 5.1 and 5.2. The inverters are fed by connecting a three-phase diode rectifier bridge to the PV input. This kind of inverter has a boost converter between the input and the DC bus that is used to implement the Maximum Power Point Tracking (MPPT) algorithm that guarantees that the PV modules connected to the inverter always operate at their maximum efficiency. However, in this work, the boost converter is not used and, therefore, its switch is kept always open. For this reason, the DC bus is effectively connected directly to the rectifier, since the DC impedance of the inductor and the resistance of the diode are negligible.

Table 5.1. PHB-1500-NS parameters

Parameter	Symbol	Value	
Inverter Power	S_{nom}	1500	VA
Filter Inductor	$L_{f1}\|L_{f2}$	1.0	mH
Filter ESR	$R_{f1}\|R_{f2}$	0.5	Ω
Filter Capacitor	C_f	6.6	μF

Table 5.2. PHB-3000-NS parameters

Parameter	Symbol	Value	
Inverter Power	S_{nom}	3000	VA
Filter Inductor	$L_{f1}\|L_{f2}$	0.6	mH
Filter ESR	$R_{f1}\|R_{f2}$	0.5	Ω
Filter Capacitor	C_f	6.6	μF

The testbenches also contain a protection box including a circuit breaker and semiconductor-grade fuses to provide protection for the circuitry and operating personnel, besides external command buttons, contactors and a connector for an external power resistor. The three-phase rectifier is also mounted in this box. Support equipment such as multimeters, oscilloscopes, voltage and current probes and a computer are also available for use in the laboratory. The inverter output is connected to a coupling

transformer, with a 1:1 ratio, that provides galvanic isolation between the input and output. This is done to prevent that different phases are short-circuited through the inverter during the PWM switching, since there is no significant impedance between the active phase of the rectifier and the output when the H-bridge switches are closed.

Figures 5.1 and 5.2 show the setup used to obtain the experimental results using the PHB-1500-NS inverter. Although the setup for a 1.5 kVA inverter is shown, the setup remains almost unchanged if a 3 kVA inverter is to be used. The rectifier, protection box and power resistor do not have to be changed and, thus, it is sufficient to substitute the isolation transformer for a 3 kVA one.

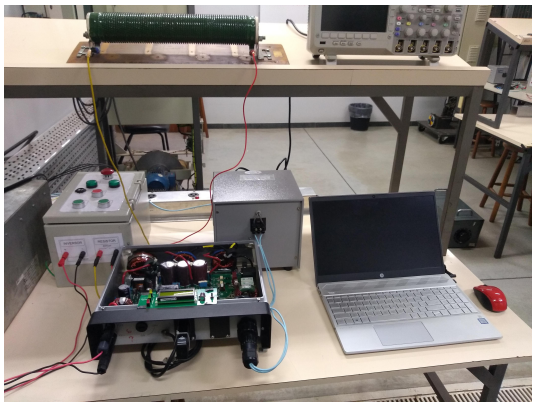

Figure 5.1. Complete experimental setup (PHB-1500-NS).

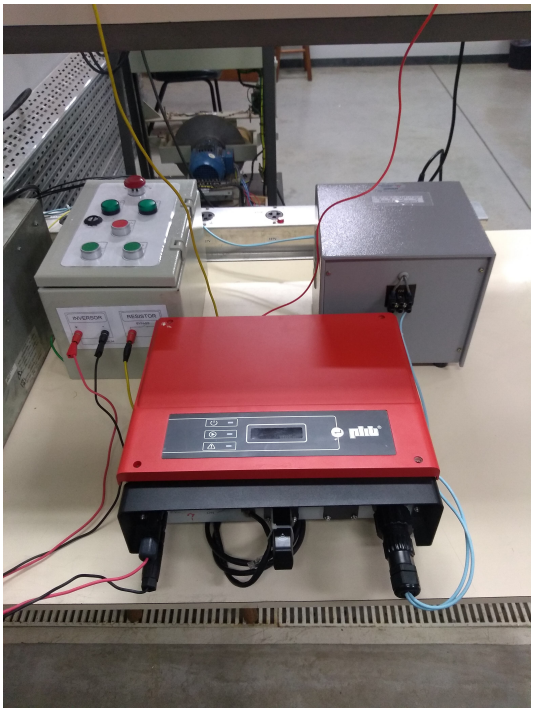

Figure 5.2. Protection box, transformer and PHB-1500-NS.

The developed protection box allows the connection of an external power resistor in series to the inverter input for extra protection, providing an impedance that limits the current if a short-circuit happens. This resistor can also be used to create a voltage divider characteristic, limiting the power that can be transferred to the inverter. With the resistor in series, the input power that is supplied to the inverter is a function of its equivalent resistance, as shown in (5.1), where R_s is the external series resistor, R_{in} is the Boost circuit equivalent input resistance and V_r is the output rectifier voltage.

$$P_{in} = \frac{R_{in}}{(R_s + R_{in})^2} \cdot V_r \tag{5.1}$$

Figure 5.3 shows the resulting curve if the series resistor has a value of 25 Ω. The input resistance of the inverter can be modulated using the input boost converter in a way that is similar to the tracking of the maximum power point in photovoltaic modules. Thus, this setup can also be used to test MPPT algorithms and the control system of the input boost converter. When this resistor is used, a capacitor must be added between the protection box and the converter to give a voltage source characteristic to the output of the box and allow proper functioning of the Boost converter.

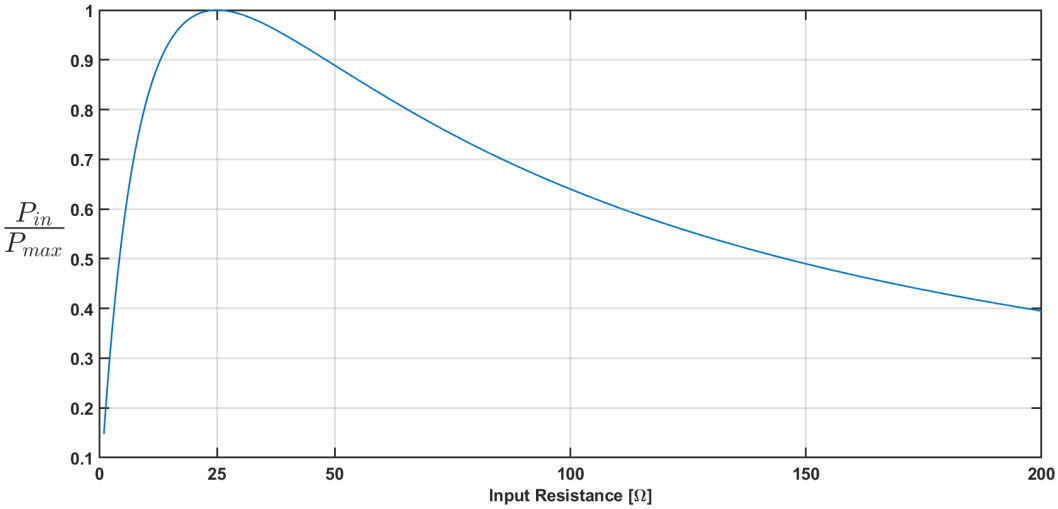

Figure 5.3. Input power as a function of the input resistance

Figure 5.4 illustrates the complete electrical circuit of the microgrid built in the laboratory as well as the schematic of the testbenches. It can be seen that the inverter output is connected to the microgrid bus while the rectifier is supplied by a different circuit. This is done so that the sum of currents at the PCC of the microgrid is not zero.

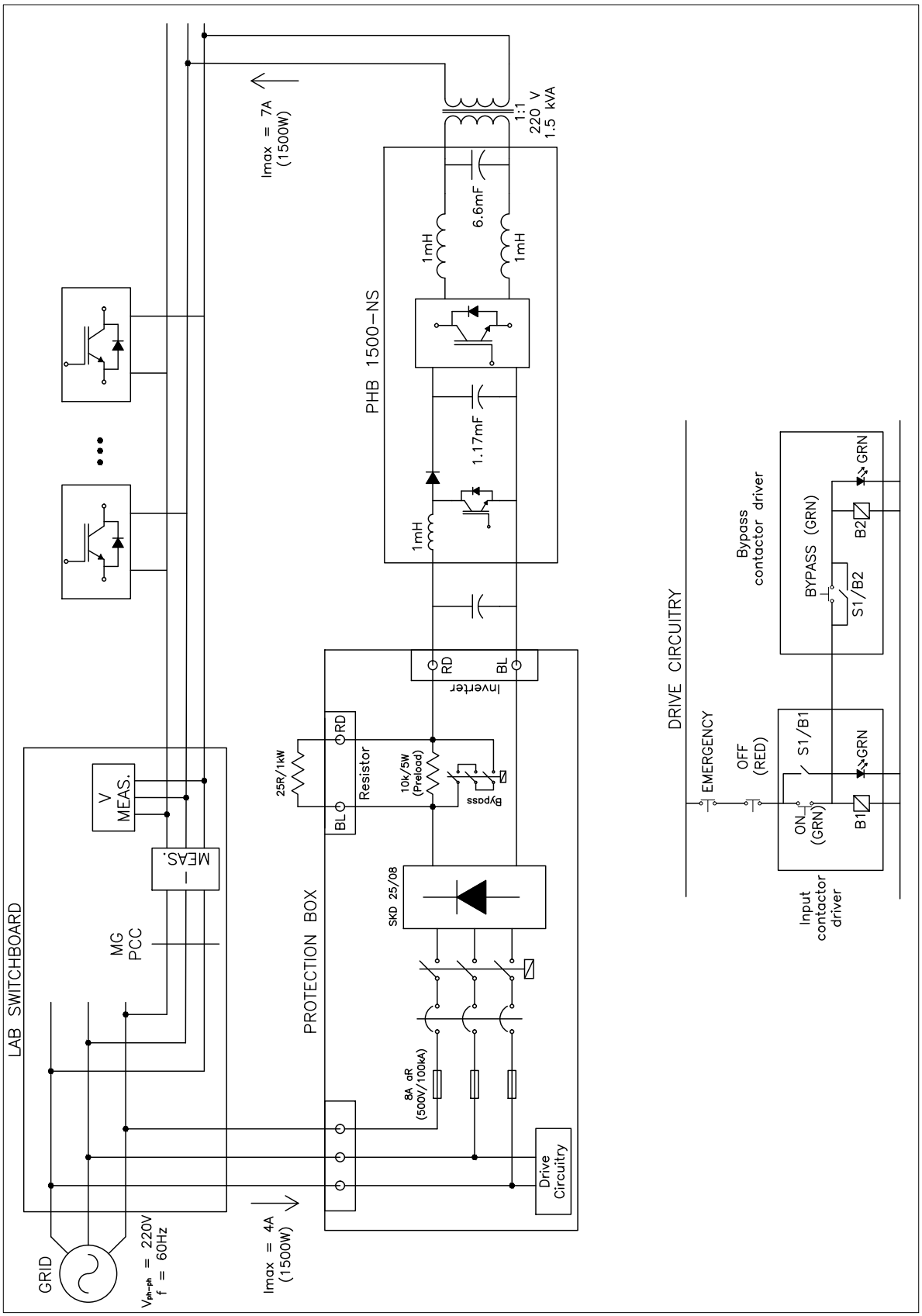

Figure 5.4. DG Laboratory testbench schematic

5.4.1 Coupling Transformer Impedance Measurement

The operation of grid-connected inverters is greatly affected by the impedance of the grid to which they are connected. Since it is essential that an isolation transformer is used in the developed testbench, the grid impedance is greatly increased. Because of that, it is necessary to analyze the impact that it may have on the developed experiments and, to do this, it is required that the exact impedance of the coupling transformer is known.

The equivalent circuit model of a transformer is shown in Figure 5.5. Its parameters are determined by means of a short-circuit and a no-load test [50]. For the no-load test, the primary of the transformer is connected to the grid while the secondary is left open. Since the magnetizing impedance is much higher, the winding impedance can be disregarded and, therefore, it can be assumed that all the current that flows into the transformer is due to the magnetization. Thus, by measuring the input voltage and current and calculating the active and reactive power, the magnetizing parameters are calculated as:

$$L_m = \frac{1}{2\pi \cdot 60} \cdot \frac{V_{rms}}{Q} \qquad R_m = \frac{V_{rms}}{P} \tag{5.2}$$

The short-circuit test consists in short-circuiting the secondary winding and applying a low voltage on the primary such that the current reaches its nominal value. In this case, the current associated with the magnetization is disregarded. From the voltage and current measurements, the active and reactive power are determined and the winding impedance is calculated as:

$$L_w = \frac{1}{2\pi \cdot 60} \cdot \frac{Q}{I_{rms}} \qquad R_m = \frac{P}{I_{rms}} \tag{5.3}$$

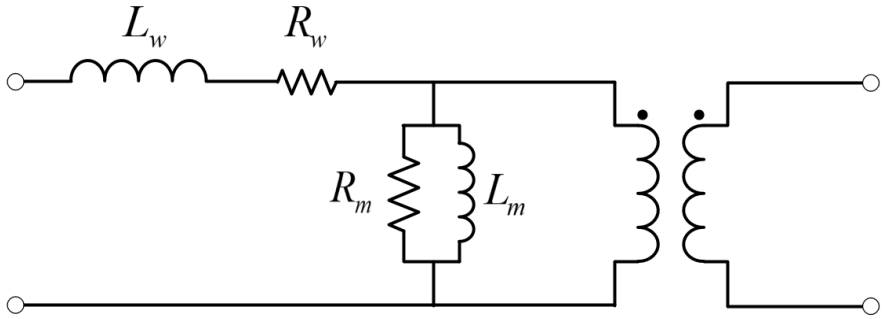

Figure 5.5. Transformer equivalent circuit

5.4.2 Conclusions

This chapter presented the Microgrids Laboratory that is currently being developed at the Federal University of Minas Gerais and whose construction was started as part of this work. The experimental setup developed for testing the proposed strategy was presented and the main parameters of the used inverters were shown.

An important part of this setup is the protection and rectifying box, that was designed to help the operation of the inverters and improve the safety of its users. Its electrical and wiring diagrams were also presented.

Finally, the necessity of an isolation transformer was discussed. It was determined that, since the inverter DC bus is supplied by the same grid that its output is connected to, there is a short-circuit may happen if the system is not galvanically isolated. However, it is necessary to estimate the impedance of the transformer, since it may influence the behaviour of the control system. Therefore, a simple and quick method to obtain the transformer model was also presented.

Chapter 6

Simulation and Experimental Results

6.1 Simulation Results

6.1.1 Grid-Connected Converter

This section presents the simulation results obtained for the Grid-Connected inverter. The electrical parameters considered, shown in Table 6.1, have been chosen to be equal to the 1.5kVA PHB inverter, so that the simulations could be representative of the experimental setup. Table 6.2 lists the controller parameters, whose tuning is shown in Section 3.2.2 and Section 4.1.2.4. The integral gain values shown are multiplied by the switching period.

Table 6.1. System parameters

Parameter	Symbol	Value	
Inverter Power	S_{nom}	1.5	kVA
Filter Inductor	$L_{f1}\|L_{f2}$	1.0	mH
Filter ESR	$R_{f1}\|R_{f2}$	0.1	Ω
Filter Capacitor	C_f	6.6	μF
Capacitor ESR	R_c	1.0	mΩ
Grid inductance	L_g	2.0	mH
Grid resistance	R_g	0.9	Ω
DC bus voltage	V_{dc}	311	V
Switching Freq.	f_{sw}	24	kHz
Sampling Freq.	f_s	48	kHz

Table 6.2. Controller parameters

Parameter	Symbol	Value	
P Gain - Curr.	K_{pi}	0.7990	Ω
I Gain - Curr.	K_{ii}	0.0320	F^{-1}
P Gain - Power	K_{pp}	0.8577	V^{-1}
I Gain - Power	K_{ip}	0.0066	A/J

The grid impedance is unknown and it is difficult to accurately determine, as the usual methods to measure its value rely on special equipment to perform short-circuit tests [51] or in the implementation of dedicated software in the PV inverter to disturb the grid and monitor the resulting variation [52, 53]. Therefore, in this work, the grid impedance is considered equal to the impedance of the coupling transformer. Because of the relatively high series resistance and inductance of the transformer, the actual grid impedance can be disregarded.

6.1.1.1 Dynamic Stiffness Validation

The Output Impedance for the Grid-Connected inverter with PI current control is derived in Chapter 2 and can be calculated as described in (2.8). For clarity, the resulting transfer function is shown again in (6.1).

$$Z_{i_f}^{v_{pcc}}(s) = \frac{v_{pcc}}{I_f}(s) = -\left(\frac{V_{DC} \cdot DPWM(s) \cdot C_i(s)}{H_i} + Z_f\right) \tag{6.1}$$

The Bode Plot of this transfer function, considering the parameters listed on Tables 6.1 and 6.2, is shown on Figure 6.1. It can be seen that for low frequencies the system has a high Dynamic Stiffness due to the large DC gain of the PI controller. In this region, the impedance is almost purely capacitive, since the inductor reactance is low and the PI has a capacitive characteristic. The diagram shows that the phase is equal to 90° because of the negative sign in (6.1). The Dynamic Stiffness also increases in the high frequency range, where the filter inductor reactance is responsible for increasing the system's output impedance. However, for the middle range, the impedance magnitude is low. This is a critical range where the most significant voltage harmonics are usually located and, thus, may compromise the inverter operation.

To validate this plot, simulations are conducted in MATLAB/Simulink. An ideal voltage source with 100V amplitude is connected directly to the PCC and the current control loop is implemented. Maintaining the current reference at zero, the disturbance current is measured and, with the use of the Simulink FFT tool, the output impedance is calculated. This procedure is repeated for several frequencies and the red dots on Figure 6.1 represent the obtained results. It is clear that the derived model matches the simulation results with great accuracy. The same procedure is conducted to analyze the output impedance regarding the grid current. The results are shown in Figure 6.2. In this case it is possible to see the resonance frequency between the inverter output filter and the grid impedance.

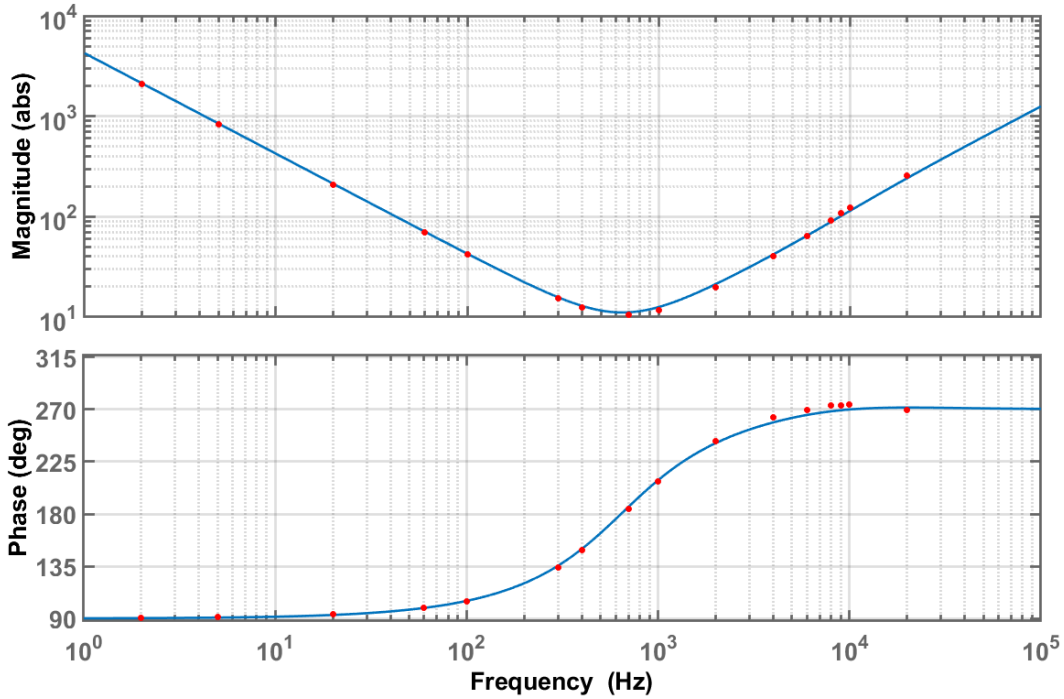

Figure 6.1. Output Impedance for a current-controlled grid-connected inverter from the PCC perspective ($Z_{i_f}^{v_{pcc}}$).

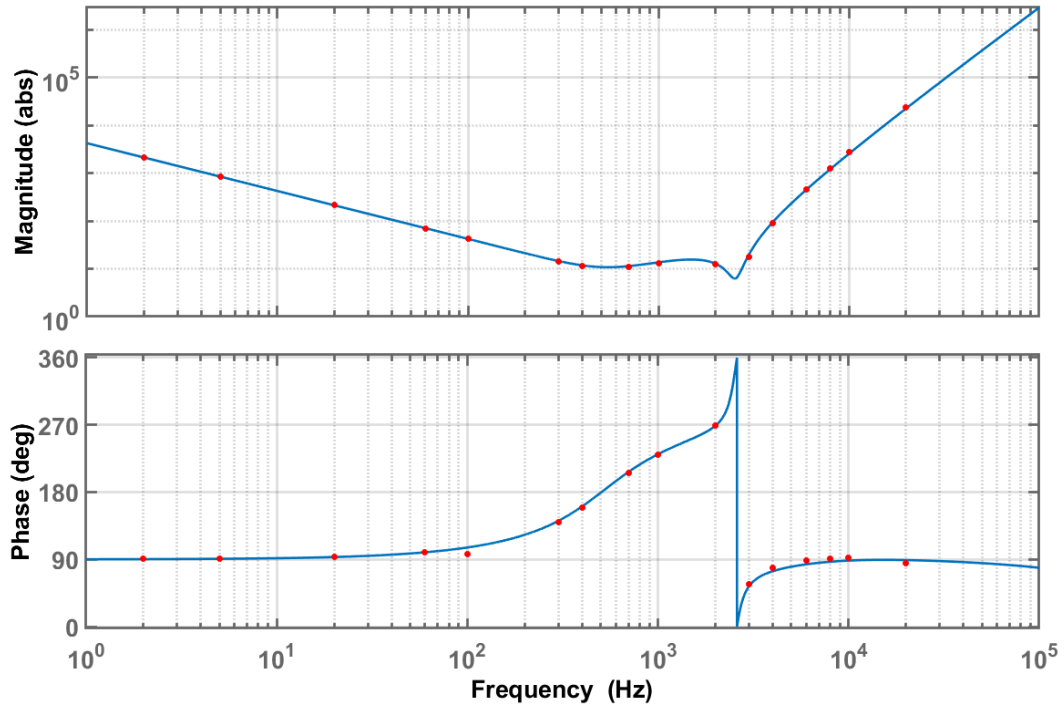

Figure 6.2. Output Impedance for a current-controlled grid-connected inverter from the grid perspective ($Z_{i_f}^{v_g}$).

6.1.1.2 Selective Output Impedance Based Power and Harmonics Control

To evaluate the power and harmonics control strategy proposed on Section 4.1.2.1, a simulation of a power-controlled converter connected to a grid with highly distorted voltage is designed in Simulink. The harmonic components used in this simulation are shown in Table 6.3. In this simulation, the active and reactive power references are kept at zero until a step of 0.3 p.u. is given to the $P*$ reference at $t = 0.5s$, as illustrated in Figure 6.3 (a). Then, a step of the same size is given to the $Q*$ reference at 0.75 seconds, as shown in Figure 6.3 (b). The references of the harmonic distortion control loops are kept at zero during the entire simulation. It is seen that there are no disturbance currents flowing through the filter before 0.3 s, which indicates that the power control is capable of effectively compensating the low output impedance of the current control loop and rejecting disturbances. Therefore, the output current is not affected by the grid distortion, having a THD equal to 2.7%, being this small distortion due to the remaining switching ripple.

Regarding the steady-state performance, it can be seen from Figure 6.4, in which the calculated power terms and harmonic distortion quantities are shown, that the system has a satisfactory behaviour, since the active and reactive power track the reference signals and stabilize in less than 0.1 seconds, while the harmonics remain at zero during the entire simulation.

Table 6.3. Grid voltage harmonic components

Harmonic order	Magnitude (%)
1^{st}	100
3^{rd}	10
5^{th}	10
7^{th}	5
THD	15.0 %

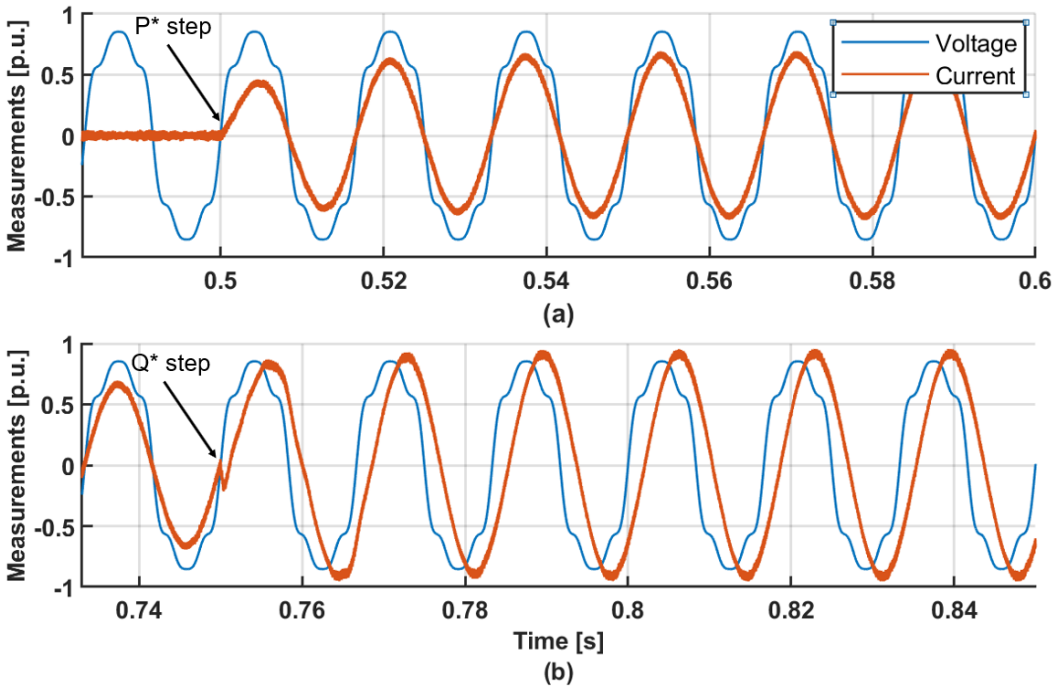

Figure 6.3. PCC voltage and filter current.

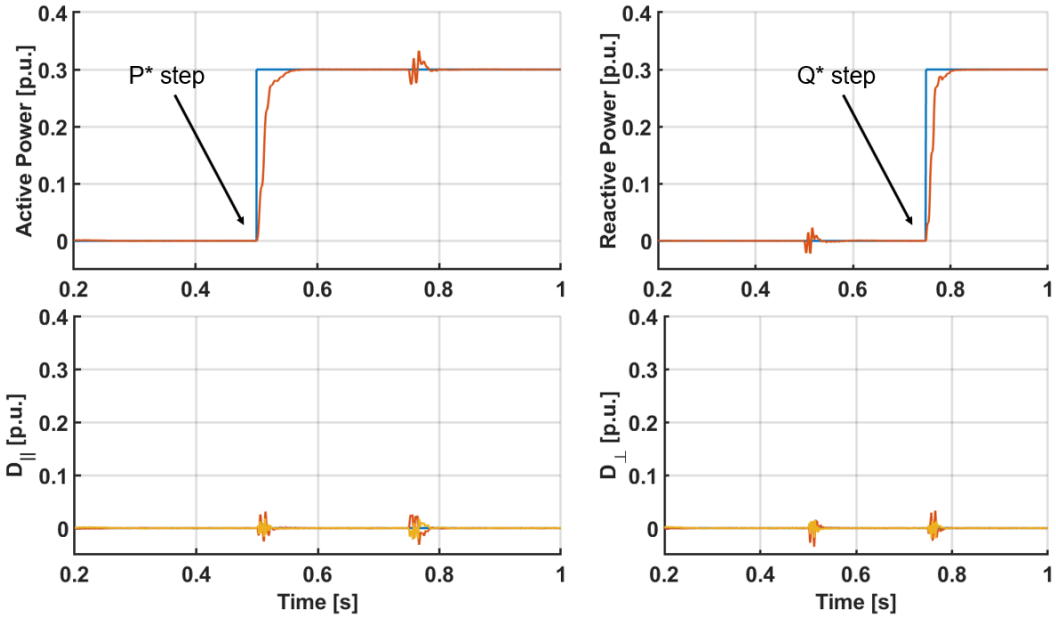

Figure 6.4. Calculated power terms.

6.1.1.3 Sensitivity Analysis

Finally, it is important to determine the robustness of the proposed strategy to parameter variations. In this work, all inverter parameters can be accurately determined and, therefore, the only parameter that presents an uncertainty regarding its value is the grid impedance. To evaluate the sensitivity of the proposed strategy to its variations, several simulations with different values of grid inductance and resistance are conducted.

The nominal grid impedance is shown on Table 6.1 and is equal to the impedance of the coupling transformer. First, the value of the grid inductor is changed, while the resistance value is kept equal to 0.9 Ω. Then, the inductor is kept at its rated value (2 mH) while the resistance is changed.

Figure 6.5 shows the simulation results for a step change in the active power reference. It can be seen that even a relatively high variation in the grid parameters does not significantly affect the behaviour of the system. Therefore, it is possible to conclude that the proposed strategy is robust to parameter variations.

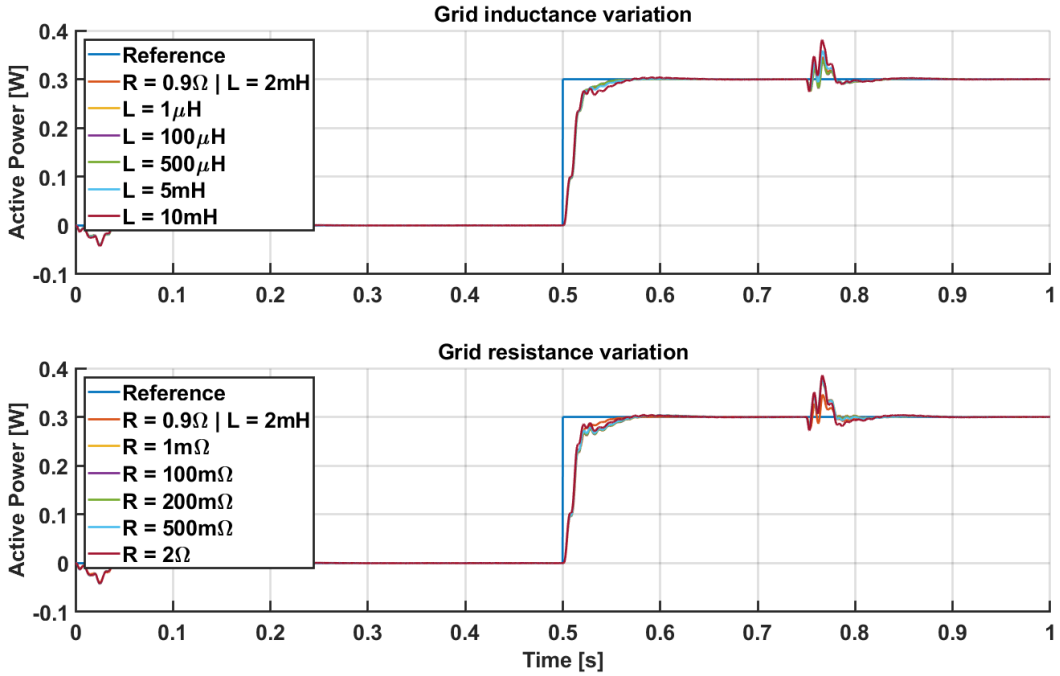

Figure 6.5. Analysis of the sensitivity of the proposed strategy to grid parameter variations.

6.1.2 Double Converter

Figure 6.6 shows the operation of the standalone main converter in a situation with a highly distorted grid voltage, whose harmonic components are listed in Table 6.4. Before 0.4 s it is possible to see the disturbance current that flows through the output filter when the active power reference is equal to zero. After that, a reference equal to 0.2 p.u. is applied to the P loop. It is clear that the main inverter is incapable of adequately controlling the output current and is susceptible to current disturbances. In this case, the current THD value is equal to 24.9%.

Table 6.4. Grid voltage harmonic components

Harmonic order	**Magnitude (%)**
1^{st}	100
3^{rd}	10
5^{th}	10
7^{th}	3
9^{th}	2
11^{th}	2
THD	14.70 %

Figure 6.7 shows the operation of the double converter with the supplemental unit configured to operate on all harmonic frequencies shown on Table 6.4. It is seen that the disturbance is completely eliminated and the grid current is in-phase with the voltage, as desired. In this case, the THD value of the grid current is equal to 2.3%. It is clear that the supplemental converter is very effective and dramatically improves the system performance. Figures 6.8 and 6.9 show a visual comparison of the THD reduction in the grid current when the supplemental converter is active.

To provide better clarity about the operation of the supplemental converter, Figure 6.10 shows the output current of both converters. It is seen that the current injected by supplemental unit into the PCC is the exact opposite of the disturbance that flows into the main unit. Thus, the proposed power control strategy makes the supplemental converter acts similarly to an active power filter.

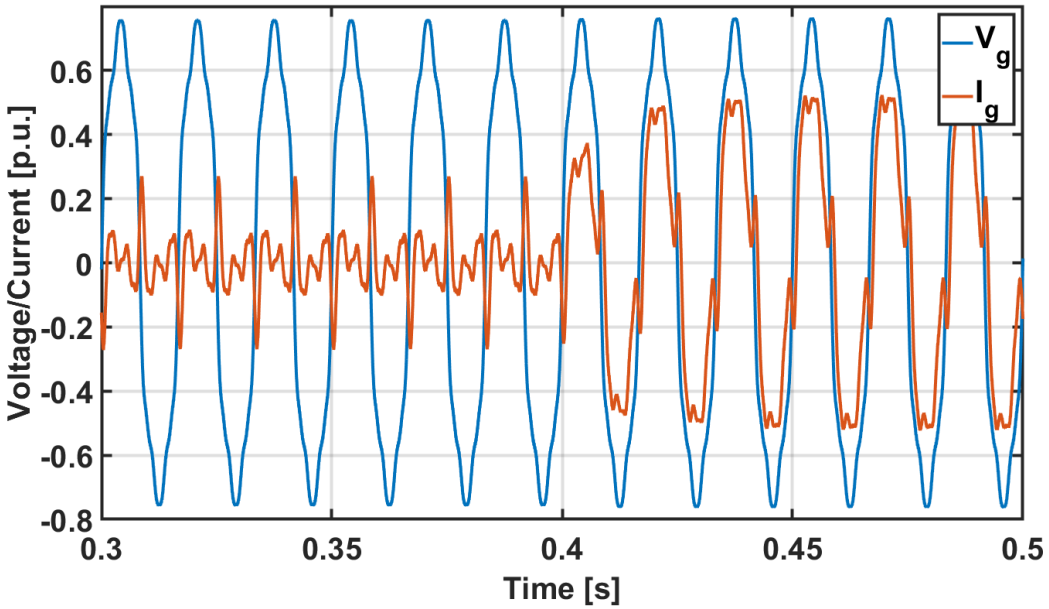

Figure 6.6. Grid current when only the main converter is active

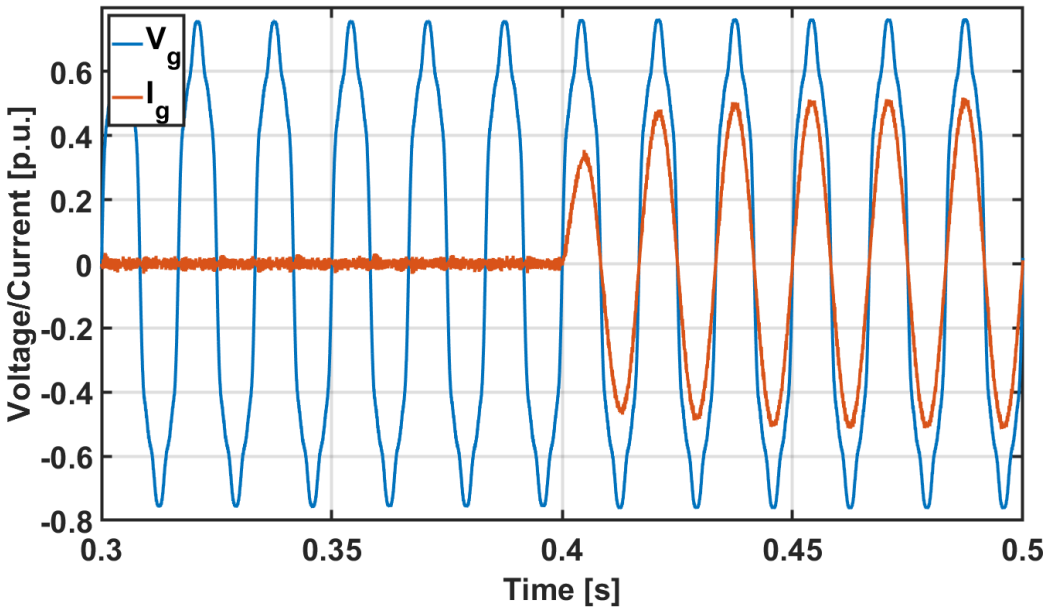

Figure 6.7. Grid current when both converters are active

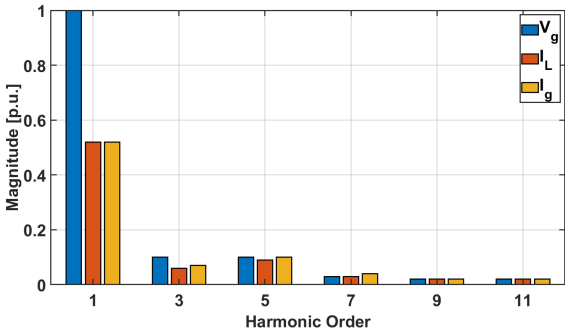

Figure 6.8. THD of the voltage and current when only the main converter is active (THD = 24.9%).

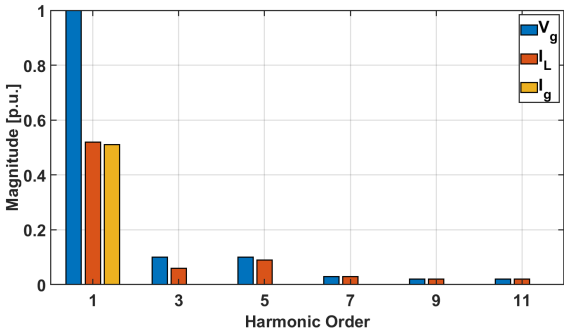

Figure 6.9. THD of the voltage and current when both converters are active (THD = 2.3%).

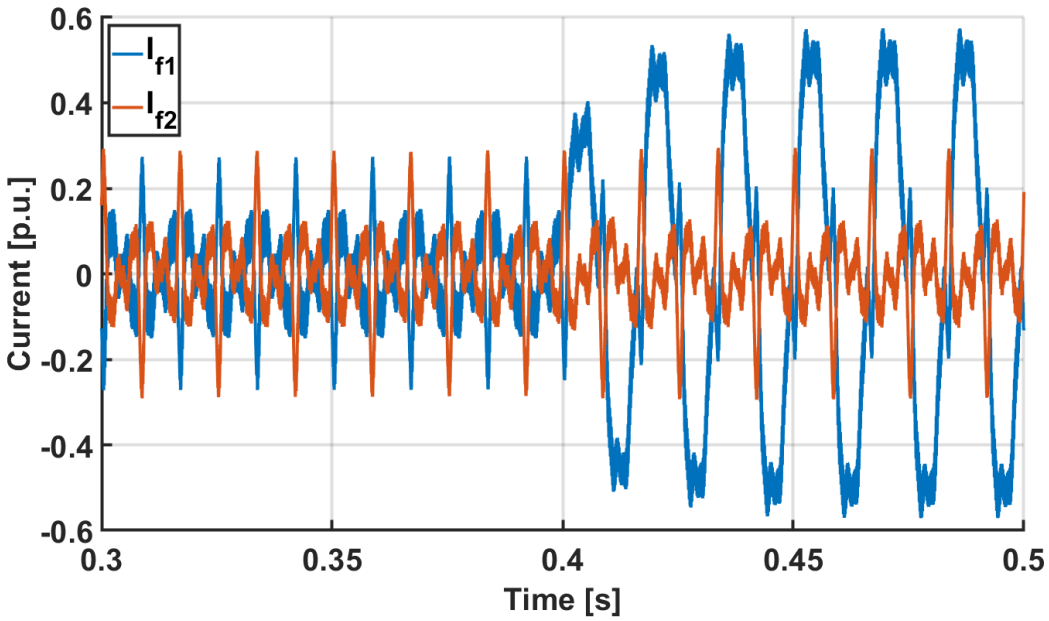

Figure 6.10. Output current of both converters

6.1.2.1 Dynamic Stiffness Evaluation

The calculation of the output impedance of a parallel connection of two inverters is very straightforward as long as each one controls only their own output filter current. In this case, both converters can be simplified to a complex impedance equal to their Dynamic Stiffness at the frequency of interest, and the total output impedance of the resulting double configuration is the parallel association of both output impedances and their respective filter capacitors, as calculated and shown in Section 2.2.2 (Figure 2.11).

In this section, the Dynamic Stiffness of the double converter is evaluated through simulations, similarly to what was done before for the grid-connected inverter. First, each one of the converters is evaluated separately. Figure 6.11 shows the analytically calculated output impedance for each converter, Z^1_{out} and Z^2_{out}, whose transfer functions are shown in (2.14) and repeated in (6.2) for convenience, and the values obtained on simulation by using the same procedure explained in Section 6.1.1.1. Once more, it is seen that the developed model is accurate.

$$Z^1_{out} = \frac{Z^{v_{pcc}}_{I_f1} \cdot Z_{c1}}{Z^{v_{pcc}}_{I_f1} - Z_{c1}} \qquad Z^2_{out} = \frac{Z^{v_{pcc}}_{I_f2} \cdot Z_{c2}}{Z^{v_{pcc}}_{I_f2} - Z_{c2}} \tag{6.2}$$

Finally, the Dynamic Stiffness of the Double Converter, Z^{dual}_{out}, which is the parallel association of the main and supplementary units, is measured. Its transfer function is shown in (2.15) and repeated in (6.3). Again, the simulation results show that the derived model is correct and can be used to accurately predict the current that flow into the system due to an external voltage disturbance.

$$Z^{double}_{out} = -\left(Z_g + \frac{Z^1_{out} \cdot Z^2_{out}}{Z^1_{out} + Z^2_{out}} \right) \tag{6.3}$$

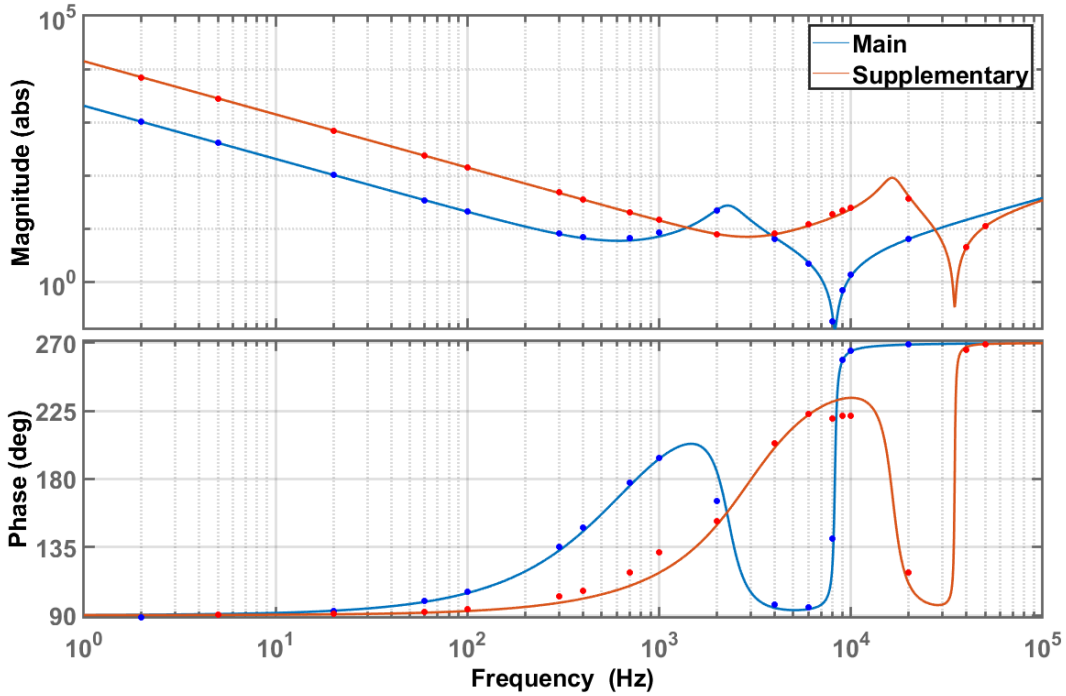

Figure 6.11. Simulation validation of the output impedance for the main and supplementary converters

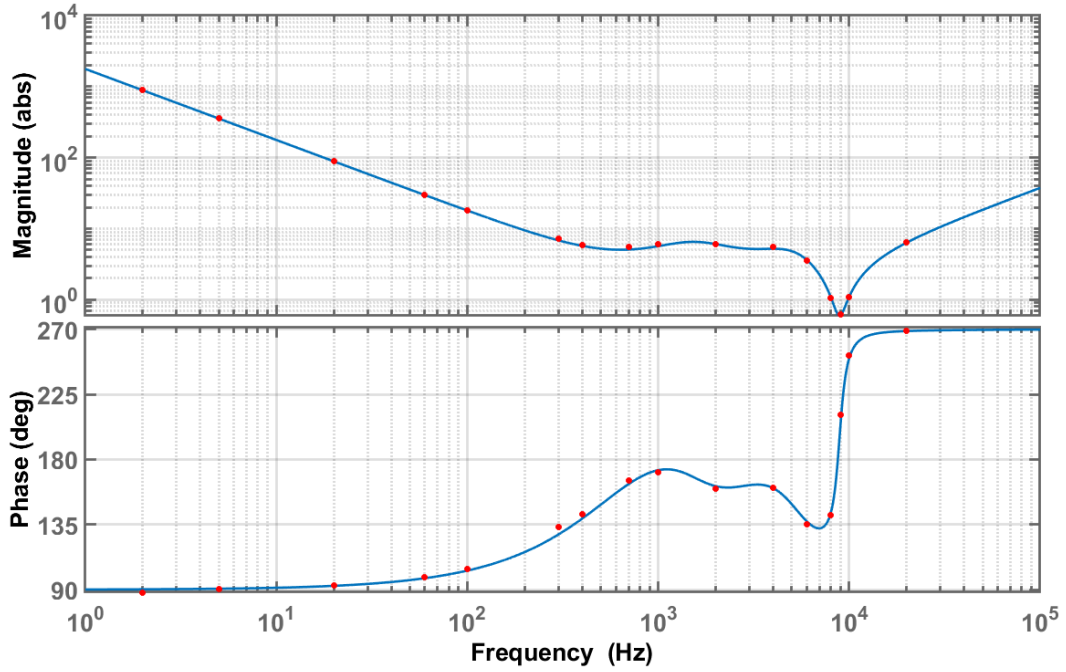

Figure 6.12. Simulation validation of the output impedance for the dual converter configuration

6.2 Experimental Results

6.2.1 Dynamic Stiffness

To complement the simulation results and validate the proposed control strategy operation, it is also implemented on the PHB-1500-NS. The control setup of this inverter is composed of a current sensor that measures the output filter current and a voltage sensor that measures the capacitor voltage. Conditioning circuits feed these signals into an F28034 fixed point Digital Signal Processor (DSP), with 60 MHz clock frequency and 128 kB of flash memory. This DSP can be programmed through a JTAG probe, using a connector that is available in the main circuit board of the inverter.

First, it is necessary to test the behaviour of the DS to validate the current control and the model described in Section 2.1.2. Thus, the control loop presented in Section 2.1.1 is implemented and the system is connected to a *Pacific 354-ASX* controlled voltage source. Then, the disturbance current flowing into the inverter is measured. By applying an FFT to the measured voltage and current waveforms, the magnitude and phase of each harmonic component are determined and the output impedance is calculated. This process is repeated for the entire operating range of the source. Figure 6.13 shows the analytical output impedance between the PCC voltage and the filter current ($Z_{i_f}^{v_{pcc}}$), as defined in (2.8), and the experimental values. It is seen that the measured values are very close to the theoretical curve.

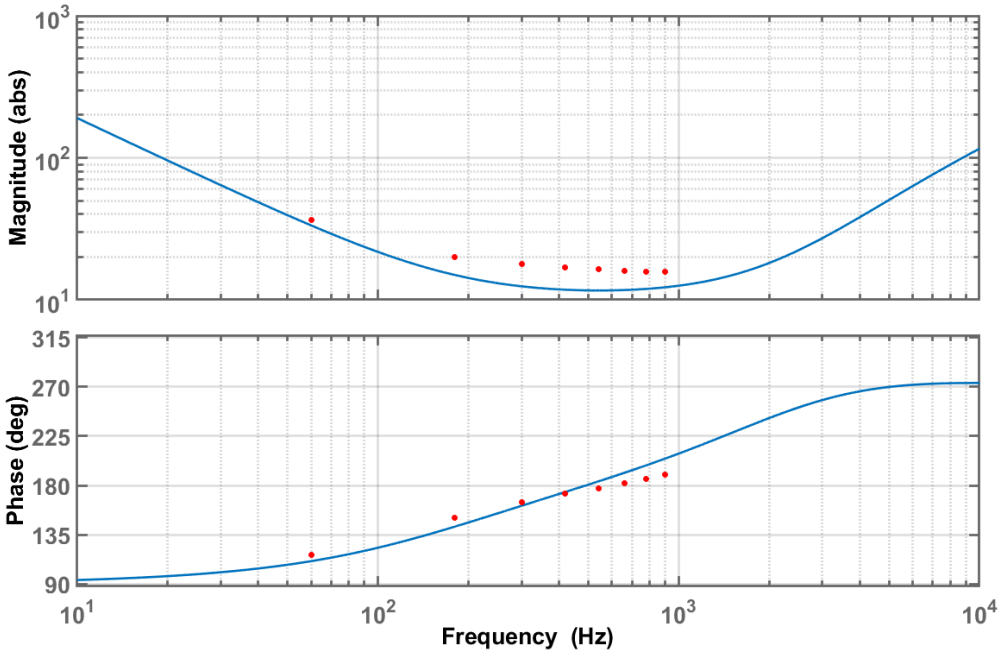

Figure 6.13. Theoretical and experimentally measured output impedance (Z_{pcc})

6.2.2 Selective Output Impedance-Based Control

Having validated the current control and the Output Impedance model, the next step is the validation of the power and harmonics control performance. For that, it is necessary to first establish a benchmark. Herein, the reference case is the operation with only the single-loop current control. Figure 6.14 shows the grid voltage and the disturbances current that flow through the inverter when the current reference is equal to zero (i.e. $i_f^* = 0$). Due to the transformer and other inherent grid conditions, the grid voltage is distorted, with a significant presence of 3rd, 5th and 7th harmonics.

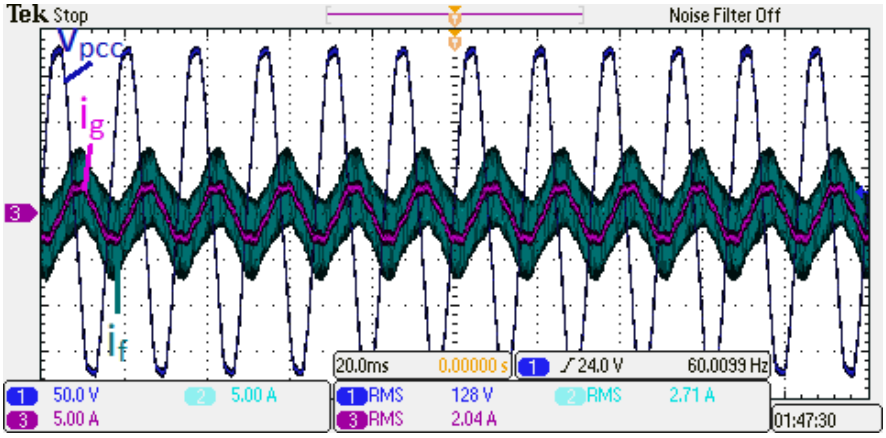

Figure 6.14. Disturbance current with only the current loop.

The first test realized to validate the proposed strategy is the implementation of the active power control loop. Figure 6.15 shows that when this loop is included and its reference is set to zero, the in-phase component of the current is completely eliminated. Therefore, the phase difference between the grid voltage and the disturbance is -90°.

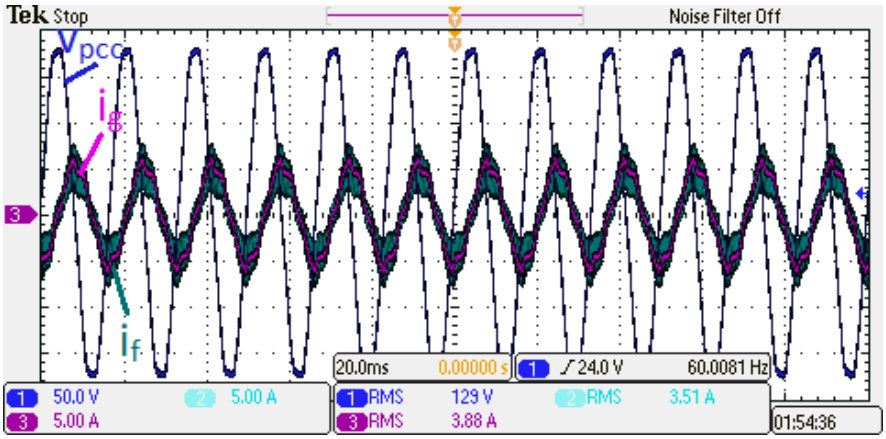

Figure 6.15. Disturbance current with the active power loop.

In sequence, the active power control was removed and the reactive power control loop was implemented in its place. As shown in Figure 6.16, in this case, it is the quadrature component of the disturbance current that is eliminated and the phase difference between the voltage and current is 180 degrees. As shown on Figure 2.8, the output impedance phase is approximately 100° at 60 Hz and, therefore, its reactive component is much larger than the active one. This explains why the magnitude of the disturbance current is much lower in this case.

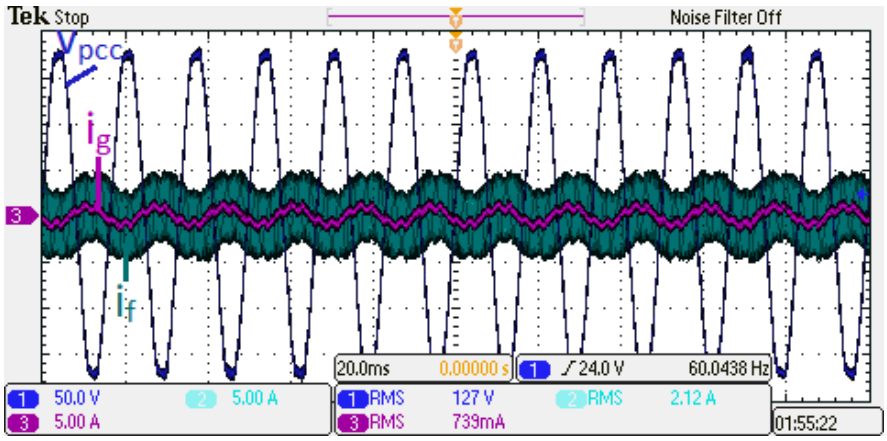

Figure 6.16. Disturbance current with the reactive power loop.

Having validated the independent operation of both P and Q control, they are now implemented together. Figure 6.17 shows the results. It is clear that the fundamental component of the filter current is eliminated and only the higher order harmonics are left. A small quadrature component is still present in the grid current, due to the filter capacitor, but could be eliminated considering a constant offset value in the reactive power reference corresponding to the capacitor reactive power.

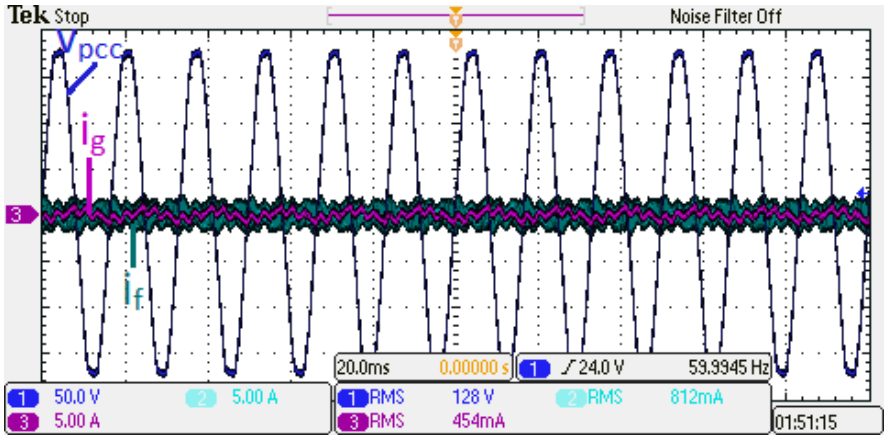

Figure 6.17. Disturbance current with the P and Q loops.

Finally, the harmonic control loops are included, completing the implementation of the proposed strategy, as shown on Figure 4.4. As mentioned, the most significant voltage harmonics components are the 3rd, 5th and 7th and, therefore, the three harmonic control loops relative to these frequencies are implemented. Figure 6.18 shows the resulting disturbance current. It is clear that the higher frequency components that are evident in previous figures have been completely eliminated, validating the operation of the proposed strategy. By applying an FFT to the waveforms shown in Figures 6.18 and 6.14, the magnitudes of each component are determined. Figures 6.19 and 6.20 show the comparison of the obtained results, where "M" stands for the modulation index ($M = f_{sw}/f_{grid}$) and represents the switching frequency ripple. It is seen that there is a significant reduction in the harmonic circulation, validating the operation of the proposed strategy.

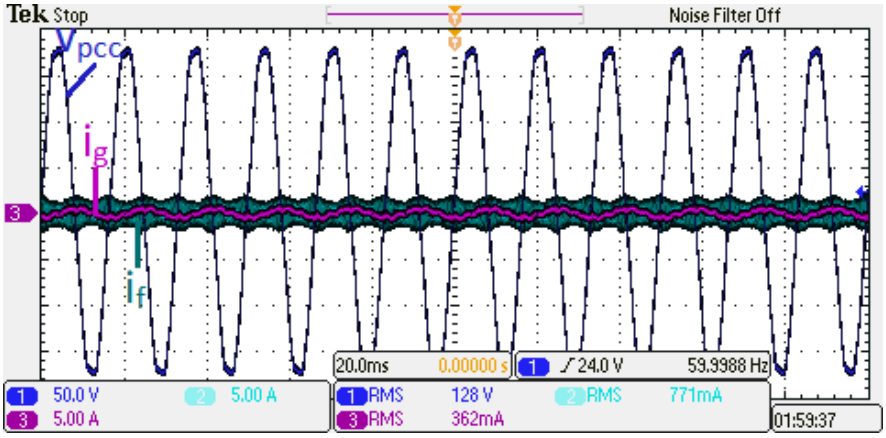

Figure 6.18. Disturbance current with the PQD loops

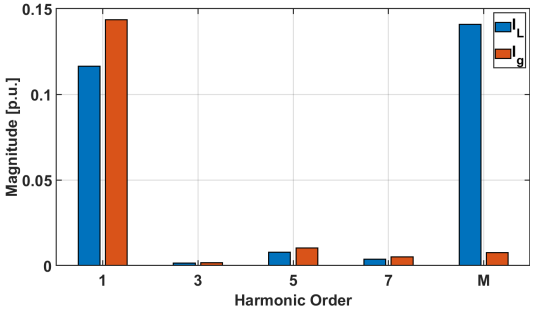

Figure 6.19. Components of the filter and grid currents without compensation.

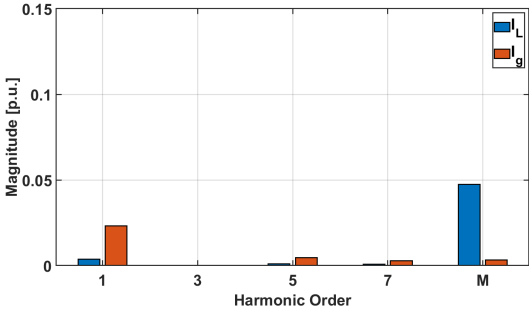

Figure 6.20. Components of the filter and grid currents with active PQD loops.

The last experiments have the objective of validating the power factor control. First, a reference equal to 0.15 p.u. (300 W) is applied to the active power control loop, while the reference of the reactive power is zero. Since the objective of this work is to inject a purely sinusoidal current into the grid, the harmonic control loop references are always set to zero. Figure 6.21 shows the transient behaviour of the filter and grid currents and Figure 6.23 shows the steady-state results. It is seen that the filter current is in-phase with the grid voltage with no significant harmonic distortion other than the switching frequency, as expected, yielding a THD of 3.91%. It is noteworthy that, because of the current sensor direction adopted, as shown in Figure 2.1, a phase shift of zero degrees is obtained. Then, a final test is conducted, in which both the active and reactive power loop references are set equal to 0.1 p.u. Again, the distortion control references are all set to zero. Figure 6.22 shows the transient response of the control system while Figure 6.24 shows the steady-state behaviour. It is seen that the resulting current waveform is phase-shifted from the grid voltage by 45°, as expected. In this case, the grid current THD is equal to 3.58%. Therefore, it is possible to conclude that the proposed Selective Output Impedance-Based Control works as intended and is capable of actively regulating the converter output current while minimizing the disturbances and regulating undesired harmonic components.

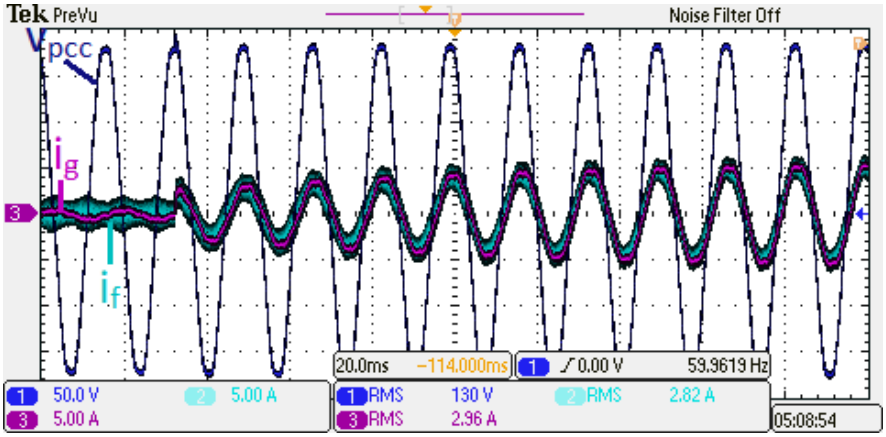

Figure 6.21. Filter and grid current current for a step of 0.15 in P^*.

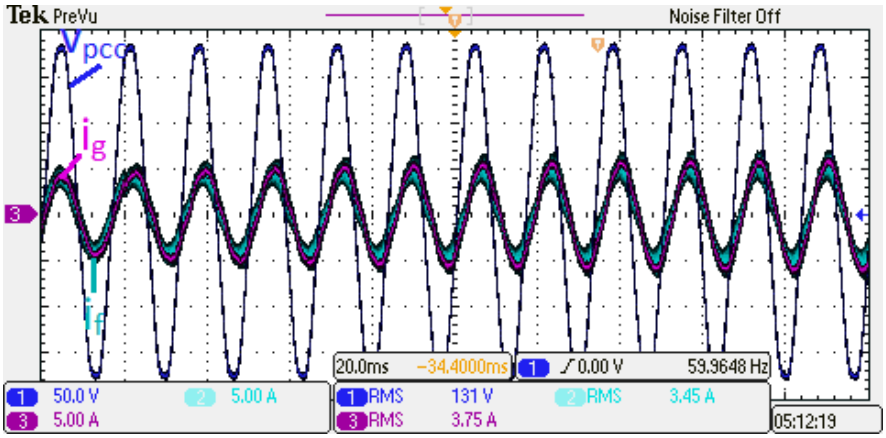

Figure 6.22. Filter and grid current current for a step of 0.15 in Q^*.

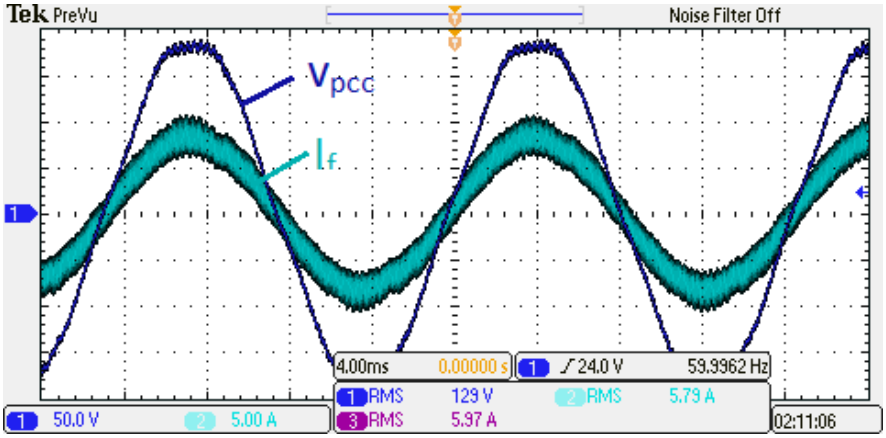

Figure 6.23. Filter current for $P^* = 0.2$ (THD = 3.91%).

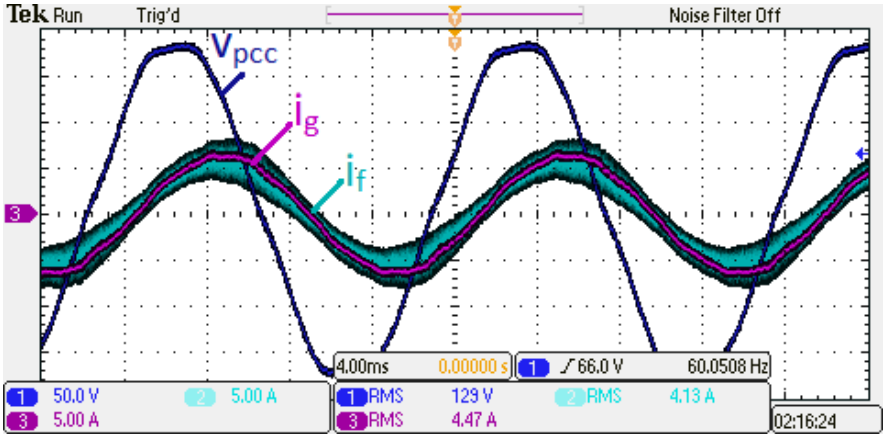

Figure 6.24. Filter current for $P^* = 0.1$ and $Q^* = 0.1$ (THD = 3.58%).

6.2.3 Analysis of the computational calculation time

6.2.3.1 Current control loop

An important characteristic of digital control strategies is the time spent by the DSP to calculate the control signal. In a PWM controlled inverter, the update of the reference waveform must be synchronized with the zero or peak of the carrier to avoid changing the reference during its ramping up/down, which could lead to multiple switch transitions in a single cycle [36]. Additionally, if the sampling is also synchronized, it coincides with the average value of the filter inductor current, as shown on Figure 6.25. This creates an aliasing effect that naturally filters the measured current and eliminates the switching ripple from the input signal.

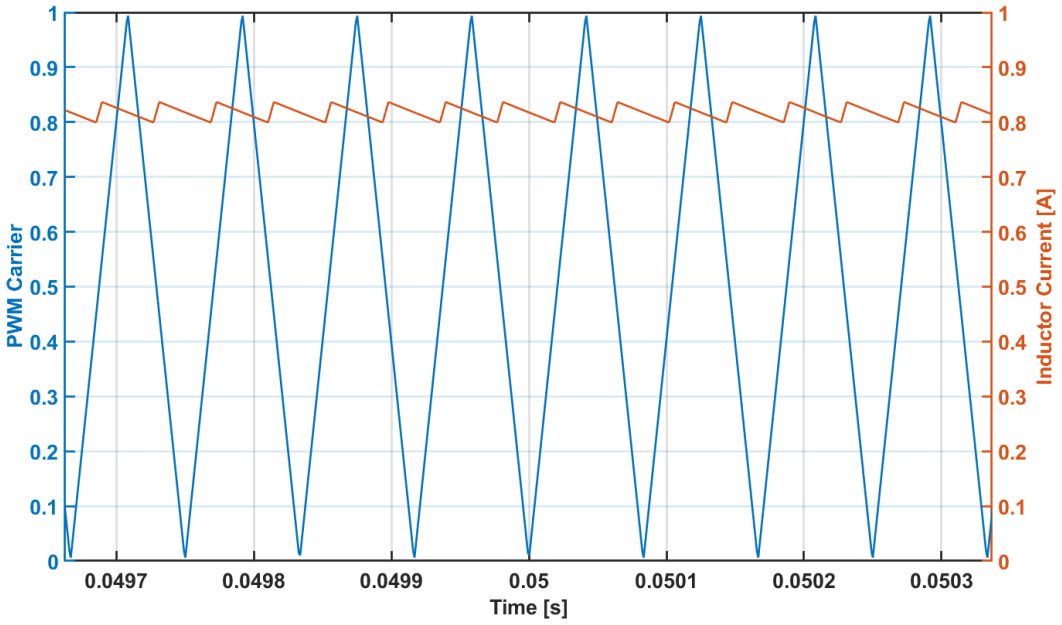

Figure 6.25. PWM carrier and output inductor current (I_f)

To assure correct synchronization, many DSPs have an embedded interruption system that triggers when the PWM carrier reaches zero, peak or both, inside which the current control algorithm can be programmed and the input sampling can be done. This algorithm must be entirely calculated before the next interruption triggers, and, therefore, the maximum allowed time for its execution is equal to $\frac{1}{2 \cdot f_{sw}}$ for asymmetrical PWM and $\frac{1}{f_{sw}}$ for symmetrical PWM. If this interruption surpasses the maximum allowed execution time, one of two possibilities may happen: 1) The DSP keeps calculating the control algorithm and discards the new measurement; 2) The DSP stops calculating the control algorithm and starts the calculation again with the new measurement. In either case, the performance of the current control is compromised.

In this work, as shown on Table 6.1, the switching frequency is equal to 24 kHz and the PWM interruptions trigger on both the zero and peak of the carrier waveform. Therefore, the maximum execution time for the code placed inside the interruption is approximately $20\mu s$. This limit is narrow, especially when other algorithms, such as overcurrent or overvoltage protection and PLL, also needed to be executed. To overcome this problem, these algorithms are divided into two groups. The first one includes the protections and PLL and is calculated when the carrier reaches zero. The second one comprises the current control and is executed when the carrier reaches its peak. In both groups the sampling is also executed. The value of both measurements is then averaged and used as input to the current control.

In current-driven grid-connected inverters, it is usual to implement the current control using proportional-resonant controllers [16, 27, 28]. As shown on Section 2.1.2, this kind of controller increases the output impedance at the selected frequencies and improves the steady-state response of the system. However, the resonant controller is more complex and demands an increased execution time when compared to the PI controller. To determine this difference, a simple experiment is conducted. It consists in setting an output port of the DSP to *high* just before the calculations of the control algorithm begin and setting it back to *low* when they are finished. By measuring the duration of the time that the signal stays in *high* with an oscilloscope, it is possible to determine the execution time of the control algorithm. Because of how the code was implemented in this work, the time measurement also included the ADC conversion time and processing of input variables. To eliminate this interference, the first measurement was done with the PWM turned off, as shown on Figure 6.26. This way, the control algorithm is not calculated and all the execution time is due to the input sampling.

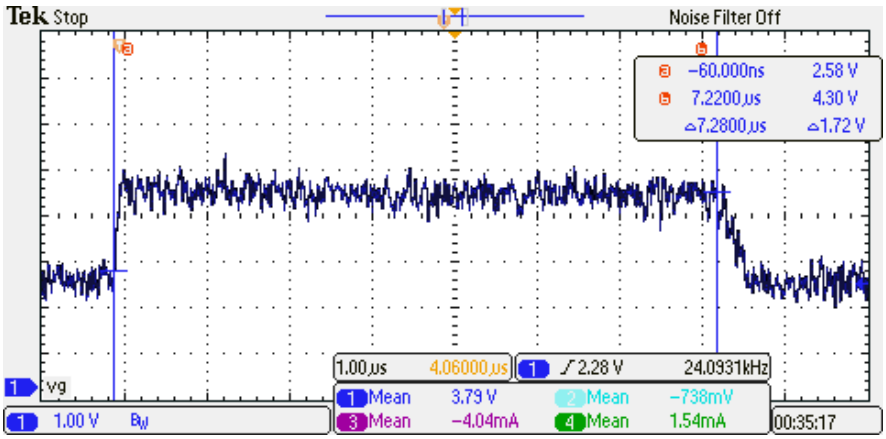

Figure 6.26. Time spent for ADC conversion and input processing ($7.28\mu s$)

Next, the execution time of each type of controller is determined by repeating the test with the PWM turned on, so that the control strategy algorithm is run. The time difference between each test and the reference case corresponds to the execution time of the control strategy. For simplicity and fairness of comparison, in this test, the PI-R controller acts only on the fundamental frequency (60 Hz) and, therefore, does not control any harmonics. Table 6.5 summarizes the obtained results.

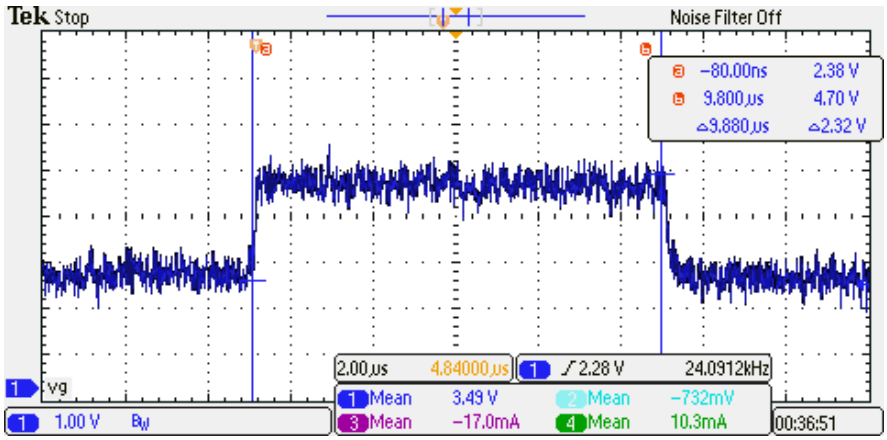

Figure 6.27. Execution time with PI controller (9.88μs)

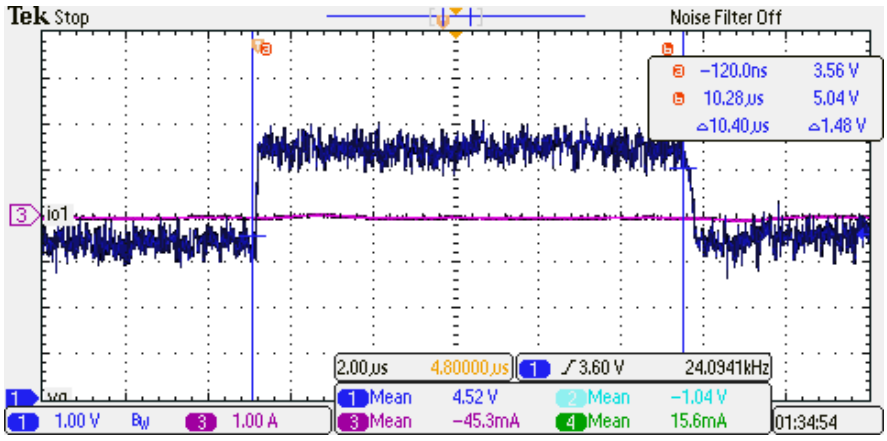

Figure 6.28. Execution time with PI-R controller (10.40μs)

Table 6.5. Execution time comparison

Test	Execution time (μs)
Measurements only	7.28
PI control	9.88
PI-R control	10.40

These results show that the time used by the DSP to calculate the control algorithm was equal to 2.6 μs for the PI controller and 2.96 μs for the PI-R controller. This represents an increase of approximately 14% and is significant since the implemented resonant controller acts only on the fundamental. When multiple harmonic frequencies are implemented, the execution time increases as well.

6.2.3.2 Power and harmonics control

It was shown that the PI-R controller demands a higher processing time than the PI controller. Depending on the DSP used and on the number of controlled harmonic components, the execution time may be too large. Therefore, it is of interest to avoid the use of resonant controllers to increase the available interruption time.

As the current control loop of the strategy proposed in this work consists only of a PI controller, its calculation does not need a large amount of processing time. However, the signal generation algorithm, shown on Figure 4.3, has slow dynamics and occupies more processing time, as shown on Figure 6.29, where it can be seen that this algorithm has a very high computational cost, demanding approximately 19μs to be executed, which is almost twice the time of a PI controller.

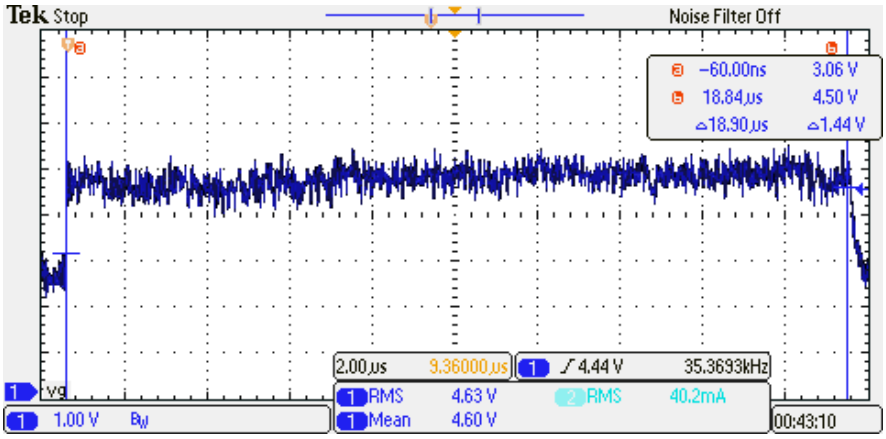

Figure 6.29. Execution time of the signal generating algorithm.

At first, this may seem like a problem that makes the proposed strategy unfeasible. However, the signal generation algorithm does not have to be executed in the same frequency as the current control. Instead, can be executed in the main program loop, outside of the PWM interruption, without significant losses.

Therefore, this is not a problem for the proposed strategy. On the contrary, it is an advantage, since it allows the calculation of the power control loop and harmonic compensation to be executed at a slower rate, while achieving a similar result to the

resonant controller regarding the steady-state response and Dynamic Stiffness of the system. This significantly reduces the burden placed on the processing system, as it reduces the number of calculations that need to be executed inside the PWM interruption and, thus, reduces the need for a high-end DSP.

Chapter 7

Conclusion

This work described an output impedance-based control for current-driven grid-connected converters, in which a double-loop control structure is used. The inner control loop consists of a PI controller that drives a sinusoidal PWM to regulate the output filter current. It was demonstrated that, due to the PI controller limitations, when the system is connected to the grid, there is an inherent error on the output that is caused by a disturbance current driven by the grid voltage and may be determined by calculating the inverter Dynamic Stiffness, which, in this particular case, is equal to the Output Impedance (Z_{out}). The current control loop model was discussed in detail and the mathematical models of its components were derived. Then, expressions were derived to analytically calculate the value of Z_{out}, which were then validated by both simulation and experiments. Chapter 3 also presented procedures for designing the output LC filter and tuning the PI current controller.

To compensate the circulation of disturbance currents, an outer power and harmonics control loop was proposed. Chapter 4 showed that this loop operates by manipulating the current reference to make it equal to the opposite of the disturbance current, compensated by the closed-loop current control dynamics. Simulations showed that this reference can also be accurately determined by analytical calculation if all parameters of the system are known. An in-depth study of the proposed control loop was also shown in this chapter and each one of its components were analyzed and had their mathematical models presented.

To validate the theoretical derivation, an experimental setup was designed and the Microgrids Laboratory was built at the Engineering School of the Minas Gerais Federal University. The tests conducted in this setup validated the operation of the proposed strategy, demonstrated that the derived model is accurate and the system behaves as expected. In Chapter 6 it was explained that the power control in the

proposed strategy can be executed outside of the interruption that is synchronized with the PWM, reducing the burden on the DSP and presenting an advantage over the resonant controller regarding the execution time and implementation.

Simultaneously, the Double Converter Configuration was presented and similar studies were carried in relation to it. It was demonstrated that the Dynamic Stiffness of the supplementary converter is higher than the main one, showing that a higher sampling frequency and larger bandwidth controllers directly translate in greater resiliency to external disturbances. This configuration, although impractical to implement in practice with the current available resources, was evaluated through extensive and detailed simulation.

In conclusion, it can be stated that this work accomplished the objectives laid out in Chapter 1. The digital control strategy presented in Chapter 4 in fact achieves a high output impedance at the selected frequencies. The setup developed at the Microgrids laboratory allowed its implementation in the PHB-1500-NS inverter and experimental validation. Since a comprehensive study of the current-driven grid connected converter was carried out, this work contributes to further understanding the behaviour of distributed generators and presents a viable strategy for the implementation of smart multi-functional converters in microgrids.

7.1 Future Work

Regarding the experimental setup developed for testing the grid-connected converter, more functionalities must be programmed into its firmware, to make it compliant to the current grid standards and enable the implementation of ancillary functions.

Concerning the Microgrids Laboratory, there is still work to be done in the built setup. Although functional, its operation is still complicated and requires a great amount of familiarity to be operated. It can be greatly simplified, in order to facilitate the use of the converter for future researchers and students.

Finally, regarding the theoretical aspect, it is worth investigating the possibility of applying the proposed strategy to three-phase grid-connected converters. Although the application of the Conservative Power Theory and PLL systems is straightforward for three-phase systems, the generation of the sinusoidal signals and current reference must be further studied. In this case, there is also the possibility of adapting the proposed strategy to compensate for unbalances that may be present in the three-phase system. Additionally, it is still necessary to derive an expression to explicit the output impedance of the Dual converter when the power and harmonics control loops

are implemented on the supplementary unit. It is expected that this expression has a frequency response similar to the one shown in Figure 4.10 regarding the grid-connected converter. However, in this case, since the supplementary converter does not regulate the active power, it is speculated that the in-phase and quadrature components must be analyzed separately.

7.2 Related Publications

H. P. Couto, D. I. Brandao, S. M. Silva, T. Caldognetto, S. Sanchez, E. Tedeschi, "Selective Output Impedance Based Control for Grid-Connected Inverters", *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019

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Appendix A

Microgrids Laboratory Rectifying and Protection Box

The Rectifying and Protection Box was designed and built for application at the Microgrids Laboratory to allow safe and easy operation of the grid-connected converter. Its electrical diagram in shown in Figure A.1. It is composed of a commercial three-phase rectifier module (model Semikron SKD 25/08) that connected to the inverter DC-link either directly or through a power resistor. The use of the power resistor provides additional protection to the circuit, as it can limit the current if a short-circuit may occur, and can be used to simulate the V-I curve of PV modules and provide a way to test MPPT algorithms. Semiconductor-grade fuses are used, even though they cannot reliably prevent damage to the H-bridge IGBTs, to provide additional protection for the equipment and personnel.

The external interface of the box is shown on Figure A.2. The uppermost button in the emergency shutdown. Below it are the two signaling LEDs, that indicate that the system is turned on and that the power resistor is bypassed, respectively. Then, there is the turn off button and, finally, the turn on and resistor bypass buttons. The box circuitry is shown on Figure A.3, in which the fuses, circuit breaker and contactors can be seen.

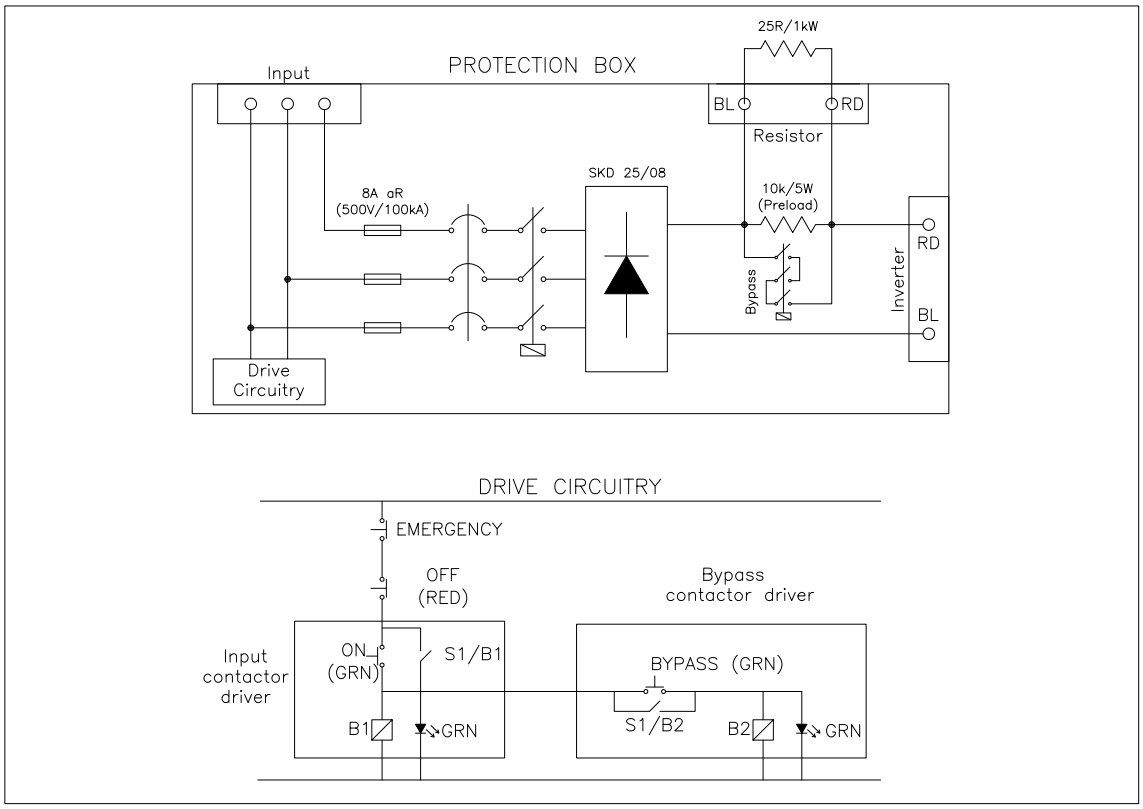

Figure A.1. Protection box electrical diagram.

Figure A.2. Interface of the rectifying and protection box.

Figure A.3. Rectifying and protection box circuitry.