Allan Fagner Cupertino

Modeling, Design and Fault-Tolerant Strategies for Modular Multilevel Cascaded Converter-based STATCOMs

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Orientador: Prof. Dr. Seleme Isaac Seleme Júnior

Coorientador: Prof. Dr. Heverton Augusto Pereira

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MODELING, DESIGN AND FAULT-TOLERANT STRATEGIES FOR MODULAR MULTILEVEL CASCADED CONVERTER-BASED STATCOMS

Allan Fagner Cupertino

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DELT (UFMG)

Aos meus pais Waldery e Erciléia
Ao meu irmão Marcel
À minha família
Aos meus mentores e amigos
Aos meus "braços direitos" do GESEP.

Agradecimentos

In order to reach all important people, initially I will write some words in Portuguese.

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Now, I need to write some words in English.

One year in Denmark was really important for me. This was my first opportunity living abroad. This experience was challenging, scaring and amazing $\cdots$ amazing because I met fantastic and flower people there.

First of all, I would like to thank prof. Remus Teodorescu for the opportunity to work in his research group. I learned a lot with you, not only about MMC, but also about life and music. I would like to thank my lab colleagues, Songda, Yu Jin and Qian for all

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"Prediction is very difficult, especially if it's about the future."

Niels Bohr

"[...] before the time runs out there's somewhere to run... Wake up!"

Foo Fighters
Run

"[...] hoje eu tenho que esperar, mas meu dia vai chegar... O mundo dá voltas!"

CPM 22
O Mundo dá Voltas

Resumo

Compensadores Estáticos Síncronos (do inglês, *Static Synchronous Compensators* – STATCOMs) têm um papel fundamental no controle de potência reativa no sistema elétrico de potência. O cenário atual é caracterizado por uma elevada penetração de usinas eólicas e solares, o que pode resultar em redes elétricas com baixo nível de curto-circuito. Portanto, o suporte de tensão durante condições desbalanceadas é exigido pelos códigos de rede modernos. Estes são fatores importantes que motivam o desenvolvimento de STATCOMs com capacidade de injeção de corrente de sequência positiva e negativa. Além disso, os custos operacionais associados as perdas de potência e a manutenção são fatores que afetam diretamente a relação custo-benefício dos STATCOMs. A família dos conversores modulares multinível em cascata (do inglês, *Modular Multilevel Cascaded Converter* – MMCC) apresentam diversas vantagens, dentre as quais podem-se citar: alta eficiência, baixa distorção harmônica, além de uma inerente tolerância a falhas. Devido a estas características, a família MMCC apresenta opções de topologias interessantes para a construção de STATCOMs. Contudo, existem na literatura poucos trabalhos discutindo a modelagem, projeto e estratégias de tolerância a falhas para MMCC-STATCOMs. Esta tese de doutorado pretende preencher esta lacuna através das seguintes contribuições: (i) comparação e seleção da topologia MMCC mais adequada para a construção de um STATCOM; (ii) proposta de uma metodologia de projeto baseada na relação de compromisso entre custo e confiabilidade; (iii) análise comparativa de estratégias de redundância com a finalidade de definir a abordagem mais adequada para um MMCC-STATCOM; (iv) modelo analítico para cálculo da fronteira entre a região linear e a sobremodulação; (v) discussão da redundância inerente a estrutura do MMCC-STATCOM na região de sobremodulação. Todas os resultados e conclusões são baseados em modelos analíticos e simulações desenvolvidas nos "softwares" MATLAB® e PLECS®. O estudo de caso consiste em um STATCOM de 17 MVA / 13,8 kV. Os resultados mostram que a topologia *double-star chopper cell* (DSCC-MMCC) é a mais indicada para a construção de um STATCOM quando compensação de correntes de sequência negativa é considerada. Além disso, para o estudo de caso adotado, dispositivos de potência com tensão de bloqueio de 3,3 kV podem atingir os requisitos de confiabilidade com o menor custo. Outrossim, a análise comparativa das estratégias de redundância indica que os esquemas de redundância fria e redundância inerente resultam em maiores eficiências e menores custos. Finalmente, quando a operação na região de sobremodulação é levada em consideração, um projeto com menor custo inicial pode ser alcançado.

Palavras-chaves: STATCOM; Conversor Modular Multinível em Cascata; Eficiência; Confiabilidade; Tolerância a falhas.

Abstract

Static Synchronous Compensators (STATCOMs) play an important role in the power system regarding the reactive power control. The current power system scenario is characterized by a high penetration of solar and wind power plants, which can lead to weak grid conditions. Therefore, voltage support during unbalanced conditions is required by the modern grid codes. These factors can be considered important drivers of the development of STATCOMs with positive and negative sequence current injection capability. Moreover, the operational costs due to power losses and non-scheduled maintenance are factors which directly affects the benefit-cost ratio of the modern STATCOMs. The modular multilevel cascaded converters (MMCC) family presents several advantages, such as: high efficiency, low harmonic distortion and inherent fault tolerance. These features make the MMCC family members interesting candidates for STATCOM realization. Nevertheless, there is a lack in the technical literature regarding the modeling, design and fault-tolerant strategies for MMCC based STATCOMs. This Ph.D dissertation aims to fill this void, providing the following contributions: (i) Comparison and selection of the most suitable MMCC topology for STATCOM realization; (ii) Proposal of a reliability-oriented design for MMCC based STATCOMs using the trade-off between cost and reliability; (iii) Benchmarking of redundancy strategies to define the most suitable fault-tolerant scheme; (iv) Methodology to analytically compute the boundary between linear and overmodulation region for a MMCC; (v) Discussion of the MMCC inherent redundancy in the overmodulation region. All the conclusions are supported by analytical and simulation models developed in the softwares MATLAB® and PLECS®. The case study is based on a 17 MVA/13.8 kV MMCC based STATCOM. The results show the double-star chopper cell topology (DSCC-MMCC) as an interesting candidate for STATCOM realization. Moreover, for the adopted case study, power devices with 3.3 kV blocking voltage can reach the reliability requirements with the lowest cost. Additionally, the redundancy strategies benchmarking indicates the cold redundancy and inherent redundancy schemes as the most interesting in terms of converter efficiency and cost. Finally, a cost-effective design can be obtained when the operation in the overmodulation region is taken into account.

Keywords: STATCOM; Modular Multilevel Cascaded Converter; Efficiency; Reliability; Fault tolerance;.

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List of abbreviations and acronyms

ABB	Asea Brown Boveri (Swedish-Swiss multinational corporation)
ac	Alternating current
AlN	Aluminum Nitride
AlSiC	Aluminum Silicon Carbide
ANPC	Active Neutral Point Clamped
APLC	Active Power Line Conditioner
ATB	Average Tolerance Band
BESS	Battery Energy Storage Systems
CAPEX	Capital Expenditure
CDF	Cumulative Density Function
COBEP	Brazilian Power Electronics Conference (*Conferência Brasileira de Eletrônica de Potência*)
CPD	Custom Power Device
CTB	Cell Tolerance Band
dc	Direct current
DCMC	Diode Clamped Multilevel Converter
DFR	Design for Reliability
DSBC	Double-Star Bridge Cell
DSCC	Double-Star Chopper Cell
DSOGI-PNSE	Positive and Negative Sequence Extractor based on the Double Second-Order Generalized Integrator
DTC	Direct Torque Control
DVR	Dynamic Voltage Restorer
D-STATCOM	Distribution Static Synchronous Compensator

FACTS	Flexible ac transmission systems
FC	Flying Capacitor
FCMC	Flying Capacitor Multilevel Converter
FEM	Finite Element Method
GaN	Gallium Nitride
GE	General Electric
GESEP	Power Electronics and Power Systems UFV laboratory (*Gerência de Especialistas em Sistemas Elétricos de Potência*)
GTO	Gate Turn-Off Thyristors
HVDC	High-Voltage Direct Current
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristors
iGSE	Improved Generalized Steinmetz Equation Method
Induscon	IEEE/IAS International Conference on Industry Applications
IPFC	Interline Power Flow Controller
LC	Life Consumption
LVRT	Low-Voltage Ride-Through
MAF	Moving Average Filter
Matlab	Matrix Laboratory
MCIA	Mission Critical Industrial Applications
MMC	Modular Multilevel Converter
MMCC	Modular Multilevel Cascaded Converter
MTTF	Mean Time to Failure
MV	Medium Voltage
NLC	Nearest Level Control

NPC	Neutral Point Clamped
OCFM	Open-Circuit Failure Mode
OPEX	Operational Expenditure
OR	Inherent Redundancy in Overmodulation Region
PCC	Point of Common Coupling
PDF	Probability Density Function
PIM	Plastic IGBT Module
Ph.D	Philosophiae Doctor
PLECS	Piecewise Linear Electrical Circuit Simulation
POF	Physics-of-Failure
PPI	Press-pack IGBT
PR	Proportional Resonant
PS-PWM	Phase-Shifted Pulse-Width Modulation
pu	Per unit
PV	Photovoltaic
PWM	Pulse-Width Modulation
RAC	Redundancy based on Additional Cells
RACO	Optimized Redundancy based on Additional Cells
rms	Root Mean Square
RSC	Redundancy based on Spare Cells
RXPE	Rongxin Power Electronics
SCFM	Short-Circuit Failure Mode
SDBC	Single-Delta Bridge Cell
SiC	Silicon Carbide
SOC	State of Charge
SR	Standard Redundancy operation

SSBC	Single-Star Bridge Cell
SSC	Static Series Compensator
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
STC	Static Transfer Switch
SVC	Static Var Compensator
SVR	Static Voltage Regulator
TB	Tolerance Band
TCSC	Thyristor controlled Series Capacitor
THD	Total Harmonic Distortion
TSO	Transmission System Operator
UFMG	Federal University of Minas Gerais (*Universidade Federal de Minas Gerais*)
UFV	Federal University of Viçosa (*Universidade Federal de Viçosa*)
UPFC	Unified Power Flow Controller
UPQC	Unified Power Quality Conditioner
VSC	Voltage Source Converter

List of symbols

Here is a list of the mathematical typography and notation used throughout this Thesis. Most are referenced on first use and are standard in the literature, still they are collected here for easy reference.

A_h	Heatsink surface area
A_p	Area product of the inductors
B_x	Time at which x percent of devices fail
C_{h-a}	Heatsink-to-ambient thermal capacitance
C_{h-f}	Heatsink-to-fluid thermal capacitance
C_Δ	Cell capacitance for SDBC-MMCC
C_{2Y}	Cell capacitance for DSCC-MMCC
C_1, C_2, ... C_{18}	Case studies evaluated in Chapter 4
c_h	Heatsink material specific heat capacity
D_1	Bottom anti-parallel diode of the chopper cell
D_2	Top anti-parallel diode of the chopper cell
d_h	Heatsink thickness
E_c	Converter energy consumption
$E_{c_{10}}$	Converter energy consumption in 10 years
E_{dc}	Error in dc-link voltage
E_Δ	Energy storage in the converter for SDBC-MMCC
E_{2Y}	Energy storage in the converter for DSCC-MMCC
e_{cl}	Instantaneous energy variation in the converter clusters
e_u	Instantaneous energy variation in the converter upper arms
F	Number of failures

$F_{arm}(x)$	Arm-level unreliability function
$F_{cell}(x)$	Cell-level unreliability function
$F_{conv}(x)$	Converter-level unreliability function
$F_{D1}(x)$	Diode D_1 unreliability function
$F_{D2}(x)$	Diode D_2 unreliability function
$F_{S1}(x)$	IGBT S_1 unreliability function
$F_{S2}(x)$	IGBT S_2 unreliability function
$F(x)$	Unreliability function
f_c	Carrier frequency
f_{ma}	Moving average filter frequency
f_n	Grid frequency
f_r	Redundancy factor
f_s	Sampling frequency
f_{us}	Semiconductor utilization factor
$f_{us,0}$	Initial semiconductor utilization factor
$f_{us,f}$	Final semiconductor utilization factor
f_1	NLC-CTB important frequency 1
f_2	NLC-CTB important frequency 2
$f(x)$	Failure probability density function
h_c	Fluid flow convection coefficient
$\widehat{I}^+$	Amplitude of positive sequence grid current component
$\widehat{I}^-$	Amplitude of negative sequence grid current component
$\widehat{I}_g$	Amplitude of the grid current component
$\widehat{I}^z$	Amplitude of circulating current for SDBC-MMCC
$\widehat{I}_n$	Converter rated peak current
I_{svc}	Semiconductors rated current

i_{cl}	Current in a cluster (used in equations valid for the three phases)
i_g	Grid current (used in equations valid for the three phases)
$i_{g,\alpha\beta}$	Grid current in stationary reference frame
$i^-_{g,\alpha\beta}$	Negative sequence current in stationary reference frame
$i^*_{g,\alpha\beta}$	Grid current reference in stationary reference frame
i_l	Current in lower arm (used in equations valid for the three phases)
i_u	Current in upper arm (used in equations valid for the three phases)
$i_{u,rms}$	Rms value of arm current
i_z	Circulating current
$i_{t,i}$	Current used by the individual balancing control loop (corresponding cluster current for SDBC-MMCC and corresponding arm current for DSCC-MMCC)
K_c	Ration between the cell capacitance value
K_e	Ratio between the energy storage requirements
K_I	Ratio between the peak current
K_{mag}	Cost of the magnetic devices
K_N	Ratio between the number of cells
K_o	Price per kilowatt-hour
k_b	Proportional gain for individual balancing control
k_u	Perceptual increase in the utilization factor
k_v	Voltage unbalance factor
k_+	Droop gain for positive sequence
k_-	Droop gain for negative sequence
L_{arm}	Arm inductance
L_{cl}	Cluster inductance
L_g	Equivalent grid inductance
$MTTF$	Mean time to failure

m	Converter modulation index
m_b	Modulation index in the boundary between the linear and overmodulation region
m_b	Maximum modulation index
N	Number of cells per arm/cluster (used when the diagram is valid for N_{2Y} and N_{Δ}
N_f	Number of cycles to failure
N_{mag}	Number of inductors
N_s	Total number of semiconductors
N_T	Total number of cells ($6N_{2Y}$ for DSCC-MMCC and $3N_{\Delta}$ for SDBC-MMCC)
N_{Δ}	Number of cells per cluster for SDBC-MMCC
N_{2Y}	Number of cells per arm for DSCC-MMCC
$N(t)$	Number of surviving devices at time t
n_i	Number of cycles counted by Rainflow algorihm
n_u	Insertion index in upper arm
n_l	Insertion index in lower arm
P	Instantaneous active power reference
P^*	Instantaneous active power reference
P_{losses}	Power losses in one IGBT module
P_L	Sum of the power losses in all semiconductor devices in the converter
P_{sw}	Converter rated switching power
p_{cl}	Instantaneous active power delivered by a cluster
$\bar{p}_{cl}$	Average component of instantaneous active power delivered by a cluster
$\tilde{p}_{cl}$	Oscillating component of instantaneous active power delivered by a cluster
$\bar{p}_g$	Average component of instantaneous active power exchanged with the grid

$\tilde{p}_g$	Oscillating component of instantaneous active power exchanged with the grid
Q	Instantaneous reactive power
Q^*	Instantaneous active power reference
R_{arm}	Arm inductor resistance
R_b	Bleeder resistor
R_{cl}	Cluster inductor resistance
R_{f-a}	Fluid-to-ambient thermal resistance
R_g	Equivalent grid resistance
R_{h-a}	Heatsink-to-ambient thermal resistance
R_{h-f}	Heatsink-to-fluid thermal resistance
$R_{thermal}$	Power module thermal resistance
$R(t)$	Reliability function
S_n	Converter rated power
S_T	Bypass switch (used for fault tolerance)
S_1	Bottom IGBT of the chopper cell
S_2	Top IGBT of the chopper cell
T_c	Case temperature
T_d	Dead-time
T_h	Heatsink temperature
T_j	Junction temperature
$T_{[j,c],m}$	Mean junction/case temperature
$T_{[j,c],max}$	Maximum junction/case temperature
$T_{[j,c],min}$	Minimum junction/case temperature
$t_{on[j,c]}$	Junction/case heating time
t	Time

U_x	Unreliability level
$\widehat{V}^+$	Amplitude of positive sequence grid voltage component (phase-to-neutral)
$\widehat{V}^-$	Amplitude of negative sequence grid voltage component (phase-to-neutral)
V_g	Line-to-line converter output voltage rms value
V_s	Line-to-line converter output voltage rms value
$\widehat{V}_{s,max}$	Maximum value of the phase-to-neutral converter voltage in the linear region of the modulator
V_{svc}	Semiconductor blocking voltage capability
v_{avg}	Average capacitor voltages (all cells)
v^*_{avg}	Reference value for average capacitor voltages
v^*_b	Individual voltage reference
v^*_c	Cell capacitor voltage reference
v_{ce}	On-state voltage drop in the semiconductor device
v_{cl}	Voltage synthesized by a cluster (used in equations valid for the three phases)
$\bar{v}_{cl}$	Average capacitor voltages (per cluster)
$v_{c,i}$	Cell capacitor voltage
$v_{cf,i}$	Filtered cell capacitor voltage
v^{Σ}_{cu}	Sum of capacitor voltages in upper arm
v^{Σ}_{cl}	Sum of capacitor voltages in upper arm
$\tilde{v}^{\Sigma}_{cu}$	Estimation of the sum of capacitor voltages in upper arm
$\tilde{v}^{\Sigma}_{cl}$	Estimation of the sum of capacitor voltages in lower arm
v_{dc}	Converter (effective) dc-link voltage
$v_{dc,min}$	Minimum required dc-link voltage for operation in the linear region of the modulator
$v_{dc,2Y}$	Dc-link voltage for DSCC-MMCC

$v_{dc,\Delta}$	Effective dc-link voltage for SDBC-MMCC
v_g	Phase-to-neutral grid voltage
$v^+_{g,\alpha\beta}$	Positive sequence voltage in stationary reference frame
$v^-_{g,\alpha\beta}$	Negative sequence voltage in stationary reference frame
$v_{g,\alpha\beta}$	Grid voltage in stationary reference frame
v_l	Voltage synthesized by lower arm (used in equations valid for the three phases)
v_s	Converter phase-to-neutral output voltage (drives i_g)
v^*_s	Converter phase-to-neutral output voltage reference
v_u	Voltage synthesized by upper arm (used in equations valid for the three phases)
v_z	Converter internal voltage (drives i_z)
v^*_z	Converter internal voltage reference
W_{2Y}	Energy storage requirements for DSCC-MMCC
W_Δ	Energy storage requirements for DSCC-MMCC
x_{arm}	Per unit equivalent arm reactance
x_{eq}	Per unit equivalent output reactance
x_g	Per unit output reactance
Z_{j-c}	Junction-to-case thermal impedance
Z_{c-h}	Case-to-heatsink thermal impedance
Z_{h-a}	Heatsink-to-ambient thermal impedance
α	Maximum current rise rate
β	Shape parameter of Weibull distribution
γ	Angular displacement among upper an lower arm carriers for DSCC-MMCC
Δi_z	Maximum peak to peak ripple in circulating current
$\Delta k(\%)$	Perceptual variation in the cost

$\Delta P_L(\%)$	Perceptual variation in the power losses
$\Delta T_{[j,c]}$	Junction/case cycle amplitude
ΔV_g	Maximum variation assumed in the grid voltage
Δx_{eq}	Maximum variation assumed in the output reactance
δ^+	Positive sequence voltage angle
δ^-	Negative sequence voltage angle
η	Scale parameter of Weibull distribution
θ_v	Phase angle displacement of a three-phase system
θ_c^i	Angular displacement of the carriers for SDBC-MMCC
$\theta_{c,l}^i$	Angular displacement of the lower arm carriers for DSCC-MMCC
$\theta_{c,u}^i$	Angular displacement of the upper arm carriers for DSCC-MMCC
κ_h	Thermal conductivity of the heatsink material
$\lambda(t)$	Failure rate
Λ_{2Y}	Modulator gain for DSCC-MMCC
Λ_Δ	Modulator gain for SDBC-MMCC
μ	Mean value of normal distribution
φ^+	Positive sequence current angle
φ^-	Negative sequence current angle
ρ	Heatsink material density
σ	Standard deviation of normal distribution
ω_n	Grid angular frequency

Superscripts

$+$	Positive sequence system
$-$	Negative sequence system
$*$	Reference value
$'$	Equivalent static value

Subscripts

u	Upper arm (used in equations valid for the three phases)
l	Lower arm (used in equations valid for the three phases)
cl	Cluster (used in equations valid for the three phases)
$,a$	phase A
$,b$	phase B
$,c$	Phase C
$,ab$	Cluster connected to phases A and B
$,bc$	Cluster connected to phases B and C
$,ca$	Cluster connected to phases C and A
j,c	Valid for both junction and case temperatures
$\alpha\beta$	Variable in stationary reference frame
$+$	Positive sequence system
$-$	Negative sequence system

Contents

1 Introduction

1.1 Context and Relevance

Power systems are very complex structures with time varying parameters and configurations, which require careful operation, design and planning. The modern power system scenario related with an increasing power demand, interconnected transmission systems, nonlinear loads and large renewable power plants implies in strict requirements of reliability, operation and control. These factors affect the electrical grid at the transmission and distribution levels.

At the transmission level, the flexible ac transmission systems (FACTS) and high voltage direct current (HVDC) systems have been developed to improve the transmission capabilities over long distances, so as to enhance the performance of weak grids and prevent outages (Shahgholian et al., 2010; Behrouzian, 2016). According to Sze et al. (2003), the FACTS controllers can be classified into four categories:

- series controllers: the device introduces voltage in series with the line. The thyristor controlled series capacitor (TCSC) and static synchronous series compensator (SSSC) are included in this category;
- shunt controllers: the device injects current into the system at the point of common coupling. The static var compensator (SVC) and static synchronous compensator (STATCOM) are included in this category;
- combined series shunt controllers: the device combines separate shunt and series controllers. The unified power flow controller (UPFC) is a example of this category;
- combined series-series controllers: the device combines separate series controllers. The interline power flow controller (IPFC) is an example of this category.

At the distribution level, the custom power devices (CPD) are employed. According to the IEEE P1409 Guideline (IEEE, 2012), CPDs are active power electronic devices in medium voltage distribution systems for the purpose of supplying a level of power quality required by electric power customers. The CPDs can be classified into two categories (Moghbel et al., 2018):

- category 1: CPDs protecting the electric grid from the load by injecting reactive power and compensating harmonics. Examples include SVC, D-STATCOM (distribution

STATCOM), unified power quality conditioner (UPQC) and active power line conditioner (APLC).

- category 2: CPDs protecting the load from the source by mitigating voltage interruptions such as voltage sags and swells. Examples include static transfer switch (STS), static series compensator (SSC) and static voltage regulator (SVR) as well as D-STATCOM and dynamic voltage restorer (DVR) with energy storage.

In the current power system scenario, shunt-connected FACTS and CPDs practically dominate the market, since series-connected devices present some drawbacks in the protection structures (Behrouzian, 2016; Shahgholian et al., 2010). When reactive power compensators are considered, two power conversion technologies are employed: thyristor-based structures, as in SVCs, and voltage source converters (VSC)-based structures, as in STATCOMs. The STATCOMs present a behavior analogous to that of the traditional synchronous compensators. Nevertheless, the STATCOM presents a fast dynamic response, since it has no mechanical inertia. Therefore, this device can support the power system during fast transients. Additionally, compared to SVCs, STATCOMs present higher power density, higher efficiency and does not contribute to short-circuit currents (Chakraborty et al., 2012).

According to Hingorani, Gyugyi and El-Hawary (2000), the thyristor-based structures are preferred in installations with high power ratings (in the range of hundreds of Mvar). Nevertheless, VSC technology presents several advantages, including (Behrouzian, 2016):

- fast response;
- good dynamics for various operating conditions (e.g., different short-circuit strength);
- higher power density;
- low harmonic distortion in the injected/absorbed currents;
- higher operation flexibility.

The main drawback of STATCOMs is the cost, since STATCOMs are more expensive than SVC systems. Nevertheless, the technical benefits and recent advances in power converters technology are slowly leading to the use of VSC topologies instead of thyristor-based systems, similarly to the modernization process observed in HVDC systems (Behrouzian, 2016).

STATCOMs have been employed at different power and voltage levels, as presented in Fig. 1. Regarding the applications, at the distribution voltage level, STATCOMs are

mainly used to mitigate power quality problems (voltage transients, flicker, harmonics, etc) (Reed; Takeda; Iyoda, 1999). At the transmission and sub-transmission voltage level, STATCOMs have been employed for voltage control and power oscillations damping (Hingorani; Gyugyi; El-Hawary, 2000; Zhang; Rehtanz; Pal, 2006). In large renewable energy power plants, STATCOMs have been employed for fast reactive power compensation and grid code fulfillment (Behrouzian, 2016). The inclusion of energy storage systems in STATCOMs has been discussed in recent years, providing inertia and frequency regulation functions to solar and wind power plants (Chakraborty et al., 2012).

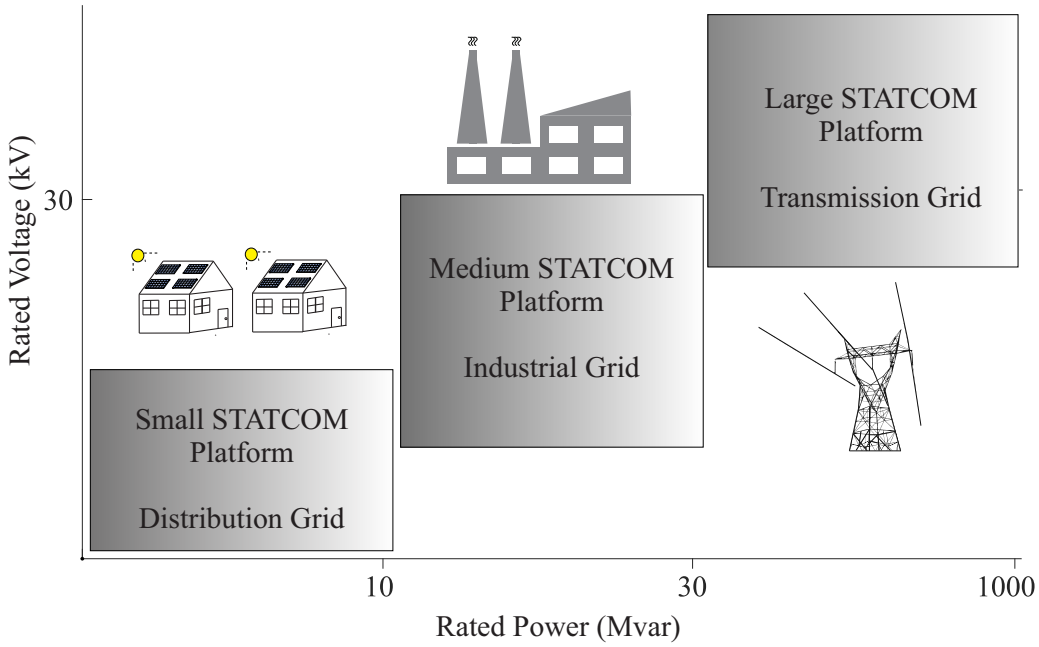

Figure 1 – Different power and voltage levels of STATCOMs. *Adapted from* Shahnia, Rajakaruna and Ghosh (2015).

1.2 STATCOM Realization

The most recent research efforts in STATCOM realization are targeted at finding efficient and reliable topologies for medium and high voltage systems (Muñoz et al., 2014). The major task is to design a converter topology which must reach higher power and voltage levels with standard rated semiconductor switches (Valdez-Fernández et al., 2013; Fujii; Schwarzer; De Doncker, 2005). The main scientific contributions (patents and journal papers) to the development of multilevel converters are summarized in the timeline presented in Fig. 2. This section aims to describe some of these developments.

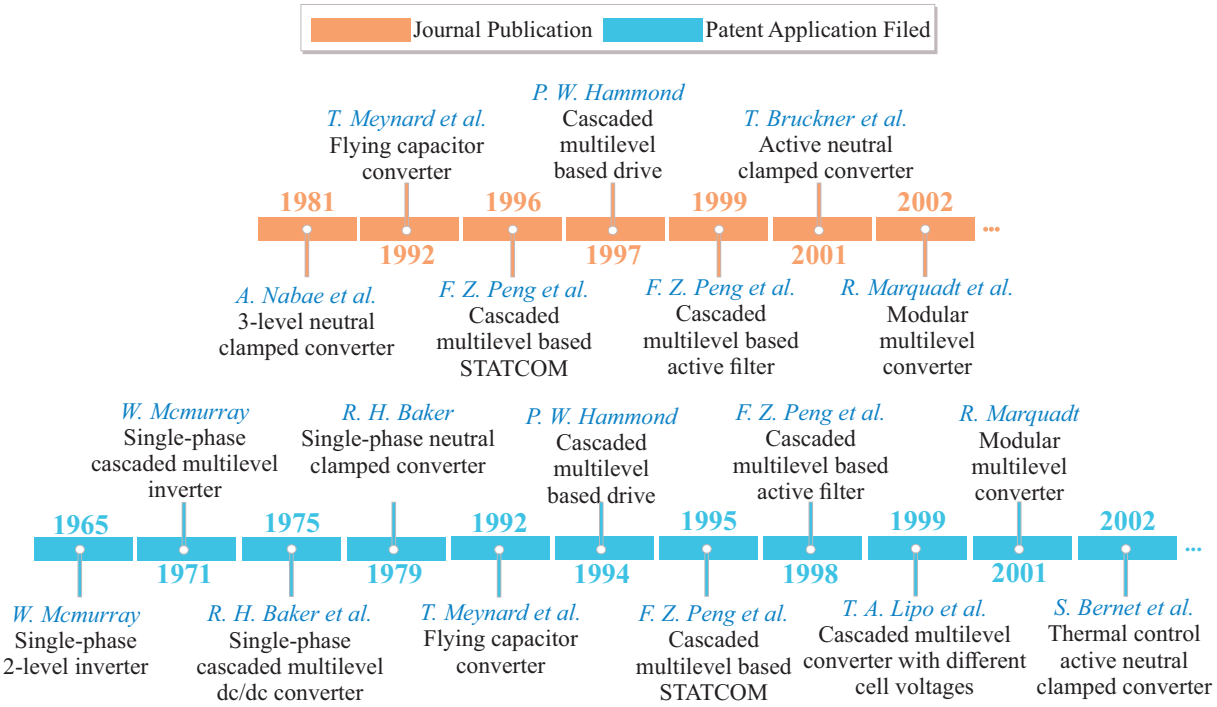

Figure 2 – Summary of the main contributions in the development of multilevel converters.

1.2.1 Two-level and Early Multilevel Converters

The two-level converter schematic is presented in Fig. 3. This topology is currently preferred in low voltage applications. Nevertheless, when the voltage level increases to some kilovolts, this topology is less useful, due to the voltage blocking capability of power devices available in the market. Even considering the new silicon carbide (SiC) and gallium nitride (GaN) devices, the field application of this topology is limited, to some extent. A step-up transformer (T_x) is usually connected to the converter output when it is used in STATCOMs to allow the connection to medium voltage (MV) (Shahnia; Rajakaruna; Ghosh, 2015). However, this transformer makes the STATCOM bulky and heavy, and affects the overall efficiency (Hagiwara; Akagi, 2009).

The series connection of power devices is another solution to increase the voltage rating, as shown in Fig. 4. This approach results in an equivalent valve able to block higher voltage. Nevertheless, this solution is very complex due to some practical issues, such as voltage equalization between the series switches and fault-tolerant operation (Shammas; Withanage; Chamund, 2006; Fortes; Mendes; Cortizo, 2019). Snubber structures are usually required to compensate the voltage unbalance leading to slower switching times and higher switching losses (Shahnia; Rajakaruna; Ghosh, 2015). Press-pack devices are employed to increase the fault tolerance capacity because they present a guaranteed short-circuit failure mode (Ladoux; Serbia; Carroll, 2015). Since this technology is not commercialized by many manufactures due some patents (Bijlenga et al., 2004; Gunturi; Schneider, 2006),

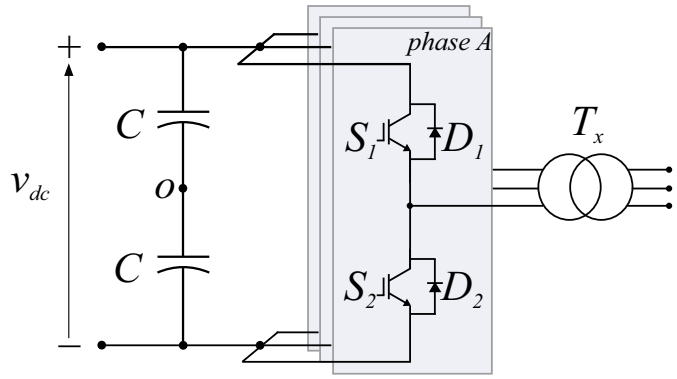

Figure 3 – Schematic of the three-phase two-level voltage source converter with step-up transformer.

the series connection becomes costly and, to some extent unsuitable.

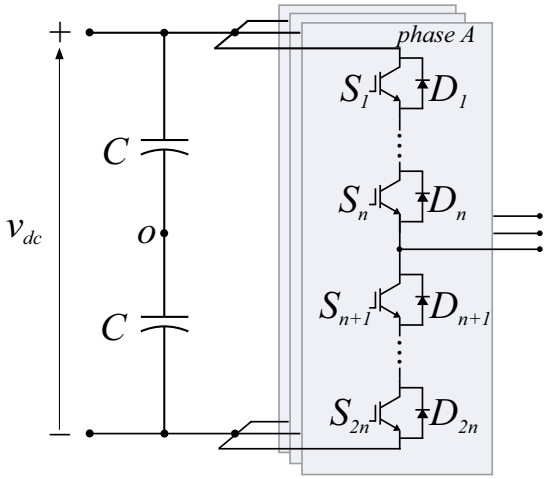

Figure 4 – Schematic of the three-phase two-level voltage source converter with series connection of semiconductor switches.

Fujii, Schwarzer and De Doncker (2005) and Fujii et al. (2007) discuss the use of multi-stage transformer topologies. However, this transformer tends to be expensive, inefficient besides rendering the converter bulky and heavy (Hagiwara; Akagi, 2009). According to Fang Zheng Peng et al. (1996), field experiences show the transformer can produce about 50 % of the total power losses, occupy up to 40 % of the system space and hamper the control due to inrush currents and saturation effects.

In face of the step-up transformer drawbacks, multilevel converter topologies can be an alternative. The multilevel converter concept employs medium voltage devices to obtain a converter with higher voltage capability. In this case, the multilevel approach can employ mature semiconductor technology to reach medium and high voltage levels (Franquelo et al., 2008). The multilevel topologies present various advantages, such as lower common mode voltage, lower voltage stresses on semiconductors and lower harmonic contents in

the output voltage and current, if compared to the two level topologies. Furthermore, the multilevel converters tend to present better power density, since the output filters can be reduced or removed in some cases. Finally, multilevel converters present lower voltage steps (dv/dt), which reduces stresses in the insulation of any equipment connected at the converter output (Franquelo et al., 2008).

The diode clamped multilevel converter (DCMC), initially proposed by Nabae, Takahashi and Akagi (1981) in a three-level version was the first multilevel converter employed in large scale. The DCMC topology is presented in Fig. 5. The three-level DCMC, commonly called neutral point clamped (NPC) converter, was adopted by many manufactures and widely employed in medium voltage electric drives, railway traction systems and wind turbines.

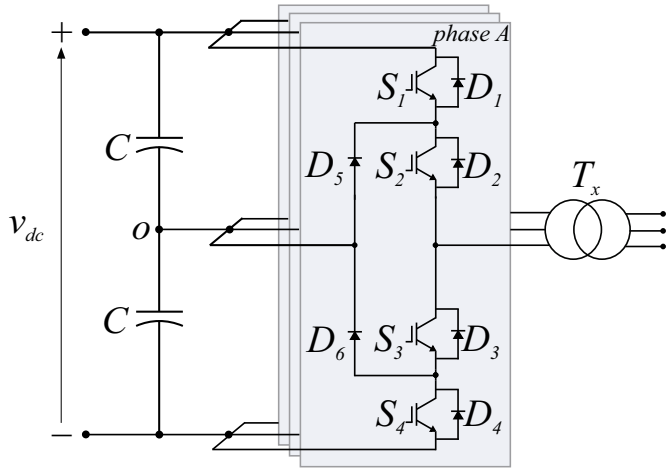

Figure 5 – Schematic of the three-phase three-level diode clamped multilevel converter (NPC converter) with step-up transformer.

Nevertheless, clamp diodes must block more than two times the IGBT voltage when more than three voltage levels are necessary (Fujii; Schwarzer; De Doncker, 2005; Hagiwara; Akagi, 2009), requiring series connection. Yuan and Barbi (2000) proposed an alternative DCMC topology to solve this particular issue, which avoids the series association of the clamping diodes. DCMC topology also presents issues related to the dc-link control. The inherent imbalance in the series connected dc capacitors requires an external balancing circuit (Hagiwara; Akagi, 2009). Finally, when the number of levels increases, the number of interconnections between the converter switches also increases and the mechanical design of the converter becomes more complex (Sharifabadi et al., 2016). In view of the aforementioned tasks, in practical applications, the number of levels is usually limited to five or seven levels (Fujii; Schwarzer; De Doncker, 2005; Hagiwara; Akagi, 2009). Therefore, the field of application is limited to the medium voltage range.

Other inherent problem in the NPC topology is the thermal unbalance between the outer and inner devices of each phase. Therefore, the power devices must be overrated

or different switches must be employed (Ma; Blaabjerg, 2016). The active neutral point clamped (ANPC) converter was introduced to solve this particular issue (Bruckner; Bemet, 2001). The three-level version of ANPC topology is presented in Fig. 6. The clamping diodes are replaced by active switches. In this case, the zero voltage state can be implemented with more possibilities, which results in a thermal balance between the converter switches (Bruckner; Bemet, 2001; Bijlenga, 2002). Due to these advantages, ANPC converters were applied to HVDC projects (Sharifabadi et al., 2016).

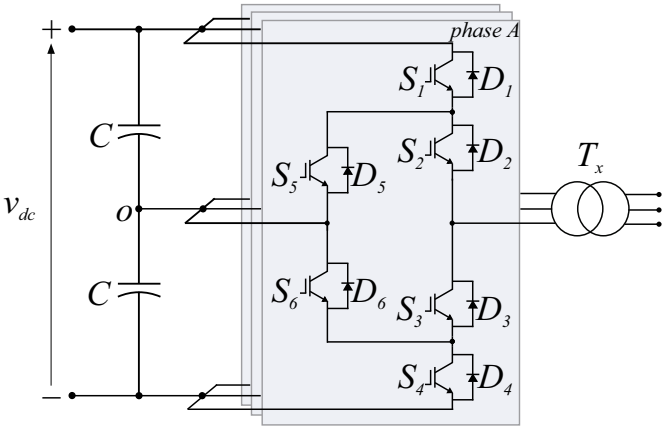

Figure 6 – Schematic of the three-phase three-level active neutral point clamped converter (ANPC converter) with step-up transformer.

The flying capacitor multilevel converter (FCMC) was introduced by Meynard and Foch (1992). The FCMC is a further topology, in which the clamping capacitors are used to step down the dc-link voltage. The three-level version of FCMC is presented in Fig. 7. When an adequate modulation strategy is employed, the clamping capacitors are automatically balanced (Fujii; Schwarzer; De Doncker, 2005; Meynard et al., 2002). According to Sharifabadi et al. (2016) and Akagi (2017), Alstom Power and Grid, presently a part of General Electric (GE), employs four-level FCMC in medium voltage drives.

However, when the number of levels increase, the voltages at the flying capacitors differ. Therefore, capacitors with different ratings must be employed. Additionally, when the number of levels increases, the flying capacitors must be connected to different points, creating meshes. This fact results in a complex mechanical design still related to the insulation between the points at different potentials (Sharifabadi et al., 2016). Finally, the high cost of flying capacitors at low carrier frequencies (lower than 1 kHz) is another disadvantage of this topology (Fujii; Schwarzer; De Doncker, 2005).

Among the solutions previously presented, early STATCOMs were often implemented with two-level converters or three-level NPC converters with step-up transformers (Mori et al., 1993; Schauder et al., 1995). When high power levels were required, the parallel connection of several converters was usually employed. Three-level NPC converters with series connected devices were also used to avoid parallel connection

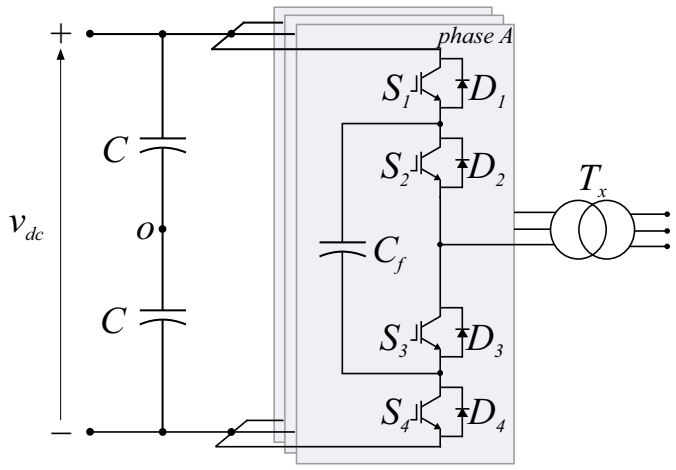

Figure 7 – Schematic of the three-phase three-level flying capacitor multilevel converter (FCMC) with step-up transformer.

of converters (Larsson; Grunbaum; Ratering-Schnitzler, 2000). However, this solution includes all issues associated with the series connection of semiconductor devices.

1.2.2 Cascaded Multilevel Converters

Cascaded multilevel converters are a more straightforward way to provide a voltage source converter for STATCOM realization. This topology is based on cascaded connection of cells (or submodules) to build up the output voltage. Some manufacturers (e.g. Alstom and ABB) often refer to this configuration as chain-link multilevel converter. The connection can be implemented in star or delta, as presented in Fig. 8 (a) and (b), respectively. The advantages of this topology include:

- low switching frequency can be employed, which results in high efficiency;
- a higher number of voltage levels can be reached, since no clamping components are necessary;
- design flexibility, since the voltage rating can be increased by installing more cells;
- fault-tolerance and redundancy are inherent to the converter structure.

Cascaded connection of bridge cells date back to the 1970s for single-phase systems (Mcmurray, 1971; Baker; Bannister, 1975). However, a three-phase STATCOM based on star-connected cascaded multilevel converter was proposed in 1996 by Fang Zheng Peng et al. (1996). This converter was first adopted by Alstom for high power STATCOMs, and gate turn-off (GTO) thyristors were initially employed in the full bridges (Ainsworth et al., 1998). Nowadays, this concept is widespread in the industry and most products are

based on IGBTs (Insulated Gate Bipolar Transistors) or press-pack IGCTs (Integrated Gate-Commutated Thyristors) (Sharifabadi et al., 2016).

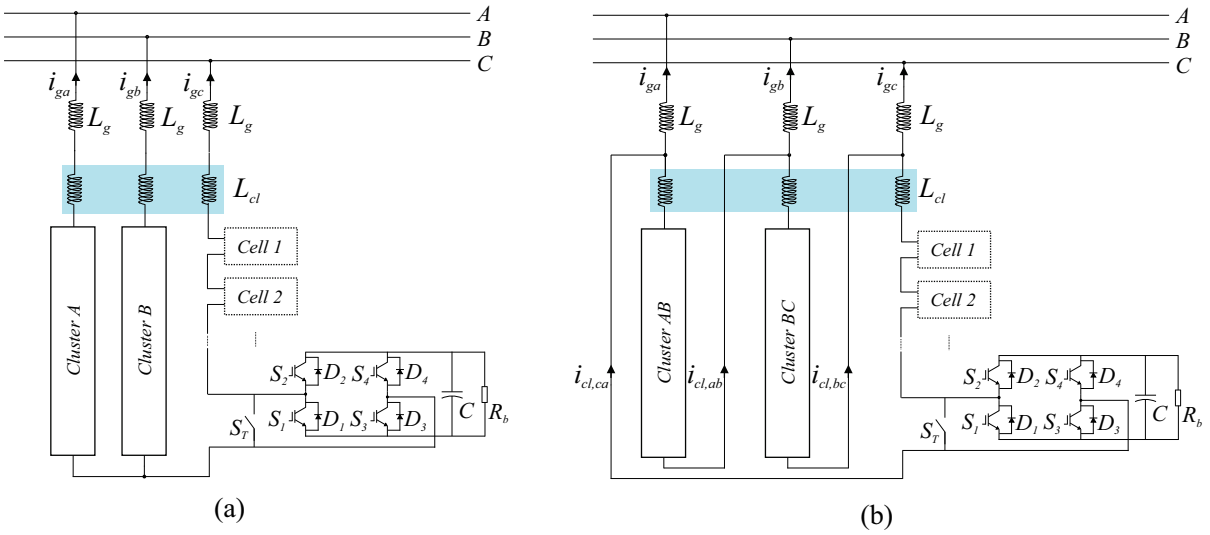

Figure 8 – Schematic of the cascaded multilevel converter: (a) star-connected cascaded multilevel converter; (b) delta-connected cascaded multilevel converter.

In 2001, the patent of the modular multilevel converter (MMC) was filed (Marquadt, 2001). This topology is illustrated in Fig. 9. The MMC presents a dc-link, as observed in traditional 2-level converters, while maintaining the important benefits of cascaded multilevel converters (Marquardt; Lesnicar; Hildinger, 2002; Baroni, 2012). This fact resulted in the commercial success of this topology for HVDC systems.

Indeed, the term "modular multilevel converter" does not refer to a specific circuit topology, since different cell topologies can be employed. Furthermore, the modular multilevel converter (Fig. 9) is based on the same concept of the cascaded multilevel converters (Fig. 8). Basically, the topologies differ only in the circuit configuration. Therefore, the inclusion of both topologies in the same family of multilevel converters is reasonable.

In view of this nomenclature problem, Akagi (2011) proposes the term modular multilevel cascaded converter (MMCC) for this family of converters. Moreover, the different circuit configurations are named as follows:

- topology of Fig. 8 (a): SSBC-MMCC (Single Star Bridge Cell MMCC);
- topology of Fig. 8 (b): SDBC-MMCC (Single Delta Bridge Cell MMCC);
- topology of Fig. 9 (a): DSCC-MMCC (Double Star Chopper Cell MMCC);
- topology of Fig. 9 (b): DSBC-MMCC (Double Star Bridge Cell MMCC).

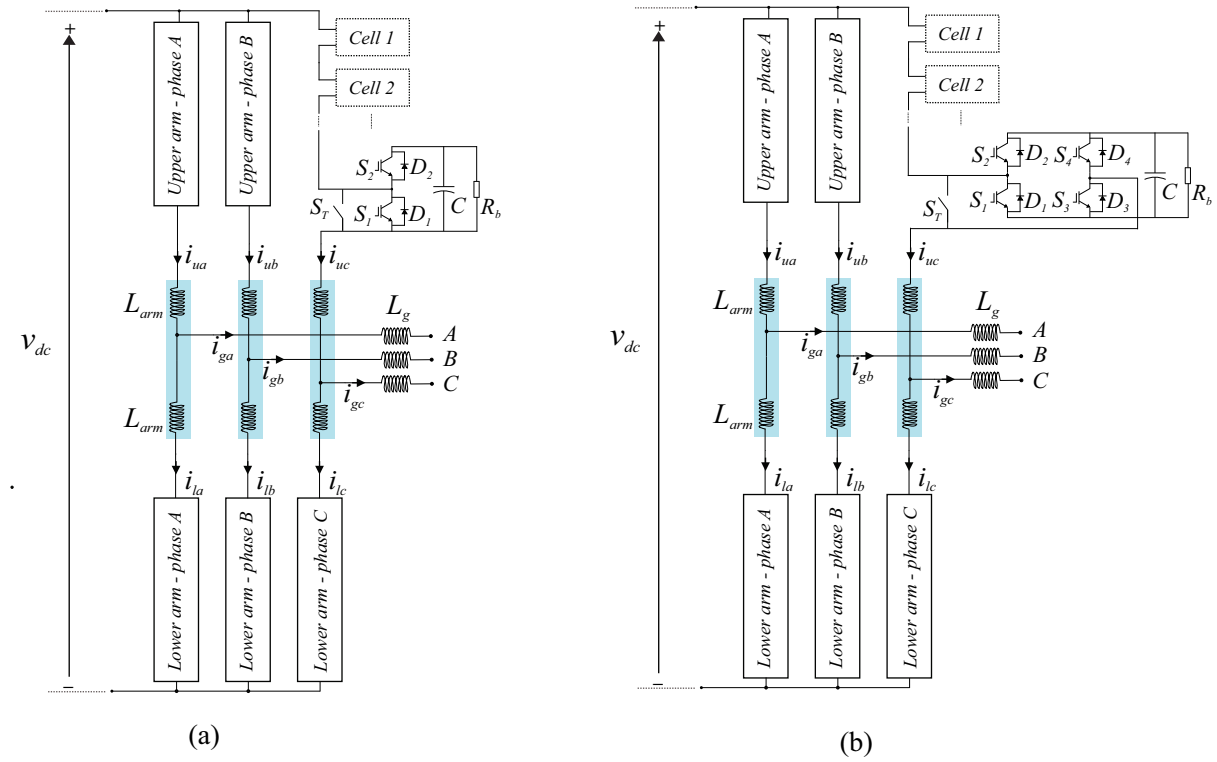

Figure 9 – Schematic of the three-phase modular multilevel converter: (a) topology based on chopper cells; (b) topology based on bridge cells.

Table 1 presents some STATCOMs currently available in the market. As observed, the major companies in the sector of STATCOMs provide some solutions based on cascaded multilevel converters. In fact, STATCOMs are always in hot stand-by and the operational costs due to energy losses are very important (ABB, 2013). Since cascaded multilevel converters are featured of high efficiency, such kind of converter is widespread in industry. Furthermore, according to Siemens (2019), Siemens installed the 100th STATCOM based on cascaded multilevel converter in July 2019, reaching two thirds of the multilevel STATCOMs installed worldwide.

Table 1 – Overview of some STATCOMs commercially available.

Trade Mark	Converter Configuration	Manufacturer
VArPro^{TM}	Two-level VSC + Transformer	ABB
PCS 100	Two-level VSC + Transformer	ABB
PCS 6000	Three-level VSC (NPC) + Transformer	ABB
MaxSine	Three-level VSC (NPC) + Transformer	GE
SVC Light	SDBC-MMCC	ABB
GE-STATCOM	SDBC-MMCC	GE
SVC Plus	SDBC-MMCC	Siemens

1.3 Purpose and Contributions

1.3.1 Motivations

STATCOMs play an important role in power system in terms of grid voltage regulation and reactive power control, since they can provide precise and flexible control to mitigate disturbances and effectively improve grid power quality. The latest research efforts have focused on STATCOMs for medium and high voltage systems. Currently, three main factors are driving researchers in STATCOMs.

First of all, operational cost reduction is very important for STATCOMs. This factor drives research that seek to increase STATCOM efficiency (Hassanpoor; Norrga; Nami, 2015; Wu et al., 2015; Li et al., 2018; Yang et al., 2018) and converter reliability (Tu; Yang; Wang, 2019; Hui et al., 2019; Zheng et al., 2019). Accordingly, different modulation strategies, redundancy schemes and design approaches have been proposed.

Secondly, the modern grid codes for renewable energy power plants require negative sequence support during voltage sags (VDE, 2015), which means the STATCOM converter must provide negative sequence injection (Wijnhoven et al., 2014). According to Behrouzian and Bongiorno (2017), SSBC-MMCC and SDBC-MMCC present a singular operation point during unbalanced conditions. If the system reaches this point, the converter will probably trip from the electrical grid and it will not be able to provide voltage support (Behrouzian, 2016). Under such conditions, double star topologies may be proposed to deal with this issue.

Finally, in recent years, the increasing demand for inertia and frequency regulation has favored the development of research targeted at the integration of energy storage systems and STATCOMs (Bharadwaj; Maiti, 2017; Jeon et al., 2019; Feng et al., 2018). Under such conditions, the same converter can be employed to provide voltage regulation, low voltage ride through, inertia and frequency regulation services (Bharadwaj; Maiti, 2017).

As observed, the MMCC family has many advantages in comparison with the traditional multilevel converters (diode clamp multilevel and flying capacitor multilevel converters) for STATCOM realization. Finally, most publications on double star topologies are focused on HVDC systems and, most recently, industrial electric drive systems. However, there are some important issues related to the control and hardware implementation of an MMCC-based STATCOM:

- the cells must operate with balanced voltages during normal operation, negative sequence compensation, unbalanced voltage sags and other disturbances. Therefore, control strategies to balance the capacitor voltages are required;

- excepting SSBC, the MMCC topologies present circulating currents. The circulating currents must be controlled to reduce power losses and provide capacitor voltages balancing;
- modulation strategies for the converter, which result in lower output current ripple or lower power losses;
- the measurement of a high number of signals (cell voltages, for example), since hundreds of cells can be employed in high voltage applications.

These issues have sparked the interest of researches in MMCC. In terms of publications, Fig. 10 presents the number of published journal papers on this topic since 2010. These data are obtained searching the term "Modular Multilevel Converter" in IEEE Xplore (IEEE, 2019) and Science Direct databases (ELSEVIER, 2019). As observed, modular multilevel converters have been widely investigated in last 5 years.

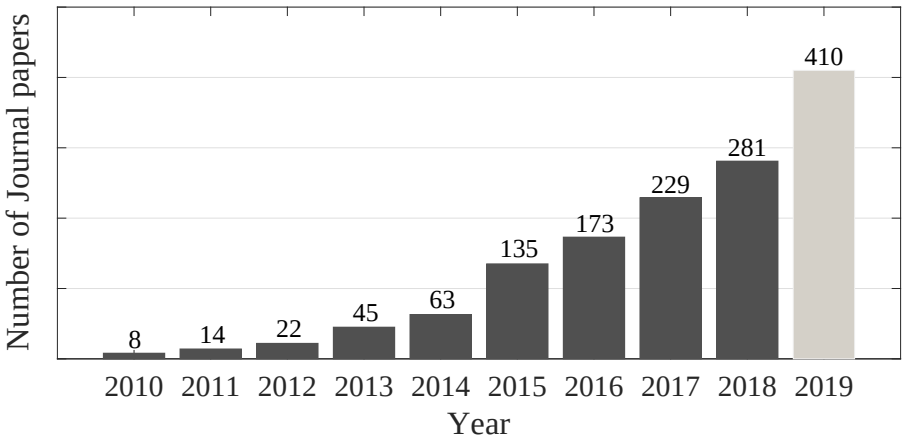

Figure 10 – Evolution of the number of published journal papers containing the term "modular multilevel converters" in IEEE Xplore and Science Direct databases (IEEE, 2019; ELSEVIER, 2019).

1.3.2 Objectives

In fact, the design and control of MMCC-based STATCOMs have important open issues, which are approached in the present Ph.D dissertation. This work aims to explore the design, operation and control of an MMCC-based STATCOM considering positive and negative sequence compensation.

Based on the general purpose, the following topics will be approached in this work.

1. *Modeling, design and comparison for MMCC-based STATCOMs*: this topic proposes a deep comparison between the MMCC topologies to choose the most suitable

topology for STATCOM realization. Analysis on the number of cells, required cell capacitances, output filter design, losses and costs are studied in the present Ph.D dissertation for both positive and negative sequence compensation, along with other particular features of STATCOMs;

2. *Reliability-Oriented Design of MMCC-based STATCOMs*: this topic proposes the selection of the semiconductor devices of an MMCC-based STATCOM using the reliability as a figure of merit. Physics-of-failure (POF) models are employed to predict the wear-out of the converter components. A decision making process is discussed to define the necessary ratings for the converter power modules to fulfill the reliability requirements;

3. *Fault-Tolerant Strategies for MMCC-based STATCOMs*: this topic proposes the study of alternatives to explore fault-tolerant strategies applied to MMCC. Two approaches are discussed and evaluated. Firstly, a benchmarking of several redundancy strategies proposed in literature is conducted. Control complexity, dynamic performance, power losses and cost are the figures of merit employed. Secondly, the inherent redundancy in the converter overmodulation region is explored to guarantee a cost-effective design for MMCC-based STATCOMs.

Regarding the comparison of MMCC topologies, the following contributions are targeted:

- comparison of topologies, considering the number of cells, effective dc-link voltage, circulating current behavior and current rating. These comparisons are supported by analytical results;
- definition and comparison of the energy storage requirements of MMCC topologies when negative sequence currents are compensated;
- evaluation of dynamic behavior, power losses and costs.

Regarding the reliability-oriented design, the following contributions are targeted:

- proposal of a reliability-oriented design based on the trade-off between cost and system-level reliability;
- discussion on the unreliability level U_x as a reliability indicator to evaluate the failure probability in the converter for a given time;
- introduction of the $U_x - cost$ map as a tool to compare different designs with respect to the reliability requirement and cost.

Then, regarding the redundancy strategy analysis, the following contributions are targeted:

- discussion of the necessary changes in the control strategy when additional cells are employed, considering phase-shift modulation;
- comparison of the dynamic performance for the redundancy strategies when both positive and negative sequences are compensated by an MMCC-based STATCOM;
- evaluation of the converter power losses when redundancy strategies are employed.

Finally, regarding the use of overmodulation as a fault-tolerant strategy, the following contributions are targeted:

- development of analytical expressions for the linear region boundary for a DSCC-MMCC;
- sensitivity analysis on the limits for the cell capacitance, grid impedance, grid voltage power factor and injected current;
- discussion on the potential for fault-tolerance in the overmodulation region.

It is important to remark that the present research has been developed in the Universidade Federal de Minas Gerais in cooperation with the Gerência de Especialistas em Sistemas Elétricos de Potência (GESEP-UFV) and the Department of Energy Technology of the Aalborg University.

1.4 Organization of this Ph.D Dissertation

This Ph.D dissertation is organized in 7 chapters, following the structure presented in Fig. 11. Chapter 1 presented the motivations and objectives of the present Ph.D dissertation. Chapter 2 contains a bibliographic review on the MMCC family. Furthermore, two topologies which are suitable for STATCOM application are selected. Chapter 3 discusses the design of MMCC-based STATCOM and presents a benchmarking of the two selected topologies. Minimum effective dc-link voltage, energy storage requirements and current ratings during positive and negative sequence compensation are approached. Chapter 4 discusses the reliability-oriented design of an MMCC. The design for reliability (DFR) is approached and the rating of the semiconductor devices is then defined. Chapter 5 presents a benchmarking redundancy strategies for an MMCC-based STATCOM. Chapter 6 discusses the boundary of the linear region and cost-effective design of MMCC-based STATCOMs considering overmodulation. Finally, chapter 7 presents the conclusions and the future developments of this work.

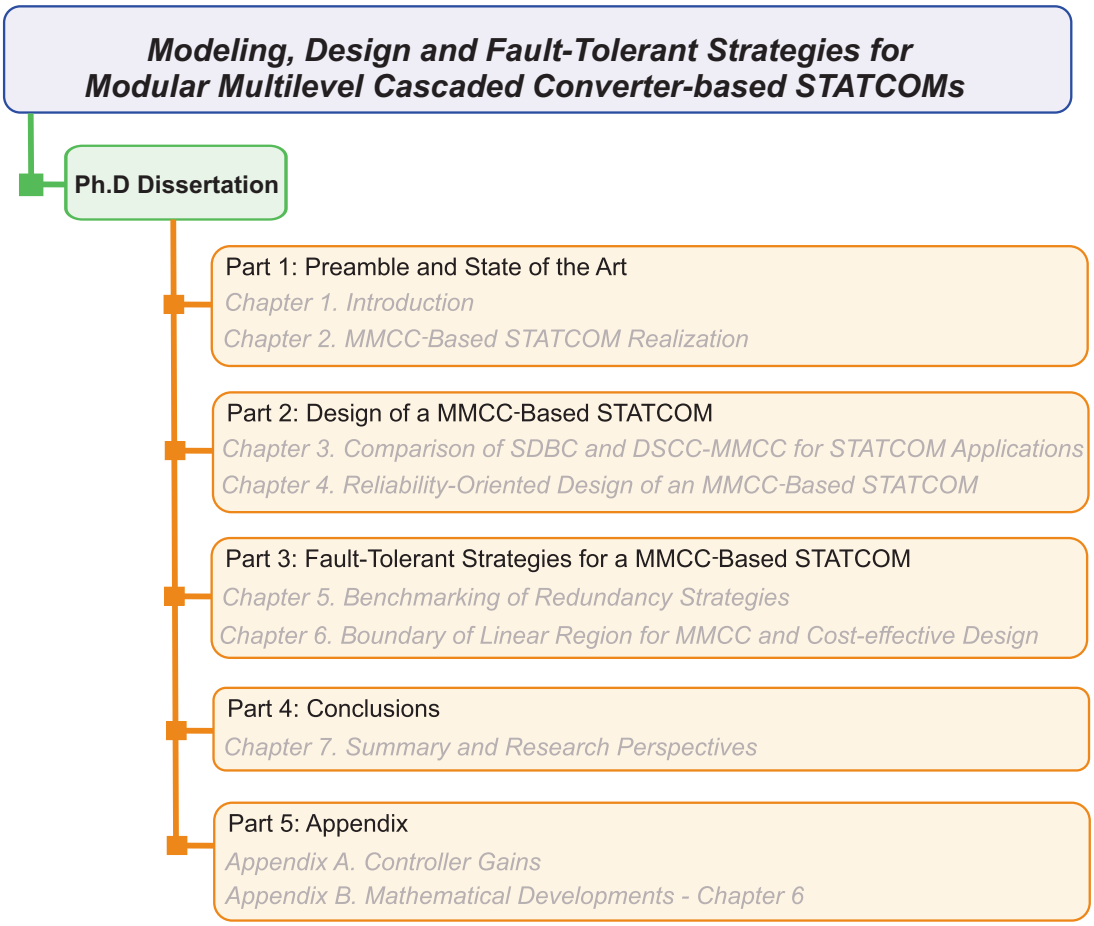

Figure 11 – Structure of the Ph.D dissertation.

1.5 List of Publications

The findings of this Ph.D project have resulted in the publication of 5 journal papers, one conference paper and one book chapter. These publications are presented as follows:

1. J. V. M. Farias, A. F. Cupertino, H. A. Pereira, S. I. S. Junior and R. Teodorescu, "On the Redundancy Strategies of Modular Multilevel Converters," in IEEE Transactions on Power Delivery, vol. 33, no. 2, pp. 851-860, April 2018. doi: 10.1109/TPWRD.2017.2713394.

2. A. F. Cupertino, J. V. Farias, H. A. Pereira, S. I. Seleme and R. Teodorescu, "DSCC-MMC STATCOM Main Circuit Parameters Design considering Positive and Negative Sequence Compensation," in Journal of Control, Automation and Electrical Systems, v. 29, p. 62-74, February 2018, doi: 10.1007/s40313-017-0349-4.

3. A. F. Cupertino, J. V. M. Farias, H. A. Pereira, S. I. Seleme and R. Teodorescu,"Comparison of DSCC and SDBC Modular Multilevel Converters for STATCOM Application During Negative Sequence Compensation," in IEEE

Transactions on Industrial Electronics, vol. 66, no. 3, pp. 2302-2312, March 2019. doi: 10.1109/TIE.2018.2811361.

4. J. V. M. Farias, A. F. Cupertino, V. De Nazareth Ferreira, H. A. Pereira, S. I. Seleme Junior and R. Teodorescu, "Reliability-Oriented Design of Modular Multilevel Converters for Medium-Voltage STATCOM," in IEEE Transactions on Industrial Electronics, *Early Access*. doi: 10.1109/TIE.2019.2937050.

5. A. F. Cupertino, H. A. Pereira, S. I. Seleme and R. Teodorescu, "On Inherent Redundancy of MMC based STATCOMs in the Overmodulation Region," in IEEE Transactions on Power Delivery, *Early Access*. doi: 10.1109/TPWRD.2019.2936784.

6. J. V. M. Farias, A. F. Cupertino, V. N. Ferreira, S. I. Seleme, H. A. Pereira and R. Teodorescu, "Design and lifetime analysis of a DSCC-MMC STATCOM," 2017 Brazilian Power Electronics Conference (COBEP), Juiz de Fora, 2017, pp. 1-6. doi: 10.1109/COBEP.2017.8257312.

7. H. A. Pereira; A. F. Cupertino; S. I. Seleme. "Basic Concepts of Modular Multilevel Converters and Applications in Medium and High Voltage Fields." In: COBEP 2017 Tutorials. 1ed.Juiz de Fora: 2017, v.1, p. 01-91. ISBN 978-1-5090-6247-8.

The author also contributed to the following journal publications in the topic of modular multilevel converters:

1. A. F. Cupertino, W. C. Amorin, H. A. Pereira, S. I. Seleme, S. Chaudhary and R. Teodorescu, "High Performance Simulation Models for ES-STATCOM based on Modular Multilevel Converters," in IEEE Transactions on Energy Conversion, *Early Access*. doi: 10.1109/TEC.2020.2967314.

2. W. C. S. Amorin, D. C. Mendonça, R. O. de Souza, A. F. Cupertino and H.A. Pereira, "Analysis of Double Star Modular Multilevel Topologies Applied in HVDC System for Grid Connection of Offshore Wind Power Plants." in Journal of Control, Automation and Electrical Systems, *Early Access*. doi: 10.1007/s40313-019-00542-2.

3. P. R. Matias Jr, J. V. M. Farias, A. F. Cupertino, H. A. Pereira, M. M. Stopa and J. T. de Resende, "Redundancy and Derating Strategies for Modular Multilevel Converter for an Electric Drive." in Journal of Control, Automation and Electrical Systems, *Early Access*. doi: 10.1007/s40313-019-00542-2.

4. J.V.M. Farias, A.F. Cupertino, V. N. Ferreira, H.A. Pereira and S. I. Seleme Jr., "Redundancy Design for Modular Multilevel Converter based STATCOMs." in Microelectronics Reliability, v. 100-101, September 2019. doi: 10.1016/j.microrel.2019.113471.

5. L. S. Xavier, W. C.S. Amorim, A. F. Cupertino, V. F. Mendes, W. C. Boaventura, H. A. Pereira. "Power Converters for Battery Energy Storage Systems Connected to Medium Voltage Systems: A Comprehensive Review." in BMC Energy, v. 1, p. 7, November 2019. doi: 10.1186/s42500-019-0006-5.

6. P. R. Matias Jr., A. F. Cupertino, G. A. Mendonça, H. A. Pereira. "On Lifetime Evaluation of Medium-Voltage Drives Based on Modular Multilevel Converter.", IET Electric Power Applications, v. 13, p. 1453-1461, October 2019. doi: 10.1049/iet-epa.2018.5897.

7. R.O. de Sousa, J.V.M. Farias, A.F. Cupertino and H.A. Pereira, "Life consumption of a MMC-STATCOM supporting wind power plants: Impact of the modulation strategies." in Microelectronics Reliability. v. 88-90, p. 1063 – 1070, September 2018. doi: 10.1016/j.microrel.2018.06.111.

8. V. N. Ferreira, A. F. Cupertino, H. A. Pereira, A. V. Rocha, S. I. Seleme and B. J. Cardoso Filho, "Design and Selection of High Reliability Converters for Mission Critical Industrial Applications: A Rolling Mill Case Study," in IEEE Transactions on Industry Applications, vol. 54, no. 5, pp. 4938-4947, Sept.-Oct. 2018. doi: 10.1109/TIA.2018.2829104.

Finally, the author also contributed to the following conference publications in the topic of modular multilevel converters:

1. R. O. Sousa, W. C. S. Amorim, D. C. Mendonça, A. F. Cupertino, L. M. F. Morais and H. A. Pereira, "Thermal Stress Evaluation of a Multifunctional Modular Multilevel Converter - STATCOM Operating as Active Filter." 5th Southern Power Electronics Conference and 15th Brazilian Power Electronics Conference (COBEP), Santos, 2019.

2. D. C. Mendonça, A. F. Cupertino, H. A. Pereira, S. I. Seleme Jr and R. Teodorescu, "Inherent Redundancy Analysis of SDBC-MMC in the Overmodulation Region." 5th Southern Power Electronics Conference and 15th Brazilian Power Electronics Conference (COBEP), Santos, 2019.

3. R. O. de Sousa, D. C. Mendonça, W. C. S. Amorim, A. F. Cupertino, H. A. Pereira and R. Teodorescu, "Comparison of Double Star Topologies of Modular Multilevel Converters in STATCOM Application." 13th IEEE/IAS International Conference on Industry Application (Induscon), São Paulo, 2018. doi: 10.1109/INDUSCON.2018.8627199.

4. R. O. de Sousa, D. C. Mendonça, W. C. S. Amorim, A. F. Cupertino, H. A. Pereira and R. Teodorescu, "Comparison of Double Star Topologies of

Modular Multilevel Converters in STATCOM Application." 13th IEEE/IAS International Conference on Industry Application (Induscon), São Paulo, 2018. doi: 10.1109/INDUSCON.2018.8627199.

5. V. N. Ferreira, A. F. Cupertino, H. A. Pereira, A. V. Rocha, S. Isaac Seleme and B. J. Cardoso, "Design of high-reliable converters for medium-voltage rolling mills systems," 2017 IEEE Industry Applications Society Annual Meeting, Cincinnati, OH, 2017, pp. 1-9. doi: 10.1109/IAS.2017.8101826.

2 MMCC-Based STATCOM Realization

This chapter aims to present the main topologies and characteristics of modular multilevel cascaded converters and their applications. Next, a discussion about the possible candidates for the realization of the MMCC-based STATCOM is presented. Two topologies of MMCC family are selected. Average dynamic models are used to describe the behavior of the topologies during unbalanced conditions. Finally, the control and modulation strategies are presented.

2.1 MMCC Family

The classification of MMCC topologies is related to the type of cell used and the circuit topology. The cells can be represented by the following circuits (Debnath et al., 2015):

- half bridge circuit or chopper cells (Marquardt; Lesnicar; Hildinger, 2002; Ahmed et al., 2014; Antonopoulos et al., 2014; Ilves et al., 2015a; Ilves et al., 2015b);
- full bridge circuit or bridge cells (Baker; Bannister, 1975; Hagiwara; Maeda; Akagi, 2012; Ota et al., 2015; Ota; Shibano; Akagi, 2015);
- clamp double circuit (Marquardt, 2010; Marquardt, 2011);
- three-level converter circuit (NPC or flying capacitor(FC)) (Solas et al., 2013a; Solas et al., 2013b);
- five-level cross-connected circuit (Nami et al., 2013).

The scheme of each cell is presented in Fig. 12. A comparison of these cells taking into account the power losses, and the dc short circuit fault handling capability is presented in Tab. 2. The chopper and bridge cells are the topologies most adopted by manufacturers (Debnath et al., 2015).

Considering only chopper and bridge cells, the topologies of modular multilevel cascaded converters can be classified into four types (Akagi, 2011):

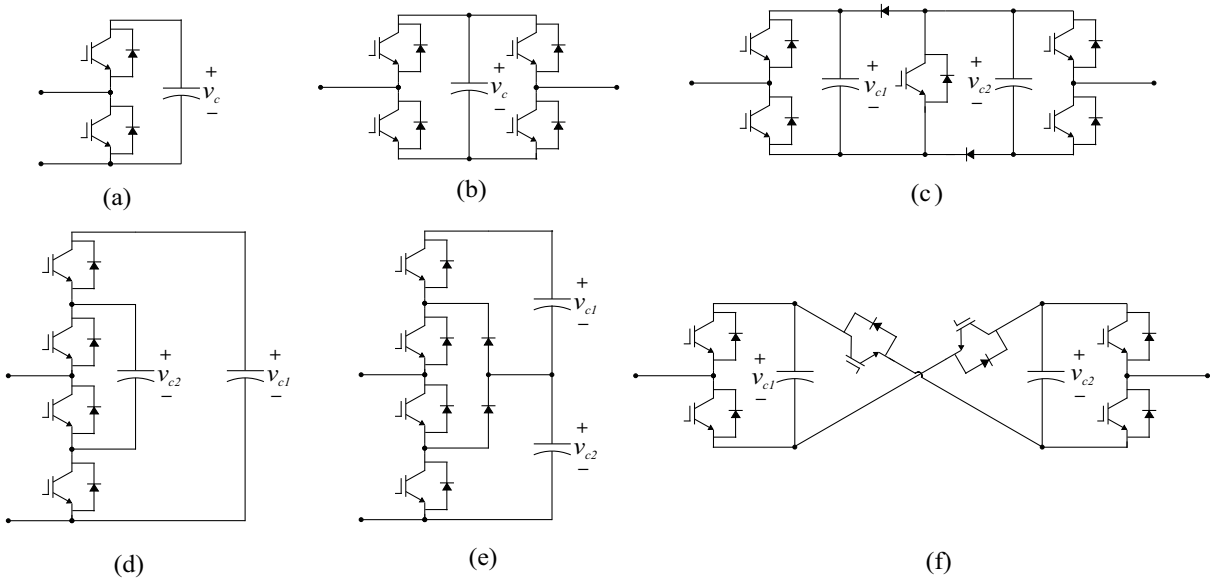

Figure 12 – Possible topologies for MMCC cells: (a) chopper cell; (b) bridge cell; (c) clamp-double cell; (d) three-level FC cell; (e) three-level NPC cell; (f) five-level cross-connected cell.

Table 2 – Comparison of various cell topologies (Debnath et al., 2015).

Topology	Dc-fault handling	Losses
Half bridge	No	Low
Full Bridge	Yes	High
Clamp double	Yes	Moderate
Three-Level FC	No	Low
Three-Level NPC	No	Moderate
Five-level cross-connected	Yes	Moderate

- SSBC-MMCC - Single-Star Bridge Cells MMCC;
- SDBC-MMCC - Single-Delta Bridge Cells MMCC;
- DSCC-MMCC - Double-Star Chopper Cells MMCC;
- DSBC-MMCC - Double-Star Bridge Cells MMCC;

SSBC-MMCC topology is presented in Fig. 13 (a). Regarding the number of power devices required to reach a given voltage level, SSBC is the most advantageous, since it employs less components. Its application to active power transfer (electric drives, photovoltaic inverters, etc) is not feasible unless galvanically isolated multiple dc voltage sources are employed (Akagi, 2011). Furthermore, this topology does not have circulating current. Therefore, the capacitor voltage balancing is based on zero sequence voltage injection (Behrouzian; Bongiorno, 2017).

This topology is suitable for battery energy storage systems (BESS). In this application, the main tasks to be performed are the state of charge (SOC) balancing control, fault tolerant control and active power control of individual cells, which are discussed by Maharjan et al. (2009), Maharjan et al. (2010), Maharjan, Yamagishi and Akagi (2012), Mathe et al. (2016). Ota et al. (2015), Ota, Shibano and Akagi (2015) and Behrouzian and Bongiorno (2017) also discuss the application for STATCOMs. SSBC-MMCC is suitable for STATCOMs only when positive sequence currents are injected. Nevertheless, the ability to control the negative sequence reactive current (necessary for flicker or unbalance compensation) is limited by the voltage rating of the converter, since it can require the injection of a zero sequence voltage equal to the phase voltage (Behrouzian; Bongiorno, 2017).

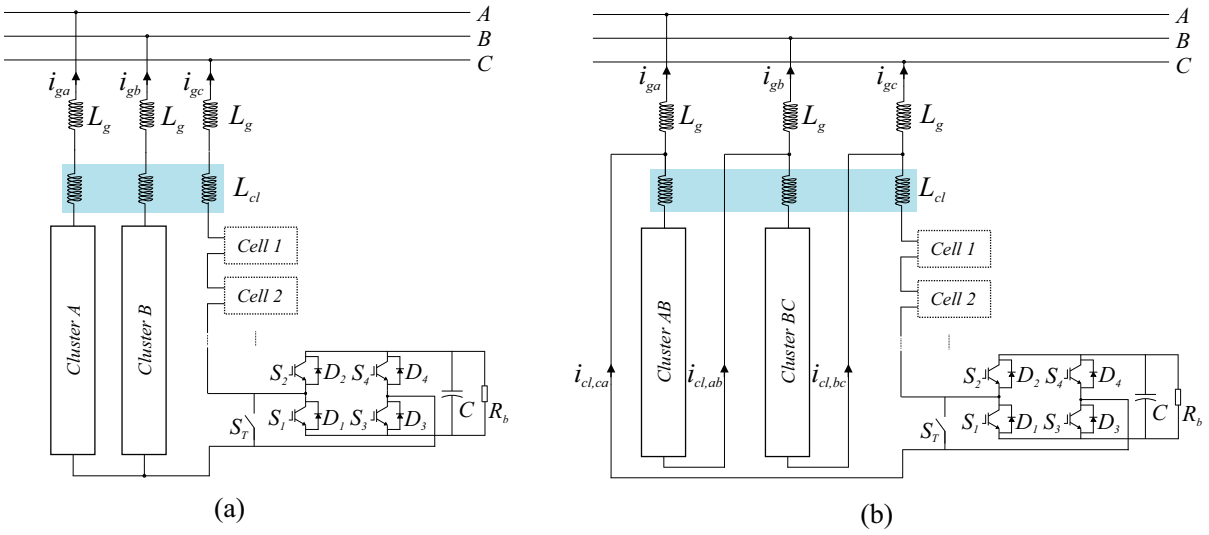

Figure 13 – Schematic of the MMCC family members (part I): (a) SSBC-MMCC; (b) SDBC-MMCC. *Remark*: L_g refers to the grid inductance and leakage inductance of the isolation transformer (when galvanic isolation is required).

SDBC-MMCC is presented in Fig. 13 (b). This topology presents a circulating current with one degree of freedom, which corresponds to the zero sequence current (Akagi, 2011). The capacitor voltage balancing is performed by the circulating current control, which provides power exchange among the clusters. Therefore, this topology is suitable for STATCOMs for flicker compensation, where both positive and negative sequence current compensations are necessary (Hagiwara; Maeda; Akagi, 2012; Behrouzian; Bongiorno, 2017). For SDBC-MMCC, the amplitude of the circulating current is proportional to the amount of negative sequence current injected by the converter. This fact must to be included in the converter design to avoid overrating (Hagiwara; Maeda; Akagi, 2012).

Nevertheless, during unbalanced voltage conditions, this topology poses some limitations. Since the circulating current presents only one degree of freedom, when the

positive and negative sequence components of the point of common coupling (PCC) voltage are equal, SDBC-MMCC cannot to perform the capacitor voltage balancing (Behrouzian; Bongiorno, 2017). Under such conditions, the SDBC-MMCC protection system will trip the converter.

Regarding the applications in electric drives, SSBC-MMCC and SDBC-MMCC require galvanically isolated sources for each converter cell. Few proposals present electric drives based on these topologies and employ batteries in each converter cell (Tolbert; Fang Zheng Peng; Habetler, 1999; Akagi, 2011). The structure proposed by Robicon Corporation (presently a part of Siemens) (Hammond, 1997) is a very successful solution. This electric drive presents a multiwinding phase-shifted line-frequency transformer which supplies diode rectifiers connected to each cell of a SSBC-MMCC. The phase-shift angles of the transformer windings are computed in order to minimize the harmonics in the current supplied by the grid. Although high power quality indexes can be reached, the transformer is very complex and nonstandard, which affects the cost and power density of the converter (Marzoughi et al., 2018).

DSCC-MMCC topology is shown in Fig. 14 (a). This topology presents a common dc-link and can be applied to HVDC transmission systems, electric drives and renewable energy conversion systems. The circulating currents present three or two degrees of freedom (if the dc-link capacitor is included or not) (Akagi, 2011). Differently from the SDBC-MMCC, the DSCC-MMCC shows no limitations during unbalanced voltage conditions.

Regarding the application to electric drives, DSCC-MMCC presents some important limitations in low speed range. Indeed, when the output frequency is small, the capacitor voltage ripples increase considerably and some strategies are required to guarantee adequate drive operation (Hagiwara; Nishimura; Akagi, 2010; Antonopoulos et al., 2014). Unfortunately, most strategies limit the maximum torque obtained in the low speed range. Therefore, this topology is more suitable for electric drives employing loads with quadratic-torque-to-speed profile, such as fans, pumps, blowers and compressors (Okazaki et al., 2017).

DSBC-MMCC topology is illustrated in Fig. 14 (b). Since this topology presents a higher number of components when compared to the other MMCC family members, its application range is more limited. Some works propose this topology for electric drives, since the ripples in the cell capacitors can be reduced (He et al., 2016; Kumar; Poddar, 2017a; Kumar; Poddar, 2017b). Moreover, DSBC-MMCC can operate as a three-to-single-phase direct frequency changer, similarly to the traditional cycloconverters based on thyristors (Akagi, 2011). Nevertheless, this topology makes it possible to obtain sinusoidal current waveforms and unitary power factor, at both sides of the converter. In HVDC systems, the use of DSBC-MMCC is interesting, since the bridge cells are able to handle dc short

circuits.

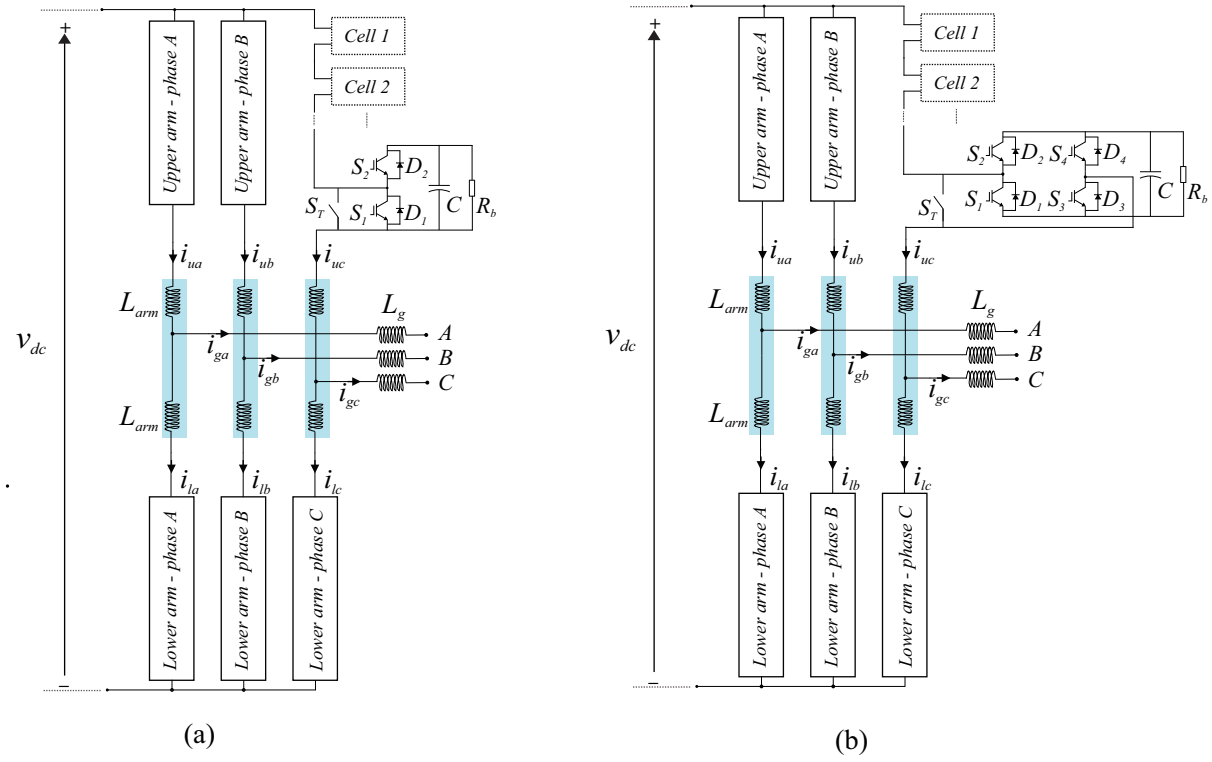

Figure 14 – Schematic of the MMCC family members (part II): (a) DSCC-MMCC; (b) DSBC-MMCC. *Remark*: L_g refers to the grid inductance and leakage inductance of the isolation transformer (when galvanic isolation is required).

At this point, an important question may be asked: which is the best MMCC topology for STATCOM application? An initial discussion on this topic is presented as follows.

Topologies with high number of components are not usually preferred, due to their complexity and cost. Therefore, as expected, DSBC-MMCC topology is unsuitable for STATCOM applications. Moreover, from the cost point of view, the SSBC-MMCC seems to be a good choice. Nevertheless, this topology presents no circulating current (Akagi, 2011). Thereby, the capacitor voltage balancing in SSBC-MMCC must be performed through zero sequence voltage. For this reason, the capacitor voltage balancing during negative sequence injection and power unbalances is limited by the voltage rating of the converter, as discussed by Sochor and Akagi (2016) and Behrouzian and Bongiorno (2017).

Additionally, Behrouzian and Bongiorno (2017) demonstrate that the SSBC-MMCCC and SDBC-MMCC topologies have a singular operation point where the capacitor voltage balancing cannot be reached. This is also observed for SSBC-MMCC, when the amplitudes of positive and negative sequence currents are equal. Regarding the SDBC-MMCC, singularity occurs when the amplitudes of positive and negative sequence

voltages are equal. It is noteworthy, in practice, that the condition of singularity for the SDBC-MMCC topology is less likely to occur than the condition for SSBC-MMCC, which contributes to the commercial success of SDBC-MMCC for STATCOM applications.

Table 3 summarizes the main characteristics of the MMCC family members. A recent benchmarking reported by reference (Tanaka et al., 2019) considers DSCC-MMCC as a very attractive solution for the next generation of STATCOMs for wind power plants. Therefore, SDBC-MMCC and DSCC-MMCC are approached in this Ph.D dissertation.

Table 3 – Summary of the main characteristics of MMCC family members.

Topology	**SSBC-MMCC**	**SDBC-MMCC**	**DSCC-MMCC**	**DSBC-MMCC**
Number of terminals	3 terminals	3 terminals	3 or 5 terminals	3 or 5 terminals
Circulating Current	No circulating current	1 degree of freedom	2 or 3 degrees of freedom	2 or 3 degrees of freedom
Singularity	Unitary current unbalance factor	Unitary voltage unbalance factor	No singularity	No singularity
STATCOM Realization	Only Positive Sequence	Positive and negative sequence compensation	Positive and negative sequence compensation	Higher losses

2.2 Steady-State Operation during Unbalanced Conditions

This section aims to analyze the SDBC-MMCC and DSCC-MMCC steady-state operation during unbalanced conditions. Therefore, the grid voltage v_g is assumed to be given by:

$$v_g = \widehat{V}^+ \cos(\omega_n t + \delta^+ + \theta_v) + \widehat{V}^- \cos(\omega_n t + \delta^- - \theta_v), \tag{2.1}$$

where $\widehat{V}^+$ and $\widehat{V}^-$ are the amplitudes of positive and negative sequence components of the line-to-neutral voltage, respectively. Additionally, δ^+ and δ^- are the positive and negative sequence voltage angles, respectively. Finally, $\theta_v \in \left\{-\frac{2\pi}{3}, 0, \frac{2\pi}{3}\right\}$ refers to the phase angle of each phase and ω_n is the nominal grid angular frequency.

Furthermore, the grid currents are assumed to be given by:

$$i_g = \widehat{I}^+ \cos(\omega_n t + \varphi^+ + \theta_v) + \widehat{I}^- \cos(\omega_n t + \varphi^- - \theta_v), \tag{2.2}$$

where $\widehat{I}^+$ and $\widehat{I}^-$ are the amplitudes of positive and negative sequence currents, respectively. Finally, φ^+ and φ^- are the positive and negative sequence current angles, respectively.

2.2.1 SDBC-MMCC during Negative Sequence Compensation

A detailed schematic of SDBC-MMCC topology, which has three clusters, is presented in Fig. 13 (b). This topology presents three clusters. The inductance L_{cl} reduces the harmonics in the circulating current (Harnefors et al., 2013; Akagi, 2011). Coupled inductors can be employed in order to increase the converter power density (Kawamura et al., 2017). The converter presents N_{Δ} cells per cluster and is connected to the main grid through a three-phase transformer represented by the inductance L_g.

Generally, there is a permanent bypass switch S_T (e.g., a vacuum contactor and a parallel connected thyristor [1]) in each cell, which bypasses it in case of failures (Gemmell et al., 2008). R_b refers to the bleeder resistor, which discharges the cell capacitor when the converter is turned off. C is the capacitance of each cell capacitor.

Assuming balanced capacitor voltages, a sufficiently high switching frequency and high number of cells, the cluster voltage v_{cl} can be considered a controlled voltage source, as presented in Fig. 15 (a). The dynamics of SDBC-MMCC can be modeled based on the two equivalent circuits shown in Fig. 15 (b) and (c). The output current dynamics per phase is given by:

$$v_s - \left(\frac{1}{3}L_{cl} + L_g\right)\frac{di_g}{dt} - \left(\frac{1}{3}R_{cl} + R_g\right)i_g = v_g, \tag{2.3}$$

where v_s is the line-to-neutral voltage synthesized by the STATCOM (also referred as *output voltage*), v_g is the grid line-to-neutral voltage, R_{cl} is the cluster inductor equivalent resistance, R_g is the transformer equivalent resistance and i_g is the grid current. The factor $\frac{1}{3}$ appears in the cluster inductance due to the $\Delta \rightarrow Y$ transformation.

On the other hand, the circulating current dynamics can be obtained based on Fig. 15 (c), as follows:

$$v_z - L_{cl}\frac{di_z}{dt} - R_{cl}i_z = 0, \tag{2.4}$$

where v_z is defined as the converter *internal voltage* (which drives the circulating current) given by:

$$v_z = \frac{1}{3}\left(v_{cl,ab} + v_{cl,bc} + v_{cl,ca}\right), \tag{2.5}$$

and i_z is defined as the converter circulating current given by:

$$i_z = \frac{1}{3}\left(i_{cl,ab} + i_{cl,bc} + i_{cl,ca}\right). \tag{2.6}$$

[1] Different implementations for the bypass structure can be adopted. This specific topic is discussed in chapter 5.

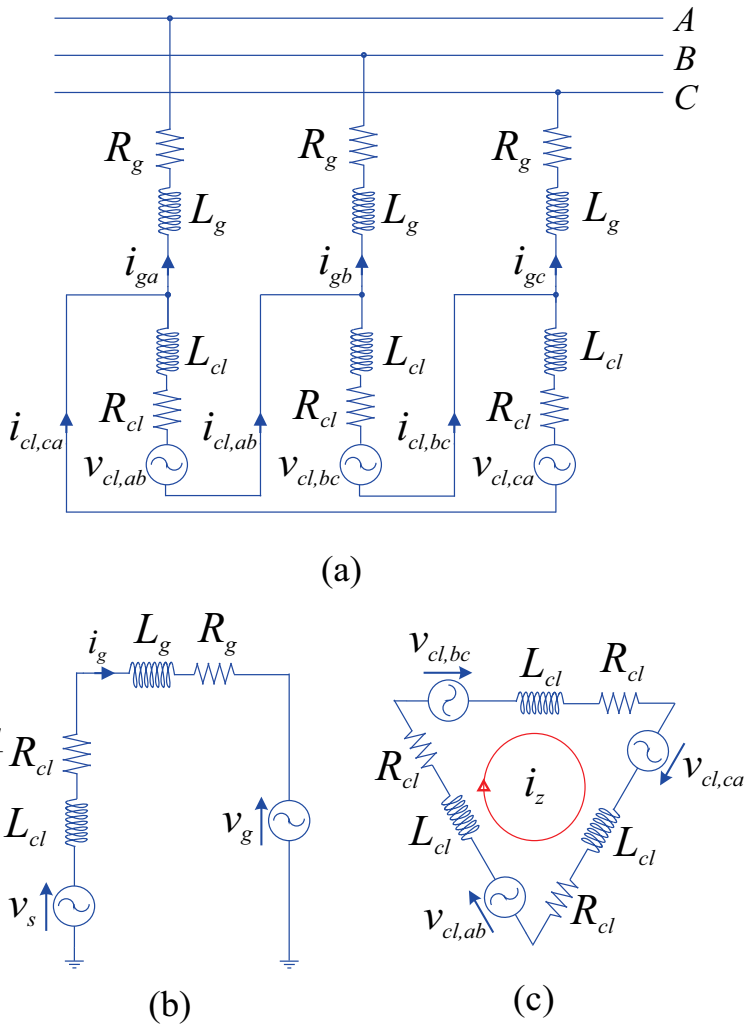

Figure 15 – Detailed schematic of the SDBC-MMCC-based STATCOM topology: (a) average model; (b) equivalent circuit describing the output current dynamics; (c) equivalent circuit describing the circulating current dynamics.

The dynamic equations (2.3) and (2.4) are useful to propose and design control algorithms for SDBC-MMCC. This topic will be approached in the next section. Assuming grid currents in steady-state given by (2.2), the cluster current i_{cl} [2] in steady-state is given by (Behrouzian; Bongiorno, 2017):

$$i_{cl} = \frac{\widehat{I}^{+}}{\sqrt{3}}\cos(\omega_n t + \varphi^{+} + \theta_v + \frac{\pi}{6}) + \frac{\widehat{I}^{-}}{\sqrt{3}}\cos(\omega_n t + \varphi^{-} - \theta_v - \frac{\pi}{6}) - \widehat{I}^{z}\cos(\omega_n t + \varphi^{z}), \quad (2.7)$$

where the circulating current (zero sequence component) is included. The amplitude of this component is $\widehat{I}^{z}$ and its phase angle is given by φ^{z}.

[2] Most of the developments presented in this Ph.D dissertation consider equations which are valid for all converter clusters. Under such conditions, the subscripts identifying each cluster are removed for simplification. For example, instead of presenting the equations for $i_{cl,ab}, i_{cl,bc}$ and $i_{cl,ca}$, only one equation is presented for i_{cl}. The parameter θ_v assumes the values $\{0, -\frac{2\pi}{3}, -\frac{4\pi}{3}\}$, depending on the analyzed cluster.

This modeling neglects the effect of the cluster inductance. Therefore, the voltages across each cluster are given by:

$$v_{cl} = v_{gl} = \sqrt{3}\widehat{V}^{+}\cos(\omega_n t + \delta^{+} + \theta_v + \frac{\pi}{6}) + \sqrt{3}\widehat{V}^{-}\cos(\omega_n t + \delta^{-} - \theta_v - \frac{\pi}{6}), \tag{2.8}$$

where v_{gl} is the grid line-to-line voltage.

The instantaneous active power delivered by each cluster is given by:

$$p_{cl} = v_{cl} i_{cl} = \bar{p}_{cl} + \tilde{p}_{cl}, \tag{2.9}$$

where $\bar{p}_{cl}$ and $\tilde{p}_{cl}$ are the average and oscillating components of the instantaneous active power. Replacing (2.8) and (2.7) into (2.9) yields:

$$\bar{p}_{cl} = \frac{\widehat{V}^{+}\widehat{I}^{+}}{2}\cos(\delta^{+} - \varphi^{+}) + \frac{\widehat{V}^{-}\widehat{I}^{-}}{2}\cos(\delta^{-} - \varphi^{-}) +$$

$$+\frac{\widehat{V}^{+}\widehat{I}^{-}}{2}\cos(\delta^{+} - \varphi^{-} + 2\theta_v + \frac{\pi}{3}) + \frac{\widehat{V}^{-}\widehat{I}^{+}}{2}\cos(\delta^{-} - \varphi^{+} - 2\theta_v - \frac{\pi}{3}) -$$

$$\frac{\sqrt{3}\widehat{V}^{+}\widehat{I}^{z}}{2}\cos(\delta^{+} - \varphi^{z} + \theta_v + \frac{\pi}{6}) - \frac{\sqrt{3}\widehat{V}^{-}\widehat{I}^{z}}{2}\cos(\delta^{-} - \varphi^{z} - \theta_v - \frac{\pi}{6}), \tag{2.10}$$

and

$$\tilde{p}_{cl} = \frac{\widehat{V}^{+}\widehat{I}^{+}}{2}\cos(2\omega_n t + \delta^{+} + \varphi^{+} + 2\theta_v + \frac{\pi}{3}) + \frac{\widehat{V}^{-}\widehat{I}^{-}}{2}\cos(2\omega_n t + \delta^{-} + \varphi^{+} - 2\theta_v - \frac{\pi}{3}) -$$

$$-\frac{\sqrt{3}\widehat{V}^{+}\widehat{I}^{z}}{2}\cos(2\omega_n t + \delta^{+} + \varphi^{z} + \theta_v + \frac{\pi}{6}) + \frac{\sqrt{3}\widehat{V}^{-}\widehat{I}^{z}}{2}\cos(2\omega_n t + \delta^{-} + \varphi^{z} - \theta_v - \frac{\pi}{6}) +$$

$$+\frac{\widehat{V}^{+}\widehat{I}^{-}}{2}\cos(2\omega_n t + \delta^{+} + \varphi^{-}) + \frac{\widehat{V}^{-}\widehat{I}^{+}}{2}\cos(2\omega_n t + \delta^{-} + \varphi^{+}). \tag{2.11}$$

Therefore, the following conclusions can be stated:

- a double line frequency component is observed in the instantaneous active power. This component generates a second harmonic ripple in the cell capacitor voltages;

- the first and second dc terms of the instantaneous active power in (2.10) represent an effective active power flow from the STATCOM to the grid. Considering a STATCOM without energy storage system, only reactive power will be injected and these terms will be canceled, since the voltage and current will be in quadrature;

- the existence of negative sequence components results in different average instantaneous power values in each cluster. However, the sum of the average values is null, since these terms are dependent on θ_v;

- if the zero sequence current (circulating current) is controlled to zero, the average power in each cluster will be different from zero and the capacitor voltage balancing among the clusters will not be reached. Therefore, the circulating current performs the energy exchange among the clusters to reach the capacitor voltage balancing.

Therefore, the circulating current exchanges power among the clusters. Indeed, the capacitor voltage balancing can be reached in the SDBC-MMCC if the average instantaneous power in each cluster is zero. The following condition is guaranteed if:

$$\frac{\widehat{V}^{+}\widehat{I}^{-}}{2}\cos(\delta^{+}-\varphi^{-}+2\theta_v+\frac{\pi}{3})+\frac{\widehat{V}^{-}\widehat{I}^{+}}{2}\cos(\delta^{-}-\varphi^{+}-2\theta_v-\frac{\pi}{3})=$$

$$=\frac{\sqrt{3}\widehat{V}^{+}\widehat{I}^{z}}{2}\cos(\delta^{+}-\varphi^{z}+\theta_v+\frac{\pi}{6})+\frac{\sqrt{3}\widehat{V}^{-}\widehat{I}^{z}}{2}\cos(\delta^{-}-\varphi^{z}-\theta_v-\frac{\pi}{6}), \tag{2.12}$$

which can be rewritten as:

$$\frac{\widehat{V}^{+}\widehat{I}^{-}}{2}\cos(\delta^{+}-\varphi^{-}+2\theta_v+\frac{\pi}{3})+\frac{\widehat{V}^{-}\widehat{I}^{+}}{2}\cos(\delta^{-}-\varphi^{+}-2\theta_v-\frac{\pi}{3})=$$

$$=\frac{\sqrt{3}\widehat{V}^{+}\widehat{I}^{z}}{2}\cos(\delta^{+}+\theta_v+\frac{\pi}{6})\cos\varphi^{z}+\frac{\sqrt{3}\widehat{V}^{+}\widehat{I}^{z}}{2}\sin(\delta^{+}+\theta_v+\frac{\pi}{6})\sin\varphi^{z}+$$

$$+\frac{\sqrt{3}\widehat{V}^{-}\widehat{I}^{z}}{2}\cos(\delta^{-}-\theta_v-\frac{\pi}{6})\cos\varphi^{z}+\frac{\sqrt{3}\widehat{V}^{-}\widehat{I}^{z}}{2}\sin(\delta^{-}-\theta_v-\frac{\pi}{6})\sin\varphi^{z} \tag{2.13}$$

As observed, there are two unknown variables ($\widehat{I}^{z}$ and δ^{z}). Thus, two equations are necessary. These equations can be obtained by computing the relations for clusters AB

and BC [3], and replacing the values of $\theta_v = 0$ and $\theta_v = -\frac{2\pi}{3}$ in (2.13) . Using this approach, the following nonlinear system is obtained:

$$\begin{cases} A = \widehat{I}^z X_1 \cos\varphi^z + \widehat{I}^z X_2 \sin\varphi^z, \\ B = \widehat{I}^z X_3 \cos\varphi^z + \widehat{I}^z X_4 \sin\varphi^z, \end{cases} \tag{2.14}$$

where:

$$\begin{cases} A = \frac{\widehat{V}^+\widehat{I}^-}{2}\cos(\delta^+ - \varphi^- + \frac{\pi}{3}) + \frac{\widehat{V}^-\widehat{I}^+}{2}\cos(\delta^- - \varphi^+ - \frac{\pi}{3}), \\ B = \frac{\widehat{V}^+\widehat{I}^-}{2}\cos(\delta^+ - \varphi^- - \pi) + \frac{\widehat{V}^-\widehat{I}^+}{2}\cos(\delta^- - \varphi^+ + \pi), \\ X_1 = \frac{\sqrt{3}}{2}\widehat{V}^+\cos(\delta^+ + \frac{\pi}{6}) + \frac{\sqrt{3}}{2}\widehat{V}^-\cos(\delta^- - \frac{\pi}{6}), \\ X_2 = \frac{\sqrt{3}}{2}\widehat{V}^+\sin(\delta^+ + \frac{\pi}{6}) + \frac{\sqrt{3}}{2}\widehat{V}^-\sin(\delta^- - \frac{\pi}{6}), \\ X_3 = \frac{\sqrt{3}}{2}\widehat{V}^+\cos(\delta^+ - \frac{\pi}{2}) + \frac{\sqrt{3}}{2}\widehat{V}^-\cos(\delta^- + \frac{\pi}{2}), \\ X_4 = \frac{\sqrt{3}}{2}\widehat{V}^+\sin(\delta^+ - \frac{\pi}{2}) + \frac{\sqrt{3}}{2}\widehat{V}^-\sin(\delta^- + \frac{\pi}{2}). \end{cases} \tag{2.15}$$

The methodology proposed by Betz and Summers (2009) provides the following solution:

$$\widehat{I}^z = \frac{A}{X_1\cos(\varphi^z) + X_2\sin(\varphi^z)} = \frac{B}{X_3\cos(\varphi^z) + X_4\sin(\varphi^z)}, \tag{2.16}$$

$$\tan(\varphi^z) = \frac{BX_1 - AX_3}{AX_4 - BX_2}. \tag{2.17}$$

Equations (2.16) and (2.17) present the theoretical values of the amplitude and phase of the circulating current in SDBC-MMCC during unbalanced conditions. If the grid voltage is assumed to be balanced, these expressions are strongly simplified. If $\widehat{V}^- = 0$, the equation (2.12) can be rewritten as follows:

$$\frac{\widehat{V}^+\widehat{I}^-}{2}\cos(\delta^+ - \varphi^- + 2\theta_v + \frac{\pi}{3}) = \frac{\sqrt{3}\widehat{V}^+\widehat{I}^z}{2}\cos(\delta^+ - \varphi^z + \theta_v + \frac{\pi}{6}). \tag{2.18}$$

[3] Since the sum of the average instantaneous power of the three phases is null, the equation for cluster CA is a linear combination of equations from clusters AB and BC.

Accordingly,

$$\frac{\widehat{V}^{+}\widehat{I}^{-}}{2} = \frac{\sqrt{3}\widehat{V}^{+}\widehat{I}^{z}}{2}, \tag{2.19}$$

and

$$\left|\delta^{+} - \varphi^{-} + 2\theta_v + \frac{\pi}{3}\right| = \left|\delta^{+} - \varphi^{z} + \theta_v + \frac{\pi}{6}\right|. \tag{2.20}$$

Since $2\theta_v \equiv -\theta_v$, the amplitude and the phase of the circulating current are given by:

$$\widehat{I}^{z} = \frac{\widehat{I}^{-}}{\sqrt{3}}, \tag{2.21}$$

$$\varphi^{z} = \frac{\pi}{2} - \varphi^{-}. \tag{2.22}$$

As observed, when the grid voltage is balanced, the circulating current of SDBC-MMCC is proportional to the negative sequence component processed by the converter. It is important to remark that the results obtained in this section are in agreement with Hagiwara, Maeda and Akagi (2012) and Behrouzian and Bongiorno (2017).

2.2.2 DSCC-MMCC during Negative Sequence Compensation

A detailed schematic of DSCC-MMCC topology, which presents six arms, is presented in Fig. 14 (a). The inductance L_{arm} reduces the high order harmonics in the circulating current and limits the currents during faults (Akagi, 2011; Harnefors et al., 2013). Three coupled inductors can also be employed to increase the converter power density (Akagi, 2011). Similarly to the previous analysis, the DSCC-MMCC is connected to the main grid through a three-phase transformer represented by the inductance L_g. The converter presents N_{2Y} cells per arm.

Assuming balanced capacitor voltages, sufficiently high switching frequency and high number of cells, the arm voltages v_u and v_l can be assumed controlled voltage sources, as presented in Fig. 16 (a). The DSCC-MMCC dynamics can be modeled based on the two equivalent circuits shown in Fig. 16 (b) and (c). The dynamics of the output current per phase can be obtained from Fig. 16 (b), based on Millman's theorem (Millman, 1940), as follows:

$$v_s - \left(\frac{1}{2}L_{arm} + L_g\right)\frac{di_g}{dt} - \left(\frac{1}{2}R_{arm} + R_g\right)i_g = v_g, \tag{2.23}$$

where v_g is the grid line-to-neutral voltage, R_{arm} is the arm inductor resistance and i_g is the grid current. The factor $\frac{1}{2}$ appears in the arm inductance due to the Millman's theorem. v_s is the line-to-neutral voltage synthesized by the STATCOM (also referred as *output voltage*), given by:

$$v_s = \frac{1}{2}\left(-v_u + v_l\right). \tag{2.24}$$

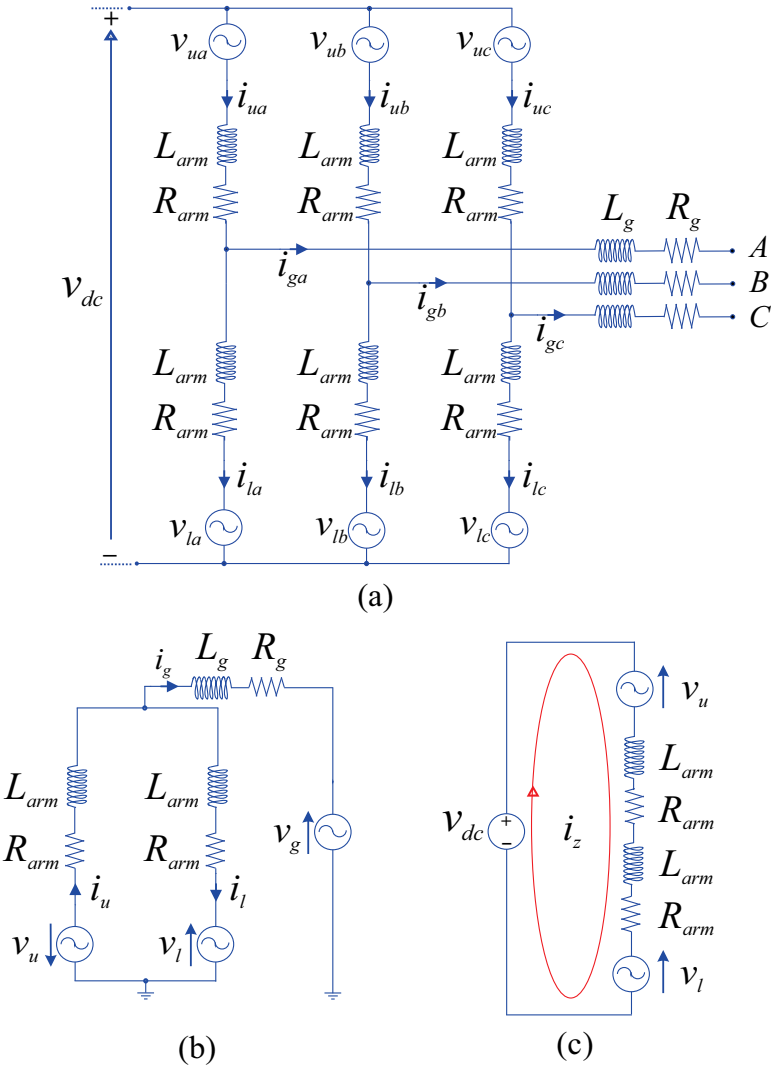

Figure 16 – Detailed schematic of the DSCC-MMCC-based STATCOM topology: (a) average model; (b) equivalent circuit describing the output current dynamics; (c) equivalent circuit describing the circulating current dynamics.

On the other hand, the circulating current dynamics can be obtained based on Fig. 15 (c), as follows:

$$v_z - L_{arm}\frac{di_z}{dt} - R_{arm}i_z = 0, \tag{2.25}$$

where v_z is the converter *internal voltage* (which drives the circulating current) given by:

$$v_z = \frac{1}{2}\left(v_{dc} - v_u - v_l\right), \tag{2.26}$$

and i_z is the converter circulating current giving by:

$$i_z = \frac{1}{2}\left(i_u + i_l\right). \tag{2.27}$$

It is important to note that DSCC-MMCC presents one term of circulating current per phase [4]. The dynamic equations (2.23) and (2.25) are useful to propose and design control algorithms for the DSCC-MMCC. This topic will be approached in the next section.

In this section, the effect of the arm inductance is neglected. Therefore, the output ac voltage is given by:

$$v_s \approx v_g = \widehat{V}^+ \cos(\omega_n t + \delta^+ + \theta_v) + \widehat{V}^- \cos(\omega_n t + \delta^- - \theta_v). \tag{2.28}$$

The instantaneous active power delivered by each phase is given by:

$$p_g = v_g i_g = \bar{p}_g + \tilde{p}_g, \tag{2.29}$$

where $\bar{p}_g$ and $\tilde{p}_g$ are the average and oscillating instantaneous power components. Replacing (2.28) and (2.2) in (2.29) yields:

$$\bar{p}_g = \frac{\widehat{V}^+\widehat{I}^+}{2}\cos(\delta^+ - \varphi^+) + \frac{\widehat{V}^-\widehat{I}^-}{2}\cos(\delta^- - \varphi^-) +$$

$$+\frac{\widehat{V}^+\widehat{I}^-}{2}\cos(\delta^+ - \varphi^- + 2\theta_v) + \frac{\widehat{V}^-\widehat{I}^+}{2}\cos(\delta^- - \varphi^+ - 2\theta_v), \tag{2.30}$$

and

$$\tilde{p}_g = \frac{\widehat{V}^+\widehat{I}^+}{2}\cos(2\omega_n t + \delta^+ + \varphi^+ + 2\theta_v) + \frac{\widehat{V}^-\widehat{I}^-}{2}\cos(2\omega_n t + \delta^- + \varphi^+ - 2\theta_v) +$$

$$+\frac{\widehat{V}^+\widehat{I}^-}{2}\cos(2\omega_n t + \delta^+ + \varphi^-) + \frac{\widehat{V}^-\widehat{I}^+}{2}\cos(2\omega_n t + \delta^- + \varphi^+). \tag{2.31}$$

Therefore, the following conclusions can be stated:

[4] This Ph.D dissertation describes the circulating current per phase, as adopted in most works in literature. However, for a DSCC-MMCC-based STATCOM, the circulating currents will present only 2 degrees of freedom, since no element is connected to the converter dc-link. Therefore, the reference current of the third phase must be a linear combination of the current references of other two phases.

- The first and second dc terms of instantaneous power in (2.31) represent an effective active power flow from the STATCOM to the grid. Considering a STATCOM without energy storage system, only reactive power will be injected and these terms will be canceled, since the voltage and current will be in quadrature;
- The existence of negative sequence components results in different average instantaneous power in each leg. Nevertheless, the sum of the average values is null since these terms are dependent on θ_v and the STATCOM does not present an active power source;
- If the circulating current is controlled to zero, the average powers in each phase will be different from zero and the capacitor voltage balancing between the phases will not be reached. Therefore, the circulating current performs the energy exchange in order to obtain the capacitor voltage balancing.

Once the DSCC-MMCC presents one circulating current per phase, this current must guarantee power balance (Yue et al., 2016). Accordingly:

$$v_{dc} i_z = \bar{p}_g. \tag{2.32}$$

Replacing (2.31) in (2.32) yields:

$$i_z = \frac{\widehat{V}^+ \widehat{I}^-}{2v_{dc}} \cos(\delta^+ - \varphi^- + 2\theta_v) + \frac{\widehat{V}^- \widehat{I}^+}{2v_{dc}} \cos(\delta^- - \varphi^+ - 2\theta_v). \tag{2.33}$$

By defining the following modulation indexes:

$$m^+ = \frac{2\widehat{V}^+}{v_{dc}}, \tag{2.34}$$

$$m^- = \frac{2\widehat{V}^-}{v_{dc}}, \tag{2.35}$$

the circulating current expression for DSCC-MMCC is given by:

$$i_z = \frac{m^+ \widehat{I}^-}{4} \cos(\delta^+ - \varphi^- + 2\theta_v) + \frac{m^- \widehat{I}^+}{4} \cos(\delta^- - \varphi^+ - 2\theta_v), \tag{2.36}$$

As observed, in DSCC-MMCC, the circulating currents are dc. Additionally, the sum of circulating currents is zero, since no power source is connected to the dc-link. Under such conditions, the third circulating current is a linear combination of the other two phases. Therefore, the DSCC-MMCC-based STATCOM presents two degrees of freedom in the circulating currents.

It is important to remark that some references in literature propose the use of harmonic components in the circulating current of SDBC-MMCC and DSCC-MMCC. The main objectives are reducing the capacitor voltage ripples (Picas et al., 2013; Pou et al., 2015; Li et al., 2018; Tanaka; Wang; Blaabjerg, 2019), improving the balancing capability during unbalances (Nieves et al., 2014) and reducing converter losses (Yang et al., 2018). Nevertheless, the use of these strategies will not be approached in the present Ph.D dissertation.

2.2.3 Comparison Between DSCC-MMCC and SDBC-MMC During Unbalanced Conditions

The modern grid codes, weak power systems and high penetration of renewable power plants can be considered important development drivers of STATCOMs with negative sequence injection capability during unbalanced conditions. The grid codes in countries with high penetration of wind and solar power plants require grid connected systems to remain connected during balanced and unbalanced grid faults. Moreover, the power plant must inject reactive currents during the grid fault. This process is called low-voltage ride-through (LVRT). STATCOMs have been employed to support power systems to comply with grid code requirements (Windpower E&D, 2013; Tanaka et al., 2019). Typically, the positive sequence current is computed as follows:

$$\widehat{I}^{+} = k_{+}\left(0.9 - \widehat{V}^{+}\right), \tag{2.37}$$

where k_{+} is the droop factor, which can be within the $[0, 10]$ interval. This curve is presented in Fig. 17 (a) where $k_{+} = 2.5$. Typically, a non injection band is considered.

Nevertheless, the positive sequence injection can increase the negative sequence voltage and voltage unbalance (Sharifabadi et al., 2016). In Germany, for example, the technical requirements for connection in the high voltage system imposes negative sequence injection during unbalanced faults (VDE, 2015). Negative sequence current is used to reduce the negative sequence voltage during the fault. Accordingly,

$$\widehat{I}^{-} = -k_{-}\left(0.05 - \widehat{V}^{-}\right), \tag{2.38}$$

where k_{-} is the droop factor, which can be within the interval $[0, 10]$. This curve is presented in Fig. 17 (b) when $k_{-} = 2.5$. As observed, a non injection band is also considered.

During unbalanced voltage conditions, the circulating current plays an important role in the power exchange between the arms/clusters of the SDBC-MMCC and DSCC-MMCC. Relations (2.16), (2.17) and (2.36) show that the circulating current

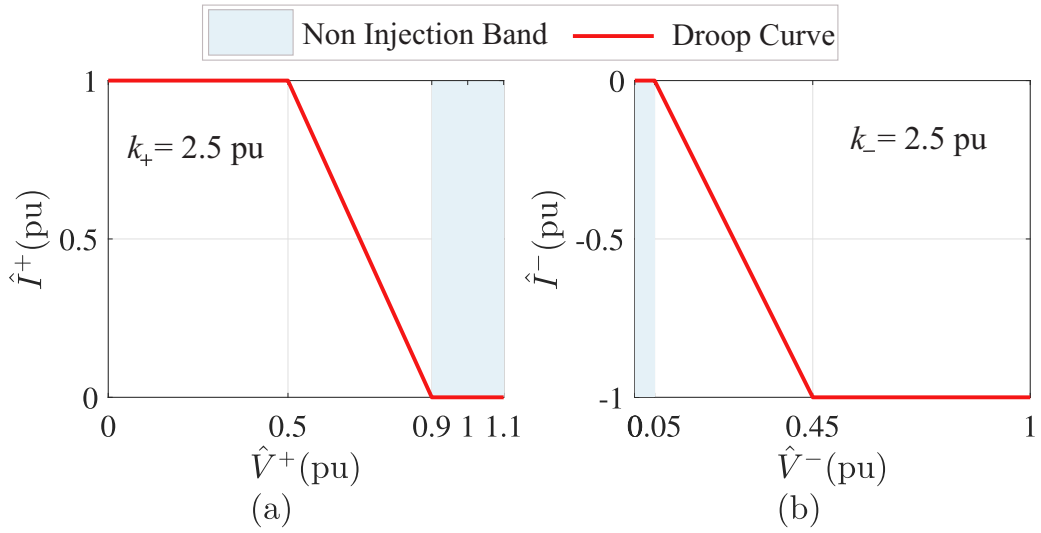

Figure 17 – Low voltage ride through current injection in Germany: (a) positive sequence injection requirements; (b) negative sequence injection requirements.

value for both topologies depends on the amplitude $\widehat{V}^-$ and phase δ^- of negative sequence voltage.

Moreover, Behrouzian and Bongiorno (2017) show the SDBC topology has a singular operation point that requires an infinity circulating current to reach the capacitor voltage balancing. This operating point is observed when the amplitudes of positive and negative sequence voltages are equal:

$$K_v = \frac{\widehat{V}^-}{\widehat{V}^+} = 1, \tag{2.39}$$

where K_v is the voltage unbalance factor.

In order to compare the topologies, $\delta^+ = 0$ is assumed and 1 pu of positive sequence current is injected into the grid. In this case, the per unit circulating current amplitude is calculated according to K_v and δ^-, based on equations (2.17) and (2.36).

The circulating current amplitudes for SDBC-MMCC and DSCC-MMCC are shown in the contour plots of Fig. 18, under various unbalance factors and negative sequence voltage angles. The voltage unbalance factor is limited to 0.5 for the sake of visualization. As observed, the circulating current amplitude increases when K_v increases. For the selected operation conditions, the SDBC-MMCC topology reaches almost 0.9 pu of circulating current. For DSCC-MMCC, the maximum value of circulating current reaches 0.12 pu. Consequently, the SDBC-MMCC presents higher current ratings than DSCC-MMCC during unbalanced voltage sags. Interestingly, the phase with maximum circulating current in DSCC-MMCC depends on δ^-, and a 120 degree symmetry is observed in the maximum values obtained in each phase. Indeed, since no active power transfer is observed from the dc side to the ac side, the sum of the three circulating currents must be zero.

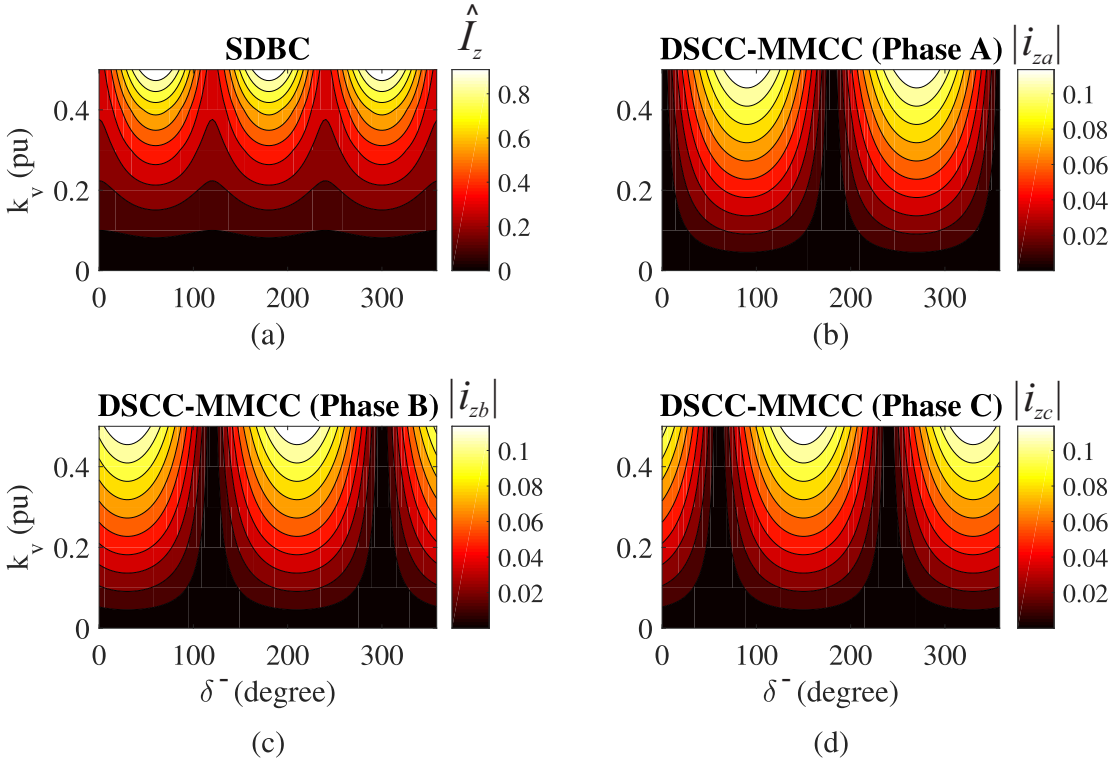

Figure 18 – Effect of negative sequence voltage on the converter circulating current magnitude: (a) SDBC-MMCC; (b) DSCC-MMCC (Phase A, absolute value); (c) DSCC-MMCC (Phase B, absolute value); (d) DSCC-MMCC (Phase C, absolute value).

2.3 Modulation and Cell Energy Balancing

The modulation strategy computes switching times of the converter power switches. For voltage source converters, this computation is generally based on the desired output voltage. In fact, the power converters can obtain discrete values of voltage at their output. The purpose of any modulation method is to obtain an output voltage that, *in average*, follows the reference voltage waveform. Therefore, the converter output voltage contains harmonics generated by the switching process.

Figure 19 presents an overview of the modulation strategies employed in multilevel converters. In the context of modular multilevel cascaded converters, the phase-shifted PWM and the nearest level control approach are the most explored in technical literature (Sousa, 2019). Therefore, this work will focus on the carrier-based pulse-width modulation (PWM) and nearest level control (NLC) approaches.

2.3.1 Phase-Shifted PWM (PS-PWM)

For phase-shifted PWM strategy, the carriers are symmetrically phase shifted. For SDBC-MMCC, the angular displacements of the carriers are given by (Mora et al., 2016;

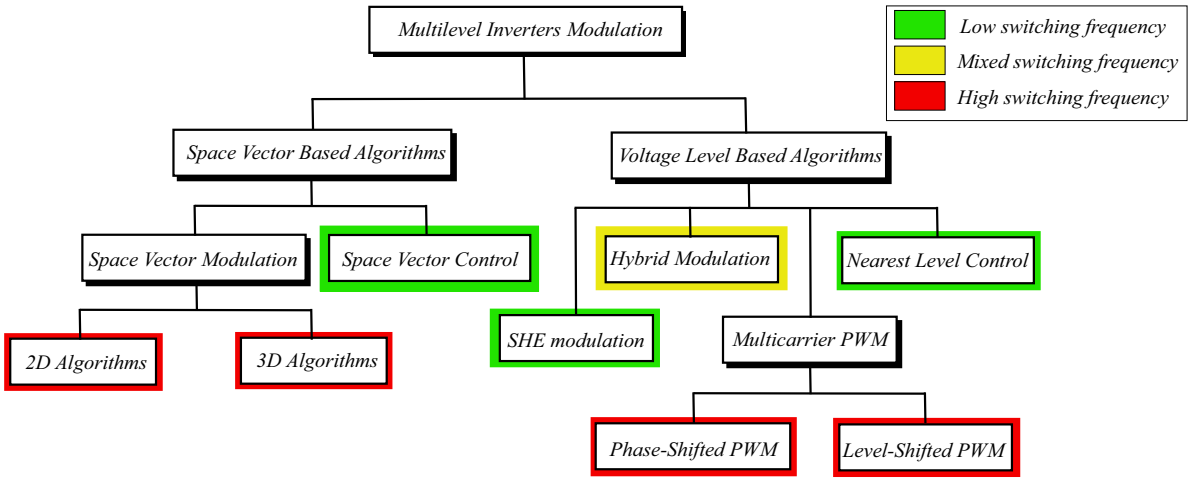

Figure 19 – Overview of the modulation strategies employed in multilevel converters. *Adapted from* Franquelo et al. (2008).

Lamb; Mirafzal; Blaabjerg, 2018):

$$\theta_c^i = \pi \left(\frac{i-1}{N_\Delta} \right), \tag{2.40}$$

where $i = 1, 2, ..., N_\Delta$. The carrier signals and the reference voltage are presented in Fig. 20. As observed, the carrier waveforms are symmetric. The cells are modulated in order to generate a 3-level waveform, as illustrated in Fig. 21 (a). Figure 21 (b) shows the phase-to-phase output voltage, which presents $(2N_\Delta + 1)$ levels.

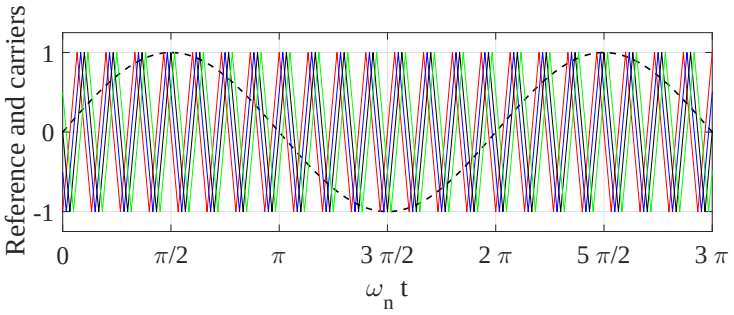

Figure 20 – Phase-shifted modulation for SDBC-MMCC. *Remark*: the reference voltage is normalized.

For DSCC-MMCC topology, the angular displacements of the lower arm carriers $\theta_{c,l}^i$ are calculated by the following equation:

$$\theta_{c,l}^i = 2\pi \left(\frac{i-1}{N_{2Y}} \right), \tag{2.41}$$

where $i = 1, 2, ..., N_{2Y}$.

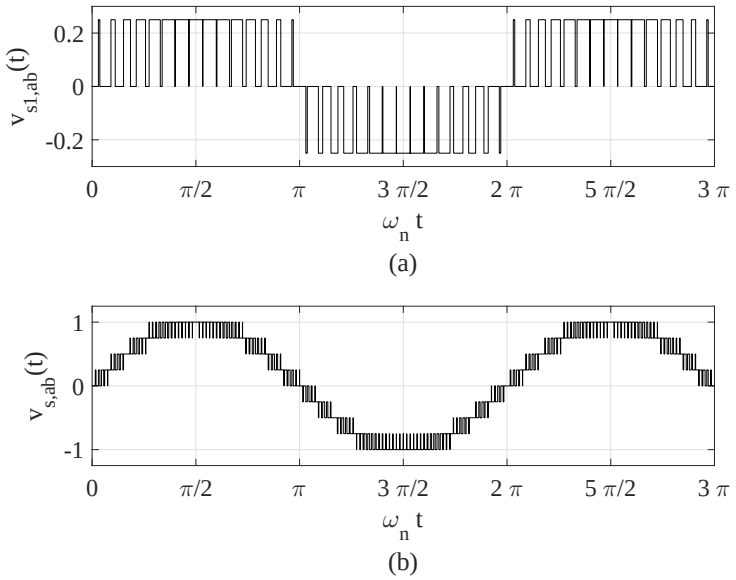

Figure 21 – Voltages generated by SDBC-MMC using PS-PWM: (a) cell output voltage ($v_{s1,ab}$) in pu; (b) converter output voltage ($v_{s,ab}$). *Operation conditions*: carrier frequency is 900 Hz, maximum modulation index, $N_\Delta = 4$. Base value: v_{dc}.

On the other hand, the angular displacements of the upper arm carriers are given by:

$$\theta^i_{c,u} = \theta^i_{c,l} + \gamma, \tag{2.42}$$

where γ indicates the angular displacement among the carrier waveforms in the upper and lower arms. The carrier signals and the reference voltage are presented in Fig. 22. Asymmetric carriers are employed since the arms are able to generate dc voltages.

The angular displacements of the carrier waveforms can be chosen in terms of the desired harmonic performance. According to Ilves et al. (2015a), two different modulation strategies can be employed in DSCC-MMCC:

- $(N + 1)$ level modulation: in this strategy, the angular displacement is given by:

$$\gamma = \pi. \tag{2.43}$$

This modulation strategy results in no harmonics in the internal voltage (in theory), since the cell string voltages will be complementary. Therefore, this modulation strategy presents relatively clean circulating current and dc-link current without high order harmonics. Furthermore, the converter phase voltage[5] will present $N_{2Y} + 1$ levels.

[5] Phase voltage refers to the voltage difference between one of the converter phases and the dc-link middle point.

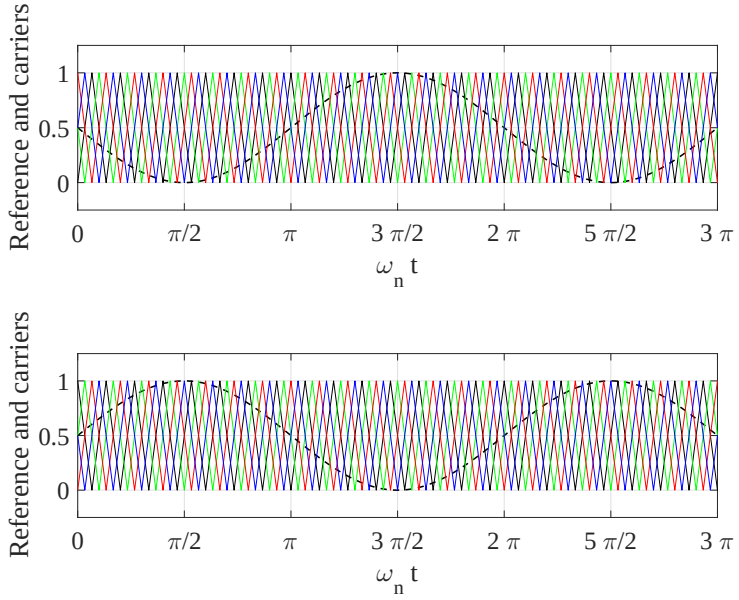

Figure 22 – Phase-shifted modulation for DSCC-MMCC: (a) modulator signals for upper arms; (b) modulator signals for lower arms. *Remark*: in this example, $\gamma = \pi$ is adopted.

- $(2N + 1)$ level modulation: in this strategy, the angular displacement is chosen to cancel the first group of harmonics in the phase voltage. This angular displacement is given by:

$$\gamma = 0 \quad , \quad \text{if } N_{2Y} \text{ is odd}$$

$$\gamma = \frac{\pi}{N_{2Y}} \quad , \quad \text{if } N_{2Y} \text{ is even.} \tag{2.44}$$

This modulation strategy results in $2N_{2Y} + 1$ levels in the converter phase voltage. Nevertheless, the number of inserted cells in the upper and lower arm are not the same, which results in a higher circulating current ripple.

Therefore, the $(N + 1)$ level modulation is interesting for applications in which the dc-link current quality is preferred, such as in HVDC systems. When the ac-voltage quality is preferred, as in STATCOM applications, the $(2N + 1)$ level modulation can be employed. A comparison between the line to neutral output voltage waveforms of $(N+1)$ and $(2N+1)$ level modulation methods is presented in Fig. 23. As observed in Fig. 23 (b), the use of $(2N + 1)$ level strategy leads to the cancellation of the first harmonic group. Furthermore, Fig. 23 (c) shows the internal voltage v_z for each modulation. As noted, $(N + 1)$ level modulation, in theory, presents no harmonics in the internal voltage, which reduces the ripple in the circulating current, when compared with $(2N + 1)$ level modulation.

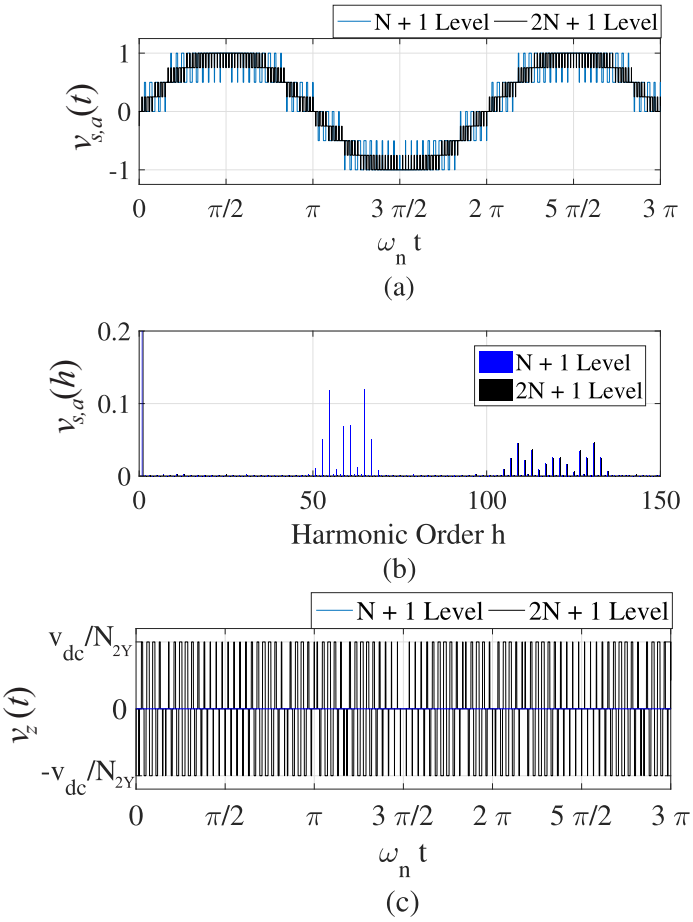

Figure 23 – Comparison of $(N+1)$ and $(2N+1)$ level phase-shifted modulation schemes: (a) converter phase voltage ($v_{s,a}$) in pu; (b) harmonic spectrum obtained; (c) internal voltage v_z. *Operation conditions*: carrier frequency is 900 Hz, maximum modulation index, $N_{2Y} = 4$. Base value: $v_{dc}/2$.

2.3.2 Nearest Level Control (NLC)

As observed, the carrier-based PWM strategies can be easily adapted to modular multilevel cascaded converters. Nevertheless, for a high number of cells, the switching losses may become intolerably high due to many avoidable switching actions (Siddique et al., 2016). In this case, the nearest level control is an alternative to the carrier-based PWM which is simpler to implement. This modulation strategy was originally introduced for electric drives with direct torque control (DTC) (Kouro et al., 2007). The NLC concept is based on the sampling of the reference voltage and its approximation using the nearest available voltage level. The block diagram of this strategy is presented in Fig. 24.

NLC can be mathematically represented by the round function, which approximates a continuous function to the closest integer. The reference voltage is firstly normalized and then multiplied by the number of cells. When the round function is applied, the output signal defines the number of cells which must be inserted. This process is illustrated in Fig. 25. As observed, when the number of cells is small (e.g, $N = 3$), the voltage obtained

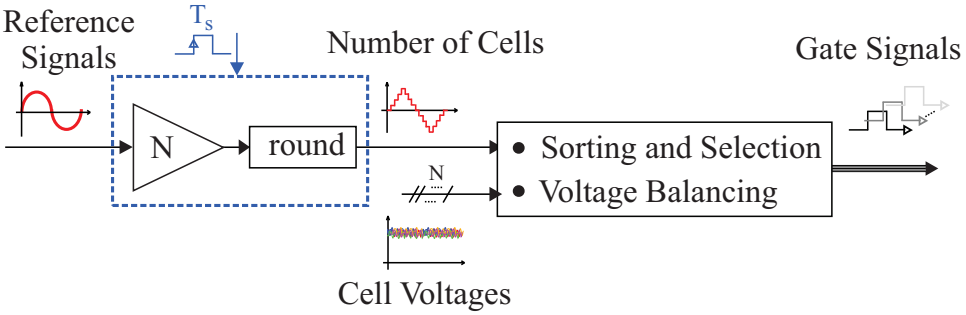

Figure 24 – Block diagram of the nearest level control modulation method. *Remark*: for SDBC-MMCC, N is replaced by N_Δ. For DSCC-MMCC, N is replaced by N_{2Y}.

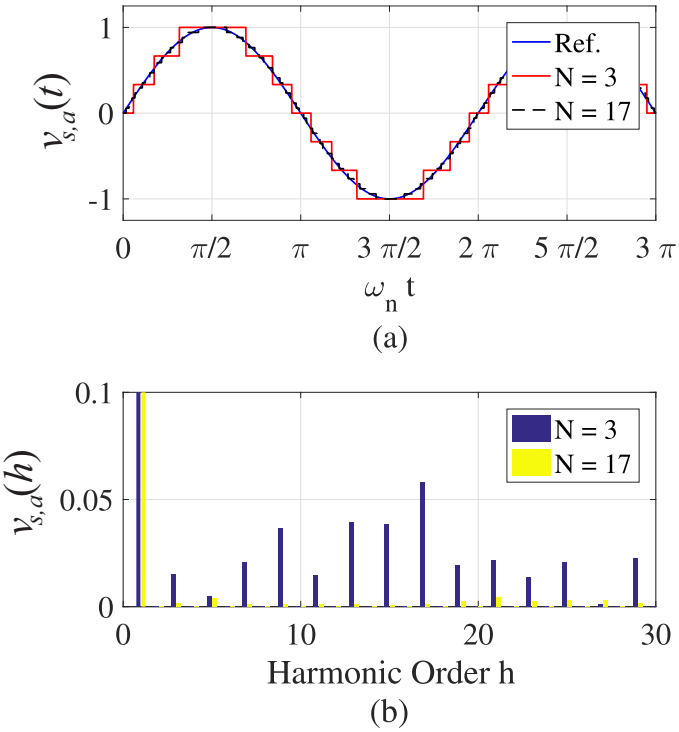

Figure 25 – Operation principle of round algorithm: (a) ideal converter phase voltage v_a synthesized by NLC modulation strategy; (b) harmonic spectrum of the phase voltage.

presents a considerable harmonic distortion. Furthermore, when NLC is employed, the output voltage presents a stationary tracking error related to the difference between the staircase voltage and the reference. Nevertheless, when the number of cells increases, the approximation becomes reasonable and the low harmonic frequency content is attenuated to acceptable values.

Differently from the carrier-based PWM methods, the harmonic spectrum of NLC presents no characteristic behavior with concentrated energy in some frequency range.

The output voltage waveform presents practically all harmonic orders. This fact is a positive characteristic when electromagnetic interference is taken into account. However, this fact makes harder the design of inductors and filters to comply with the harmonic standards. Furthermore, if the cell capacitances are infinitely large, the ideal switching frequency of NLC will be equal to the line frequency. Therefore, when NLC is applied, the converter presents lower switching losses and higher efficiency. Indeed, considering practical capacitance values, some additional switching events must be accomplished to guarantee the capacitor voltage balancing (Sousa et al., 2018).

Another important NLC parameter the sampling period T_s. Based on the operation principle, T_s must be sufficiently high to avoid voltage steps exceeding one level. If this condition disregarded, low harmonic orders in the output voltage will increase considerably (Tu; Xu, 2011a). Tu and Xu (2011a) presented an interesting study relating the sampling period T_s to the MMCC output voltage harmonic distortion. According to this reference, total harmonic distortion (THD) behavior of the output voltage is related to two important frequencies, f_1 and f_2, given by:

$$f_1 = \pi f_n \sqrt{2mN},$$

$$f_2 = \pi f_n mN. \tag{2.45}$$

When $f_s \leq f_1$, the THD of output voltage is strongly deteriorated. When $f_1 \leq f_s \leq f_2$, the THD decreases almost linearly with f_s. Finally, when $f_s \geq f_2$, the THD is almost independent of f_s, since all cells are completely used in the modulation process. For example, considering $f_n = 60$ Hz, $m = 1$ and $N = 17$, the minimum sampling frequency is $f_2 = 3.21$ kHz.

2.3.3 Cell Energy Balancing

When the PS-PWM method is employed, an extra individual balancing control loop must be included, in order to ensure that the individual capacitor voltage balancing will comply with the reference value (Debnath et al., 2015). For such strategy, the individual balancing controller is basically a simple proportional controller, as shown in Fig. 26. Then, its output is multiplied by the branch current $i_{t,i}$. For SDBC-MMCC, $i_{t,i}$ is the cluster current. For DSCC-MMCC, $i_{t,i}$ is the arm current. The obtained signal is added to the modulator reference signal.

The proportional gain k_b must be sufficiently small to avoid disturbances in the modulation. Therefore, $k_b << 1$. The appropriate tuning is not a simple task. The value is generally obtained through simulations (Sharifabadi et al., 2016).

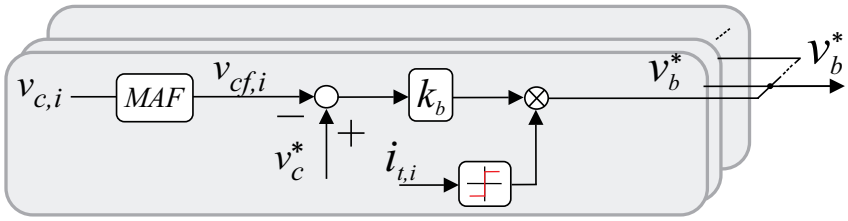

Figure 26 – Individual balancing control loop for PS-PWM strategy.

Regarding the NLC modulation strategy, in order to ensure the capacitor voltage balance, this strategy requires a sorting and selection algorithm to properly select the cell in the arm/cluster to be inserted or bypassed. Basically, the cell capacitor voltage is measured and sorted. Then, during the positive arm/cluster currents, the cell with the low voltage will be selected to be inserted, while the cell with high voltage will be bypassed. The opposite action will be performed during the negative arm/cluster currents. Using this strategy, all the cell voltages will be balanced. However, the conventional sorting and selection algorithm proposed in (Lesnicar; Marquardt, 2003) usually results in a high switching frequency operation. Therefore, other sorting and selection methods have been proposed to reduce the switching losses.

In this context, the predictive sorting method was proposed (Ilves et al., 2015b), which employs the estimation of the sum-capacitor-voltage ripple. When the instantaneous value is higher than the predicted ripple, the algorithm performs the cells exchange. Therefore, a lower average switching frequency is obtained.

Another approach is the use of some capacitor voltage tolerance band methods (TB), which were proposed to improve the performance of the NLC strategy. In general, the sorting and selection are carried out only when some monitored variable (e.g., cell voltages) reaches the limit, which is defined as a tolerance band (e.g., 10% of the nominal voltage).

A general benefit of TB methods is the reduced the switching frequency, since switching events occur only when necessary. Therefore, the switching frequency will change during the converter operation. In general, the switching frequency will increase during disturbances and will decrease in steady-state. On the other hand, the harmonic spectrum will not be characteristic and it is more difficult to verify the compliance with standards of harmonic distortion (Sharifabadi et al., 2016). Moreover, the average switching frequency will increase when the tolerance band is reduced.

Basically, the tolerance band methods can be classified into 2 groups (Hassanpoor et al., 2015):

- average tolerance band (ATB): this method employs the tolerance band concept for the average voltage ripple of the cells;

- cell tolerance band (CTB): this method employs the tolerance band concept for the individual cell voltage ripple.

Hassanpoor et al. (2015) and Hassanpoor, Norrga and Nami (2015) compare some tolerance band methods proposed in literature considering average switching frequency, dynamic behavior and power losses. As a conclusion, the CTB-based methods present smaller losses if compared with other strategies and acceptable dynamic performance.

Finally, advanced tolerance band methods have been discussed in literature. Hassanpoor et al. (2016) propose a CTB method that concentrates the switching events when the arm currents are crossing to zero minimizing the switching losses. Sangwongwanich et al. (2016) show that when cells with different capacitances are considered, the voltage balancing will result in different temperatures in the power devices. Therefore, CTB methods that can reach both voltage and thermal balancing were proposed by Sangwongwanich et al. (2016) and Hahn et al. (2018).

2.4 Control Strategies of MMCC-based STATCOM

Three main goals are aimed by the MMCC control:

- controlling the output current i_g;
- driving the circulating current i_z such that the energy balance between the dc and ac circuits is dynamically met and the cell capacitors remain charged at a predefined level;
- balancing the cell capacitor voltages.

The studied control strategies for both MMCC-based STATCOM topologies are presented as follows.

2.4.1 DSCC-MMCC and SDBC-MMCC Control Strategies

The control strategy for the MMCC-based STATCOM topologies is presented in Fig. 27. The proposed grid current control injects positive and negative sequence currents into the grid. This strategy is performed by the inner loops, implemented in stationary ($\alpha\beta$) reference frame, which results in a simultaneous control of positive and negative current sequences, as shown in Fig. 27 (a). Basically, the external loop controls the square of the average voltage v_{avg} of all converter cells. This loop calculates the amount of active

power P^* required to flow from the grid to the converter due to the power losses. The average voltage is computed by:

$$v_{avg} = \frac{1}{N_T} \sum_{i=1}^{N_T} v_{c,i}, \tag{2.46}$$

where $v_{c,i}$ is the ith cell voltage. N_T is the total number of operating cells in the MMCC.

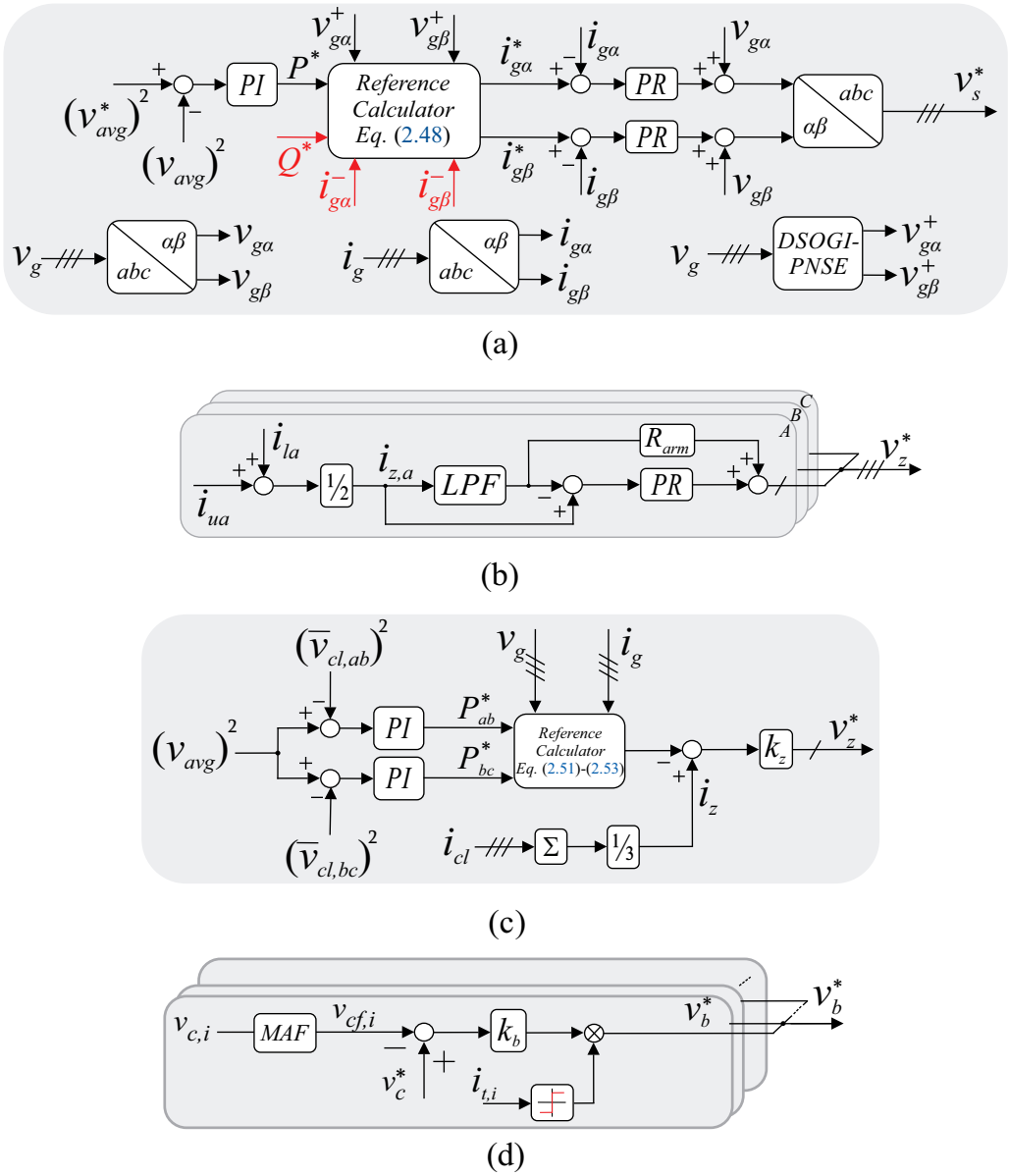

Figure 27 – Control Strategies of MMCC-based STATCOM: (a) grid current control - DSCC-MMCC and SDBC-MMCC; (b) circulating current control - DSCC-MMCC; (c) circulating current control - SDBC-MMCC; (d) individual balancing control - DSCC-MMCC and SDBC-MMCC.

The average voltage reference v^*_{avg} is given by:

$$v^*_{avg} = \frac{v_{dc}}{N}, \tag{2.47}$$

where v_{dc} is the nominal MMCC effective dc-link voltage. For SDBC-MMCC, N is replaced by N_Δ, while for DSCC-MMCC, N is replaced by N_{2Y}. Despite the absence of physical dc-link in SDBC-MMCC-based STATCOM, the effective dc-link voltage is an important parameter to avoid overmodulation (Fujii; Schwarzer; De Doncker, 2005).

Using the instantaneous power theory (Akagi; Watanabe; Aredes, 2007), the grid current reference can be computed by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = \frac{1}{(v^+_{g\alpha})^2 + (v^+_{g\beta})^2} \begin{bmatrix} v^+_{g\alpha} & v^+_{g\beta} \\ v^+_{g\beta} & -v^+_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} + \begin{bmatrix} i^-_{g\alpha} \\ i^-_{g\beta} \end{bmatrix}, \tag{2.48}$$

where $v^+_{g\alpha}$ and $v^+_{g\beta}$ are the positive sequence components of the grid voltage represented in stationary reference frame. These components are obtained through the positive and negative sequence extractor based on the double second-order generalized integrator (DSOGI-PNSE), proposed by Rodriguez et al. (2006). The references Q^*, $i^-_{g\alpha}$ and $i^-_{g\beta}$ are dependent on the STATCOM operation mode. For example, in the case of reactive power and unbalance compensation of local loads, these values are obtained from the load current (Yue et al., 2016). In the case of voltage support or LVRT operation, these variables will be obtained through droop controllers defined in the grid codes (Sharifabadi et al., 2016).

Two proportional resonant (PR) controllers tuned to the fundamental frequency are employed in order to track the reference current. The dynamics of the grid current in the stationary reference frame for both topologies are given by:

$$v_{s,\alpha\beta} = v_{g,\alpha\beta} + L_{eq}\frac{di_{g,\alpha\beta}}{dt} + R_{eq}i_{g,\alpha\beta}, \tag{2.49}$$

where the values of L_{eq} and R_{eq} are dependent on the topology and inductor realization (coupled or uncoupled). For instance, when DSCC-MMCC topology is implemented with uncoupled inductors, $L_{eq} = L_g + 0.5L_{arm}$ and $R_{eq} = R_g + 0.5R_{arm}$.

Using this dynamic model, the PR controllers can be adjusted using the design methodology proposed by Yepes et al. (2011). Feedforward actions of the grid voltage are included to improve the dynamic behavior.

Regarding the DSCC-MMCC topology, the circulating current control reduces the harmonics in the circulating current and inserts damping in the converter dynamic response (Harnefors et al., 2013; Moon et al., 2013). Figure 27 (b) presents the circulating current control loop for DSCC-MMC. As observed, this structure is implemented per phase. A butterworth second order filter is employed to remove the dc component of i_z.

Regarding the negative sequence injection, a considerable 2nd harmonic component appears in the circulating current (Xu et al., 2016). In genenral, this second order component cannot be compensated by the proportional controller (Yue et al., 2016). Therefore, three resonant controllers (one per phase) tuned to the 2nd harmonic are added to the circulating current control.

The circulating current control for the SDBC-MMCC employed in this work was proposed by Behrouzian and Bongiorno (2017) and is illustrated in Fig. 27 (c). The cluster voltage balancing control calculates the reference value of the circulating current. The cluster average voltages are calculated by:

$$\bar{v}_{cl} = \frac{1}{N_\Delta} \sum_{j=1}^{N_\Delta} v_{c,j}, \tag{2.50}$$

The square value of the average cluster voltages are controlled. In this case, the outputs of the PI controllers are the power disturbances in the clusters, denoted by P^*_{ab} and P^*_{bc}. According to Behrouzian and Bongiorno (2017), the circulating current reference can be calculated by:

$$i_z = \widehat{I}^z \cos\left(\omega_n t + \varphi^z\right), \tag{2.51}$$

where:

$$I^z = \frac{P^*_{ab} - A}{X_1 \cos(\varphi^z) + X_2 \sin(\varphi^z)} = \frac{P^*_{bc} - B}{X_3 \cos(\varphi^z) + X_4 \sin(\varphi^z)}, \tag{2.52}$$

$$\tan(\varphi^z) = \frac{(P^*_{bc} - B)X_1 - (P^*_{ab} - A)X_3}{(P^*_{ab} - A)X_4 - (P^*_{bc} - B)X_2}, \tag{2.53}$$

and the parameters A, B, X_1, X_2, X_3 and X_4 are given by equation (2.15).

A proportional controller is employed to track the reference of circulating current, as suggested by references (Hagiwara; Maeda; Akagi, 2012) and (Behrouzian; Bongiorno, 2017). Therefore, the voltage command v^*_z is obtained.

Regarding the modulation strategies, Hava, Kerkman and Lipo (1999) reveal that when zero sequence voltage components are employed, the dc-link voltage utilization is improved and the zero sequence signal is canceled in the line voltages. This study was originally proposed for 2-level converters. However, it can be extended for other topologies which do not have path for zero sequence current flow either.

Accordingly, the use of zero sequence signals can be approached for the DSCC-MMCC topology. This work uses the PS-PWM method with injection of 1/6 of third harmonic in the phase voltages (Ilves et al., 2014). The $(2N + 1)$ level modulation

is employed. The connection between the control and the modulation scheme for DSCC-MMCC is presented in Fig. 28 (a). On the other hand, the PS-PWM sinusoidal modulation is more suitable for the SDBC-MMC topology due to its path for zero sequence current flow. The connection between the control and the modulation scheme for SDBC-MMCC is presented in Fig. 28 (b).

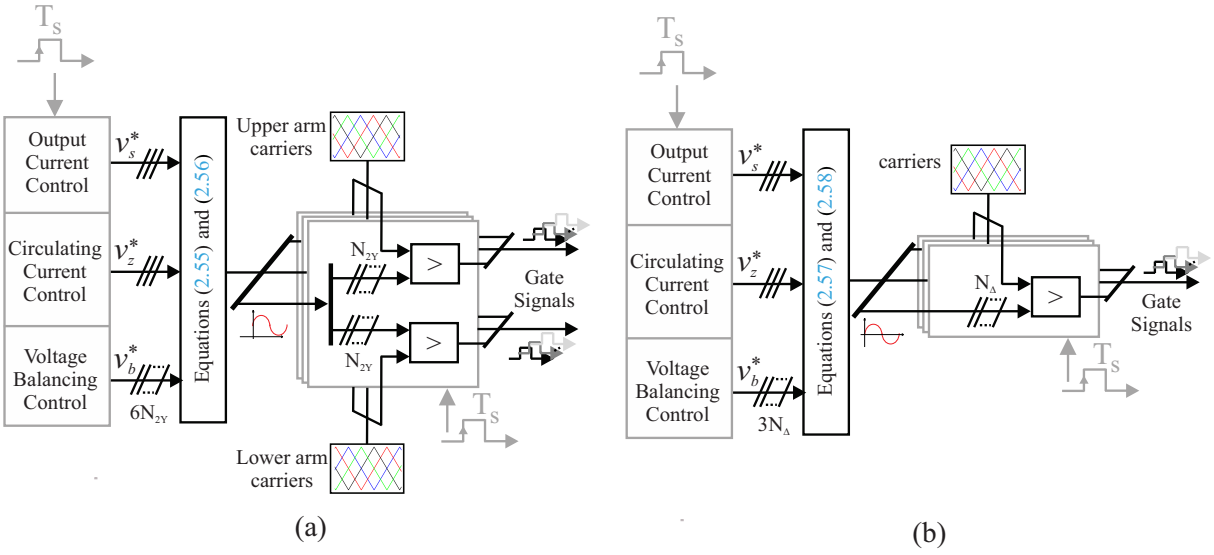

Figure 28 – Connection between the control and the modulation scheme for: (a) DSCC-MMCC; (b) SDBC-MMCC.

Since the PS-PWM method is employed, an extra individual balancing control loop is necessary to maintain the capacitor voltages following the reference v_c^*, as illustrated in Fig. 27 (d). As suggested by Hagiwara and Akagi (2009), a proportional controller k_b is employed. In this case, the individual balancing control law is given by:

$$v_b^* = k_b(v_c^* - v_{cf,i})sign(i_{t,i}), \tag{2.54}$$

where $i_{t,i}$ is the arm (i_u or i_l) or cluster current (i_{cl}) of the ith cell. $v_{cf,i}$ is obtained from the individual capacitor voltages through a moving average filter (MAF). This filter attenuates the capacitor voltage ripple, which improves the individual balancing performance (Sasongko et al., 2016).

As mentioned by Harnefors et al. (2013), the normalization strategy significantly affects the stability of the DSCC-MMCC closed loop system. The normalization performed in Hagiwara, Maeda and Akagi (2011) consists in the division of the reference signals by the measured sum of the capacitor voltages, since this sum is the real available voltage for output voltage synthesis. Nevertheless, this strategy results in instabilities, which requires the use of additional control loops (Antonopoulos; Angquist; Nee, 2009; Hagiwara; Maeda; Akagi, 2011). Interestingly, when the voltages are normalized by the voltage reference, the

circulating current control is stable and no additional control loops are required. As a drawback, errors are observed between the reference and synthesized voltages. However, such errors can be compensated by the output current control loops (Sharifabadi et al., 2016). This approach is adopted in this chapter. Therefore, for DSCC-MMCC, the normalized reference signals per phase are given by:

$$v_u^* = \frac{v_b^*}{v_c^*} + \frac{v_z^*}{v_c^*} - \frac{v_s^*}{N_{2Y} v_c^*} + \frac{1}{2}, \tag{2.55}$$

$$v_l^* = \frac{v_b^*}{v_c^*} + \frac{v_z^*}{v_c^*} + \frac{v_s^*}{N_{2Y} v_c^*} + \frac{1}{2}. \tag{2.56}$$

For SDBC-MMCC, an additional transformation is necessary since the dynamics presented in (2.49) are described per phase. The cluster voltages references v_{scl}^* can be obtained from $v_s{}^*$, based on the following transformation:

$$\begin{bmatrix} v_{scl,ab}^* \\ v_{scl,bc}^* \\ v_{scl,ca}^* \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{s,a}^* \\ v_{s,b}^* \\ v_{s,c}^* \end{bmatrix}. \tag{2.57}$$

Therefore, the normalized reference signal is given by:

$$v_{cl}^* = \frac{v_b^*}{v_c^*} + \frac{v_z^*}{v_c^*} + \frac{v_{scl}^*}{N_\Delta v_c^*}. \tag{2.58}$$

The switching pattern of the cells is generated by comparing the normalized reference signals ($v_{u,n}$ and $v_{l,n}$ for DSCC-MMCC and v_{cl}^* for SDBC-MMCC) with the phase-shifted triangular carrier waves. When the reference amplitude is above the carrier, the corresponding cell is inserted to the arm/cluster. When the reference amplitude is below the carrier, the corresponding cell is bypassed.

2.5 Chapter Conclusions

This chapter presented the main members of the MMCC family, their characteristics and predominant applications. The SDBC-MMCC and DSCC-MMCC topologies were selected as the most suitable for STATCOM application.

The mathematical modeling of both topologies was developed in order to verify their characteristics during unbalanced conditions. As observed, SDBC-MMCC is more affected by the negative sequence voltage than DSCC-MMCC, since its circulating increases considerably with the voltage unbalance factor.

Finally, the modulation and control strategies for an MMCC-based STATCOM were discussed and the details of each topology were presented.

Next chapter presents the design methodology of an MMCC-based STATCOM. A benchmarking of DSCC-MMCC and SDBC-MMC is presented, aiming to select the most suitable topology for STATCOM application.

3 Comparison of SDBC-MMCC and DSCC-MMCC for STATCOM Applications

3.1 Introduction

The main parameters of the MMCC circuit must be correctly designed to reduce the costs and to guarantee proper operation, Among the circuit parameters, the cell capacitance (Fujii; Schwarzer; De Doncker, 2005; Ilves et al., 2014; Xu; Xiao; Zhang, 2016), arm inductances (Tu et al., 2010; Xu; Xiao; Zhang, 2016) and power semiconductor specifications (Xu; Xiao; Zhang, 2016; Tsolaridis et al., 2016) are important issues already discussed in the literature. Many works consider HVDC applications, where balanced currents flow through the converter. Nevertheless, when the negative sequence currents are compensated by the MMCC-based STATCOM, different voltage ripples and current stresses are observed in the converter cells. Therefore, literature lacks a detailed design methodology of the MMCC-based STATCOM considering both positive and negative sequence current compensation.

Conversely, few works in the literature present a comparison between SDBC-MMCC and DSCC-MMCC topologies for STATCOM applications. Akagi (2011) only discuss the differences in terms of the number of cells. Additionally, Tsolaridis et al. (2016) compare the losses and costs of SDBC-MMCC and DSCC-MMCC topologies for STATCOM application based on a 100 MVA case study. However, the cell capacitances are designed using different approaches and the comparisons are not presented analytically. Moreover, the comparison of the energy storage requirements is not accomplished. Also, in terms of converter losses, Tsolaridis et al. (2016) only include the power semiconductor devices contributions in the power losses evaluation.

In view of the aforementioned facts, this chapter presents the following contributions:

- comparison of SDBC-MMCC and DSCC-MMCC topologies considering the number of cells, effective dc-link voltage and current rating. These comparisons are supported by analytical results;

- achievement of mathematical expressions for the energy storage requirements and the minimum required cell capacitance when positive and negative sequence currents flow through the MMCC;

- evaluation of MMCC-based STATCOM dynamic behavior, power losses and costs.

The case study considers a 17 MVA STATCOM connected to a 13.8 kV grid. The PS-PWM modulation strategy is employed. The control strategies implemented to evaluate the dynamic behavior are the previously presented in Section 2.4.

3.2 Design of passive elements

This section presents the design of both DSCC-MMCC and SDBC-MMCC topologies. The design methodology is focused on applications where positive and/or negative sequence current injection is required, as in the grid voltage regulation or support to renewable energy systems.

3.2.1 Switching frequency

The switching frequency is an important issue in the MMCC converter design. Indeed, if the switching frequency is increased, two phenomena are observed. Firstly, the power losses in the semiconductor devices increase and the overall efficiency is reduced. Secondly, the capacitor voltage balancing is more easily reached. Therefore, the choice of the switching frequency is a compromise between two tasks: reduction of power losses and acceptable capacitor voltage balancing.

Sasongko et al. (2016) discuss the stability of the DSCC-MMCC capacitor voltage balancing for various values of carrier frequency. The presented analysis shows interesting values for switching frequency are 2.5 times, 3.5 times or 4 times the line frequency. The first value results in minimum losses, while the last results in better dynamic performance and capacitor voltage balancing. Nevertheless, Ilves et al. (2015a) show switching frequencies integer multiple of the line frequency may cause instability in the capacitor voltage balancing. Therefore, $f_c = 210Hz$ is employed in this work, which corresponds to 3.5 times the line frequency (60 Hz). The same value is used in the SDBC-MMCC topology.

Since the ac component in v_c works as a disturbance in the current control system, it should be eliminated by a moving average filter. According to Sasongko et al. (2016), the moving window time must be set to:

$$1/f_{ma} = f'_n/f_n, \tag{3.1}$$

where f'_n is obtained from the irreducible fraction of the carrier frequency f_c with respect to the supply frequency f_n, denoted by f'_c/f'_n.[1] This tuning result in minimum memory

[1] For example, when $f_c = 210$ Hz and $f_n = 60$ Hz, $f'_c/f'_n = 7/2$. Therefore, $f'_c = 7$ and $f'_n = 2$. Thereby, $1/f_{ma} = 2/f_n$.

requirements for the moving average filter implementation (Sasongko et al., 2016).

3.2.2 Effective Dc-link Voltage and Number of Cells

Despite the absence of a physical dc-link in SDBC-MMCC-based STATCOM, the effective dc-link voltage is an important parameter to avoid overmodulation (Fujii; Schwarzer; De Doncker, 2005). The minimum value of the effective dc-link voltage is given by:

$$v_{dc,2Y} = \frac{2\sqrt{2}}{\sqrt{3}(1 - E_{dc} - \Delta v_{dc})} \frac{V_s}{\Lambda_{2Y} m_{max}}, \tag{3.2}$$

$$v_{dc,\Delta} = \frac{\sqrt{2}}{(1 - E_{dc} - \Delta v_{dc})} \frac{V_s}{\Lambda_{\Delta} m_{max}}, \tag{3.3}$$

where $\Delta v_{dc}(\%)$ is the dc-link voltage ripple in the worst case and $E_{dc}(\%)$ is the average error in steady-state. The modulation gain Λ is included to extend the analysis to different modulation strategies. Furthermore, the maximum modulation index m_{max} is determined according to the carrier frequency f_c and the minimum IGBTs on-time and dead-time T_d (Fujii; Schwarzer; De Doncker, 2005). Accordingly:

$$m_{max} = \left(\frac{1}{f_c} - 2T_d\right) f_c. \tag{3.4}$$

The minimum line-to-line voltage (rms) synthesized by the converter V_s is calculated according to the grid voltage V_g and the maximum per unit value of the output impedance x_{eq}. Perceptual variations in these variables are assumed. Therefore, V_s is given by:

$$V_s = [(1 + \Delta V_g) + x_{eq}(1 + \Delta x_{eq})]V_g. \tag{3.5}$$

The number of cells is determined according to the effective dc-link voltage v_{dc} by:

$$N_{2Y} = \frac{1}{f_{us}} \frac{v_{dc,2Y}}{V_{svc}}, \tag{3.6}$$

$$N_{\Delta} = \frac{1}{f_{us}} \frac{v_{dc,\Delta}}{V_{svc}}, \tag{3.7}$$

where f_{us} is defined by the ratio between the cells reference voltage v_c^* and semiconductor device voltage class V_{svc}. Manufactures suggest semiconductor devices should not operate with voltages above 60 - 75 % of V_{svc}, depending on the device technology, place of installation and incidence of cosmic rays (ABB, 2017a; Prado; Gajo, 2017).

Indeed, the ratio K_N between the number of cells of SDBC-MMCC and DSCC-MMCC topologies, can be expressed by:

$$K_N = \frac{N_\Delta}{N_{2Y}} = \frac{v_{dc,\Delta}}{v_{dc,2Y}} = \frac{\sqrt{3}}{2}\frac{\Lambda_{2Y}}{\Lambda_\Delta}. \tag{3.8}$$

As observed, if the same modulation gain is employed for both topologies, $K_N \approx 0.87$ and the SDBC-MMCC topology presents 13% less cells. Regarding the modulation strategies, Hava, Kerkman and Lipo (1999) show when zero sequence voltage components are employed, the dc-link voltage utilization is improved and the zero sequence signal is canceled in the line voltages. This study was originally proposed in 2-level converters, however, it can be extended for other topologies which also does not have path for zero sequence current flow. Therefore, the use of zero sequence signals can be approached for DSCC-MMCC topology. On the other hand, the sinusoidal modulation is more suitable for SDBC-MMCC topology since it presents a path for zero sequence current flow.

Considering the modulation with injection of 1/6 of third harmonic for DSCC-MMCC, $\Lambda_{2Y} = 1.15$. In this work, $\Delta V_g = \Delta x_{eq} = 0.05$, $x_{eq} = 0.15$, $\Delta v_{dc} = 0.1$, $E_{dc} = 0.03$ and $T_d = 1.5\mu s$. Under such conditions, $V_s \approx 16.7$ kV. Therefore, the approximate value of the effective dc-link voltage is $v_{dc,2Y} = 28$ kV. For SDBC-MMCC, considering the sinusoidal modulation, $\Lambda_\Delta = 1$. Therefore, the approximate value for the effective dc-link voltage is $v_{dc,\Delta} = 28$ kV. Thereby, considering semiconductors with voltage class of 3.3 kV and $f_{us} = 0.5$, $N_{2Y} = N_\Delta = 17$.

Finally, the total number of semiconductor switches N_s is given by:

$$N_s = 12N_{2Y,\Delta}. \tag{3.9}$$

Therefore, if $N_{2Y} = N_\Delta$, the topologies will present the same number of semiconductor switches.

3.2.3 Arm and Cluster Currents

Considering the suppression of harmonic components, the circulating current of DSCC-MMCC can be expressed by Yue et al. (2016):

$$i_z = \frac{m^+}{4}\left[\widehat{I}^+ cos(\delta^+ - \varphi^+) + \widehat{I}^- cos(\delta^+ - \varphi^- - \theta_v)\right]$$

$$+\frac{m^-}{4}\left[\widehat{I}^+ cos(\delta^- - \varphi^+ + \theta_v) + \widehat{I}^- cos(\delta^- - \varphi^-)\right]. \tag{3.10}$$

The maximum value of the upper arm current is given by (Farias et al., 2018):

$$\max(i_u) = \max(i_z) + \frac{1}{2}\max(i_g). \tag{3.11}$$

In this first analysis, for simplification, the grid voltage is assumed to be balanced and the negative sequence voltage synthesized by the converter is considered much smaller than the synthesized positive sequence. Therefore, $m^- \approx 0$. Furthermore, considering STATCOM application, $cos(\delta^+ - \phi^+) = 0$. Thus, the peak value of arm current is given by:

$$\max(i_u) = \widehat{I}_n \left(\frac{1}{2} + \frac{m^+}{4}\right) \approx \frac{3}{4}\widehat{I}_n, \tag{3.12}$$

where $m^+ \approx 1$ is assumed and:

$$\widehat{I}_n = \frac{\sqrt{2}}{\sqrt{3}}\frac{S_n}{V_g}, \tag{3.13}$$

and S_n is the STATCOM rated power.

For SDBC-MMCC, the maximum value of cluster currents can be expressed as (Hagiwara; Maeda; Akagi, 2012):

$$\max(i_{cl}) = \frac{2}{\sqrt{3}}\widehat{I}_n. \tag{3.14}$$

Thereby, the topologies can be compared through the current ratio K_I, given by:

$$K_I = \frac{\max(i_u)}{\max(i_{cl})} \approx \frac{3\sqrt{3}}{8}. \tag{3.15}$$

As observed, the SDBC-MMCC current rating is 54 % larger than the DSCC-MMCC topology.

3.2.4 Cell Capacitance

The cell capacitance can be designed based on the converter energy storage requirements. According to Ilves et al. (2014), the minimum cell capacitance for DSCC-MMCC topology is given by:

$$C_{2Y} = \frac{2N_{2Y}E_{2Y}}{v_{dc,2Y}^2}. \tag{3.16}$$

E_{2Y} is the minimum value of the nominal energy storage per arm. Considering only the upper arm due to symmetry, E_{2Y} is given by (Ilves et al., 2014):

$$E_{2Y} = \frac{\Delta E_{2Y}}{k_{max}^2 - \max(\frac{n_u^2 - e_{u,v}k_{max}^2}{1 - e_{u,v}})}, \tag{3.17}$$

where k_{max} defines the upper limit of the capacitor voltages. Typically, $k_{max} = 1.1$ is employed. Finally:

$$n_u = \frac{v_u}{v_{dc,2Y}}, \tag{3.18}$$

$$e_{u,v} = \frac{e_u}{\Delta E_{2Y}}. \tag{3.19}$$

where $\Delta E_{2Y} = max(e_u)$ is the maximum energy variation and v_u is the upper arm inserted voltage. n_u and $e_{u,v}$ are the normalized values for inserted voltages and instantaneous energy, respectively. For SDBC-MMCC, similar relations can be derived where e_u is replaced by e_{cl}.

As observed, the energy variations e_u and e_{cl} must be known to complete the design methodology. These energy variations can be obtained from:

$$e_u = \int p_u dt = \int v_u i_u dt,$$

$$e_{cl} = \int p_{cl} dt = \int v_{cl} i_{cl} dt. \tag{3.20}$$

Therefore, expressions for the instantaneous power are derived. The analysis is accomplished per phase and the most stressed one is considered in the design. For DSCC-MMCC topology, assuming the injection of 1/6 of third harmonic component, the upper arm inserted voltages can be expressed as (Ilves et al., 2014):

$$v_u = \frac{v_{dc,2Y}}{2} - \frac{v_{dc,2Y}}{2} m \cos(\omega_n t + \theta_v) + \frac{v_{dc,2Y}}{12} m \cos(3\omega_n t). \tag{3.21}$$

Furthermore, the upper arm current for DSCC-MMCC topology is given by (Hagiwara; Akagi, 2009):

$$i_u = i_z + \frac{i_g}{2}. \tag{3.22}$$

The energy variation in the upper arm can be obtained by performing the integration. Accordingly:

$$e_u = \frac{S_n}{12\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{1u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{2u}\right] + \frac{S_n}{12m\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{3u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{4u}\right], \tag{3.23}$$

where

$$f_{1u} = \frac{m}{9}\cos(\varphi^+)\sin(3\omega_n t) + \frac{1}{6}\sin(2\omega_n t - \varphi^+ - \theta_v) +$$

$$+\frac{1}{12}\sin(4\omega_n t + \varphi^+ + \theta_v), \tag{3.24}$$

$$f_{2u} = \frac{m}{9}\cos(\varphi^- - \theta_v)\sin(3\omega_n t) + \frac{1}{6}\sin(2\omega_n t - \varphi^- + \theta_v) +$$

$$+\frac{1}{12}\sin(4\omega_n t + \varphi^- - \theta_v), \tag{3.25}$$

$$f_{3u} = -2m^2\cos(\varphi^+)\sin(\omega_n t + \theta_v) -$$

$$-m\sin(2\omega_n t + \varphi^+ + 2\theta_v) + 4\sin(\omega_n t + \varphi^+ + \theta_v), \tag{3.26}$$

$$f_{4u} = -2m^2\cos(\varphi^- - \theta_v)\sin(\omega_n t + \theta_v) -$$

$$-m\sin(2\omega_n t + \varphi^-) + 4\sin(\omega_n t + \varphi^- - \theta_v). \tag{3.27}$$

The maximum energy variation is given by:

$$\Delta E_{2Y} = max(e_u). \tag{3.28}$$

From (3.23), ΔE_{2Y} is proportional to the converter rated power. From (3.17), E_{2Y} is also proportional to the converter rated power. Therefore, the converter energy storage requirements can be expressed by:

$$W_{2Y} = \frac{6}{S_n} E_{2Y}, \tag{3.29}$$

where W_{2Y} is the required energy storage per MVA.

For SDBC-MMCC, the inserted voltages are given by (Hagiwara; Maeda; Akagi, 2012):

$$v_{cl} = m v_{dc,\Delta} \cos\left(\omega_n t + \theta_v + \frac{\pi}{6}\right). \tag{3.30}$$

Therefore, the energy storage variation per cluster is given by:

$$e_{cl} = \frac{S_n}{6m\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{1cl} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{2cl}\right], \tag{3.31}$$

where

$$f_{1cl} = m \sin\left(2\omega_n t - \varphi^+ - \theta_v + \frac{\pi}{3}\right), \tag{3.32}$$

$$f_{2cl} = -m \sin\left(2\omega_n t + \varphi^- + \theta_v - \frac{\pi}{3}\right) + m \sin\left(2\omega_n t - \varphi^-\right). \tag{3.33}$$

Therefore, the energy storage requirements for SDBC-MMCC topology can be expressed by:

$$W_\Delta = \frac{3}{S_n} E_\Delta, \tag{3.34}$$

where E_Δ can be computed analogously to E_{2Y}.

Thereby, the following conclusions can be stated:

- DSCC-MMCC presents energy variations in the frequencies ω_n and $2\omega_n$ while SDBC-MMCC presents energy variations only in $2\omega_n$;
- the storage energy variation depends on the converter rated power S_n, modulation index, positive sequence power angle φ^+, negative sequence power angle φ^- and per unit values of positive and negative sequence currents;
- when the STATCOM exchanges both positive and negative sequence currents, the different angular contributions caused by θ_v in (3.27) result in different stresses in the converter phases. Therefore, the energy storage requirements must to be analyzed per phase. The phase with the highest energy requirements is used to compute ΔE_{max}. Additionally, the most critical case depends on the angle φ^-;
- the energy variation is proportional to the converter rated power.

As mentioned by Farias et al. (2018), the worst case for DSCC-MMCC topology in terms of energy requirements corresponds to $\varphi^+ = \varphi^- = \pi/2$, which means inductive

reactive power transfer. Similar conclusions can be obtained for SDBC-MMCC topology. Therefore, the energy storage requirements W_{2Y} and W_{Δ} can be computed considering $\widehat{I}^{+}$ and $\widehat{I}^{-}$, ranging from 0 to 1 pu, $k_{max} = 1.1$ and $\varphi^{+} = \varphi^{-} = \pi/2$. The surface is plotted in Fig. 29 (a) and (b). As observed, energy storage requirements increase with the current processed by the converter. Furthermore, W_{Δ} is more sensitive to the negative sequence current, due to the circulating current characteristics.

Nevertheless, the positive and negative sequence components cannot be chosen arbitrarily, since the converter rated current cannot be exceeded. Actually, since $\varphi^{+} = \varphi^{-} = \pi/2$, the capability curve of MMCC is defined by the equation:

$$\widehat{I}^{+} + \widehat{I}^{-} = \widehat{I}_{n}. \tag{3.35}$$

Therefore, the minimum energy storage requirement is given by the maximum intersection between the energy storage requirements surface and the converter capability surface. Accordingly, the maximum required value of W_{2Y} is approximately 39 kJ/MVA, as shown in Fig. 29 (a). Similarly, W_{Δ} is 20 kJ/MVA, as observed in Fig. 29 (b).

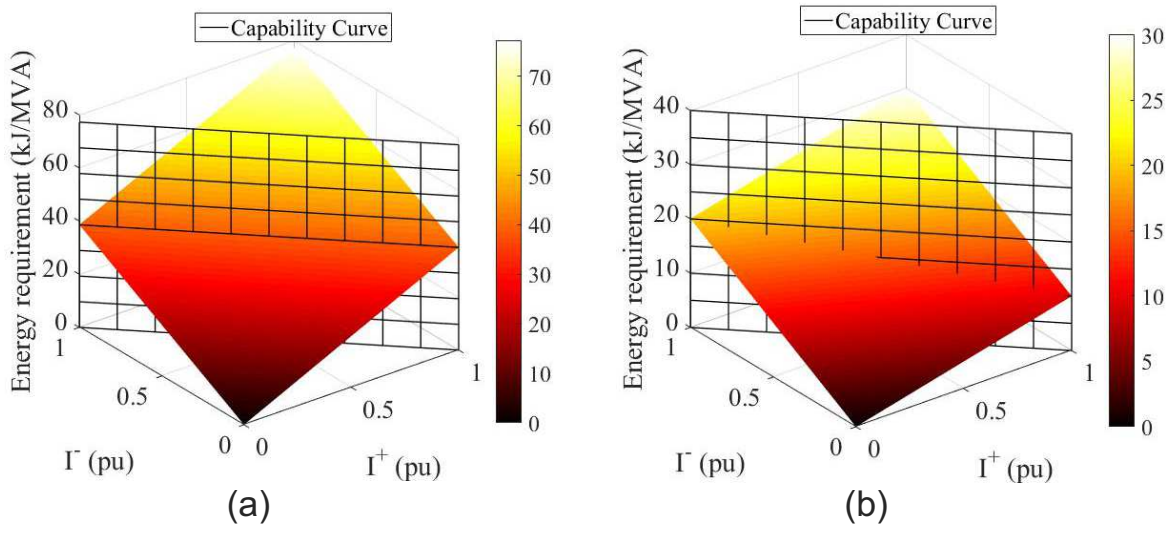

Figure 29 – Energy storage requirements according to the positive and negative sequence current components: (a) DSCC-MMCC topology; (b) SDBC-MMCC topology.

The energy ratio K_e is defined to compare the energy storage requirements of both topologies as follows:

$$K_e = \frac{W_{2Y}}{W_{\Delta}}. \tag{3.36}$$

Considering the design point, $K_e = 39/20 \approx 2$. Therefore, DSCC-MMCC topology energy storage requirement is twice the amount of SDBC-MMCC. Additionally, the cell

capacitance ratio of each topology is given by:

$$K_c = \frac{C_\Delta}{C_{2Y}} = \frac{\sqrt{3}}{K_e}\frac{\Lambda_{2Y}}{\Lambda_\Delta}. \tag{3.37}$$

For the considered modulation strategies $K_c \approx 1$ and $C_\Delta \approx C_{2Y}$. Using the effective dc-link voltage and the number of cells, $C_\Delta = C_{2Y} = 5$ mF is obtained.

At this point, two important issues must be mentioned about the energy storage requirements derived in this work. Firstly, some works in literature propose the insertion of zero sequence components and/or harmonics in the circulating current to change the shape of the capacitor voltage waveform (Picas et al., 2012; Picas et al., 2013; Perez; Bernet, 2015). Under such conditions, the energy storage requirements can be reduced. Nevertheless, these strategies tend to increase the circulating current rms value, which may increase the power losses and affect the overall converter efficiency (Li et al., 2018). For this reason, these strategies are not approached in this work.

Secondly, the energy storage requirements obtained in this section considers a STATCOM applied to grid voltage support or renewable energy systems. When flicker compensation of arc furnaces is considered, the mitigation of low-frequency oscillations are as important as the negative sequence compensation (Hagiwara; Maeda; Akagi, 2012). Under such conditions, the low frequency components will affect the energy variation and consequently higher energy storage requirements are expected. Nevertheless, the study of this phenomenon is beyond the scope of this Ph.D dissertation and it can be approached in future works.

3.2.5 Arm and Cluster Inductances

Most works in literature are focused on the design of arm inductance for DSCC-MMCC topology. First of all, the arm inductance is responsible for improving the circulating current characteristic. Li, Jones and Wang (2017) derive the following expression for the peak-peak circulating current ripple in DSCC-MMCC topology in HVDC applications:

$$\Delta i_z = \frac{N_{2Y} T}{8\omega_n L_{arm} C_{2Y}} \sqrt{\frac{9}{16}\widehat{I}_n + \frac{1}{9} i_{dc} - \frac{1}{2}\widehat{I}_n i_{dc}}, \tag{3.38}$$

where $T = 1/(N f_c)$, $\widehat{I}_g$ is the peak of grid currents and i_{dc} is the dc-link current. This relation can be simplified for STATCOM application since $i_{dc} = 0$. Furthermore, considering the design at rated conditions, the arm inductance can be computed as follows:

$$L_{arm} = \frac{3}{32 C_{2Y} \omega_n f_c}\frac{\widehat{I}_n}{\Delta i_z}. \tag{3.39}$$

Moreover, the arm inductance is responsible for limiting fault currents. If the most critical fault is considered (a short circuit fault is applied between the positive and negative dc-buses), the arm inductance which limits the fault current is calculated through (Tu et al., 2010):

$$L_{arm} = \frac{v_{dc,2Y}}{2\alpha}, \tag{3.40}$$

where α (kA/s) is the maximum current rise rate.

Finally, there is a resonance frequency resultant from the interaction of cell capacitances and arm inductances that must be avoided. Ilves et al. (2012) show the product of the arm inductor and the cell capacitance for DSCC-MMCC topology has to satisfy the following relation:

$$L_{arm}C_{2Y} > \frac{5N_{2Y}}{48\omega_n^2}. \tag{3.41}$$

According to (3.40), if the maximum current rise rate is $\alpha = 0.1$ (kA/μ s) (Xu; Xiao; Zhang, 2016), the minimum value of arm inductance is 0.14 mH (0.0047 pu), by applying (3.41), $L_{arm} > 2.5$ mH (≈ 0.08 pu).

Typically, the per unit inductance values for grid connected converters are limited at the range of 0.3 pu for both DSCC-MMCC and SDBC-MMCC topologies. This work employs 0.15 pu for both topologies. According to equation (3.39), this value results in a circulating current ripple lower than 5.5 % at rated conditions for DSCC-MMCC topology. Thus, $L_{arm} = L_{cl} = 4.5$ mH.

3.3 Comparison of MMCC STATCOM Topologies

The comparisons of MMCC topologies are based on the dynamic behavior, operation during negative sequence current injection, power losses and cost. The losses in the power semiconductors, inductors and cell capacitors are taken into account. The parameters of both converters are presented in Tab. 4. The controller gains are presented in Appendix A.

The first case study considers only positive sequence injection. Under such conditions, the trapezoidal reactive power profile presented in Fig. 30 is employed. The aim is to verify if the performance of the capacitor voltage balancing and the selected parameters are suitable for the application.

The second case study considers negative sequence current injection to prove the effectiveness of the proposed design methodology. All simulations are performed in PLECS® environment aiming to validate the proposed design methodology. Three operational conditions are analyzed:

Table 4 – Parameters of the MMCC topologies.

Parameter	Value
Grid voltage (V_g)	13.8 kV
Line frequency (f_n)	60 Hz
Effective dc-link voltage ($v_{dc,2Y}, v_{dc,\Delta}$)	28 kV
Rated power (S_n)	17 MVA
Transformer inductance (L_g)	1.35 mH
Transformer X/R ratio	18
Arm,Cluster inductances (L_{arm}, L_{cl})	4.5 mH
Arm inductor X/R ratio	15.1
Cluster inductor X/R ratio	20.4
Cell capacitance (C_{2Y}, C_{Δ})	5 mF
Nominal cell voltage ($v^*_{sm,n}$)	1.65 kV
Carrier frequency (f_c)	210 Hz
Number of cells (N_{2Y}, N_{Δ})	17

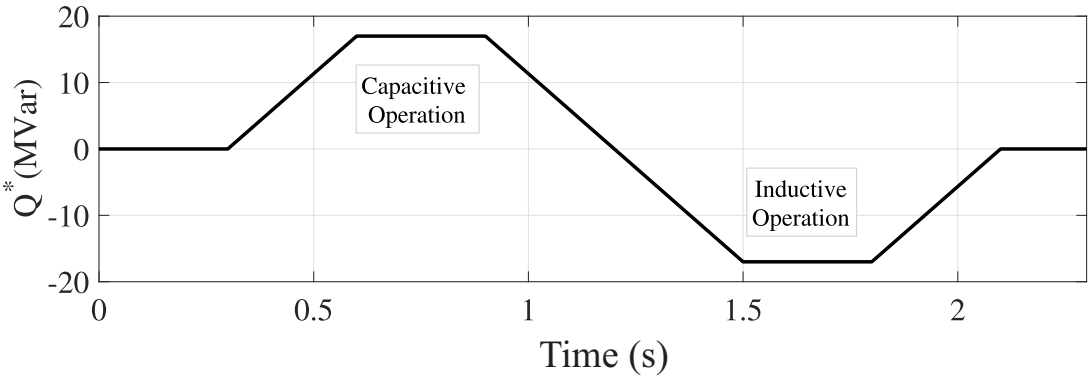

Figure 30 – Reactive power profile used in the first case study.

- Case 1: $0 \leq t \leq 0.2$ seconds: 1 pu of positive sequence reactive power is absorbed from the power grid;
- Case 2: $0.2 < t \leq 1$ seconds: 0.5 pu of positive sequence reactive power and 0.5 pu of negative sequence current are injected into the grid ($\varphi^+ = \varphi^- = \pi/2$);
- Case 3: $0.8 < t \leq 1.4$ seconds: 1 pu of negative sequence reactive current is injected into the grid ($\varphi^- = \pi/2$).

Power losses in the semiconductors are estimated through the model proposed by Tu and Xu (2011b), Sangwongwanich et al. (2016). The conduction, switching losses and thermal impedances are obtained from datasheets (Sangwongwanich et al., 2016). DSCC-MMCC topology employs an IGBT part number 5SNA 0800N330100 while SDBC-MMCC topology employs an IGBT part number 5SNA 1200E330100. Both power modules are manufactured by ABB. Different IGBTs are employed since DSCC-MMCC and SDBC-MMCC topologies present different current ratings.

Regarding the inductor losses evaluation, the powder cores and the windings are designed according to the guidelines presented in (MAGNETICS, 2006). The inputs of the design procedure are the desired inductance and the peak current. Based on these variables, the maximum energy storage in the inductor is computed and the core can be selected. Then, an iterative process is used to determine the number of turns. The winding is based on Litz wire to mitigate the skin effect.

The winding losses are calculated by simulations using the inductor resistance. For simplification, the contributions of proximity and skin effects are disregarded, as suggested by Cota et al. (2015). Additionally, the magnetic losses are estimated through the improved generalized Steinmetz equation method (iGSE) (Muhlethaler; Kolar; Ecklebe, 2011), since the flux density waveforms are not sinusoidal.

The power losses of the cell capacitors include the ohmic loss in the ESR and the dielectric losses. These losses are estimated following the methodology proposed by Electronicon (2013). High density Electronicon film capacitors are considered.

The costs are evaluated according to the methodology presented in (Engel et al., 2015). According to this reference, the cost of the capacitors employed in the cells are 150 €/kJ. Furthermore, the cost of the magnetic devices K_{mag} in euros can be estimated by (Engel et al., 2015; Siddique et al., 2016):

$$K_{mag} = 4000 N_{mag} + 723000 A_p, \tag{3.42}$$

where N_{mag} is the number of inductors. For DSCC-MMCC, $N_{mag} = 6$ is assumed while $N_{mag} = 3$ is assumed for SDBC-MMCC topology. A_p is known as area product and consists in the product of the winding window area (A_w) and the cross section area (A_c) of the magnetic core.

Finally, the additional costs (IGBTs, cabinets, control, etc) can be approximated by 3.5 €/kVA of the installed switching power P_{sw}, which is given by (Siddique et al., 2016):

$$P_{sw} = N_s V_{svc} I_{svc}, \tag{3.43}$$

where I_{svc} is the device rated current. The parameters employed in the losses and cost evaluation are presented in Tab. 5.

Table 5 – Parameters employed in the losses and cost evaluation.

Parameter	DSCC-MMCC	SDBC-MMCC
Inductor resistance	112 mΩ	83.1 mΩ
Capacitor ESR	0.167 mΩ	0.167 mΩ
Total Storage Energy	691.6 kJ	311.3 kJ
Area product	$3.4 \cdot 10^{-3}$ m^4	$7.1 \cdot 10^{-3}$ m^4
Installed Switching Power	538.56 MVA	807.84 MVA

3.4 Dynamic Performance and Steady-State Evaluation

3.4.1 Case Study 1: Positive Sequence Injection

Firstly, the reactive power reference profile of Fig. 30 is applied to DSCC-MMCC control. The instantaneous active and reactive powers are presented in Fig. 31 (a). As observed, the reactive power exchanged follows the reference profile. Furthermore, the active power presents a low average value which corresponds to the converter losses ($\approx$ 1 %). The grid currents, shown in Fig. 31 (b), present the same envelope of the reactive power.

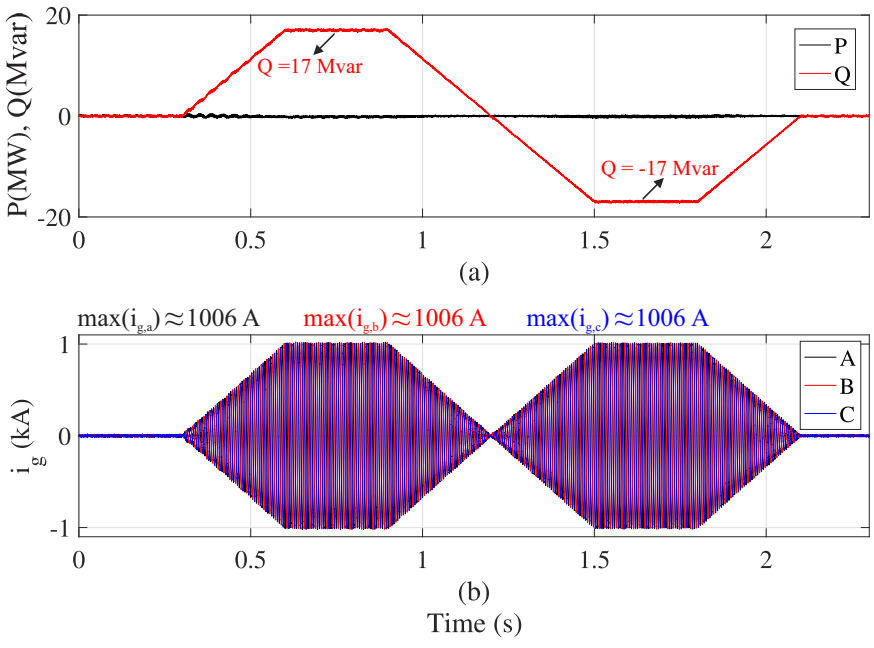

Figure 31 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive sequence injection: (a) instantaneous active and reactive power; (b) grid currents.

Figure 32 (a) shows the upper arm currents. The lower arms present similar behavior and were not presented here. Since only positive sequence currents are injected, the arm currents amplitude is the half of the grid current amplitude. The circulating currents are presented in Fig. 32 (b). As observed, its average value is null as predicted by the

theoretical analyses. Furthermore, the circulating current ripple is smaller than 5%, which validates the arm inductance design.

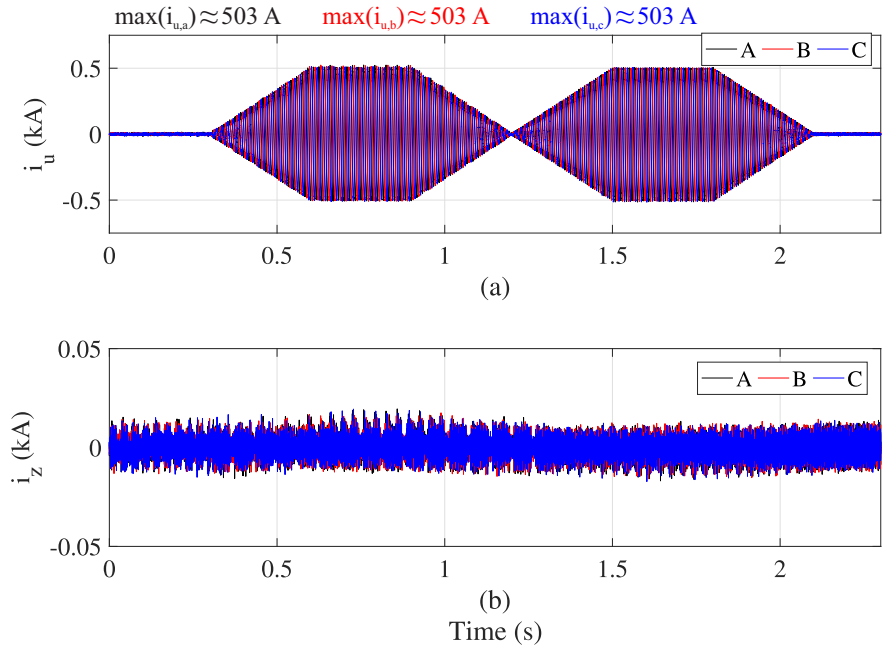

Figure 32 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive sequence injection: (a) upper arm currents; (b) circulating currents.

The cell voltages for the upper arm of phase A are presented in Fig. 33 (a). The dashed lines indicate the 10 % tolerance band adopted in the capacitance design. As observed, during the capacitive operation, the capacitor voltage waveforms present values larger than the upper tolerance band. An analogous phenomenon is observed in the lower tolerance band during inductive operation. The detailed views presented in Fig. 33 (b) and (c) show that phenomena are related to the capacitor voltage balancing.

Indeed, the energy storage requirements previously derived assume all capacitor voltages are perfectly balanced. When the capacitor voltages of the same arm are averaged, Fig. 34 (a) is obtained. As observed, the average value of capacitor voltages is within the tolerance band limits. This fact can be verified in the detailed views presented in Fig. 34 (b) and (c). These results validates the energy storage requirements previously derived. Nevertheless, as observed in Fig. 33 (a), higher values must be employed to guarantee all capacitor voltages remain within the defined tolerant bands.

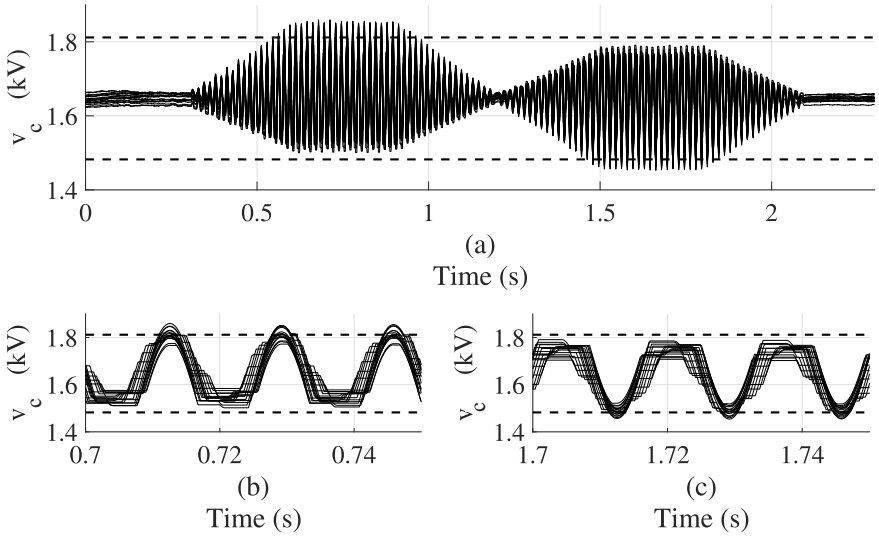

Figure 33 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive sequence injection: (a) cell voltages in the upper arm of phase A (N_{2Y} signals); (b) detailed view for capacitive operation; (c) detailed view for inductive operation.

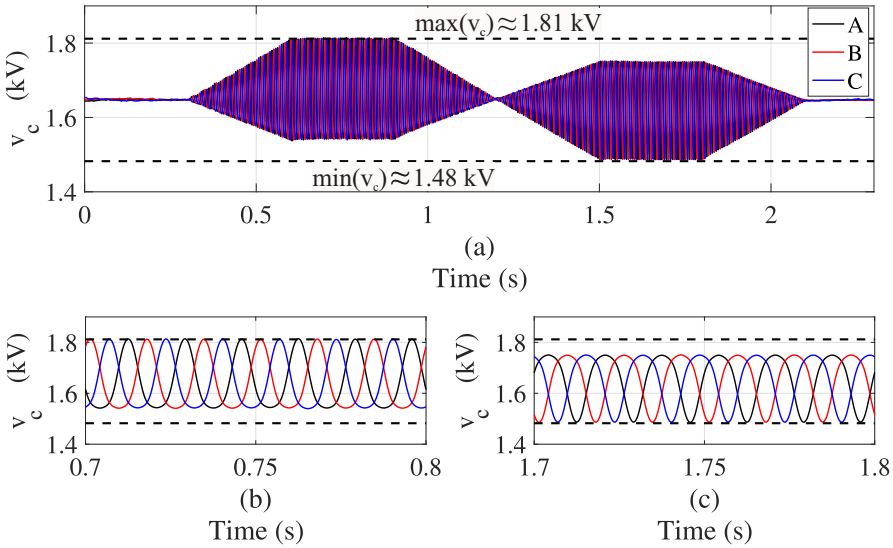

Figure 34 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive sequence injection: (a) average cell voltages (per phase); (b) detailed view for capacitive operation; (c) detailed view for inductive operation.

Then, the reactive power reference profile of Fig. 30 is applied to SDBC-MMCC control. The instantaneous active and reactive powers are presented in Fig. 35 (a). As observed, the reactive power exchanged with the grid follows the reference profile. Again, the active power presents a low average value which correspond to the converter losses ($\approx$ 0.5 %). The grid currents presented in Fig. 35 (b) also follows the same shape of reactive power.

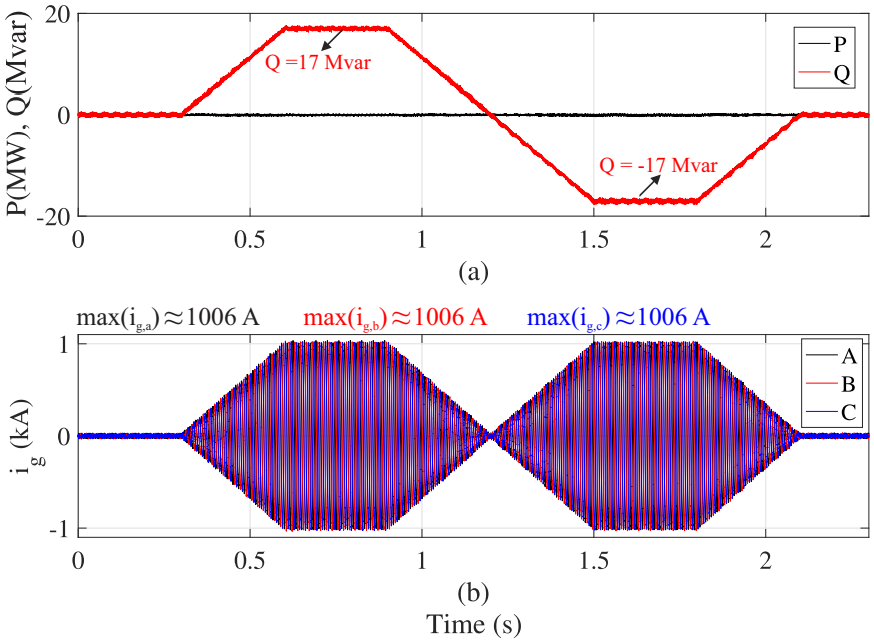

Figure 35 – Dynamic behavior of SDBC-MMCC-based STATCOM for positive sequence injection: (a) instantaneous active and reactive power; (b) grid currents.

Figure 36 (a) shows the cluster currents. Since only positive sequence currents are injected, the amplitude of arm currents is $\frac{1}{\sqrt{3}}$ of the grid currents amplitude. The circulating current is presented in Fig. 36 (b). As observed, its average value is null as predicted by the theoretical values. Furthermore, the circulating current ripple is smaller than 10%.

The cell voltages for the cluster AB are presented in Fig. 37 (a). The dashed lines indicate the 10 % tolerance band adopted in the capacitor voltage design. As observed, for both capacitive and inductive operation, the capacitor voltages waveforms are within the tolerant band limits. The detailed views presented in Fig. 37 (b) and (c) shows the capacitor voltages are well balanced. When the capacitor voltages of the same cluster are averaged, Fig. 38 is obtained. As observed, the average value of capacitor voltages is within the tolerance band limits and presents a significant second order harmonic component. Since the capacitance was designed for negative sequence injection (which is the critical condition for SDBC-MMCC), during positive sequence injection the ripple is lower than the 10 % defined in the design methodology.

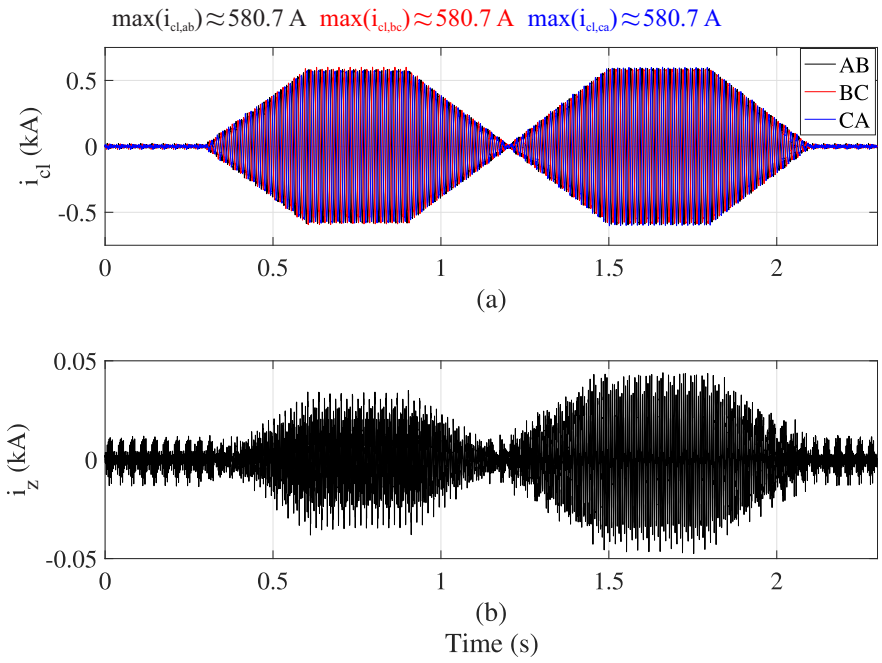

Figure 36 – Dynamic behavior of SDBC-MMCC-based STATCOM for positive sequence injection: (a) cluster currents; (b) circulating current.

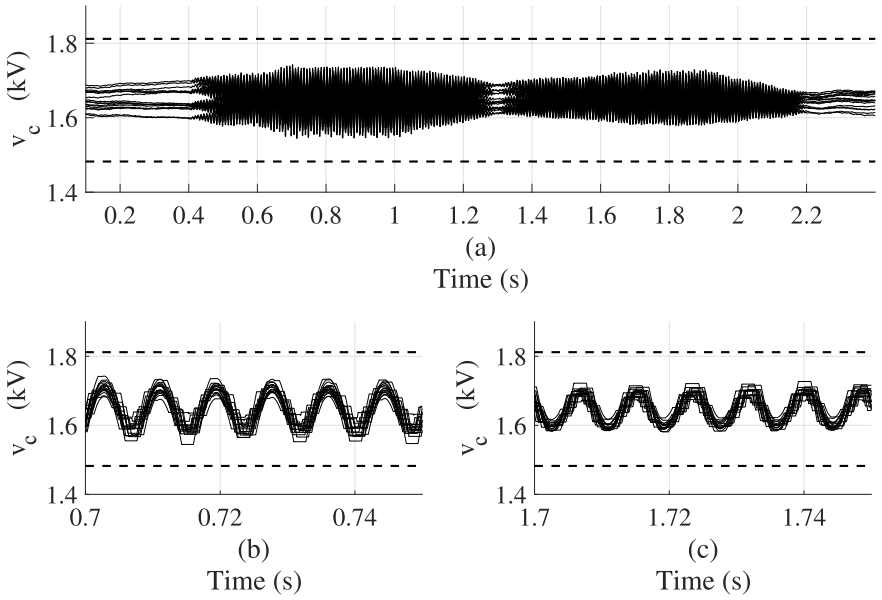

Figure 37 – Dynamic behavior of SDBC-MMCC-based STATCOM for positive sequence injection: (a) cell voltages in the cluster AB (N_Δ signals); (b) detailed view for capacitive operation; (c) detailed view for inductive operation.

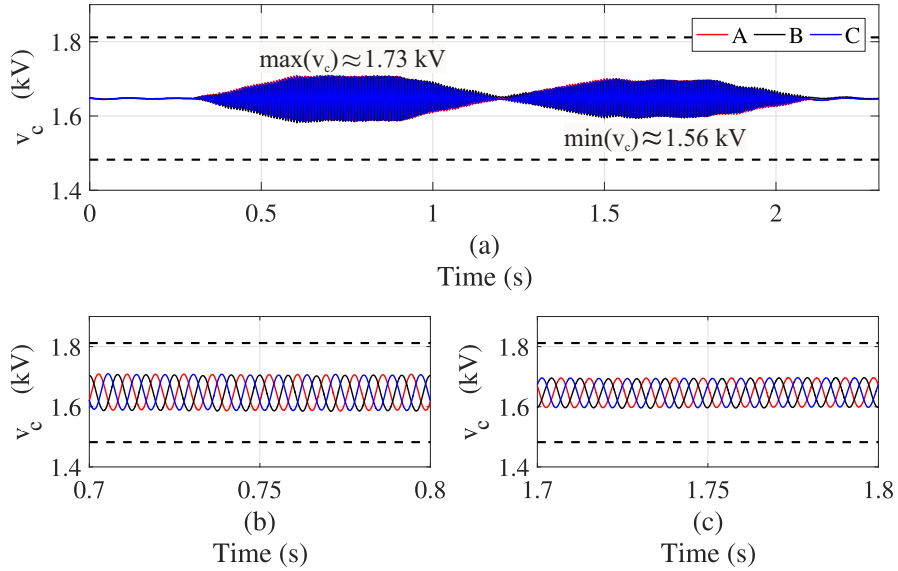

Figure 38 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive sequence injection: (a) average cell voltages (per cluster); (b) detailed view for capacitive operation; (c) detailed view for inductive operation.

3.4.2 Case Study 2: Positive and Negative Sequence Injection

Figure 39 (a) presents the instantaneous active and reactive power injected into the grid for DSCC-MMCC. Initially, the STATCOM absorbs 1 pu of positive sequence reactive power (inductive). At $t = 0.2s$, the STATCOM injects 0.5 pu of negative sequence current added to 0.5 pu of positive sequence current. Therefore, the instantaneous active and reactive power present oscillatory components at the doubled line frequency (120 Hz). At $t = 1s$, the STATCOM injects 1 pu of negative sequence current. In this case, the amplitude of the oscillations in active and reactive power reaches 1 pu. Regarding the time response, the system reaches the steady-state approximately 300 ms after the reference step.

The instantaneous power behavior reflects directly in the injected current, as shown in Fig. 39 (b). When the STATCOM absorbs 1 pu of positive sequence current, the currents are balanced and similar stresses are observed in the converter phases. Nevertheless, when the converter injects both sequences, the currents are unbalanced (unbalance factor is 50 %) and the stresses in converter phases are different. When the STATCOM injects 1 pu of negative sequence, the currents are not balanced, since there is an amount of absorbed positive sequence due to the converter power losses.

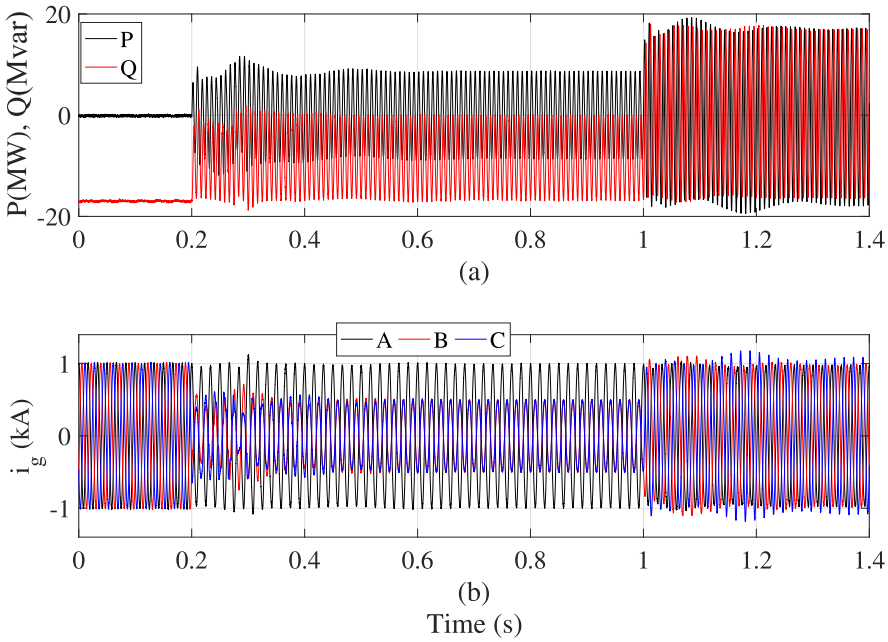

Figure 39 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive and negative sequence injection: (a) instantaneous active and reactive power; (b) grid currents.

As observed in Fig. 40 (a), the arm currents are strongly influenced by the negative sequence current injection. The circulating currents are presented in Fig. 40 (b). For case 1 the circulating currents are null, since only positive sequence currents are injected. For cases 2 and 3, the circulating currents at arms B and C present a dc value. As observed, the second harmonic component in i_z is almost fully compensated by the control strategy employed. The time response of circulating currents is around 250 ms.

The average value of cell capacitor voltages for upper and lower arms are shown in Figs. 41 (a) and (b). As observed, the cell voltage ripple depends on the values of positive and negative sequence currents. Different ripples are observed in each phase. Phase A is the most stressed one, since its current is always close to 1 pu (Fig. 39 (b)). The dashed lines indicate the 10 % range adopted in the design methodology. The transient value reaches 1.18 pu in the worst case. As observed, the designed capacitance value guarantees the maximum ripple in steady-state, since the most stressed phase is within the 10 % range. Regarding the time response of the control strategy, the cell voltages reach the steady-state in approximately 370 ms.

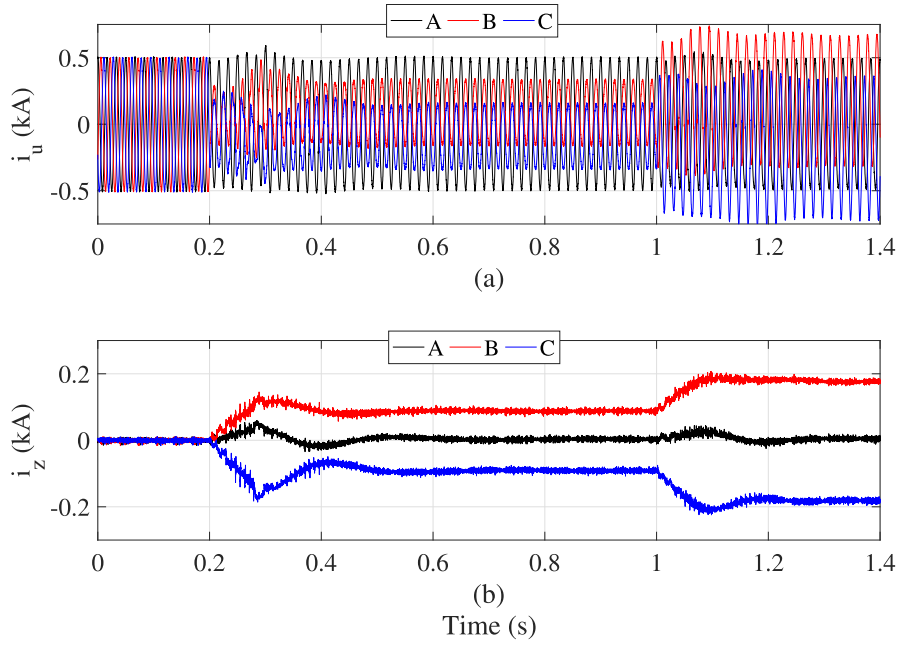

Figure 40 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive and negative sequence injection: (a) upper arm currents; (b) circulating currents.

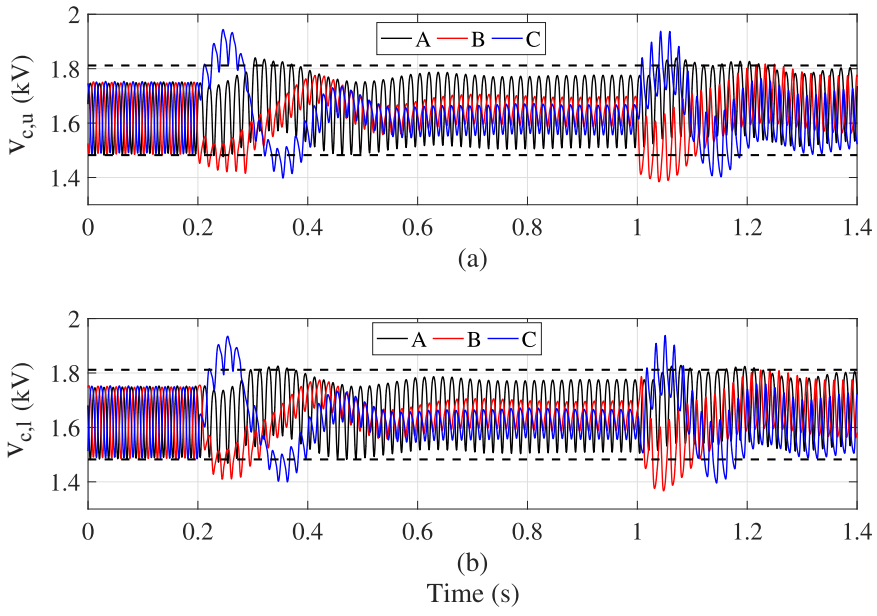

Figure 41 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive and negative sequence injection: (a) average cell voltages (upper arms); (b) average cell voltages (lower arms).

Similar behavior is observed in terms of instantaneous active and reactive power for SDBC-MMCC topology, as observed in Fig. 42 (a). Regarding the time response, the system reaches the steady-state approximately 200 ms after the reference step. The dynamics of grid current follows the reactive power profile as shown in Fig. 42 (b).

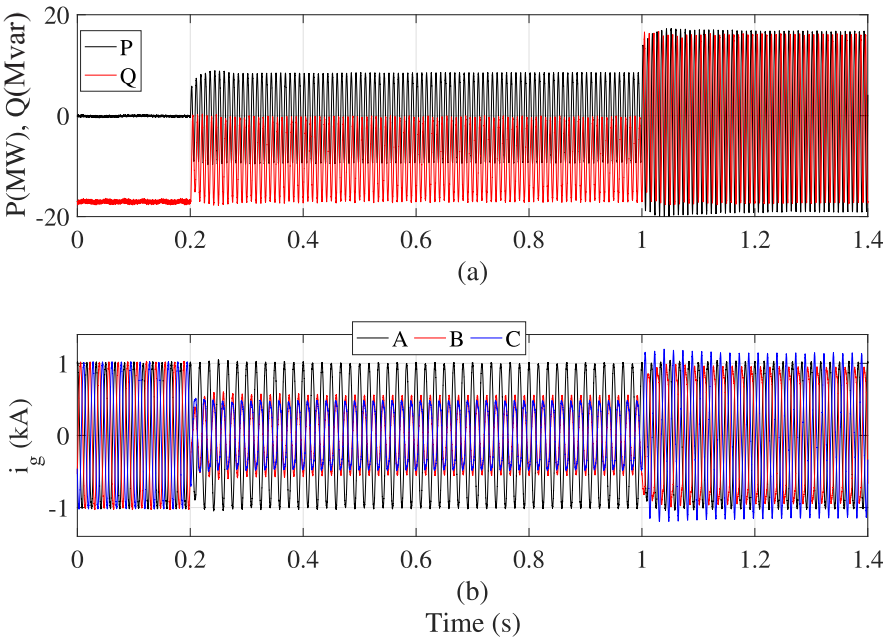

Figure 42 – Dynamic behavior of SDBC-MMCC-based STATCOM for positive and negative sequence injection: (a) instantaneous active and reactive power; (b) grid Currents.

The amplitudes of the cluster currents are strongly affected by the negative sequence injection, as observed in Fig. 43 (a). For case 1, the cluster currents are balanced and similar stresses are observed in each phase of the converter. Nevertheless, when the converter processes both sequences, the currents are unbalanced (unbalance factor is 50 %) and the phases experiment different stresses. For case 3 the cluster current reaches a value above 1 pu, due to the circulating current. The dynamics of the circulating current is presented in Fig. 43 (b). The circulating current is directly related to negative sequence injected, as provided by the theoretical results.

The average value of the cluster capacitor voltages is shown in Fig. 44. As observed, the cell voltage ripple depends on the values of positive and negative sequence currents. During the injection of 1 pu of positive sequence current, the ripples are very small, since the energy storage requirements at this condition are reduced. As observed, the designed capacitance value guarantees the maximum ripple in steady-state for the most stressed phase is within the 10 % range when the converter injects 1 pu of negative sequence current into the grid. The transient value reaches 1.19 pu in the worst case. Regarding the time response, the cell voltages reach the steady-state in approximately 250 ms.

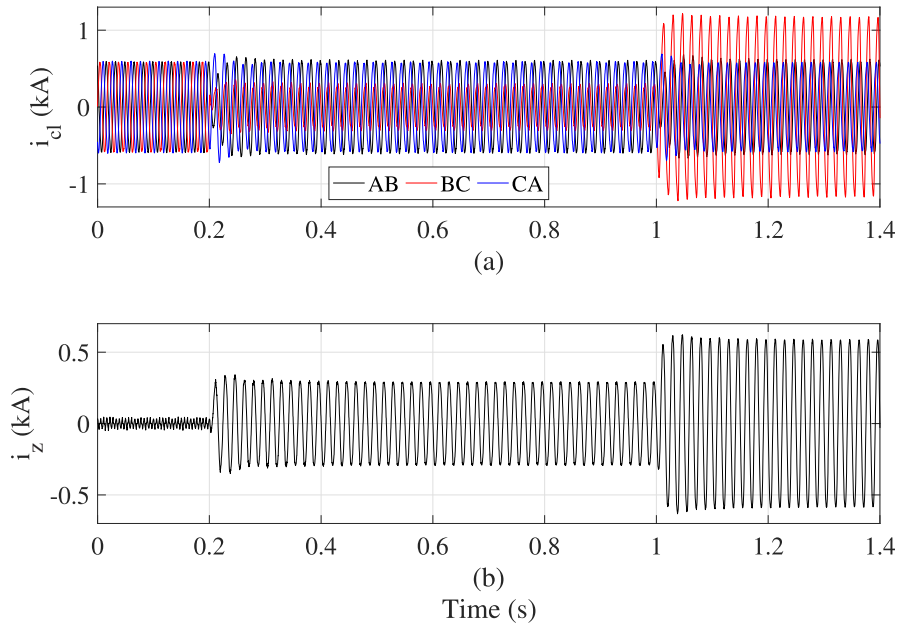

Figure 43 – Dynamic behavior of SDBC-MMCC-based STATCOM for positive sequence injection: (a) cluster currents; (b) circulating current.

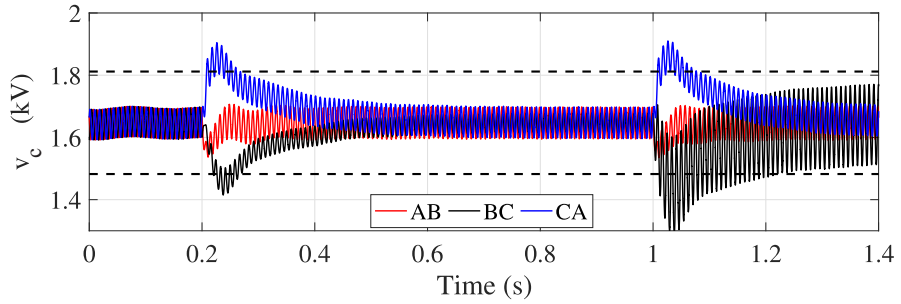

Figure 44 – Dynamic behavior of DSCC-MMCC-based STATCOM for positive and negative sequence injection: average cell voltages (per cluster).

3.5 Power Losses and Cost Analysis

Considering the three operation scenarios aforementioned, the power losses for the MMCC STATCOM topologies are evaluated. For power semiconductors, the heatsink temperature is considered constant and equal to 70 $°C$. The results obtained are presented in Tab. 6.

As observed, since a low switching frequency is employed, the conduction losses are more significant than the switching losses. The copper losses in the magnetic devices are considerable for both topologies while the core losses and ohmic losses in capacitors are negligible. For case 2 the total losses present the smaller value for both topologies. This fact happens because the arm and cluster currents present smaller magnitude at this

condition, as shown in Figs. 40 (a) and Fig. 43 (a).

Considering Case 1, the losses in SDBC-MMCC are 50 % lower than DSCC-MMCC topology. For Case 2, the losses in SDBC-MMCC are 23 % lower than the losses in DSCC-MMCC topology. Finally, the cluster currents increase considerably in Case 3 due to the circulating. Under such conditions, the power losses for SDBC-MMCC are 5 % lower than DSCC-MMCC topology for Case 3.

Table 6 – Power losses in the MMCC topologies studied.

Losses (kW)	Type	Case 1	Case 2	Case 3
Conduction losses	SDBC-MMCC	29.86	27.48	53.61
	DSCC-MMCC	69.47	43.23	75.97
Switching losses	SDBC-MMCC	11.27	10.77	14.57
	DSCC-MMCC	14.64	10.19	15.15
Core losses	SDBC-MMCC	0.39	0.35	1.14
	DSCC-MMCC	0.53	0.26	0.56
Copper losses	SDBC-MMCC	42.22	38.26	111.47
	DSCC-MMCC	85.12	45.93	98.90
Capacitor losses	SDBC-MMCC	0.31	0.32	1.34
	DSCC-MMCC	1.06	0.49	0.88
Total	SDBC-MMCC	84.06	77.17	182.13
	DSCC-MMCC	170.82	100.10	191.46

Finally, the costs of both topologies are presented in Tab. 7. These values are normalized by the DSCC-MMCC total cost. Due to the higher current requirements of SDBC-MMCC during negative sequence compensation, the cost of power electronics is approximately 60 % higher. In terms of cell capacitors, the SDBC-MMCC topology presents lower storage energy requirements and lower cost. For the magnetic devices, the SDBC-MMCC cluster inductors present higher current rating. However, the DSCC-MMCC topology presents the double of magnetic devices and the cost of magnetic devices is more expressive in this topology. Regarding the total cost, the SDBC-MMCC is 48.8 % more expensive than DSCC-MMCC.

Table 7 – Per unit costs of the studied topologies (DSCC-MMCC total cost is the base - $\approx$ 1.32 M€).

Costs (pu)	DSCC-MMCC	SDBC-MMCC	$\Delta k(\%)$
Power Electronics	0.893	1.429	+ 60 %
Capacitors	0.077	0.038	− 50 %
Magnetics	0.030	0.021	− 30 %
Total	1	1.488	+ 48.8 %

3.6 Discussion

An important question may be asked: which is better, the DSCC-MMCC or the SDBC-MMCC for STATCOM application? Answering this is not a trivial task, since it requires multidisciplinary analysis. The idea of this chapter is to assist the design engineer to find this answer.

As observed in the previous analyses, depending of the value of negative sequence component, the power losses in SDBC-MMCC can be lower or similar than those observed for DSCC-MMCC. Therefore, the mission profile of the application has an important role in the overall efficiency and must be evaluated. For example, if only positive sequence is considered, the energy losses in SDBC-MMCC will be lower and the operational cost of the converter (in terms of energy losses) may be lower. Depending on the energy tariff value, the initial extra cost of SDBC-MMCC topology can be paid by the smaller value of power losses.

The real cost of the converter will be also influenced by engineering costs, market conditions and exchange rates. Therefore, the cost evaluation is doubly challenging and few technical papers in literature includes this figure of merit. The values employed in this work are approximations implemented by Engel et al. (2015) and Siddique et al. (2016), which compare the costs of dual-active bridge, three-phase modular multilevel converters and NPC converters. This analysis is in some degree limited and will not result in the exact cost of the converter. Nevertheless, this approach can be used as an initial comparison and also can be useful in the decision making procedure.

Finally, the grid conditions are an important issue. As observed in Section 2.2.3, when unbalanced voltage conditions are considered, SDBC-MMCC presents high values of circulating current and it can be disconnected from the grid if high values of unbalance factor are taken into account. Therefore, when weak grids are considered, DSCC-MMCC topology presents advantages which can justify its application.

3.7 Chapter Conclusions

This chapter discussed two promise topologies of modular multilevel converters for STATCOM applications. The design methodology is focused on applications where positive and negative sequence injection are necessary, as in the grid voltage regulation and renewable energy systems. The comparison presented are supported by analytical results. The dynamic behavior, power losses and costs of both topologies were estimated based on a 17 MVA case study.

As observed, the SDBC-MMCC topology presents smaller energy storage requirements than the DSCC-MMCC topology. Additionally, smaller power losses were

observed during positive sequence compensation. Nevertheless, when negative sequence components are compensated, the current rating and losses of SDBC-MMCC topology increases considerably and DSCC-MMCC topology presented a superior performance. Finally, the SDBC-MMCC topology is more susceptible to unbalanced grid voltages and it is not recommended under such conditions.

Due to its superior characteristics, the further chapters will focus on the DSCC-MMCC topology. The next chapter discusses a reliability-oriented design for DSCC-MMCC-based STATCOMs.

4 Reliability-Oriented Design of an MMCC-Based STATCOM

4.1 Introduction

In recent years, the energy and industry segments have brought high reliability requirements for power electronic converters. In such application fields, the cost of a single failure can result in considerable financial losses. Furthermore, the mission critical industrial applications (MCIA) and harsh environmental conditions are important factors which drive studies regarding reliability in power electronic systems (Wang; Liserre; Blaabjerg, 2013).

According to IEEE (2009), reliability is defined as the ability of an item to perform a required function under stated conditions for a certain period of time, which is often measured by probability of failure, by frequency of failure, or in terms of availability. Additionally, robustness is defined as the ability of an item to perform a required function over a specified range of parameter variations (Falck et al., 2018). Since the probability of failures cannot be fully eliminated, they should be reduced to tolerable levels (Ferreira; Filho; Rocha, 2017).

Indeed, reliability and robustness of the system are closely related to its operating conditions, which is commonly referred as mission profile. The failure usually happens during the overlap between the stress and strength distribution, as shown in the diagram of Fig. 45 (Sintamarean et al., 2015). The stress is related to the environmental loads, such as thermal, mechanical, humidity, etc. On the other hand, the strength means the ability to endure such stressors before fatigue occurs (Wang et al., 2014; Zhou; Zhang; Blaabjerg, 2018).

Industry experience shows that power electronic converters are usually the part of commercial systems with higher failure rates (Wang; Liserre; Blaabjerg, 2013). According to field experiences in a large utility-scale photovoltaic (PV) plant between 2001 and 2006 (Moore; Post, 2008), 37 % of the unscheduled maintenance events in PV plants were related to failures in power inverters, which correspond to 59 % of the total maintenance costs.

At the component level, technical surveys indicate that electrolyte capacitors and semiconductor devices are the most vulnerable (Song; Wang, 2013; Falck et al., 2018). According to ZVEL (2008), 55 % of failures in power electronic systems are caused by steady-state temperature and thermal cycling, followed by vibration (20 %) and humidity (19 %). Under such conditions, the thermal design of the converter plays an important role in the system-level reliability.

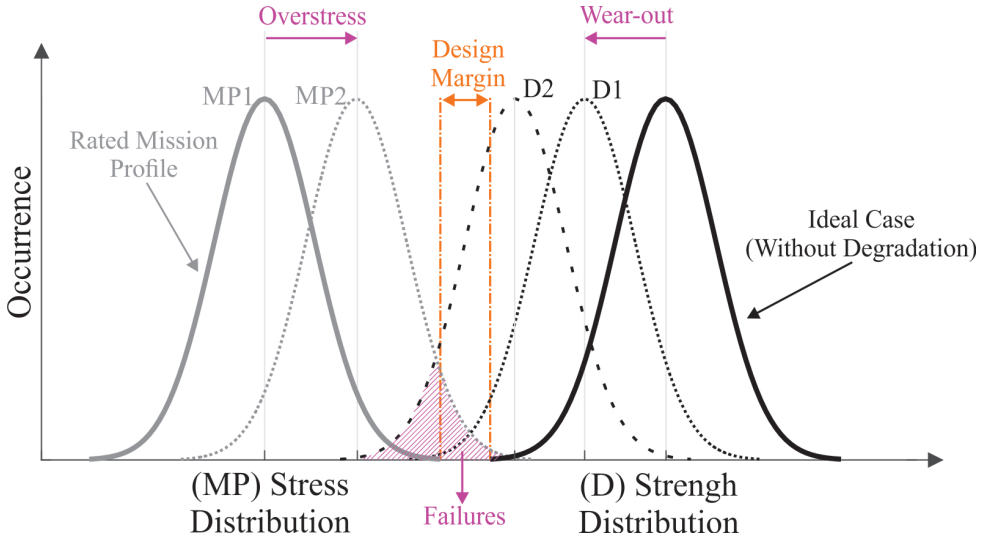

Figure 45 – Stress–strength analysis of a generic system. Note the occurrence of failures due to mission profile variation and/or aging. *Adapted from* Sintamarean et al. (2015).

4.2 Basics of Reliability Modeling

The reliability function $R(x)$ is given by (Todinov, 2007):

$$R(x) = 1 - F(x) = \frac{N(x)}{N(0)}, \tag{4.1}$$

where $N(x)$ is the number of surviving devices at time x and $N(0)$ is the number of devices at the initial time. $F(x)$ is the device unreliability function.

The failure rate function $\lambda(x)$ (or hazard rate) is the rate which a system or component fails, expressed in failures per unit of time (Tu; Yang; Wang, 2019). Accordingly,

$$\lambda(x) = \lim_{\Delta t \to 0} \frac{N(x) - N(x + \Delta x)}{N(0)\Delta x} = \frac{f(x)}{R(x)}, \tag{4.2}$$

where $f(x)$ is the failure probability density function, given by (Todinov, 2007; Tu; Yang; Wang, 2019):

$$f(x) = \lim_{\Delta t \to 0} \frac{N(x) - N(x + \Delta x)}{N(0)\Delta x} = \frac{dF(x)}{dx} = -\frac{dR(x)}{dx}. \tag{4.3}$$

The relation between the failure rate $\lambda(x)$ and $R(x)$ can be obtained from (4.2), replacing $F(x) = 1 - R(x)$. Accordingly,

$$\lambda(x) = -\frac{1}{R(x)}\frac{dR(x)}{dx} \Rightarrow R(x) = \exp\left(\int_0^x \lambda(\tau)d\tau\right). \tag{4.4}$$

A typical failure rate curve of a power electronics product is plotted in Fig. 46. This is the classical bathtub failure rate curve. The device failure rate is usually characterized by 3 regions: infant mortality; constant failure rate; and wear-out failures. The infant mortality is reduced by improvements in the design/production of the system. The constant failure rate is usually referred as device useful life. In theory, when the systems reach the wear-out region, they have finished their required missions (Kim; Lee, 2015)

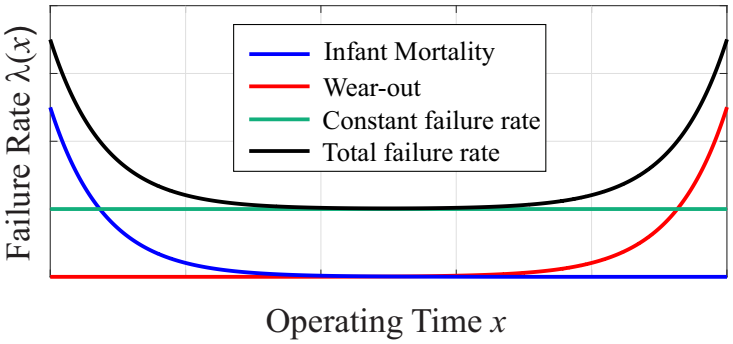

Figure 46 – Typical failure rate curve - bathtub curve.

If a constant failure rate is assumed, the reliability function can be simplified as follows:

$$R(x) = \exp(\lambda x). \tag{4.5}$$

Then, the failure rate is measured from the mean number of failures per unit time, which is expressed in failures in time (FIT) (Department of Defense - USA, 1998):

$$1 \text{ FIT} = 10^{-9}(failure/hour). \tag{4.6}$$

Among the reliability metrics for comparison of systems, mean time to failure (MTTF) is the expected value of lifetime. Based on the probability theory (Tu; Yang; Wang, 2019):

$$\text{MTTF} = \int_0^\infty x f(x) dx = \int_0^\infty R(x) dx. \tag{4.7}$$

From equation 4.7, when only the constant failure rate region is taken into account, $\text{MTTF} = \frac{1}{\lambda}$.

Another reliability index, percentiles of a lifetime, B_x, is defined as the time at which x percent of devices fail [1] (Todinov, 2007):

$$F(B_x) = \frac{x}{100}. \tag{4.8}$$

[1] E.g., B_{10} lifetime is the time at which 10 % of the samples fail.

In the traditional reliability prediction approach developed in the 1950s, constant failure rates are considered (Song; Wang, 2013; Grinberg et al., 2013), although this assumption has important limitations (Kim; Lee, 2015). Until the 1980s, empirical data or military and industry handbooks (e.g., Military-Handbook-217 series (Department of Defense - USA, 1991)) were extensively used to describe the useful life of electronic components (Wang et al., 2014). In the 1990s, many studies indicate that constant failure rate models are inadequate for reliability prediction, as discussed by McLeish (2010) (e.g., Military-Handbook-217 series was canceled in 1995). Recently, the reliability engineering is going through the physics-of-failure approach (POF). POF is a methodology based on the failure mechanism analysis and the impact on the reliability (Wang; Liserre; Blaabjerg, 2013). This approach is described in the next section.

4.3 Toward Reliable Converters

Compared to empirical failure analysis based on historical data, the POF approach requires multidisciplinary knowledge as materials, physics, chemistry and statistics. The analysis is based on the mission profiles, type of failure mechanism and the related statistical model.

For example, Fig. 47 presents an internal structure of a plastic IGBT module (PIM). As observed, the device presents various materials with different thermal expansion coefficients. Therefore, the thermal cycling results in mechanical stress in all components and joints. Indeed, the most reported failure mechanisms in power modules are the bondwire lift-off, chip solder fatigue and baseplate solder fatigue (ABB, 2004; Wang; Ma; Blaabjerg, 2012). Each specific profile leads to different stress distribution and each failure mechanism has different strength rates related to these profiles. Therefore, a power module failure rate is strongly dependent on the mission profile and the type of wear-out fatigue.

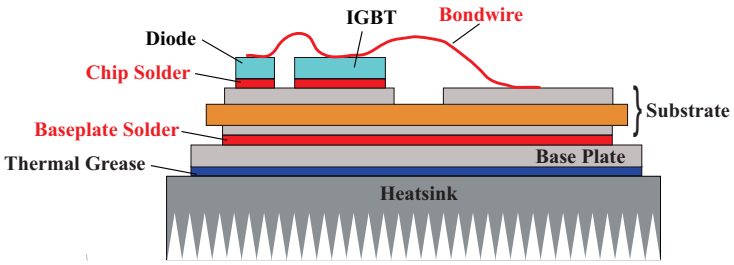

Figure 47 – Detailed structure of a plastic IGBT module (PIM). *Adapted from* Wintrich et al. (2011).

Among the possible solutions to improve the reliability of power electronic converters, the following approaches can be cited:

- design for reliability (DFR) (Sintamarean et al., 2015; Andresen et al., 2016; Yang; Sangwongwanich; Blaabjerg, 2016; Sangwongwanich et al., 2018);
- redundancy strategies (Guo et al., 2018; Farias et al., 2018; Tu; Yang; Wang, 2019; Kang et al., 2019);
- fault-tolerant topologies (Zhang et al., 2014; Muenchhof; Clever, 2009; Lian et al., 2016; Ferreira et al., 2017);
- condition Monitoring (Ghimire et al., 2014; Hu; Du; Wei, 2017; Moeini et al., 2018);
- junction temperature monitoring (Ghimire et al., 2014; Baker et al., 2017; Choi; Blaabjerg; Jørgensen, 2018);
- junction temperature control (Yang; Wang; Blaabjerg, 2014; Wu et al., 2016; Polom; Wang; Lorenz, 2017; Andresen et al., 2018; Ko et al., 2019).

Moreover, failures in electronic devices can be classified into two groups:

- *Overstress failures or catastrophic events*: overstress failures are related to single phenomenon (overvoltage, overload, etc);
- *Wear-out failures*: wear-out failures are related to cumulative damage and aging process.

Recently, some works propose the Design for Reliability (DFR) approach as a solution to ensure a target lifetime for the power converters (Blaabjerg et al., 2017). In DFR, the design is accomplished to avoid the system to move forward to the wear-out zone, where the failure rate grows faster, as shown in Fig. 46 (Scheuermann; Junghaenel, 2018). Therefore, the probability of wear-out failures can be reduced due to a proper converter design.

The DFR of MMCC-based STATCOMs is presented in this chapter. Although the wear-out failures can be predicted (to some extent) and even avoided through DFR, the catastrophic events are difficult to predict and usually modeled by constant failure rates. Thereby, to overcome these events, condition monitoring systems or some fault tolerance strategy shall be added during the MMCC design (Moeini et al., 2018). The issues about fault tolerance implementation in MMCC are discussed in chapters 5 and 6.

4.4 Design for Reliability of DSCC-MMCC-based STATCOMs

Some research efforts focused on wear-out prediction of DSCC-MMCC are identified in the literature, mainly for HVDC systems (Liu et al., 2016a; Ye et al., 2017; Zhang et al., 2017a; Farias et al., 2017). Liu et al. (2016a) present a lifetime estimation procedure for DSCC-MMCC power modules based on POF models and mission profile, considering a 18 MW HVDC station. Ye et al. (2017) propose an algorithm for fast thermal simulation of DSCC-MMCC and also estimates the power modules lifetime. In (Zhang et al., 2017a), the most commonly-used analytical lifetime models of IGBT devices are compared, considering a 30 MW HVDC application with 6.5 kV IGBT modules. Farias et al. (2017) address the estimation of lifetime comparing two IGBT solutions with differently rated current levels. The results indicate a lower temperature in devices with higher current capability, increasing the converter lifetime.

In addition to the current level, the varied voltage classes of silicon-based power semiconductor devices also challenges the MMCC design (Huber; Kolar, 2017). Thereby, some studies define the optimum semiconductor blocking voltage to be used for different power levels. According to Huber and Kolar (2017), 1.2 kV or 1.7 kV IGBT power modules are most suitable for 1 MVA systems to interface medium-voltage (MV) grids, considering only the power device efficiency.

Alvarez et al. (2016) indicate that 4.5 kV IGBT modules show the best performance for HVDC transmission considering rated powers below 900-1000 MW, when the cost of transmitted power per cell unit and the penalties for the losses are taken into account. Additionally, for values above 1050 MW, the cell designed with 6.5 kV IGBTs proved to be more attractive. Finally, Siddique et al. (2016) compare 5 designs by employing different IGBT voltage classes for a 5 MVA MMCC-based battery energy storage system. The results indicate that the 1.7 kV modules lead to the lowest cost, while 3.3 kV results in the lowest losses. Nevertheless, a reliability-oriented design methodology, including the design complexities of MMCC converters, is still missing in technical literature.

This chapter proposes a reliability-oriented design to obtain a cost-effective MMCC-STATCOM, based on the trade-off between cost and system-level reliability. The unreliability level U_x is presented as a new reliability indicator to evaluate the probability of one failure in the converter for a given time. Moreover, the $U_x - cost$ map is introduced as a tool to compare different designs with respect to the unreliability requirement and cost.

The design and selection of power electronics components demand the consideration of some factors, such as power losses, cost and the application unreliability requirement. Based on the DFR (Ferreira et al., 2018), the reliability-oriented design illustrated in Fig.

48 presents the benchmarking and selection methodology for the semiconductor devices. The methodology is described in the following subsections.

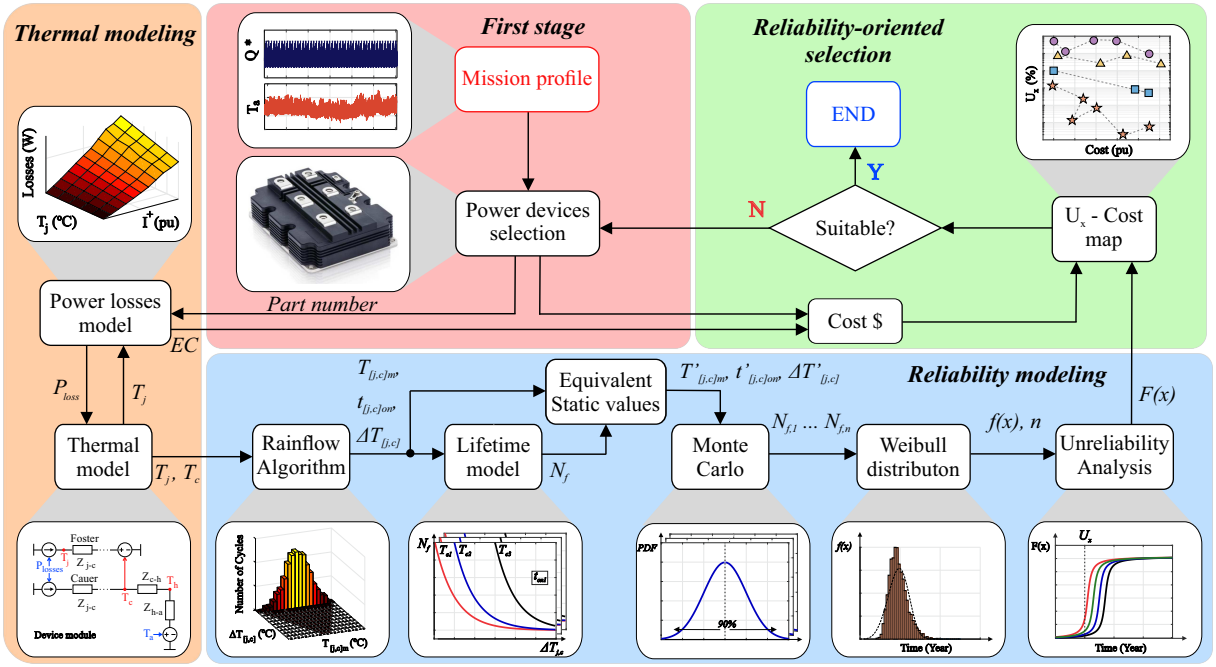

Figure 48 – Flowchart for the reliability-oriented design of power devices.

4.4.1 First Stage

Firstly, the mission profile is defined for the considered application. Measurements of reactive power (Q^*) and ambient temperature (T_a) mission profiles are employed to define the system operating condition. The most appropriate power devices can be selected according to the power rating, voltage and current levels.

4.4.2 Thermal Modeling

The power losses model employed is based on a look-up tables created in PLECS® environment. Typical on-state characteristics, switching energies and thermal impedances of the power modules are extracted from the datasheets. An example of the data extracted is presented in Fig. 49. Since the gate resistance affects the switching losses, the recommended gate resistor by the manufacturer is adopted.

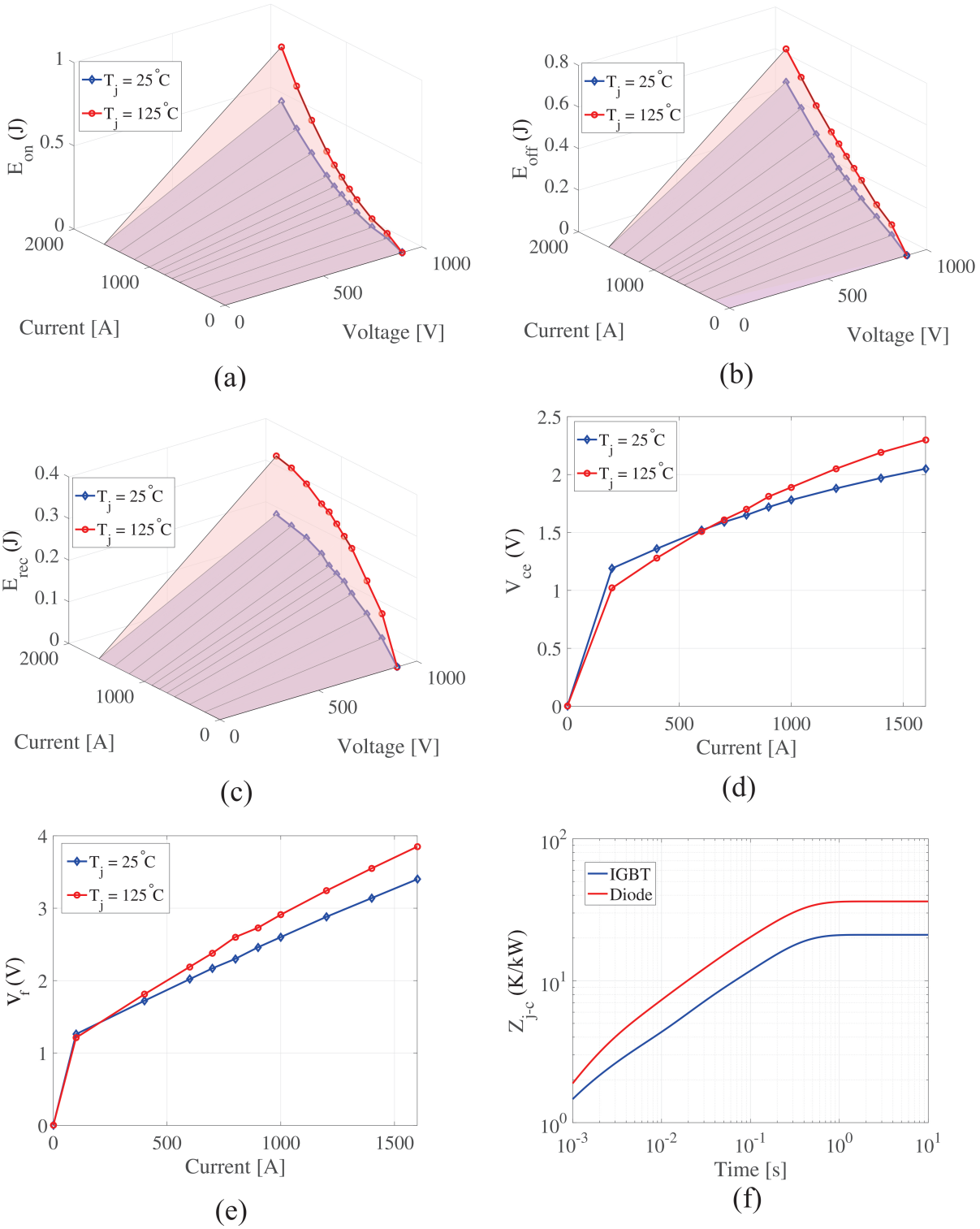

Figure 49 – Data extracted from a power module datasheet: (a) turn-on switching energy (IGBT); (b) turn-off switching energy (IGBT); (c) reverse recovery energy (diode); (d) typical IGBT on-state characteristics; (e) typical diode forward characteristics; (f) junction-to-case transient thermal impedance (IGBT and diode). In this example, the part number 5SND 0800M170100 is considered.

As observed, the power losses temperature dependence is considered. Linear interpolation and extrapolation are used. Moreover, the switching energies are assumed proportional to the blocking voltage. One limitation of this approach is the influence of converter layout (due to stray inductance) in switching losses, which is neglected (Sousa et al., 2017). Data from experimental characterization can be employed to deal with this issue. Nevertheless, this approach is time consuming and costly. Alternatively, this work consider power modules from the same manufacturer which are tested in similar conditions.

As previously discussed, the junction temperature T_j and the case temperature T_c of the semiconductor devices are important variables that directly affect the lifetime and the reliability. The temperature is computed based on the thermal model presented in Fig. 50 (Ma et al., 2016). As observed, the junction-to-case thermal impedance Z_{j-c} combines Cauer and Foster thermal networks to provide the best features of both models (Tu; Xu, 2011b). The case-to-heatsink thermal impedance Z_{c-h} is represented by a thermal resistance. Moreover, the heatsink and cooling system are employed to ensure the operation of the power devices at the safety limit (e.g., T_j below 150 °C and T_c below 125 °C). The heatsink-to-ambient thermal impedance Z_{c-a} is represented by a Foster network with parameters R_{h-a} and C_{h-a}.

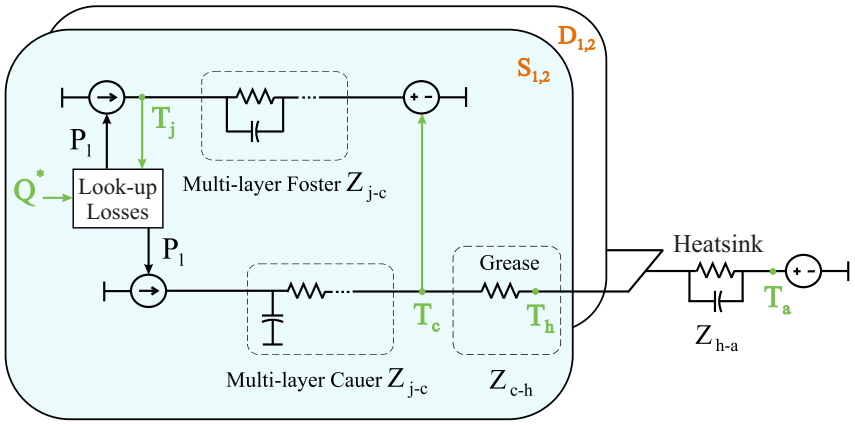

Figure 50 – Thermal model of the power devices in a chopper cell with common heatsink.

The detailed view of a plastic IGBT module and the water cooling plate is presented in Fig. 51 (a). The heatsink parameters (R_{h-a} and C_{h-a}) are estimated based on (Asimakopoulos et al., 2015), where a simplified heatsink model for the power converter is proposed (see Fig. 51 (b)). This methodology considers a uniform temperature profile throughout the power devices baseplate and cooling plate. The heatsink geometry has a simple rectangular cross-section and is approximated by a simple orthogonal brick. Under such conditions, the heatsink parameters can be computed by:

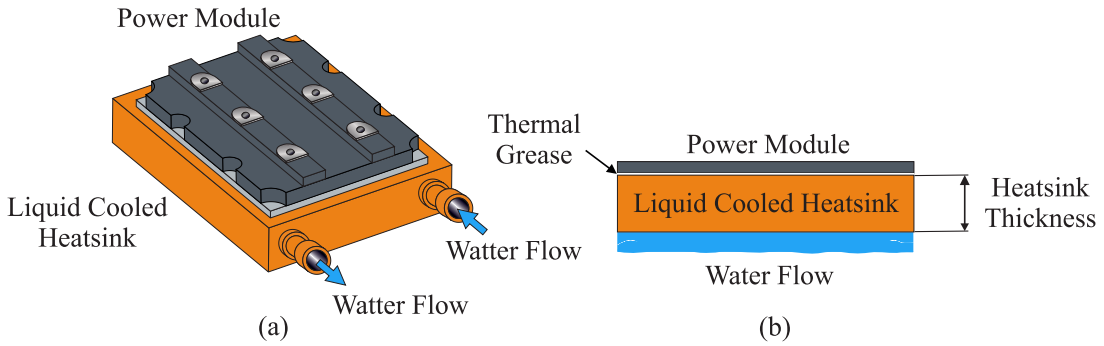

Figure 51 – Heatsink scheme of the water cooling system for PIM: (a) detailed view; (b) simplified model.

$$R_{h-a} = R_{h-f} + R_{f-a} = \frac{d_h}{\kappa_h A_h} + \frac{1}{h_c A_h}, \tag{4.9}$$

$$C_{h-f} \approx C_{h-a} = c_h \rho_h d_h A_h, \tag{4.10}$$

where d_h is the heatsink thickness, κ_h is the thermal conductivity of the heatsink material, A_h is the heatsink surface area, c_h is the specific heat capacity and ρ_h is the material density. The subscripts $h - f$ and $f - a$ mean heatsink-to-fluid and fluid-to-ambient, respectively. h_c is the fluid flow convection coefficient (Incropera; DeWitt, 1996).

In this work, the heatsink surface area is considered to be equal to the total area of the power module, from the device datasheet. Furthermore, aluminum heatsinks with 3 cm of thickness are employed (Asimakopoulos et al., 2015). Therefore, $\kappa_h = 238$ W/(m °C), $c_h = 900$ J/(kg °C) and $\rho_h = 2700$ kg/m^3. Based on these assumptions, R_{h-f} and C_{h-f} can be determined. Regarding the water cooling system, the R_{f-a} values were determined through simulations. According to Incropera and DeWitt (1996), typical values of h_c are within 50 to 2500 W/(m^{2}K), depending on the pressure, speed and type of water flow and temperature dependent properties. The necessary value is determined through thermal simulations, which are carried out to guarantee junction, case and heatsink temperatures within the limits for the worst conditions (for the selected power modules, 130 °C, 100 °C and 60 °C, respectively).

It is important to remark that parameters computed by equations (4.9) and (4.10) are a rough estimation of the heatsink parameters. A detailed modeling of heatsinks considering shape, flow characteristics and cooling liquid parameters usually involves complex heat transfer models which are solved in Finite Element Method (FEM) packages. Based on these models, the thermal parameters (thermal resistance and capacitance) can be obtained and used by the thermal simulation and lifetime estimation flowchart. Nevertheless, the analysis of complex heatsink shapes is out the scope of this work.

4.4.3 Reliability Modeling

The thermal cycling causes cyclic thermo-mechanical stresses in all joints and components of the power modules, which leads to wear-out failures. Usually, the lifetime models are obtained through active power cycling tests with constant parameters, as shown in Fig. 52 (a) (Scheuermann; Junghaenel, 2018; Zeng et al., 2019). The average temperature ($T_{[j,c],m}$), cycling amplitude ($\Delta T_{[j,c]}$) and heating time ($t_{on[j,c]}$) are controlled. The subscript $[j, c]$ indicates the test can be applied based on junction or case temperature, depending of the failure mechanism studied.

Some variables are monitored during the power cycling test. For example, the failures in the bondwires affect the on-state voltage drop (v_{ce}) while the solder delamination affects the thermal resistance $R_{thermal}$ (Zeng et al., 2019). When the monitored variables reach the failure criteria, the device is considered in its end of life, as shown in Fig. 52 (b) [2]. A set of power devices is tested and statistical analyses are implemented to compute the number of cycles N_f which results in a failure probability of x %, i.e., B_x lifetime. $x = 10$ % is commonly employed.

Due to the irregular thermal cycles presented in the junction temperature profile, a counting cycle algorithm must be used. The goal is to convert it into a set of cycles with constant parameters (Mainka; Thoben; Schilling, 2011). Among the possible solutions, the rainflow algorithm is commonly employed in fatigue analysis (Fatemi; Yang, 1998; ASTM, 2005). The number of cycles to failure N_f is computed based on lifetime models. In this work, N_f is evaluated through the ABB Hi-Pak IGBT power module lifetime model (ABB, 2004). This model analyzes N_f in all critical joints (bondwire, baseplate solder and chip solder) for each diode and IGBT using the 10% failure rate approach (B_{10} lifetime) based on look-up tables (Ma et al., 2015). Junction and case temperatures are required.

The accumulated damage due to the mission profile can be computed through the Palmgren-Miner's rule, as follows (Palmgren, 1924; Miner, 1945):

$$LC = \sum_i \frac{n_i}{N_{f,i}}, \tag{4.11}$$

where n_i is the number of cycles obtained from rainflow algorithm. LC is computed separately for bondwire, baseplate solder and chip solder and for each diode and IGBT (Zhang et al., 2017b). However, the inverse value of the damage computed in (4.11), cannot be interpreted as the converter lifetime. Since the power devices can present variations in their parameters due to the manufacturing process and stress variation (Sangwongwanich et al., 2018), this approach is not appropriate, especially for the large number of cells in

[2] Usually, the failure criteria are: increase of 5 % in the on-state voltage drop v_{ce}, increase of 20 % in the thermal resistance $R_{thermal}$ or loss of switching or blocking capability (Lutz et al., 2011). It is important to remark that the power cycling tests must be designed to excite only one failure mechanism.

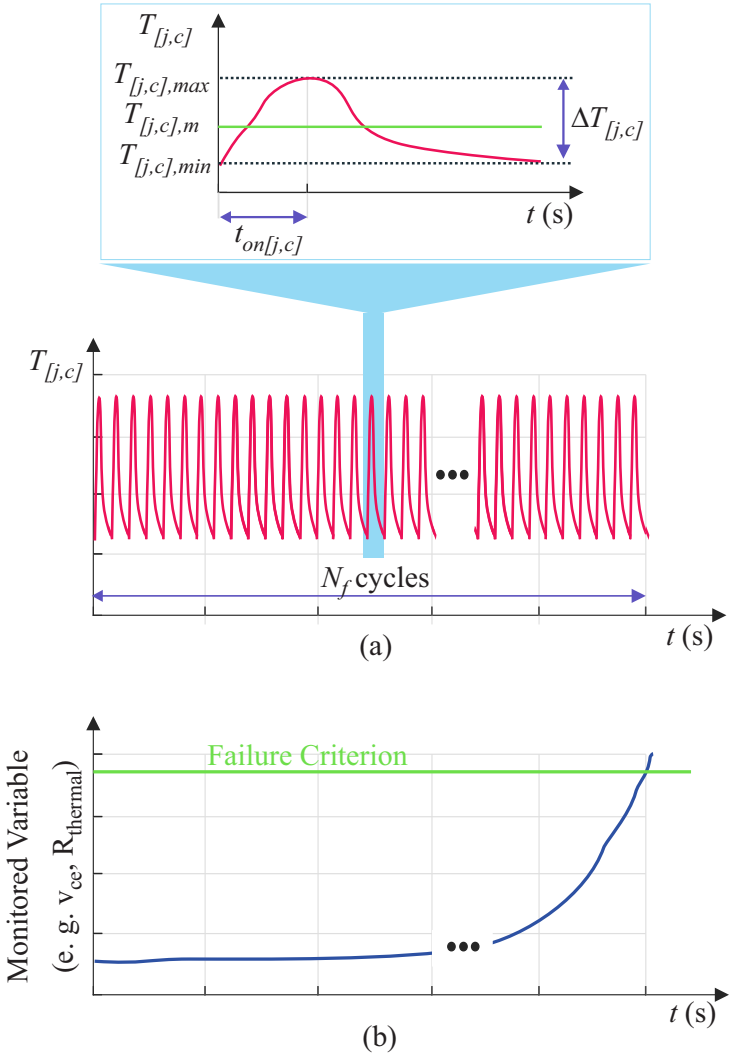

Figure 52 – Power cycling test for lifetime estimation: (a) thermal cycling during the lifetime test. The zoomed view shows the main parameters of the thermal cycle; (b) effect of the accumulated damage (caused by the thermal cycling) in the monitored variable. The subscript $[j, c]$ indicates the graphic can be interpreted for both junction and case temperature.

the MMCC. Thus, lifetime is usually expressed in terms of statistical values rather than a constant value.

Therefore, a statistical analysis is necessary. Initially, the stochastic parameters $T_{j,m}$, $T_{c,m}$, ΔT_j, ΔT_c, $t_{on,j}$ and $t_{on,c}$ are converted into equivalent deterministic static values, denoted by $T'_{j,m}$, $T'_{c,m}$, $\Delta T'_j$, $\Delta T'_c$, $t'_{on,j}$ and $t'_{on,c}$ using the methodology proposed by Reigosa et al. (2016). The physical interpretation of the static values is presented in Fig. 53 (a). The static value is a power cycling with constant parameters (amplitude, average value and heating time) which provides the same LC computed by relation (4.11).

Once the equivalent static values have been obtained, a variation of 5% is applied

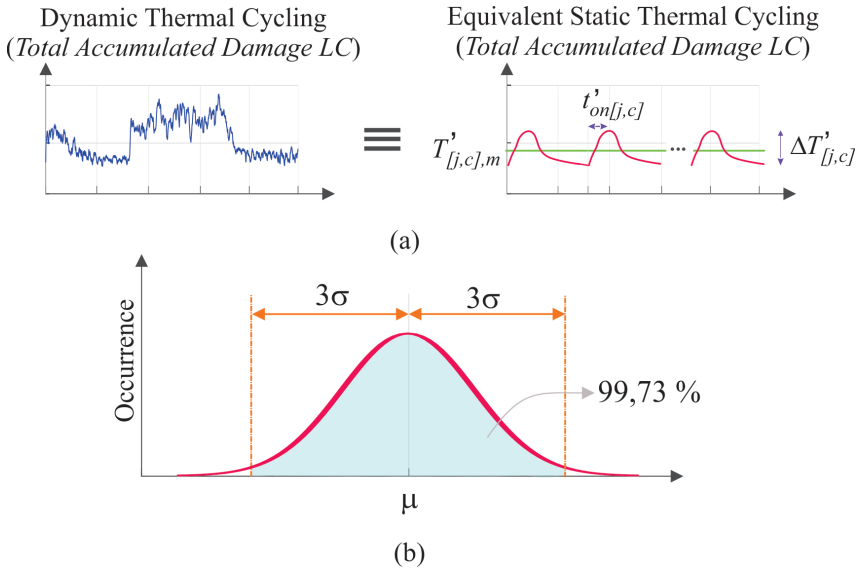

Figure 53 – Basics of the statistical lifetime analysis: (a) physical interpretation of equivalent static values; (b) normal distribution showing how the 5 % was considered in all parameters (lifetime model and its inputs).

in these parameters and in the lifetime model used[3], as illustrated in Fig. 53 (b). A normal distribution with standard deviation σ and μ is the mean value is adopted. A confidence interval of 99.97 % is chosen, i.e, $3\sigma = 5\%$. Then, the Monte Carlo simulation is performed with $10,000$ samples. Then, the lifetime distribution obtained from Monte Carlo simulation is fitted with the Weibull PDF $f(x)$ (Sangwongwanich et al., 2018), given by:

$$f(x) = \frac{\beta}{\eta^{\beta}} x^{(\beta-1)} exp\left[-\left(\frac{x}{\eta}\right)^{\beta}\right], \tag{4.12}$$

where β is the shape parameter, η is the scale parameter, and x is the operation time. The cumulative density function (CDF), also called unreliability function $F(x)$, represents the proportion of population failure, according to the time obtained through the integral of PDF, given as:

$$F(x) = \int_0^x f(x)dx. \tag{4.13}$$

The system level reliability can be computed based on the reliability block diagram presented in Fig. 54. Since only the reliability of the power devices is taken into account (i.e., S_1, S_2, D_1 and D_2), the unreliability function for each cell can be calculated as:

$$F_{cell}(x) = 1 - \prod_{i=1}^{4} (1 - F_{Comp(i)}(x)), \tag{4.14}$$

[3] Since the lifetime model is based on look-up tables of N_f in of the thermal cycle parameters, each value of the look-up is assumed to be described by a normal distribution.

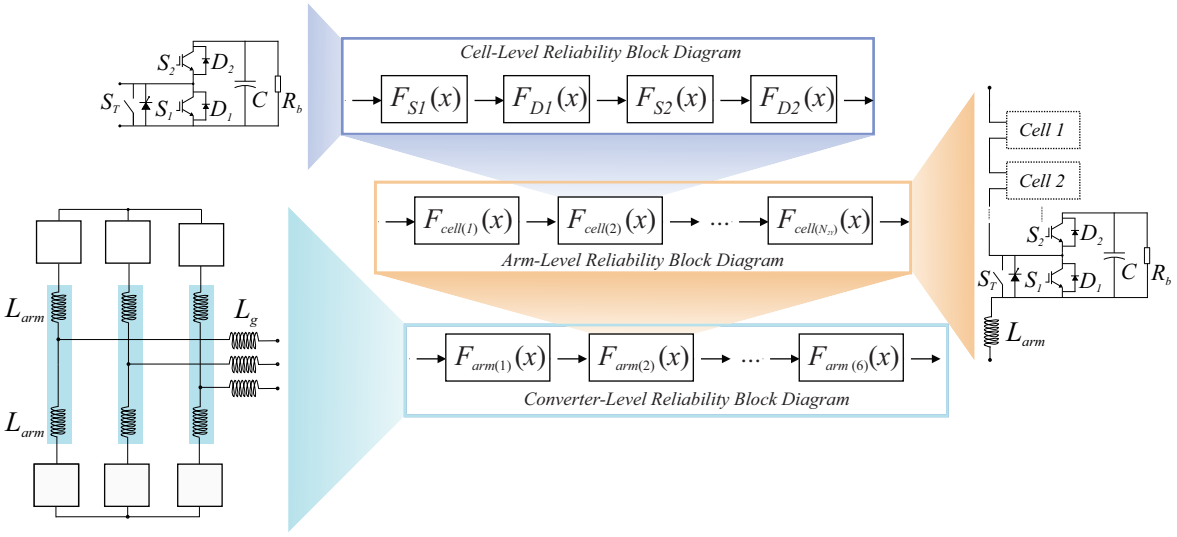

Figure 54 – Reliability block diagram of the DSCC-MMCC-based STATCOM. Only power semiconductors are considered.

where $F_{Comp(i)}(x)$ is the unreliability function of each power device. The arm-level unreliability function is computed considering N_{2Y} independent and identical cells. Accordingly:

$$F_{arm}(x) = 1 - \prod_{i=1}^{N_{2Y}} (1 - F_{cell(i)}(x)). \tag{4.15}$$

Finally, the converter-level unreliability function can be evaluated as follows:

$$F_{conv}(x) = 1 - \prod_{n=1}^{6} (1 - F_{arm(n)}(x)). \tag{4.16}$$

As observed, the unreliability of other components (capacitors, gate drivers, printed circuit boards, cooling system, power supplies, etc) can be included in the reliability block diagram if the unreliability function is known. However, the development of a complete reliability model for an MMCC-based STATCOM is beyond the scope of this work and can be approached in further researches.

4.4.4 Reliability-Oriented Selection

The reliability studies on the converters are appropriate for the maintenance schedule and the prediction of the power devices lifetime (Alam; Khan, 2014). Since the beginning of the transitioning from the reliability books to PoF in power electronics (Wang et al., 2014), the converter lifetime has been expressed in N_f. Recently, the B_x factor was introduced, and N_f was translated into the number of years where x % of the devices fail

(ABB, 2004). Even though this concept is consolidated among the reliability researchers and designers, it is still quite confusing for industry engineers, which are responsible for the selection of converters.

This work introduces the unreliability level U_x as a new reliability indicator to simplify this communication between reliability design engineers and industry engineers. Basically, for a given lifetime target x, the probability of failure is evaluated through the system unreliability. In addition, the $U_x - cost$ map is introduced as a tool to compare different designs with respect to the unreliability requirement and the overall cost. Finally, the most suitable design will find the lifetime target with the lowest cost.

Regarding the overall cost of each design, the figure of merit employed includes the capital expenditure (CAPEX) and operational expenditure (OPEX). The CAPEX is mainly related to investment in power electronics (e.g., semiconductor devices, controls, cabinets), capacitors and inductors which are dominant in the initial investment of the converter (Siddique et al., 2016). The CAPEX is evaluated according to the methodology presented in Section 3.3.

Moreover, the OPEX is mainly associated to the semiconductor conduction and switching losses (Tu; Yang; Wang, 2019). Therefore, the operational expenditure of the converter is considered as follows:

$$OPEX = K_o E_c, \tag{4.17}$$

where K_o is the price per kilowatt-hour and E_c is energy consumption of the converter. Based on loss penalty for transmission system, $K_o = 0.11$ €/kWh (Alvarez et al., 2016). Thus, the overall cost is given by:

$$Cost = CAPEX + OPEX. \tag{4.18}$$

4.5 Case Study

In this chapter only the DSCC-MMCC topology is analyzed. The ABB Hi-Pak family is considered in the converter design. These modules use aluminum silicon carbide (AlSiC) baseplate material and aluminum nitride (AlN) isolation with low thermal resistance. These materials present matched thermal expansion coefficients, which results in better performance in power cycling (ABB, 2017b). This family contains devices for 1.7 kV, 3.3 kV, 4.5 kV and 6.5 kV blocking voltage classes.

A 17 MVA STATCOM connected to the 13.8 kV grid is considered. The rated current of the power devices is defined by the MMCC arm current. Due to symmetry, only

the upper arm current is verified. The maximum and rms upper arm current is defined by (Cupertino et al., 2018):

$$\max(i_u) = \widehat{I}_n \left(\frac{1}{2} + \frac{\Lambda_{2Y} m_{max}}{4} \right), \tag{4.19}$$

$$i_{u,rms} = \frac{\widehat{I}_n}{2} \sqrt{\frac{(\Lambda_{2Y} m_{max})^2}{4} + \frac{1}{2}}, \tag{4.20}$$

where $\widehat{I}_n$ is defined by (3.13). Thus, the $\max(i_u) = 788$ A and $i_{u,rms} = 456$ A.

Using the methodology proposed in chapter 3, the parameters of the DSCC-MMCC are computed for four different blocking voltages (1.7, 3.3, 4.5 and 6.5 kV denoted by I - IV, respectively). The obtained parameters are shown in Tab. 8. As observed, the same switching frequency is adopted for all designs. The arm inductance is designed to guarantee the same ripple in the circulating current for all voltage classes. The grid impedance is considered unchanged. Based on these assumptions, the total harmonic distortion (THD) in output current i_g for all designs was lower than to 5% at rated conditions.

Table 8 – DSCC-MMCC parameters for four analyzed blocking voltages.

Parameter	Value			
	I	II	III	IV
V_{svc} (kV)	1.7	3.3	4.5	6.5
N_{2Y}	33	17	13	9
$v_{dc,2Y}$ (kV)	28	28	28	28
v_c^* (V)	848	1647	2154	3111
C_{2Y} (mF)	9.5	5	3.8	2.6
L_{arm} (mH)	2.4	4.5	5.9	8.7
f_c (Hz)	210	210	210	210

Simulations were performed using PLECS® and MATLAB® software systems, aiming to estimate the lifetime, energy losses and cost of each design. Figure 55 (a) shows the one-week mission profile based on the reactive power measurements obtained from a factory. This profile was replicated for one year. Furthermore, the one-year ambient temperature profile is illustrated in Fig. 55 (b). These data were collected from the southeastern Brazil with a sampling time of 1 second.

Table 9 shows the part numbers evaluated in this work. These case studies consider all commercial ABB Hi-pak IGBT solutions with rated currents from 750 A to 1600 A and the blocking voltages from 1.7 kV to 6.5 kV. Implementations based on parallel connection are also employed. As a result, 18 different implementations are evaluated. The objective

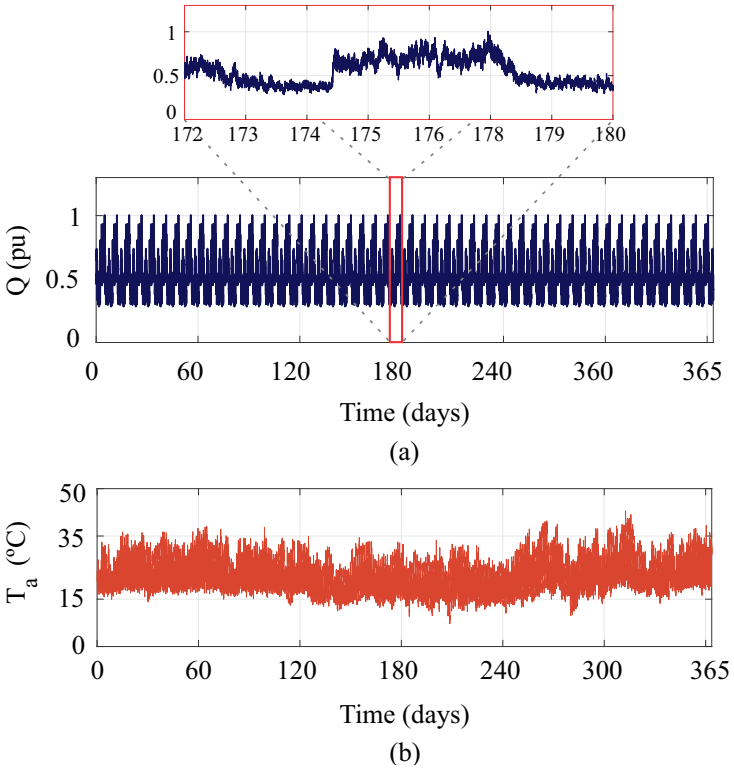

Figure 55 – Mission profiles: (a) reactive power; (b) ambient temperature.

Table 9 – Evaluated case studies considering different power modules.

Voltage (V)	Current (A)	Part Number	Design
1700	800	5SND 0800M170100	C_1
	2x800	5SND 0800M170100	C_2
	1600	5SNA 1600N170100	C_3
3300	800	5SNA 0800N330100	C_4
	2x500	5SND 0500N330300	C_5
	1000	5SNA 1000N330300	C_6
	1200	5SNA 1200E330100	C_7
	1500	5SNA 1500E330305	C_8
	2x800	5SNA 0800N330100	C_9
4500	800	5SNA 0800J450300	C_{10}
	1200	5SNA 1200G450300	C_{11}
	2x650	5SNA 0650J450300	C_{12}
	2x800	5SNA 0800J450300	C_{13}
6500	750	5SNA 0750G650300	C_{14}
	2x400	5SNA 0400J650100	C_{15}
	2x500	5SNA 0500J650300	C_{16}
	2x600	5SNA 0600G650100	C_{17}
	2x750	5SNA 0750G650300	C_{18}

is to analyze the effect of the power modules ratings in the converter lifetime. The energy losses and costs are also evaluated. Four base cases (i.e., C_1, C_4, C_{10}, C_{14}) are considered, which are the lowest rated current devices for each blocking voltage.

The data used in the power losses and thermal impedances Z_{j-c} and Z_{c-h} are extracted from the datasheets. The water flow convection coefficient is adjusted to maintain the heatsink temperature close to 60 °C at rated conditions for the base cases. Table 10 presents the parameters of the heatsink and cooling systems. As observed, a lower thermal resistance in the cooling system is required for the power modules that present higher losses. The case studies with same blocking voltage employ the same heatsink and cooling system parameters given in Tab. 10.

Table 10 – Heatsink and cooling system parameters for power modules of the base cases.

Parameters		I	II	III	IV
R_{h-f}	(°C/kW)	6.9	6.9	6.9	4.7
C_{h-f}	(J/°C)	1327	1327	1327	1939
R_{f-a}	(°C/kW)	142.8	70.2	52.1	36.1

The area product per inductor A_p and converter energy storage E_{2Y} values are given in Tab. 11. The DSCC-MMCC presents 6 inductors and the energy stored is 40 kJ/MVA for all cases.

Table 11 – Cell capacitors and magnetic devices parameters for cost design.

Parameters		DSCC-MMCC specifications			
		C_1	C_4	C_{10}	C_{14}
A_p	(m^4)	$1.8 \cdot 10^{-3}$	$3.4 \cdot 10^{-3}$	$4.4 \cdot 10^{-3}$	$6.5 \cdot 10^{-3}$
E_{2Y}	(kJ)	680	680	680	680

The converter lifetime target is defined as 10 years of operation. Thus, the converter energy consumption is computed for 10 years of operation and denoted by $E_{c_{10}}$. Finally, U_{10} is applied for reliability-oriented design, which means the probability of the converter failure in 10 years of operation.

4.6 Results

Initially, the power losses, including conduction and switching losses of a power module device are obtained. Figure 56 shows the look-up table of losses for the base cases. For simplification, only the losses in the IGBT S_1 are shown. As observed, an increase in power rated or junction temperature in the power devices causes an increase in power losses. Moreover, power modules with higher blocking voltages present higher power losses.

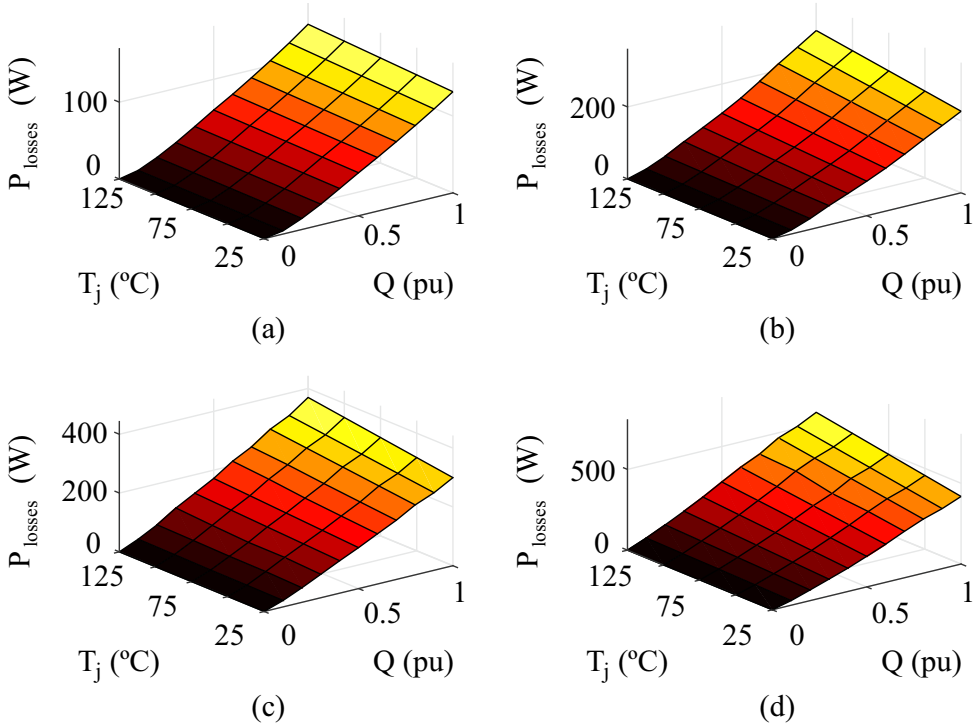

Figure 56 – Power losses of IGBT S_1 for the base cases: (a) C_1; (b) C_4; (c) C_{10}; (d) C_{14}.

Using the look-ups and the thermal model, the power losses in the DSCC-MMCC can be estimated. The power losses of the case studies were evaluated for various power levels. Figure 57 (a) compares the power losses for designs C_1 and C_2. As observed, the power losses reduce when parallel connection is employed. The same can be observed for designs C_6 and C_7 in Fig. 57 (b), where the current capability of the power module increases. Interestingly, when the designs C_8 and C_9 are compared in Fig. 57 (c), it can be concluded that the design with higher current capability not necessarily presents lower losses. The behavior is different depending on the converter current. The same phenomenon is observed when the designs C_{11} and C_{12} are compared. Therefore, the relation between the current rating and the device power losses is not straightforward.

The thermal stresses in the junction temperature of the power devices are illustrated in Fig. 58. For simplification, only case studies C_1 and C_3 are shown for one week. As observed, the junction temperature variations are similar to the mission profile of Fig. 55 (a). Furthermore, the zoomed view in Fig. 58 (a) shows that D_2 is the most stressed semiconductor device in the cells, since STATCOM operation is treated. The solution with the lowest rated current level (C_1) presents a thermal amplitude of 70.7 °C, approximately 18% higher than the C_3 solution. In addition, it is observed that the average temperature and its maximum instantaneous value increase. However, the maximum values are below 130 °C.

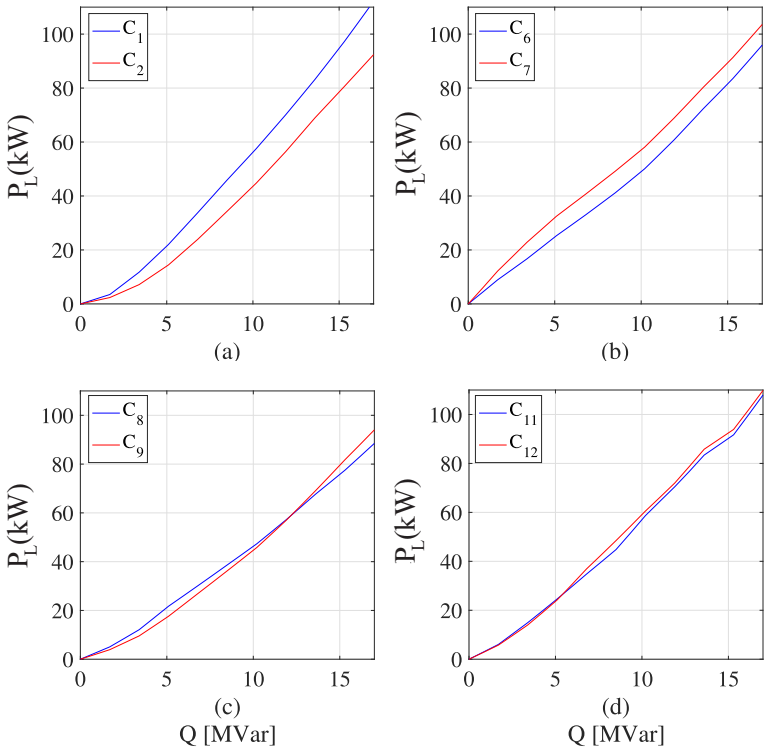

Figure 57 – Power losses in the DSCC-MMC converter in function of the power level: (a) comparison of designs C_1 and C_2; (b) comparison of designs C_6 and C_7; (c) comparison of designs C_8 and C_9; (d) comparison of designs C_{11} and C_{12}.

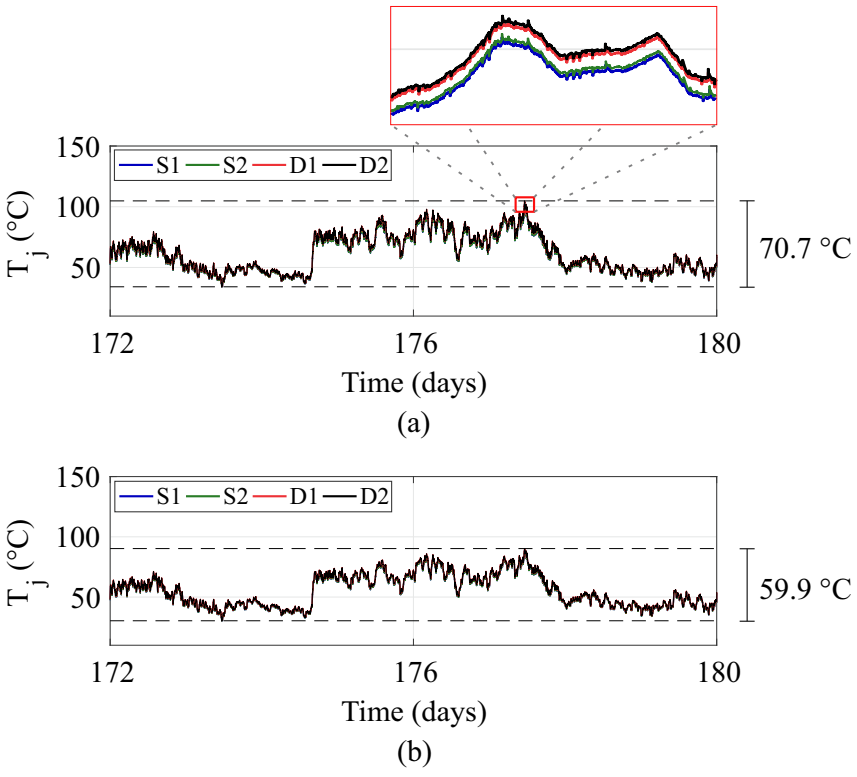

Figure 58 – Junction temperatures of the devices in a cell for two 1700V IGBT solutions: (a) C_1; (b) C_3.

Since the thermal cycling is obtained, the rainflow algorithm and the lifetime model are applied. Figure 59 shows the life consumption in one year for all critical joints of the power devices. As observed, C_1 presents higher LC in all devices and joints. Moreover, the baseplate solder is the most damaged joint. Therefore, for the sake of simplification, the Monte Carlo simulation is implemented only for this failure mechanism.

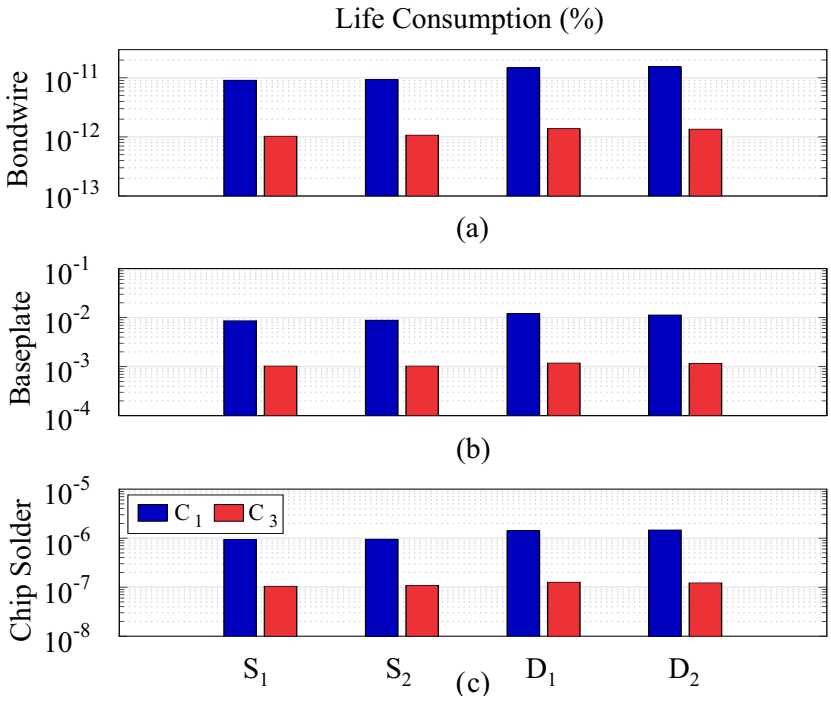

Figure 59 – Static life consumption in power devices for the one-year mission profile (semi-logarithmic scale): (a) bondwire; (b) baseplate; (c) chip Solder.

The Weibull distribution PDF is obtained by employing the static values and the lifetime model into the Monte Carlo simulation with $10,000$ samples and 5% variation. For the sake of simplicity, only the lifetime distribution of D_2 device is presented. Figure 60 shows the result obtained for the four base cases. Figure 60 (c) and (d) show that the 4.5 kV and 6.5 kV voltage classes have more concentrated distribution due to higher thermal losses and stresses in the devices.

The previously lifetime analysis is based on component-level assessment. Equations (4.14)-(4.16) are used to obtain a converter-level reliability assessment. Thus, the unreliability functions for the base cases are shown in Fig. 61 (a). Considering 10 years of operation, the U_{10} unreliability level is analyzed. As observed, the STATCOM based on the design C_4 presents the lowest failure probability (0.12%), when power devices with similar rated current are compared. Furthermore, C_{14} has the highest probability of failure (54.53%). Figure 61 (b) illustrates the effect of increasing the rated current of semiconductor devices, considering the 6.5 kV voltage class. As observed, it can be concluded that the design with higher current rating C_{18} presents a failure probability of 19.61%, while C_{16} presents 88.12%.

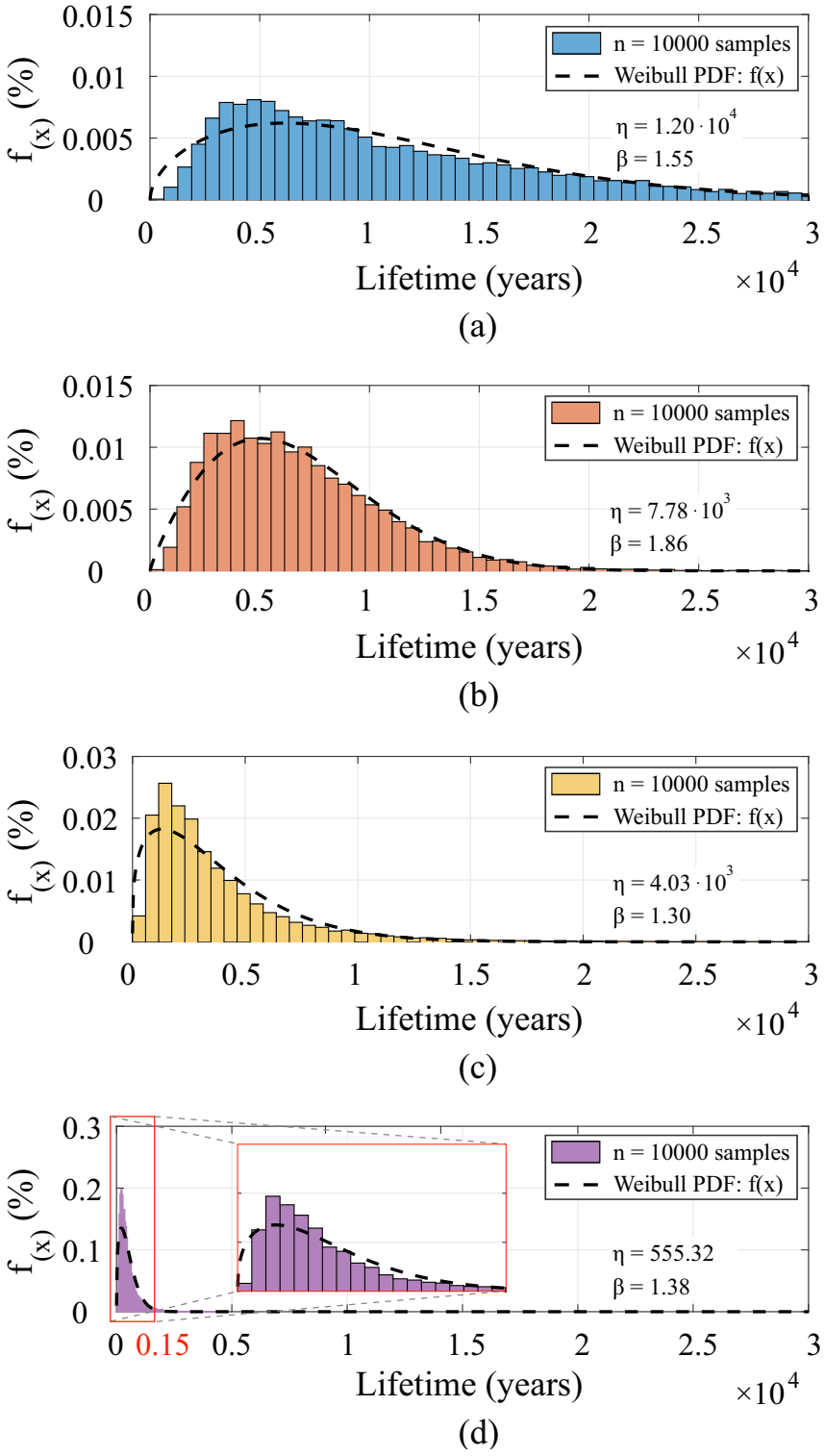

Figure 60 – Lifetime distribution (i.e., the Weibull PDF function) of the most stressed device D_2 for base cases: (a) C_1; (b) C_4; (c) C_{10}; (d) C_{14}.

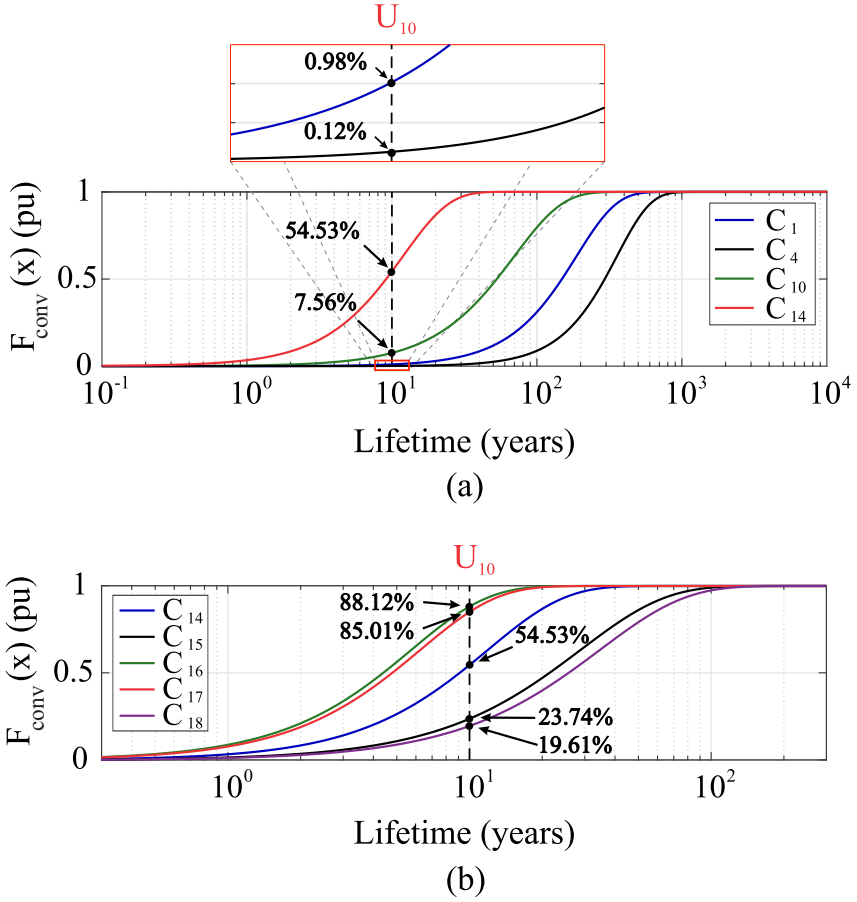

Figure 61 – Converter level unreliability function (semi-logarithmic scale): (a) power devices with the lowest rated current devices for each voltage class (b) power devices with 6.5 kV blocking voltage.

Table 12 summarizes the unreliability level, energy losses and cost for all solutions proposed in this work considering 10 years of operation. The energy consumption is given for 10 years of operation $E_{c_{10}}$, the values are given in per unit (pu) in the base of the 444.2 MWh per year. The total cost is also presented in pu and its base value is 2.53 M.€ The base values refer to the C_1 design. Moreover, the three best performances of each figure of merit are highlighted in Tab. 12. As observed, the solution C_8 has the lowest U_{10} unreliability, whereas C_2 presents the lowest energy consumption and C_4, the lowest cost among the studied solutions.

Finally, Fig. 62 presents the $U_{10} - cost$ map. Two examples are considered to exemplify the reliability-oriented design, $U_{10} < 10$ % and $U_{10} < 0.1$ %. As observed, the voltage class of 6.5 kV is not suitable for an unreliability level less than 10 %. Furthermore, C_4 meets the requirement, with the lowest cost among the eligible designs. However, if the unreliability level is more restricted, for example, less than 0.1 %, the only possible solutions are in the voltage classes of 1.7 kV and 3.3 kV. In this case, C_6 is the most attractive design.

Table 12 – Comparison of the proposed designs.

Case	**U_{10} (%)**	**$E_{c_{10}}$ (pu)**	**Cost (pu)**
C_1	0.98	1	**1**
C_2	0.10	**0.77**	1.70
C_3	0.08	0.89	1.72
C_4	$11.78 \cdot 10^{-2}$	0.95	**0.99**
C_5	$2.22 \cdot 10^{-2}$	0.92	1.18
C_6	$\mathbf{0.11 \cdot 10^{-2}}$	0.90	1.17
C_7	$0.62 \cdot 10^{-2}$	1.06	1.39
C_8	$\mathbf{0.01 \cdot 10^{-2}}$	**0.83**	1.62
C_9	$\mathbf{0.09 \cdot 10^{-2}}$	**0.80**	1.71
C_{10}	7.56	1.05	1.05
C_{11}	2.78	1.01	1.43
C_{12}	15.24	1.05	1.54
C_{13}	4.91	0.97	1.81
C_{14}	54.53	1.10	**1.02**
C_{15}	23.74	0.97	1.04
C_{16}	88.12	1.17	1.28
C_{17}	85.01	1.12	1.46
C_{18}	19.61	0.98	1.72

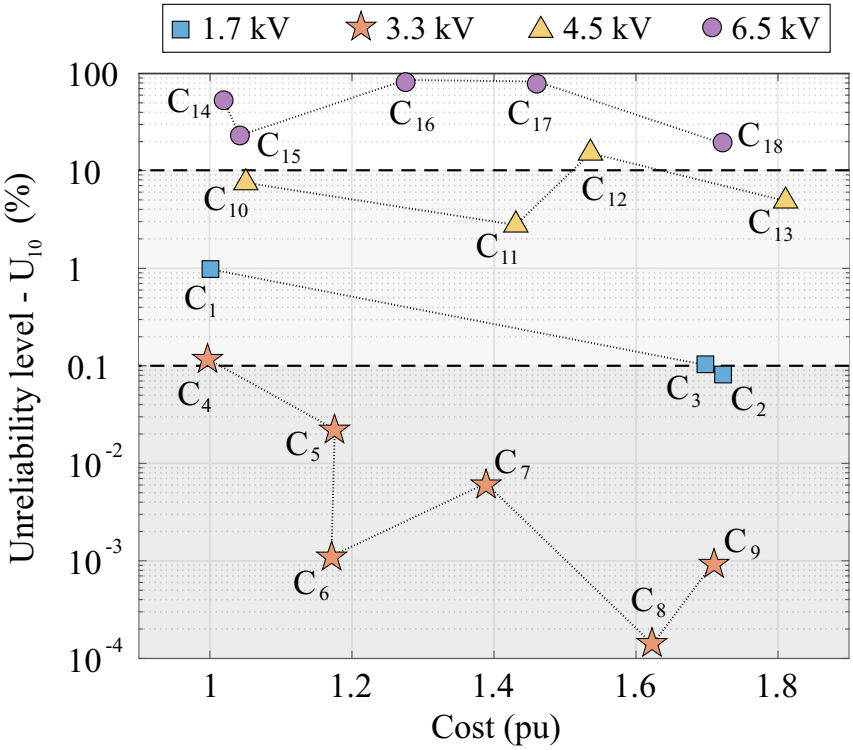

Figure 62 – $U_{10} - cost$ map for the reliability-oriented design (semi-logarithmic scale).

4.7 Chapter Conclusions

This chapter proposed a reliability-oriented design methodology for modular multilevel cascaded converter, based on wear-out failure events of power devices. For that, the unreliability level U_x is presented as a new reliability indicator to evaluate the probability of one failure in the converter for a specified time. The $U_x - cost$ map allows the design engineer to select the most suitable power device according to the converter reliability requirement.

A 17 MVA/13.8 kV DSCC-MMCC-based STATCOM case study is adopted. The simulation results indicate that the solutions based on 3.3 kV present the best $U_x - cost$ trade-off, followed by the 1.7 kV devices. The higher losses and thermal stresses indicate that the 6.5 kV devices are unsuitable for the proposed case study.

It is important to remark that the reliability-oriented design methodology proposed in this chapter can be extended to other multilevel converters, semiconductor technologies (e.g. wide-bandgap devices), applications and cost methodologies. Additionally, U_{10} was employed because the expected operation time of the converter is 10 years. However, this analysis can be easily extended according to the target lifetime and the unreliability requirement of each application.

Although the wear-out failures can be predicted (to some extent) and even avoided, the catastrophic events are difficult to predict. Thereby, to overcome these events, redundant cells shall be added during the converter design. The issues about redundancy implementation in MMCC are discussed in chapter 5.

5 Benchmarking of Redundancy Strategies

5.1 Introduction

MMCC family is often featured with its robustness in terms of cell failures. When failures are identified, the corresponding cell should be bypassed (Son et al., 2012). Under such conditions, some redundancy strategy must be used to ensure the converter remains operating without affecting the overall performance (Davies et al., 2017; Konstantinou; Ciobotaru; Agelidis, 2012). Usually, this condition is fulfilled for a perceptual number of cell failures (Xu; Zhao; Zhao, 2016). This perceptual number of failures is commonly known as *redundancy factor* (f_r) [1].

The MMCC reliability can be improved by redundancy if the following conditions are fulfilled:

- the faulty cell must be identified and removed from the MMCC circuit through some bypass structure;
- the redundant cell must be inserted in the circuit;
- the transient caused by the bypass and insertion procedure must not trigger any converter protection system.

Most publications on MMCC and redundancy strategies investigate the following issues:

- fault detection methods (Shao et al., 2013; Deng et al., 2015; Haghnazari; Shahbazi; Zolghadri, 2015; Liu et al., 2015b; Liu et al., 2016b; Abdelsalam; Marei; Tennakoon, 2017);
- redundancy factor design (Kim; Lee, 2015; Xu; Zhao; Zhao, 2016; Wang et al., 2017; Xu; Jing; Zhao, 2018; Alharbi; Isik; Bhattacharya, 2018; Tu; Yang; Wang, 2019; Farias et al., 2019);
- redundancy strategies implementation (Konstantinou; Ciobotaru; Agelidis, 2012; Liu et al., 2015a; Kim et al., 2015; Ahmed et al., 2015; Farias et al., 2018).

[1] If $f_r = 0.1$, the converter must continue its normal operation if less than 10 % of the cells fail.

As observed, redundancy strategies for MMCC have sparked the interest of researchers. This chapter presents a benchmarking of redundancy strategies applied to MMCC. The redundancy strategies are described and compared considering a 17 MVA DSCC-MMCC-based STATCOM.

5.2 Redundancy Strategies for MMCC

Li et al. (2015) classified the MMCC redundancy strategies into two schemes: hot reserve and cold reserve. In hot reserve-based strategies the redundant cells operate in the same way as other cells. When failures occur, the faulty cells are bypassed while the MMCC keeps working correctly (Li et al., 2015; Hu et al., 2014). In cold reserve-based strategies the redundant cells are bypassed and initially discharged. When failures occur, the corresponding faulty cells are bypassed and redundant cells are inserted into the main circuit (Li et al., 2015; Hu et al., 2014). Thereby, the hot reserve-based strategies can lead to asymmetrical operation in the converter (i.e., different number of cells in the upper and lower arms) and higher power losses, while the cold reserve-based strategies presents more significant transients during failures.

Nevertheless, the redundancy of the MMCC can be implemented without any additional cells. Therefore, the terminology proposed by Li et al. (2015) is incomplete, to some extent. Alternatively, this thesis classifies the redundancy strategies employed in modular multilevel converters into 2 categories, as shown in Fig. 63:

- External Redundancy Strategies: these strategies are based on redundant cells. Therefore, they directly affect the converter CAPEX. The redundancy factor can be as high as required to reach the reliability requirements;
- Inherent Redundancy Strategies: these strategies do not use redundant cells. Some inherent characteristics of the converter are explored to reach fault tolerance. In inherent redundancy strategies, the redundancy factor is limited by some constraints (controllability, maximum absolute cell voltage, etc).

This chapter approaches 4 redundancy strategies: Standard Redundancy operation (SR), Redundancy based on Additional Cells (RAC), Optimized Redundancy based on Additional Cells (RACO) and Redundancy based on Spare Cells (RSC). These strategies guarantee that MMCC is always operating in the linear region of the modulator. The inherent redundancy in overmodulation region (OR) is investigated in the next chapter.

Konstantinou, Ciobotaru and Agelidis (2012), Liu et al. (2015a), Ahmed et al. (2015), Kim et al. (2015) study the SR strategy. When failures occur, the voltage in the remaining operating cells is increased. The number of levels at the converter output is

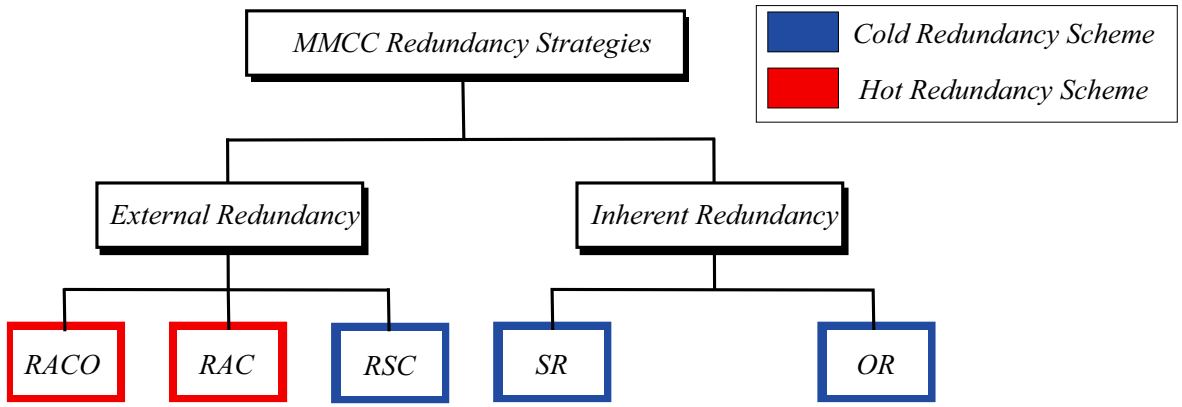

Figure 63 – Classification of the MMCC redundancy strategies proposed in this thesis. RACO - Optimized Redundancy based on Additional Cells; RAC - Redundancy based on Additional Cells; RSC - Redundancy based on Spare Cells; SR - Standard redundancy; OR - Redundancy in overmodulation region.

reduced while the overmodulation is avoided (Konstantinou; Ciobotaru; Agelidis, 2012; Ahmed et al., 2015). According to Konstantinou, Ciobotaru and Agelidis (2012), since MMCC has been built with hundreds of cells, reduce the output voltage levels would be an economic solution. Nevertheless, in practical applications, the safe operating area of the cells is generally 50 - 60 % of the semiconductors blocking voltages (ABB, 2017a). Therefore, the SR redundancy factor is limited by the maximum voltage stresses at the semiconductor devices and cell capacitors.

The RAC strategy operates the converter with more cells than the rated number. When failures occur, the faulty cells are bypassed and the control strategy will be dynamically adapted for the new number of cells (Saad et al., 2015; Choi; Han; Kim, 2016). Two approaches are possible: in the first approach, all cell voltages are controlled at the rated reference value. The reference voltage does not need to be increased after failures. Therefore, less significant transients are observed. However, RAC leads to more switching losses in steady-state and can affect the overall efficiency (Ahmed et al., 2015). A second approach controls the cell voltage to a reduced value under normal conditions. In this case, the voltage stresses in power devices are reduced. Therefore, the switching losses are reduced, leading to an increase in the converter efficiency. When failures occur, the voltage at the cells is increased to avoid overmodulation. This strategy is referred in this chapter as optimized redundancy based on additional cells (RACO).

Finally, the RSC is based on the spare cells concept (Son et al., 2012). Under normal conditions, the spare cells are always bypassed (Li et al., 2015). When failures occur, the faulty cells are replaced by spare cells. The spare cell is then charged by the control strategy. It must be remarked that RSC does not change the number of operating cells. Therefore, any control adaptation is employed. However, if compared to the other

strategies, RSC results in a larger transient unbalance in capacitor voltages, since the spare cells are discharged when it is inserted into the MMCC circuit.

Indeed, each cell has bleeder resistors installed in parallel with the cell capacitor to provide a discharge path for the capacitor when the converter is shutdown (Hassan; Davison, 2011; Sztykiel et al., 2013). Furthermore, some manufacturers generally use these resistors to make voltage divider for achieving a low-voltage input to an auxiliary power supply, which is further employed to power up the cell control card (Sharifabadi et al., 2016). Therefore, when spare cells are inserted, they cannot immediately operate requiring a period of time to charge the capacitors to nominal voltage (Li et al., 2015; Hu et al., 2014).

Li et al. (2015) discuss the application of the RSC strategy in an MMCC-HVDC system. A new control method for MMCC is proposed to seamlessly ride through the period when bypassing a faulty cell and inserting a redundant cell. The RAC strategy is approached by Hu et al. (2014) considering asymmetrical operation of the converter arms. A mathematical model of the MMCC with arms containing different numbers of cells is developed. However, the effect of the redundancy in the efficiency was not approached.

Son et al. (2012) combine RAC and RSC to extend the MMCC redundancy factor, which is modulated by NLC strategy. Whereas failures happen, the RAC strategy is employed. If the number of failures exceeds the number of additional cells, RSC is employed to avoid an extreme emergency or catastrophic failure. Nevertheless, no comparison about power losses was presented by this reference.

On the other hand, Ahmed et al. (2015) compare the dynamic behavior of two redundancy strategies: the first approach employs both SR and RAC with direct modulation. In the second approach, the average voltage of the cells is maintained constant even during failures, as discussed in Konstantinou et al. (2013). Once more, no analysis in terms of power losses was presented.

Thereby, a detailed comparison and analysis of redundancy strategies applied to MMCC has been missing in literature. The next sections aim to fill this void. The four redundancy strategies previously described are compared considering a 17 MVA DSCC-MMCC-based STATCOM.

5.3 Cell Realization and Redundancy

Usually, a bypass structure is included in the converter cell to implement some redundancy strategy. Some approaches adopted in industry are presented in Fig. 64. The bypass realization is strongly dependent on the semiconductor technology employed. Moreover, the bypass structure protects the whole converter mainly during two events: dc

short circuits (very important for HVDC systems) and short circuit failure mode (SCFM) of the semiconductor devices (Ladoux; Serbia; Carroll, 2015).

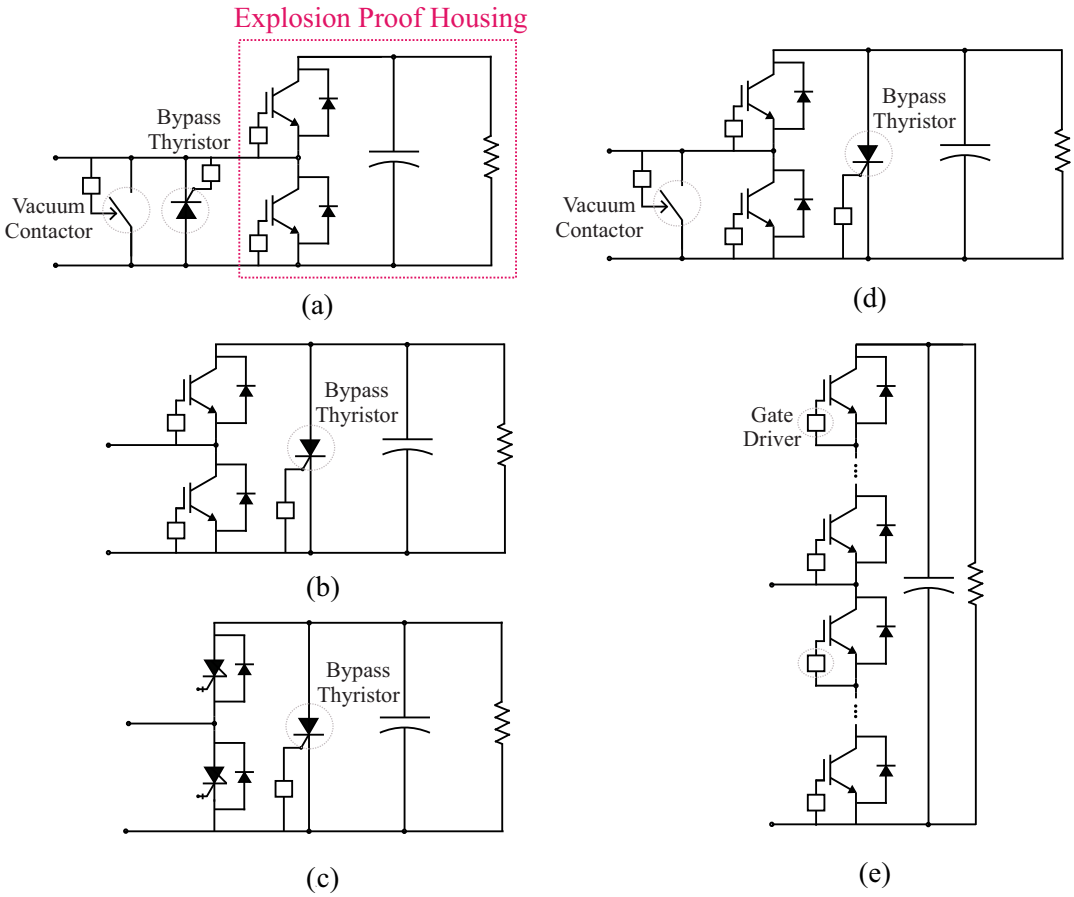

Figure 64 – Different implementations of the bypass structure: (a) bypass structure for PIM-based cells; (b) bypass structure for PPI-based cells (type 1); (c) bypass structure for IGCT-based cells; (d) bypass structure for PPI-based cells (type 2); (e) PPI-based cells without bypass structure. *Remark*: these bypass structures can be adapted for bridge cells.

When plastic IGBT modules (PIM) are employed, the bypass structure is based on one press-pack thyristor connected in parallel with one vacuum contactor, as illustrated in Fig. 64 (a). The thyristor provides a fast bypass (turn-on time of few microseconds) compared with the vacuum contactor (turn-on time of tens of milliseconds) (Wang et al., 2017).

If a dc short circuit happens, the diodes of PIM devices cannot handle the surge currents. This fact is due to the construction of standard PIM devices, which includes the diodes inside the power module. Indeed, PIM devices are mainly designed for motor drives applications, where the current stresses in the diodes are not severe (Ladoux; Serbia; Carroll, 2015; Wang et al., 2017). Therefore, during a dc short circuit, the thyristor is fired to assume the surge currents and protect the diodes. It is important to remark that the selected thyristor is a high voltage device, must present a current rating compatible with

the surge currents and forward voltage drop much lower than the diodes (Bordignon et al., 2016).

Moreover, the bypass structure plays an important role during IGBT failures. PIM presents both open-circuit failure mode (OCFM) and SCFM. During OCFM, the cell capacitor voltage cannot be controlled and the monitoring unit will bypass the cell due to undervoltage or overvoltage (Liu et al., 2015b). However, SCFM leads to a short circuit in the cell capacitor. The surge currents can be as high as 500 kA (Ladoux; Serbia; Carroll, 2015). Even if surge-limiting inductors are employed, the current is still high enough to cause the device explosion (Wang et al., 2017). Therefore, when PIM devices are employed, the cell must present an explosion proof housing (Billmann; Malipaard; Gambach, 2009). Under such conditions, the bypass structure is activated to guarantee the cell current continuity. The role of the vacuum contactor is to assume the arm current, since the thyristor cannot handle ac currents. Moreover, the contactor can handle the rated current without any cooling.

When press-pack IGBT (PPI) devices are used, different bypass structures can be employed, as shown in Fig. 64 (b), (c) and (d). The use of discrete devices allows to choose diodes which can handle the surge currents during dc short circuits. Therefore, no bypass structure is necessary to protect the diodes. Moreover, PPI devices have inherent stable short circuit failure mode (Ødegård et al., 2016). In this case, a bypass thyristor is connected in parallel with the cell capacitance. If a failure happens, the thyristor is fired to assume the discharge current. The thyristor will fail in short circuit and the cell structure will be bypassed thanks to the cell diodes, as shown in Fig. 64 (b) (Chen et al., 2015). This approach was proposed by ABB for IGCT based cells, as shown in Fig. 64 (c) (Ødegård et al., 2016). The main drawback of this approach is the power loss in the diode of the faulty cell. RXPE proposed the use of an additional bypass vacuum contactor, as shown in Figs. 64 (d), to solve this issue (Bordignon et al., 2016).

Finally, ABB proposed a cell without any bypass structure, as shown in Fig. 64 (e) (Oedegard; Monge, 2017). Series connected devices are employed in the cell to avoid the problem of surge currents during SCFM. When one PPI failures, the other IGBTs handle the cell capacitor voltage. Additional devices are included to provide redundancy (Jacobson et al., 2010). Therefore, the redundancy is implemented in device level, instead of cell level approach.

Table 13 presents the semiconductor technology employed in the cells of some commercially available MMCC-based products. The use of IGCTs is still limited since only two companies produce this component (ABB and Mitsubishi). As observed, since the PIM technology is mature and widespread in the industry, many manufactures are interested in this technology.

Table 13 – Overview of the STATCOMs commercially available.

Manufacturer	Semiconductor Technology	Reference
Siemens	Plastic IGBT Module (PIM)	(Davies et al., 2017)
ABB	Press-pack IGBT (PPI)/IGCT	(Oedegard; Monge, 2017)
Alstom	Plastic IGBT Module (PIM)	(Hassan, 2011)
GE	Plastic IGBT Module (PIM)	(GE, 2017)
RXPE	Press-pack IGBT (PPI)	(Bordignon et al., 2016)

5.4 DSCC-MMCC with Redundant Cells

This section presents the control modifications and the definition of the number of additional/spare cells of DSCC-MMCC. The topology is presented in Fig. 65. N_{2Y} operating cells and M additional cells are considered per arm.

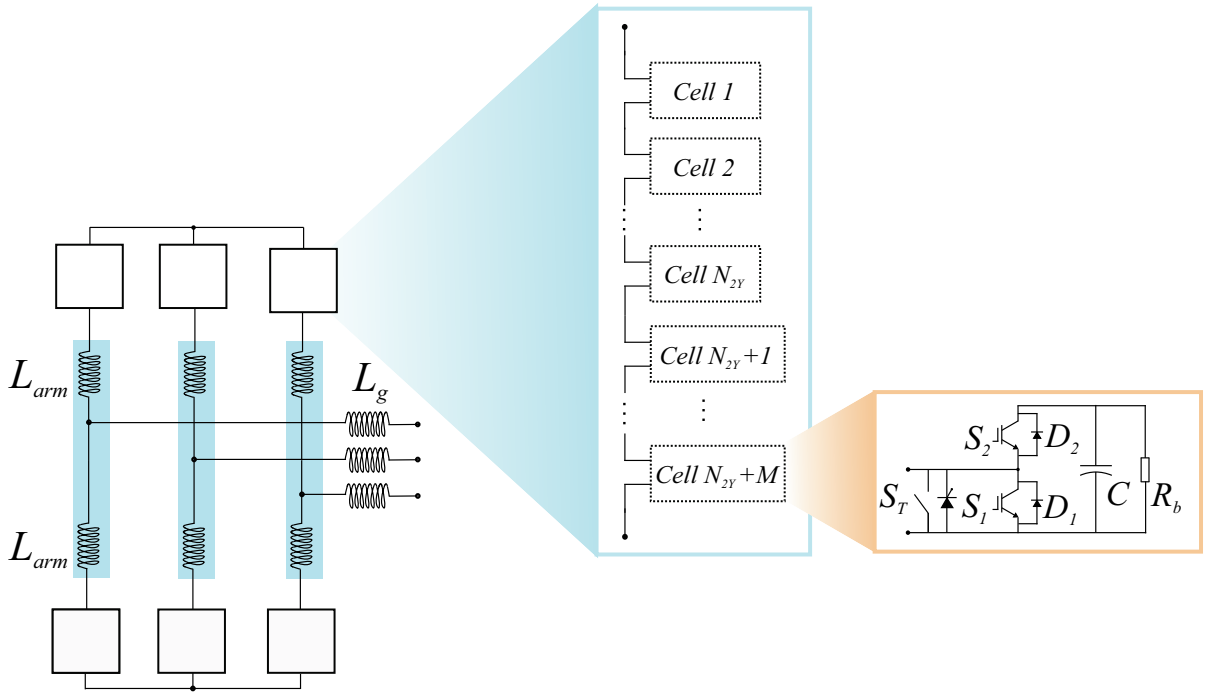

Figure 65 – Schematic of the DSCC-MMCC STATCOM with redundant cells.

5.4.1 Adaptation of the Control Strategy

The control strategy for the DSCC-MMCC STATCOM is the same discussed in section 2.4. Basically, the external loop controls the square of the average voltage v_{avg} of all cells. This average voltage is computed by:

$$v_{avg} = \frac{1}{N_T}\sum_{i=1}^{N_T} v_{c,i}, \tag{5.1}$$

where $v_{c,i}$ is the ith cell voltage. N_T is the total number of operating cells, given by:

$$N_T = \sum_{j=1}^{6} N_{o,j}, \tag{5.2}$$

where $N_{o,j}$ is the number of operating cells of the arm j.

The average voltage reference v^*_{avg} is dependent on the redundancy strategy employed. For RAC and RSC strategies, the voltage of all cells is controlled according to the reference value $v^*_{c,j}$, given by:

$$v^*_{c,j} = \frac{v_{dc}}{N_{2Y}}, \tag{5.3}$$

where v_{dc} is the nominal dc-link voltage. Even during failures, the reference voltages of the cells for RAC and RSC strategies do not change. In this case, the average voltage is given by:

$$v^*_{avg} = \frac{v_{dc}}{N_{2Y}}. \tag{5.4}$$

On the other hand, when RACO and SR strategies are employed, the cell voltage reference at the faulty arms is increased. In this case, the voltage reference is computed separately per arm. Accordingly,

$$v^*_{c,j} = \frac{v_{dc}}{N_{o,j}}. \tag{5.5}$$

Therefore, the average voltage reference v^*_{avg} for RACO and SR strategies is calculated by:

$$v^*_{avg} = \frac{6}{N_T} v_{dc}. \tag{5.6}$$

Under such conditions, the normalized reference signals per phase are given by:

$$v_{u,n} = v^*_b + \frac{v^*_z}{v^*_{c,u}} - \frac{v^*_s}{v^*_{c,u} N_{o,u}} + \frac{v_{dc}}{2 v^*_{c,u} N_{o,u}}, \tag{5.7}$$

$$v_{l,n} = v^*_b + \frac{v^*_z}{v^*_{c,l}} + \frac{v^*_s}{v^*_{c,l} N_{o,l}} + \frac{v_{dc}}{2 v^*_{c,l} N_{o,l}}, \tag{5.8}$$

where $N_{o,u}$ and $N_{o,l}$ are the number of operating cells in the upper and lower arms, respectively.

Finally, for RAC, RACO and SR strategies, the number of operating cells and the number carrier change accordingly. Thus, the phase displacement of the carriers needs

to be adaptive. Therefore, the angular displacement of the carriers is calculated by the following equation:

$$\theta_{c,l}^{i} = 2\pi \left(\frac{n-1}{N_{o,j}} \right). \tag{5.9}$$

where $n = [1, 2, ..., N_{o,j}]$ (Seleme et al., 2019). As observed, the carriers are independently generated for each arm. In this work, if the failures happen in upper arm, the lower arm carries remains unchanged. This fact results in asymmetric voltage waveforms in the MMCC output.

Table 14 resumes the main characteristics of each redundancy strategy described in this chapter, where F is the number of failures in a given arm.

Table 14 – Summary of the main characteristics of redundancy strategies.

Strategy	v_c^*	N_o	M	Reference
RAS	v_{dc}/N_{2Y}	$N_{2Y} + M - F$	$M = \text{ceil}(f_r N_{2Y})$	(Saad et al., 2015)
RASO	v_{dc}/N_o	$N_{2Y} + M - F$	$M = \text{ceil}(f_r N_{2Y})$	(Ahmed et al., 2015)
RSS	v_{dc}/N_{2Y}	N_{2Y}	$M = \text{ceil}(f_r N_{2Y})$	(Son et al., 2012; Li et al., 2015)
SR	v_{dc}/N_o	$N_{2Y} - F$	$M = 0$	(Liu et al., 2015a)

5.4.2 Number of Redundant Cells

The number of redundant cells per arm is given by:

$$M = \text{ceil}(f_r N_{2Y}), \tag{5.10}$$

The redundancy factor f_r is a tradeoff between reliable operation and costs. An empirical redundancy factor of 10% is reported in some technical publications (Ahmed et al., 2015; Konstantinou; Ciobotaru; Agelidis, 2012). For RAC, RACO and RSC, this means that the number of cells is increased in 10 %. For SR, this means that even if 10 % of cells fails there is margin for voltage increasing.

It is important to remark that the number of additional/spare cells is equal to M to obtain the same f_r. Assuming the cell voltages can oscillate with 10 % of ripple, $f_{us} = 0.5$ is employed. This assumption is valid for both RAC and RSC, where v_c^* is essentially constant. For RACO, the cells operate with reduced voltage and $f_{us} = 0.5$ is sufficient.

However, for SR strategy, v_c^* increases when failures happen. In this case, the following relation can be found for f_r and f_{us}:

$$f_r = 1 - \frac{f_{us,0}}{f_{us,f}}, \tag{5.11}$$

where $f_{us,0}$ is the utilization factor in normal conditions and $f_{us,f}$ is the utilization factor when all admissible failures happen. According to (5.11), if the required redundancy factor is 10 %, the utilization factor of semiconductors for SR strategy increases from $f_{us,0} = 0.5$ to approximately $f_{us,f} = 0.56$.

Manipulation of (5.11) yields:

$$k_u = \frac{f_{us,f}}{f_{us,o}} = \frac{N_{2Y}}{N_{2Y} - \text{ceil}(N_{2Y} f_r)}, \tag{5.12}$$

where k_u indicates the perceptual increase in the utilization factor. Since $f_{us,o} = 0.5$ is widely used, $k_u = 1.2$ would be the limit, i.e, $f_{us,f} = 0.6$. However, once the cell voltages present ripple, a safety margin is adopted. Thus, $k_u = 1.15$ is employed. Figure 66 shows the effect of the number of cells in the k_u ratio when $f_r = 10\%$. As observed, k_u exceeds 1.15 depending on the number of cells. Under such conditions, the SR strategy is not suitable because it results in high voltage stresses in the cells.

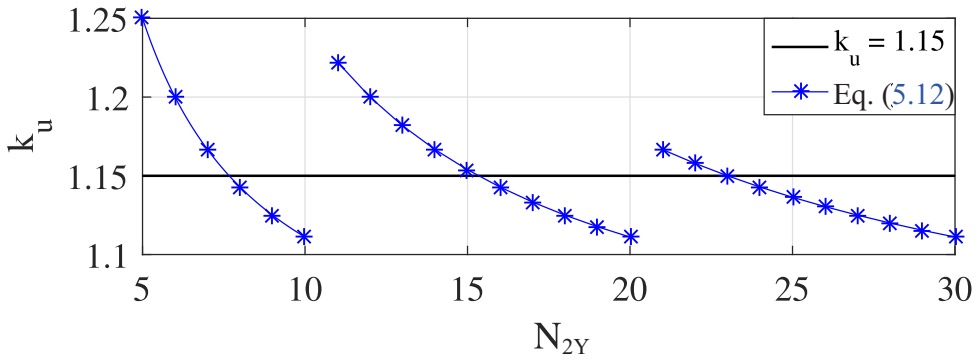

Figure 66 – Perceptual increase in the utilization factor as function of the number of cells. When $k_u \leq 1.15$, SR strategy can reach 10 % of redundancy factor.

Considering the findings of chapter 4, the design C4 is chosen. Therefore, $N_{2Y} = 17$ and $M = 2$ are considered for both RAC, RACO and RSC strategies. For RAC and RACO strategies, all 19 cells are operating. For RSC strategy, 17 cells are operating, while 2 are spare cells. Finally, for SR strategy, $N_{2Y} = 17$ is employed and all of them are operating. The parameters of the simulated system are the same of Tab. 8.

5.5 Results

The redundancy strategies previously discussed were implemented in PLECS environment. The simulation considers injection of 17 Mvar of reactive power. Once the detection of the failure is beyond the scope of this work, the simulation only bypasses the cells. The first failure happens at 0.2 seconds while the second happens at 0.5 seconds. The failures happen in cells of the upper arm of phase A. The objective is to explore all the redundancy capability.

Figure 67 presents the upper arm capacitor voltages of phase A. The cells which fail are presented in different colors for better visualization. As observed in Fig. 67 (a), for RAC strategy the reference voltage of the cells is maintained constant, which results in lower transient when the failures happen. The transient observed is justified by the adjustment of the carrier angular displacement, which is made dynamically according to relation (5.9). Before the failures, the capacitor voltage ripple is slightly lower because the cell capacitance is calculated for the nominal number of cells. Nevertheless, for RAC strategy, more cells are operating. Thereby, the energy storage in the converter is higher than the predicted in the design methodology.

For RACO strategy, as illustrated in Fig. 67 (b), the cells operate with reduced voltage under normal conditions. The average utilization factor before the failures is close to $f_{us,0} = 0.45$, in accordance with (5.11). When failures occur, the cell voltages are increased to maintain the dc-link voltage at the nominal value, avoiding overmodulation. The increase in the reference voltage generates a transient response in the capacitor voltages, which reaches steady-state after approximately 100 ms. When the redundancy factor is completely explored (10 % of failures = 2 cells), the cell voltages reach the nominal value and the average utilization factor is $f_{us,f} = 0.5$.

Figure 67 (c) illustrates the cell voltages for RSC strategy. When the failure occurs, the spare cells are inserted and their charging process is started. This process is detailed in Fig. 68. During the charging process, the cell voltages reach 1.9 kV (1.15 pu). After 150 ms, the spare cell charging process is finished and the converter reaches steady-state. It is important to observe that in RSC strategy, the number of carriers is not changed, since the faulty and spare cells are exchanged.

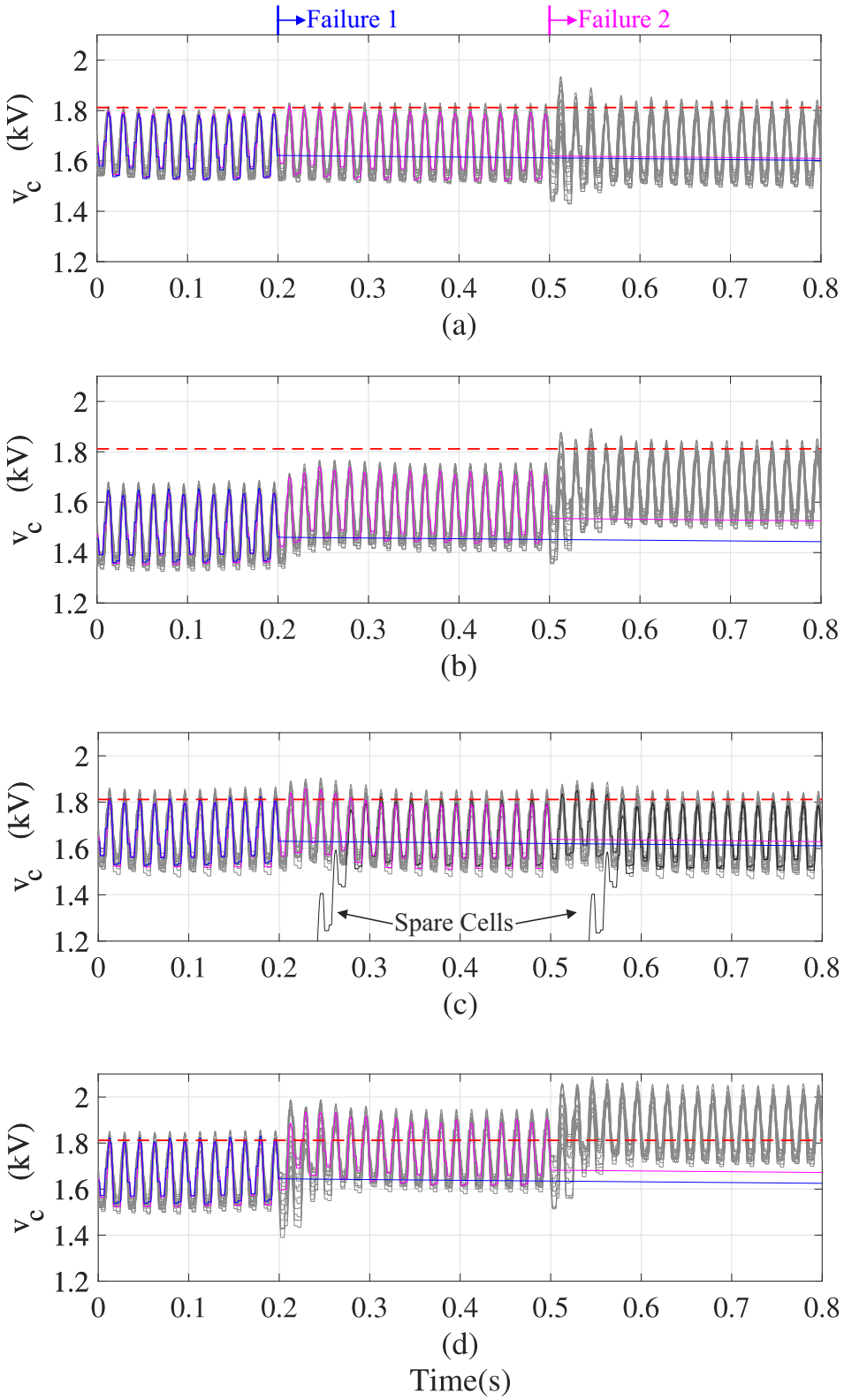

Figure 67 – Effect of the redundancy strategies in the upper arm cell voltages: (a) RAC; (b) RACO; (c) RSC; (d) SR.

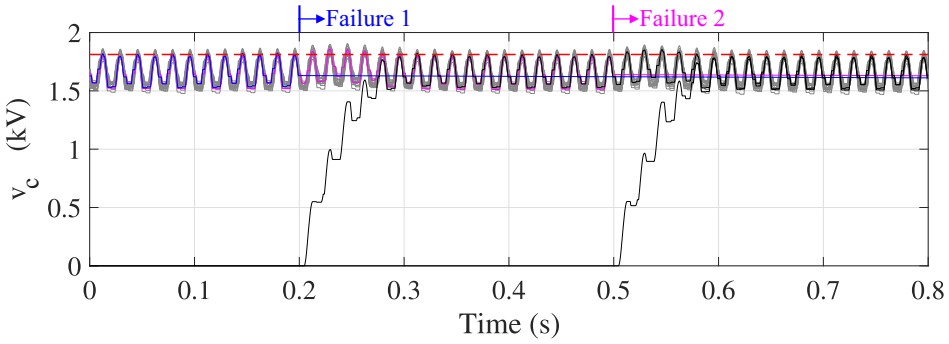

Figure 68 – Dynamic behavior of the charging process of spare cells for RSC strategy.

The results for the SR strategy are shown in Fig. 67 (d). As observed, this strategy has similar dynamic behavior to the RACO strategy. However, the SR does not present redundant cells. Thereby, the cell voltages increase to values higher than the nominal. Considering 10 % of failures, i.e. 15 cells operating, the cell voltage reference reaches approximately 1.13 pu, resulting in an utilization factor of $f_{us,f} \approx 0.56$, in accordance with (5.11). Regarding the voltage ripple, the maximum voltage reached is 1.2 pu in steady-state, leading to a maximum utilization factor of 0.6.

Figures 69 (a)-(d) present the behavior of the lower arm capacitor voltages. As observed, the capacitor voltages are controlled to the respective reference values. These values are not changed during the simulation, since the failures happen only in upper arm. As observed, the redundancy strategies do not significantly affect the remaining operating arms.

The detail of the grid current dynamic behavior during the first failure is presented in Fig. 70. As observed in Figs. 70 (a) and (e), no significant transient is observed for RAC strategy. RACO and SR strategies present a similar performance and the small current transient is rejected in approximately 50 ms, as shown in Figs. 70 (b), (d) (f) and (h). Finally, Figs. 70 (c) and (g) illustrates the response for RSC. The current becomes slightly distorted. This fact is justified by the charging process of the spare cell, which increases the portion of individual action in the relations (5.7) and (5.8).

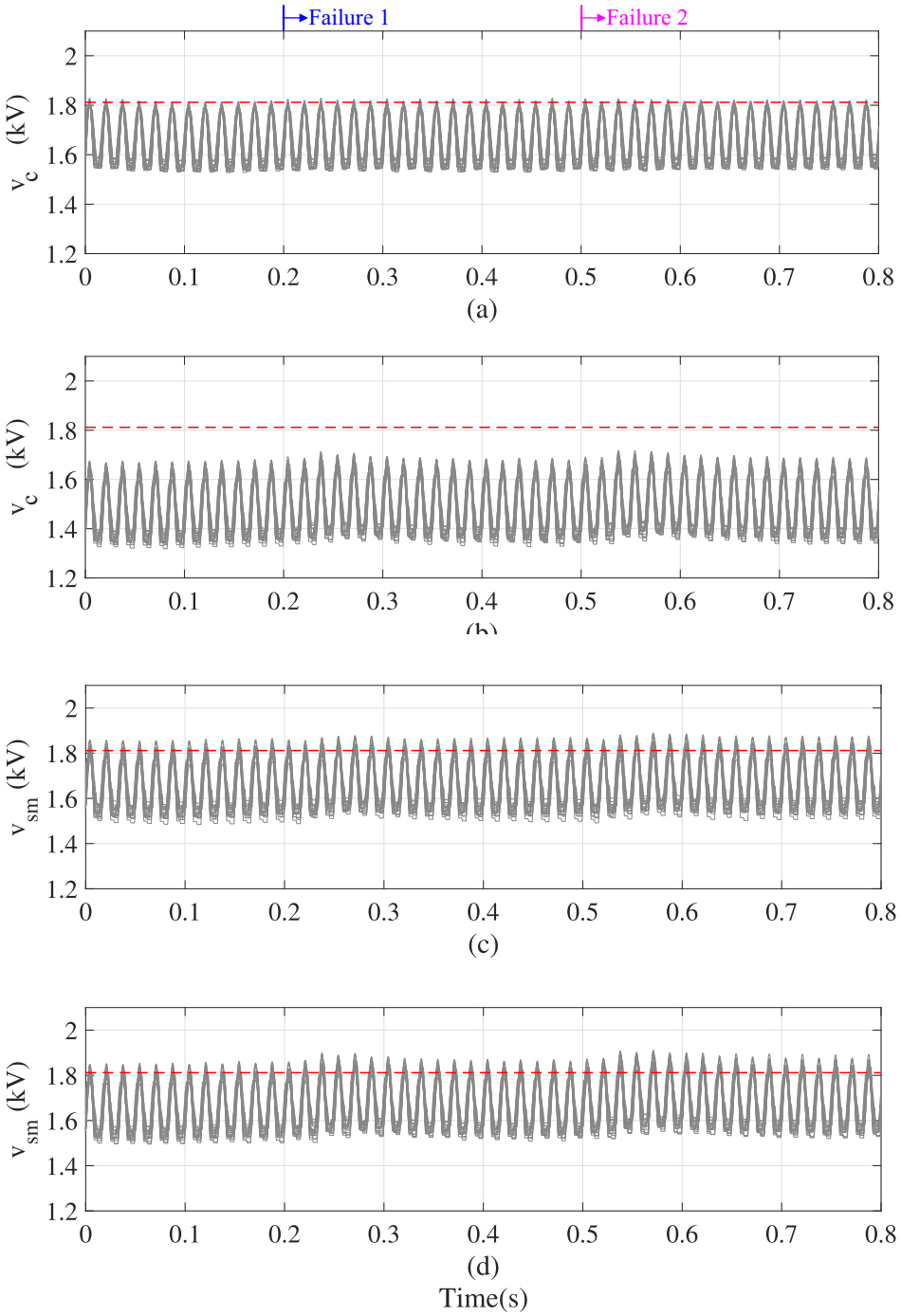

Figure 69 – Effect of the redundancy strategies in the lower arm cell voltages: (a) RAC; (b) RACO; (c) RSC; (d) SR.

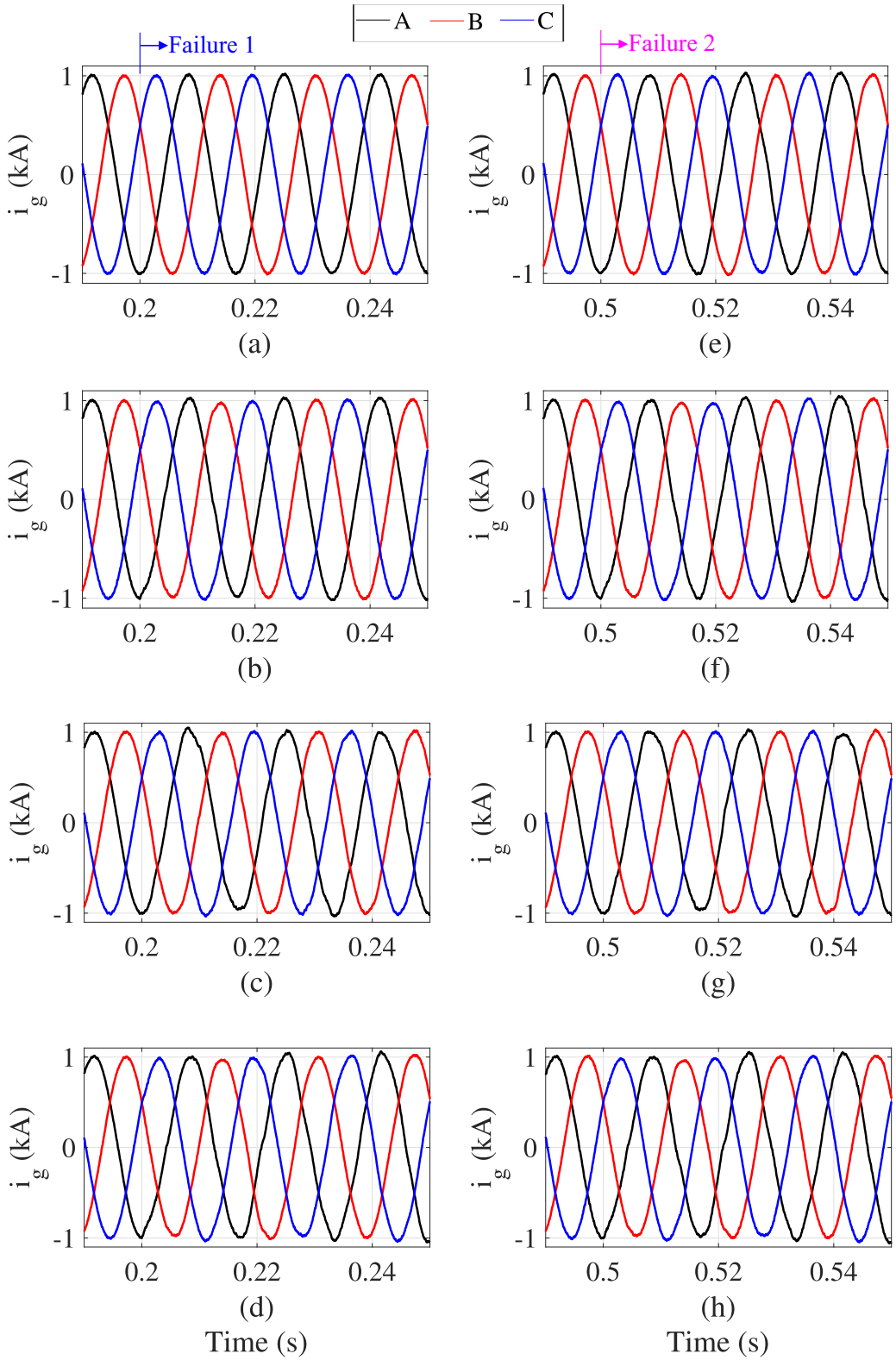

Figure 70 – Effect of the redundancy strategies in the grid current dynamic behavior: (a) RAC - first failure; (b) RACO - first failure; (c) RSC - first failure; (d) SR - first failure; (e) RAC - second failure; (f) RACO - second failure; (g) RSC - second failure; (h) SR - second failure.

The behavior of the active and reactive instantaneous power are presented in Fig. 71. As observed, more significant transients are observed for RACO and SR strategies, which changes the voltage reference of all capacitors and consequently requires a higher energy exchange with the grid.

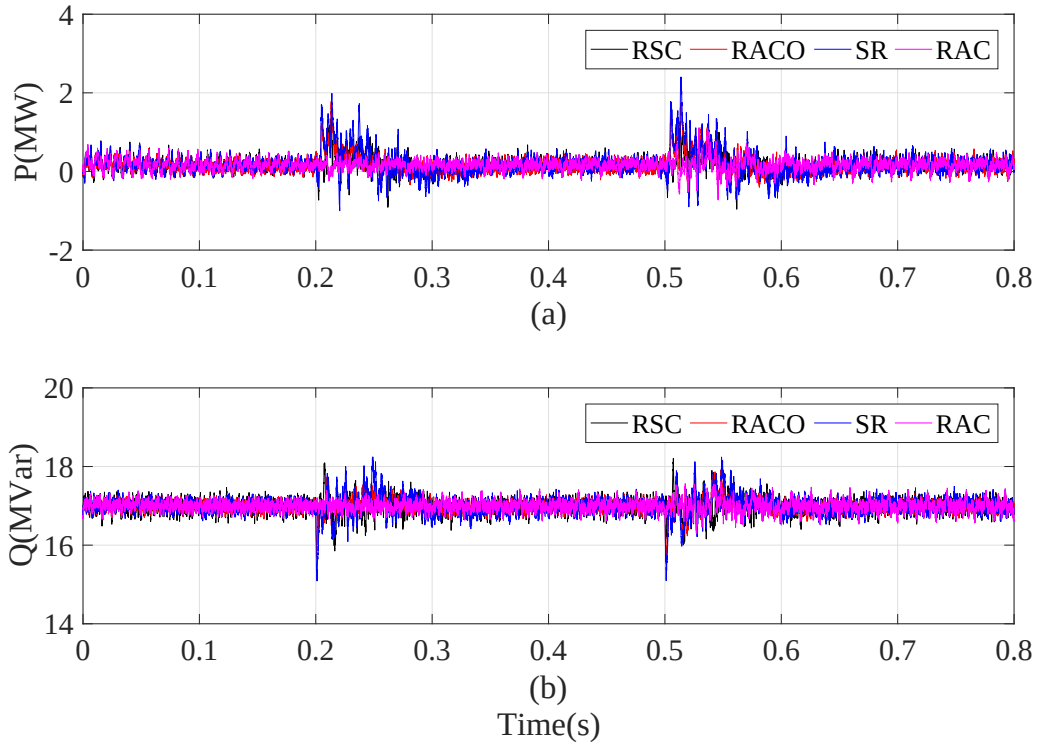

Figure 71 – Effect of the redundancy strategies in the injected power: (a) instantaneous active power; (b) instantaneous reactive power.

Finally, the semiconductor devices power losses were evaluated considering the operation under normal conditions (without failures). As observed in Tab. 15, the RAC strategy presents 11.8 % more losses than SR strategy. This fact is justified by the higher number of operating cells in RAC. The RSC does not affect the converter efficiency, since the STATCOM always operates with the same number of cells of SR strategy.

The RACO strategy presents lower switching losses, thanks the operation with reduced voltage. Nevertheless, this strategy presents 17 % less losses than RAC strategy. This fact can be justified by the low switching frequency employed (210 Hz). Under such condition, the conduction losses dominate the overall losses.

As observed in previous results, RAC strategy presents a superior performance for both cell capacitor voltage dynamics and grid current control. However, this strategy presents higher power losses. These losses are slightly reduced if the RACO strategy is employed. Furthermore, these strategies present similar costs. In terms of control complexity, both RAC and RACO strategies compute $12(N_{2Y} + M)$ gate signals and the phase displacements of the carriers need to be adaptive.

Table 15 – Effect of the redundancy strategies in the power losses (only the semiconductor devices).

Strategy	SR	RAC	RACO	RSC
Conduction Losses	69.87 kW	78.09 kW	78.18 kW	69.87 kW
Switching Losses	14.89 kW	16.67 kW	14.90 kW	14.89 kW
Total losses	84.76 kW	94.76 kW	93.08 kW	84.83 kW
$\Delta P_L(\%)$	–	+11.8 %	+9.82 %	0 %

The RACO and SR strategies presented similar overshoot and settling time for voltage control. The SR presented lower losses than RACO, even working with higher cell voltages. This strategy also presents the lower cost, since no additional cells are necessary. In terms of control complexity, SR strategy computes $12N_{2Y}$ gate signals and the phase displacements of the carriers also need to be adaptive.

The RSC strategy presented a worst dynamic performance in terms of voltage, once the spare cells are maintained discharged. However, this strategy considerably reduces the power losses in the MMCC. This strategy has similar costs if compared with RACO strategy. However, the control complexity is reduced, once RSC strategy computes $12N_{2Y}$ gate signals. Furthermore, this strategy is less complex than SR strategy, since the phase displacement of the carriers does not need to be adaptive.

It can be observed that more than one redundancy strategy can be explored to obtain a given redundancy factor with reduced cost. However, this discussion is beyond the scope of this work and should be addressed in further studies. Table 16 summarizes the main characteristics of the studied redundancy strategies. The qualitative terms excellent, good and regular indicate the best, average and worst performance, respectively.

Table 16 – Comparison of the redundancy strategies applied to DSCC-MMCC.

Strategy	RAC	RACO	RSC	SR
v_c dynamics	Excellent	Good	Regular	Good
i_g dynamics	Excellent	Good	Regular	Good
Losses	Regular	Good	Excellent	Excellent
Control complexity	Regular	Regular	Excellent	Good
Cost	Regular	Regular	Regular	Excellent

5.6 Chapter Conclusions

This chapter discussed the redundancy strategies for MMCC. The redundancy strategies were classified and explained. The implementation of the bypass structure was discussed from the industry perspective. A benchmarking of the redundancy strategies presented in literature was presented. Complexity, dynamic behavior and power losses were

used as figures of merit. The RSC and SR strategies present lower losses and seem to be a good solution for redundancy implementation in modular multilevel cascaded converters.

Next chapter presents the inherent redundancy in the overmodulation region for DSCC-MMCC-based STATCOMs.

6 Boundary of Linear Region for MMCC and Cost-Effective Design

6.1 Introduction

As discussed in the previous chapter, the redundancy strategies have been extensively explored in the literature. Nevertheless, there is gap in the technical literature when the number of failures in a given arm exceeds the number of redundant cells. Under such conditions, the required voltage can be higher than the available sum of the capacitor voltages.

Fig. 72 illustrates the reference voltages synthesized by one converter arm and the available sum of capacitor voltages for a DSCC-MMCC STATCOM operating at rated inductive reactive power to exemplify the problem. At the time 33 ms, some failures occur. In this example, the converter has no available redundant cell. Under such conditions, two approaches can be implemented. The first one is the reduction of the reactive power reference to reduce the reference voltage, as indicated in the dashed line. Thus, the converter will continue to operate in the linear region. Nevertheless, in the context of a STATCOM application, the derating will limit the STATCOM in terms of voltage regulation capability, which might be detrimental to the transmission system operator (TSO).

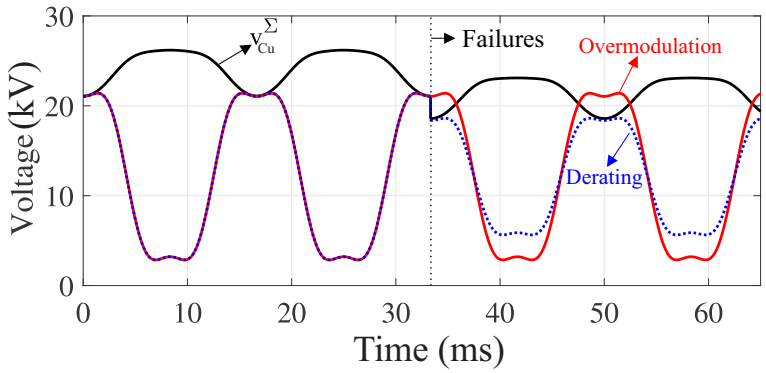

Figure 72 – Inherent redundancy strategies for a DSCC-MMCC-based STATCOM.

Other solution (frequently avoided in the literature) is operating the STATCOM in the overmodulation region. If this approach is adopted, some opportunities can be explored:

1. the converter design can be developed with the minimum number of cells. Therefore, DSCC-MMCC operates in the boundary between linear and overmodulation region

in the worst operation conditions. During transients in the grid voltage or variations in the grid impedance, the converter will operate in the overmodulation region and keep supporting the grid;

2. the extra voltage capability available in the overmodulation region implies in an inherent redundancy factor that can be explored if failures occur;

3. if the absolute minimum number of cells is employed and the design considers the inherent redundancy, a cost-effective design can be reached.

The main drawback of this approach is the increase in the current total harmonic distortion. Nevertheless, the increase in the harmonic distortion might not be an issue in the beginning of overmodulation region if the converter is already modulated by stair-case modulation schemes (e.g., nearest level control).

Briff, Moreno and Chivite-Zabalza (2017) propose a space vector modulator for an MMCC HVDC system in the overmodulation region during voltage transients. López et al. (2015) discuss the operation in the overmodulation region during the failures for a DSCC-MMCC-based HVDC system with carrier-based modulation. These approaches are limited by the modulator complexity for a high number of cells. Furthermore, these references do not discuss the boundaries between linear and nonlinear regions. Indeed, the potential of overmodulation as a fault-tolerant solution for MMCC has not been discussed in the technical literature.

Therefore, an analysis of the inherent redundancy of modular multilevel cascaded converters in the overmodulation region is missing in the technical literature. This chapter aims to fill this void, by providing the following contributions:

- analytical expression for the boundary of linear region in a DSCC-MMCC;
- sensitivity analysis of the limits with respect to the cell capacitance, grid impedance, grid voltage power factor and injected current;
- discussion on the potential for fault tolerance in the overmodulation region.

The results are based on a 17 MVA DSCC-MMCC-based STATCOM connected to a 13.8 kV electrical grid. The converter is designed in the limit of linear region. The converter is modulated based on nearest-level control with cell tolerance band algorithm.

6.2 Insertion Indexes

As discussed in Section 2.3.3, when NLC modulation strategy is employed in DSCC-MMCC, the cell capacitor voltages are balancing through a sorting and selection

algorithm. Under such conditions, the inserted voltages in upper and lower arms can be approximated by (Hagiwara; Maeda; Akagi, 2011):

$$v_u = v_z^* - v_s^*, \tag{6.1}$$

$$v_l = v_z^* + v_s^*, \tag{6.2}$$

where v_s^* is the output voltage reference (which drives i_g) and v_z^* is the internal voltage (which drives i_z). The inserted voltages must be normalized to result in the insertion indexes. As previously discussed in Chapter 2, the normalization strategy significantly affects the stability of the closed loop system (Harnefors et al., 2013). The normalization performed by Hagiwara, Maeda and Akagi (2011) consists in the division of the reference signals by the measured sum of the capacitor voltages, since this sum is the available voltage. Nevertheless, this strategy results in instabilities, which requires the use of additional control loops (Antonopoulos; Angquist; Nee, 2009; Hagiwara; Maeda; Akagi, 2011).

When the voltages are normalized by the effective dc-link voltage $v_{dc,2Y}$, errors are observed between the reference and synthesized voltages. Generally, these errors can be compensated by the current loops. However, it will affect the definition of the overmodulation limits, since the reference voltage and the voltage at the converter output will not be the same. Therefore, this work uses the approach proposed in (Angquist et al., 2011), where the reference voltages are normalized by the estimation of the sum of capacitor voltages, here denoted by $\tilde{v}_{Cu}^{\Sigma}$ and $\tilde{v}_{Cl}^{\Sigma}$. Accordingly:

$$n_u = \frac{v_z^* - v_s^*}{\tilde{v}_{cu}^{\Sigma}}, \tag{6.3}$$

$$n_l = \frac{v_z^* + v_s^*}{\tilde{v}_{cl}^{\Sigma}}. \tag{6.4}$$

By neglecting the harmonics in the circulating current, $v_z \approx v_{dc,2Y}/2$ and the insertion indexes in steady-state can be approximated by:

$$n_u \approx \frac{\frac{v_{dc,2Y}}{2} - v_s^*}{\tilde{v}_{cu}^{\Sigma}}, \tag{6.5}$$

$$n_l \approx \frac{\frac{v_{dc,2Y}}{2} - v_s^*}{\tilde{v}_{cl}^{\Sigma}}. \tag{6.6}$$

In the linear region of the modulator, it is expected that $0 \leq n_u \leq 1$ and $0 \leq n_l \leq 1$. This means that the inserted voltages are lower than the sum of capacitor voltages for all

operating conditions. Supposing now that some failures occur in one of the arms, the faulty arm will operate in the overmodulation region. Under such conditions, two strategies can be considered:

- unsymmetrical operation: only the faulty cells are bypassed;
- symmetrical operation: cells in all arms are bypassed to maintain an equal number of cells per arm.

The theoretical waveforms after the failure for each strategy are illustrated in Fig. 73. For the unsymmetrical operation, the dc-link voltage value is maintained. Under such conditions, the faulty arm must handle the dc-link voltage and synthesize the same output voltage. For the symmetrical operation, the dc-link voltage is reduced proportionally to the number of failures, since the arms always operate with the same number of cells. Therefore, the converter operation in the overmodulation region is reduced, which benefits the control. For this reason, the symmetrical operation is approached in this chapter.

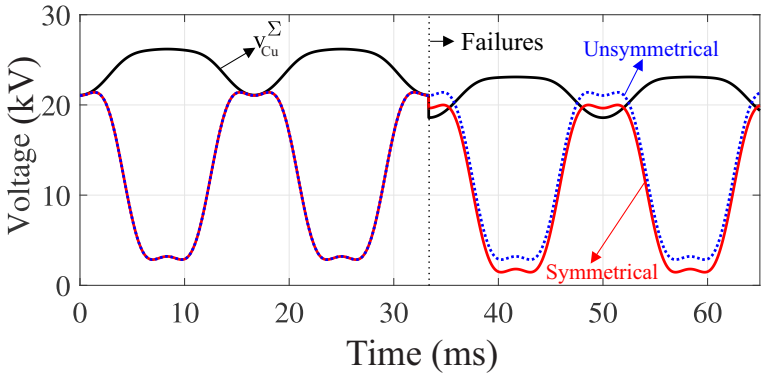

Figure 73 – Steady-state reference waveforms for the symmetrical and unsymmetrical operation of DSCC-MMCC-based STATCOM.

6.3 Boundary Between Linear and Non-Linear Region

The boundary of linear region in traditional 2-level converters modulated with carrier-based methods is usually defined in terms of the modulation index. The modulation index can be defined as (Ilves et al., 2014):

$$m = \frac{2\hat{V}_s}{v_{dc,2Y}} \tag{6.7}$$

where $\hat{V}_s$ is the fundamental component magnitude of line-to-neutral voltage. The modulation index at the boundary between linear and non-linear region is denoted as m_b.

The boundary is usually interpreted as the value of output voltage which leads to equal amplitudes in the reference and carrier signals. For example, if sinusoidal modulation is employed, $m_b = 1$ while $m_b \approx 1.15$ when 1/6 of third harmonic injection is considered in the reference voltage.

When compared with traditional 2-level converters, DSCC-MMCC has specific characteristics which affects considerably the boundary between linear and nonlinear region. Indeed, the nonlinear (overmodulation) region starts when the insertion indexes (6.5) and (6.6) are greater than 1, i.e. the inserted voltages are higher than the sum of capacitor voltages.

The output voltage depends directly on the sum of capacitor voltages in each arm, which is the available voltage. The sum of capacitor voltages presents a non-negligible ripple (typically in the range between 5 and 15 % at rated conditions) and the ripple waveform is strongly dependent of the operation conditions. Therefore, the computation of the modulation index in the boundary of linear region is not straightforward.

The limits of the linear region are important to guarantee a proper and cost-effective converter design. This section aims to study analytically this phenomenon.

6.3.1 Maximum Output Voltage

Due to symmetry, only the lower arm is analyzed. It is assumed that the error in the sum of capacitor voltages estimation is negligible, i.e. $\tilde{v}_{cl}^{\Sigma} \approx v_{cl}^{\Sigma}$. Therefore, the insertion index is given by:

$$n_l = \frac{v_z^* + v_s^*}{v_{cl}^{\Sigma}}. \tag{6.8}$$

The converter output voltage (per phase) and output current are given by:

$$v_s = \widehat{V}_s \cos(\omega_n t), \tag{6.9}$$

$$i_g = \widehat{I}_g \cos(\omega_n t - \varphi). \tag{6.10}$$

By neglecting the harmonics in circulating current and considering the control strategy discussed in the last section, the following equation can be derived for the insertion indexes:

$$n_l = \frac{\frac{N_{2Y} - F}{N_{2Y}} \frac{v_{dc,2Y}}{2} + \widehat{V}_s \cos(\omega_n t) - \frac{1}{6}\widehat{V}_s \cos(3\omega_n t)}{v_{dc,2Y}\left(\frac{N_{2Y} - F}{N_{2Y}}\right) + \Delta v_{cl}^{\Sigma}}, \tag{6.11}$$

where F is the number of failures.

Using a similar development of Angquist et al. (2011), the sum of capacitor voltage ripples in the lower arm can be estimated by:

$$\Delta v_{cl}^{\Sigma} = \frac{N_{2Y}}{2C_{2Y}v_{dc,2Y}}\left(\Delta W_{\Sigma} - \Delta W_{\Delta}\right), \tag{6.12}$$

where:

$$\Delta W_{\Sigma} = -\frac{\widehat{V}_s\widehat{I}_g}{4\omega_n}\sin\left(2\omega_n t - \varphi\right) + \frac{\widehat{V}_s\widehat{I}_g}{24\omega_n}\sin\left(2\omega_n t + \varphi\right) + \frac{\widehat{V}_s\widehat{I}_g}{48\omega_n}\sin\left(4\omega_n t - \varphi\right), \tag{6.13}$$

$$\Delta W_{\Delta} = \frac{N_{2Y} - F}{N_{2Y}}\frac{v_{dc,2Y}\widehat{I}_g}{2\omega_n}\sin\left(\omega_n t - \varphi\right) - \frac{2\widehat{V}_s i_z}{\omega_n}\sin\left(\omega_n t\right) + \frac{\widehat{V}_s i_z}{9\omega_n}\sin\left(3\omega_n t\right). \tag{6.14}$$

Assuming a sufficiently high switching frequency, the circulating current i_z in relation (6.14) can be replaced by its dc value, which can be approximated by:

$$i_z \approx \frac{N_{2Y}}{N_{2Y} - F}\frac{\widehat{V}_s\widehat{I}_g}{2v_{dc,2Y}}\cos\left(\varphi\right). \tag{6.15}$$

In the limit of the modulator linear region, $0 \leq n_l \leq 1$. The first part of this inequality results in (see Appendix B for more details):

$$0 < \frac{v_{dc,2Y}}{2} + v_s^* \Leftrightarrow \widehat{V}_{s0} \leq \frac{N_{2Y} - F}{N_{2Y}}\frac{v_{dc,2Y}}{\sqrt{3}}. \tag{6.16}$$

If $F = 0$, relation (6.16) leads to the same result obtained for 2-level converters (Hava; Kerkman; Lipo, 1998). Nevertheless, when the second inequality is taken into account, the shape of the capacitor voltage imposes a limit for the maximum output voltage. The maximum insertion index ($n_l = 1$) is obtained when v_s^* reaches the maximum value, which means $\omega_n t = \pi/6$. By replacing $\omega_n t = \pi/6$ and (6.12) in (6.11), the maximum output voltage can be computed by (see Appendix B for more details):

$$\widehat{V}_{s1} = \max\left(\frac{-b + \sqrt{b^2 - 4ac}}{2a}; \frac{-b - \sqrt{b^2 - 4ac}}{2a}\right), \tag{6.17}$$

where

$$a = \frac{2N_{2Y}^2\widehat{I}_g}{9\left(N_{2Y} - F\right)\omega_n C_{2Y}v_{dc,2Y}^2}\cos\left(\varphi\right), \tag{6.18}$$

$$b = \frac{N_{2Y}\widehat{I}_g}{4\omega_n C_{2Y}}\left[-\frac{1}{2v_{dc,2Y}}\sin\left(\frac{\pi}{3}-\varphi\right)+\right.$$

$$\left.+\frac{1}{12v_{dc,2Y}}\sin\left(\frac{\pi}{3}+\varphi\right)+\frac{1}{24v_{dc,2Y}}\sin\left(\frac{2\pi}{3}-\varphi\right)\right]-\frac{\sqrt{3}}{2}, \tag{6.19}$$

$$c = \frac{N_{2Y}-F}{N_{2Y}}\frac{v_{dc,2Y}}{2}-\frac{(N_{2Y}-F)\widehat{I}_g}{4\omega_n C_{2Y}}\sin\left(\frac{\pi}{6}-\varphi\right). \tag{6.20}$$

Finally, the maximum output voltage can be computed by:

$$\widehat{V}_{s,max} = \min(\widehat{V}_{s0};\widehat{V}_{s1}). \tag{6.21}$$

Figure 74 shows the behavior of the DSCC-MMCC maximum output voltage as function of the current angle. The parameters of Tab. 17 were employed and operation at rated current is assumed. As observed, the maximum output voltage depends on the operating power factor. For the inductive power factor, the output voltage is limited by the sum of capacitor voltages. For the capacitive power factors, the output voltage presents the same value obtained for 2-level converters.

Table 17 – Parameters of the DSCC-MMCC-based STATCOM studied in this work.

Parameter	Value
Line to line grid voltage (V_g)	13.8 kV
Line frequency (f_n)	60 Hz
Effective dc voltage ($v_{dc,2Y}$)	25 kV
Rated power (S_n)	17 MVA
Transformer X/R ratio	18
Arm inductances (L_{arm})	3 mH ($\approx$ 0.1 pu)
Arm inductor X/R ratio	17
Cell capacitance (C_{2Y})	6.8 mF
Nominal cell voltages (v_c^*)	962 V
Number of cells per arm N_{2Y}	26
Sampling Frequency f_s	10.92 kHz

6.3.2 Minimum Dc-link Voltage

The minimum output voltage required for grid connected applications when the converter injects rated current (1 pu) can be computed by [1]:

$$\widehat{V}_s = \widehat{V}_g\sqrt{\left[(1+\Delta V_g)+x_{eq}\sin(\varphi)\right]^2+\left[x_{eq}\cos(\varphi)\right]^2}, \tag{6.22}$$

[1] In the presented analyses, the resistive part of the transformer and inductor impedances are neglected.

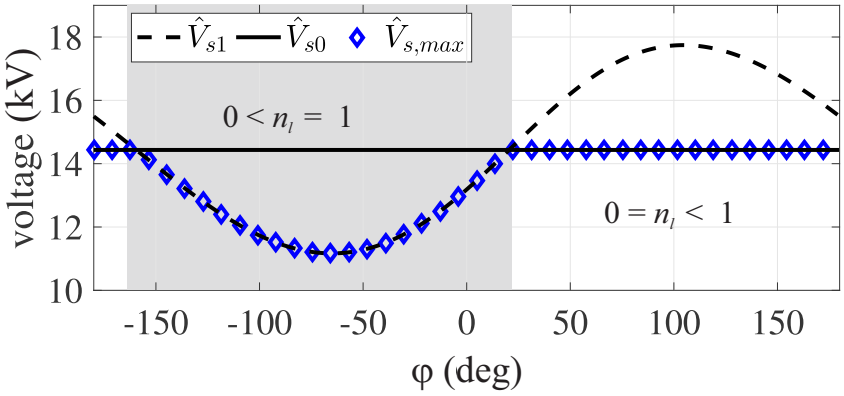

Figure 74 – Maximum obtained output voltage as function of the operating power factor in the linear region of the modulator.

where ΔV_g refers to the perceptual variations in the grid voltage. $\widehat{V}_g$ is the peak of the grid voltage (per phase). x_{eq} refers to the per unit output reactance of the converter, given by:

$$x_{eq} = \left(\frac{x_{arm}}{2} + x_g\right), \tag{6.23}$$

where x_{arm} and x_g are the arm and the output reactance in per unit values, respectively.

In the region where n_l is limited by the zero voltage, the DSCC-MMCC behavior is similar to that of 2-level converters, and the minimum dc-link is given by:

$$v_{d0} = \sqrt{3}\widehat{V}_s. \tag{6.24}$$

Nevertheless, in the region where n_l is limited by the sum of capacitor voltages ripple, the relation is not straightforward. By replacing (6.22) in (6.11) and considering $v_{dc,2Y}$ as an independent variable, a 3rd order polynomial equation is obtained, as follows (see Appendix B for more details):

$$dv_{d1}^3 + ev_{d1}^2 + fv_{d1} + g = 0. \tag{6.25}$$

where d, e, f and g are shown below:

$$d = -\frac{N_{2Y} - F}{2N_{2Y}}, \tag{6.26}$$

$$e = \frac{(N_{2Y} - F)\widehat{I}_g}{4\omega_n C_{2Y}} \sin\left(\frac{\pi}{6} - \varphi\right) + \widehat{V}_s\frac{\sqrt{3}}{2}, \tag{6.27}$$

$$f = -\frac{N_{2Y}\widehat{V}_s\widehat{I}_g}{4\omega_n C_{2Y}}\left[-\frac{1}{2}\sin\left(\frac{\pi}{3} - \varphi\right) + \frac{1}{12}\sin\left(\frac{\pi}{3} + \varphi\right) +\right.$$

$$+\frac{1}{24}\sin\left(\frac{2\pi}{3}-\varphi\right)\Bigg], \tag{6.28}$$

$$g=-\frac{2N_{2Y}\widehat{V}_s^2\widehat{I}_g}{9\omega_n C}\frac{N_{2Y}}{N_{2Y}-F}\cos(\varphi). \tag{6.29}$$

The largest real positive root of (6.25) is the minimum required dc-link voltage v_{d1} at the linear operation range. Therefore, the minimum dc-link voltage for operation in the linear region is given by:

$$v_{d,min}=\min(v_{d0};v_{d1}). \tag{6.30}$$

Figure 75 presents the minimum dc-link voltage required for each operating power factor at rated current, based on the parameters of Tab. 17. As observed, in the capacitive region, the modulator gain is described by the same equations that describes 2-level converters, and the required dc-link voltage depends on the output impedance characteristics and grid voltage. On the other hand, in the inductive operation, the required dc-link is limited by the voltage ripple.

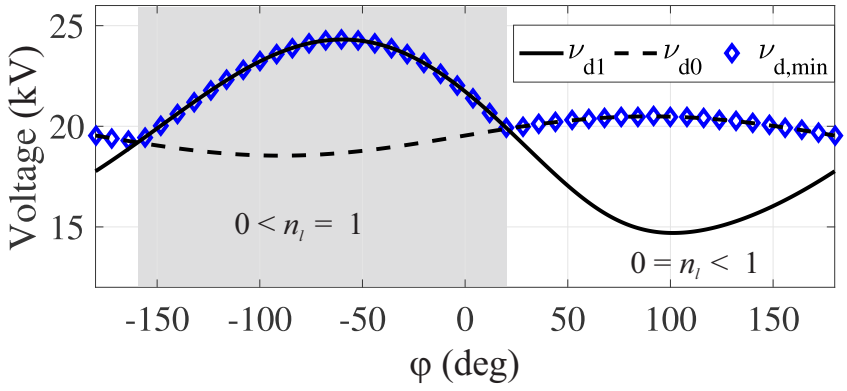

Figure 75 – Minimum required dc-link voltage as function of the operating power factor for operation in the boundary of the linear region.

The modulation index at the boundary of linear region can be computed using (6.22) and (6.30). Accordingly:

$$m_b=\frac{2\hat{V}_s}{v_{d,min}}. \tag{6.31}$$

Figure 76 shows the modulation index as function of the current angle, based on the parameters of Tab. 17. As observed, for the capacitive operation the voltage ripple does not limit the converter operation and $m_b\approx 1.15$ is obtained (the same for 2-level converters). However, for inductive operation, the voltage ripple significantly affects the converter

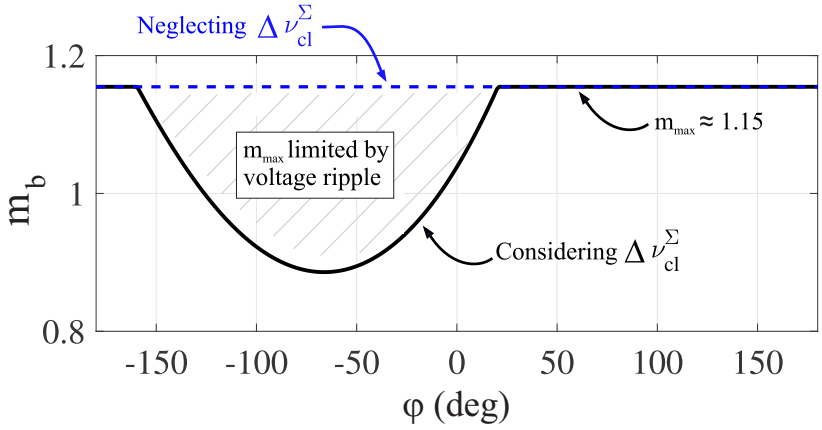

Figure 76 – Modulation index at the linear region boundary. *Remark*: operation at rated current is assumed.

operation. For the considered parameters, the minimum obtained value is $m_b \approx 0.9$, which is a significant reduction in the voltage synthesis capability.

The developed analytical model is validated through simulations of a DSCC-MMCC-based STATCOM implemented in PLECS environment. Five operation conditions are considered, as presented in Tab. 18. The dc-link voltage was slowly reduced in the simulation until reach the limit of linear region. As observed, the maximum error obtained in the dc-link voltage estimation was lower than 3.4 %. In the inductive region, the accuracy of the model is affected by both estimations of reference signal and capacitor voltage ripple. In capacitive region, the accuracy is more affected by reference signal estimation, since the overmodulation is observed in the lower limit (zero voltage). Therefore, the errors obtained in inductive operation are higher.

Table 18 – Minimum dc-link voltage for operation in linear region of the modulator. *Remark*: the parameters shown in Tab. 17 are considered.

Operation Condition	Analytical	Simulation	Relative error
$\widehat{I}_g = 1$ pu; $\varphi = \pi/2$	20.5 kV	20.6 kV	-0.5 %
$\widehat{I}_g = 1$ pu;$\varphi = -\pi/2$	23.7 kV	24.5 kV	-3.4 %
$\widehat{I}_g = 0.5$ pu;$\varphi = \pi/2$	20 kV	20.1 kV	-0.5 %
$\widehat{I}_g = 0.5$ pu;$\varphi = -\pi/2$	21.7 kV	22 kV	-1.4 %
$\widehat{I}_g = 0$ pu	19.5 kV	19.7 kV	-1 %

Figure 77 presents the waveforms for the inserted voltages and sum of the capacitor voltages, considering the minimum dc-link provided by equation (6.30), for inductive Fig. 77 (a) and capacitive Fig. 77 (c) operation. Figures 77 (b) and (d) present the inserted voltages and sum of the capacitor voltages, obtained by the simulation model, for inductive and capacitive operation, respectively. As observed, the inserted voltage is limited by the sum of capacitor voltages for the inductive operation, while for the capacitive operation,

the inserted voltage is limited by the zero voltage. Moreover, the analytical and simulation results are very similar. The small differences observed are due to the contribution of v_z^*.

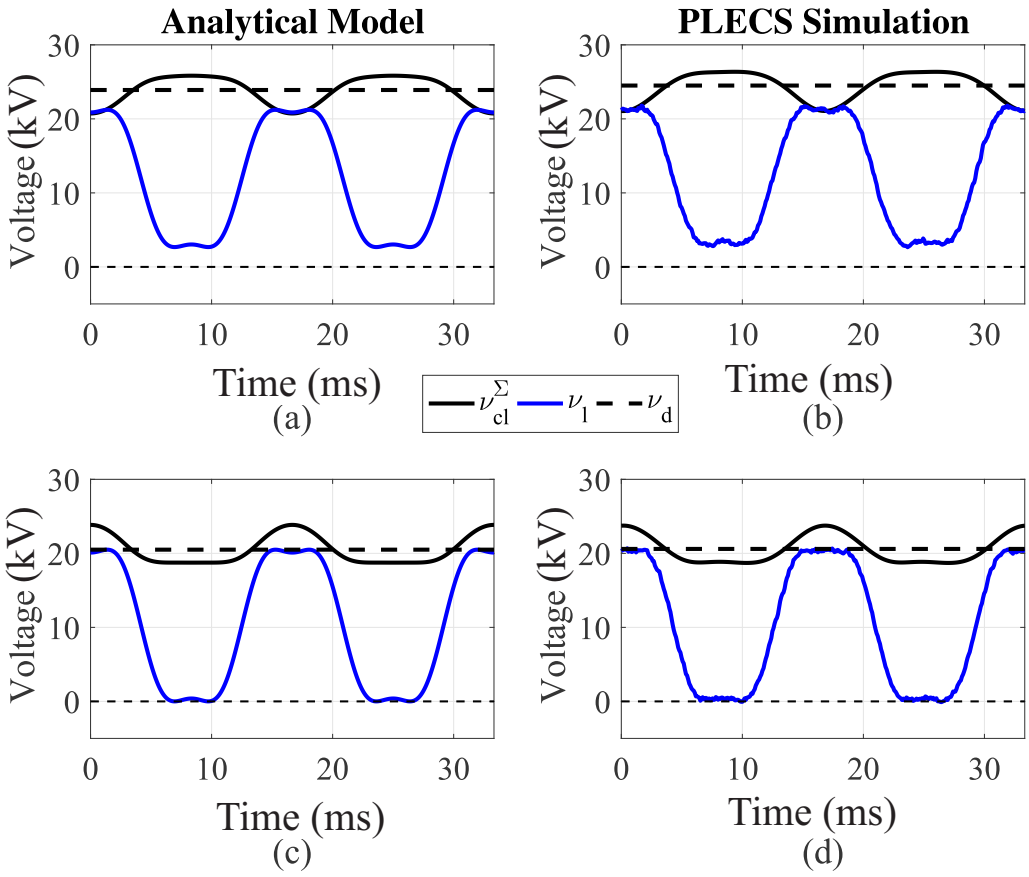

Figure 77 – Inserted voltage and sum of capacitor voltages for a DSCC-MMCC-based STATCOM in the boundary of the modulator linear region: (a) analytical result for pure inductive operation; (b) simulation result for pure inductive operation; (c) analytical result for pure capacitive operation; (d) simulation result for pure capacitive operation.

It must be remarked that the analytical model presented in this section did not consider the amount of voltage necessary to cancel out the second harmonic in circulating currents. This voltage can contribute with up to 5 % in the maximum voltage for reasonable cell capacitance values, according to the reference (Li et al., 2018). Furthermore, the minimum pulse and dead-time effects were not included, which also affect the exact boundary between linear and nonlinear regions (Hava; Kerkman; Lipo, 1998). Therefore, the minimum required dc-link voltage will be higher (e.g., 5 %) than the values computed by relation (6.30).

6.3.3 Sensitivity Analysis

This section analyzes the effect of parameter variation in the minimum required dc-link voltage, which is an important step for a cost-effective design. For a STATCOM, the variations in the grid voltage and in the output impedance are common phenomena, since a power system is a very complex structure with time varying parameters and configurations. The effects of the cell capacitance and current amplitude are also analyzed in this section.

The effect of the grid voltage variation is presented in Fig. 78 (a). Variations in the grid voltage up to 10 % were assumed. As observed, the minimum dc-link voltage increases for all operating power factors. A maximum variation of 8 % is observed. The variation in the grid voltage affects the required voltage for both inductive and capacitive conditions. The inductive region requires the maximum voltage and must be adopted in the converter design.

The effect of the equivalent output impedance is presented in Fig. 78 (b). These variations can be related to the higher arm inductance or variations in the grid impedance. Variations from 5 % to 25 % were considered. As observed, for the capacitive operation, the higher the impedance, the higher the required voltage. Nevertheless, an opposite behavior is observed in the inductive operation. This factor can be justified by relation (6.22). Basically, due to the arm inductance, when the power factor changes, the inductance voltage drop can be displaced by 0 or 180 degrees from the grid voltage. It is important to remark that the inductive region requires the maximum voltage and must be adopted in the converter design for all adopted parameters.

The effect of the cell capacitance is illustrated in Fig. 78 (c). As observed, when the capacitance increases, the required dc-link voltage decreases. This fact is justified by the voltage ripple, which reduces when the capacitance increases. Indeed, if an infinite capacitance value is considered, the required voltage is equal to v_{d0}. The capacitive region is not affected, since the dc-link requirement for this region does not depend on the voltage ripple.

Finally, the effect of the output current amplitude is presented in Fig. 78 (d). As observed, when the current is reduced, the required dc-link decreases. This fact is related to the magnitudes of the voltage ripple and required output voltage, which depend on the output current.

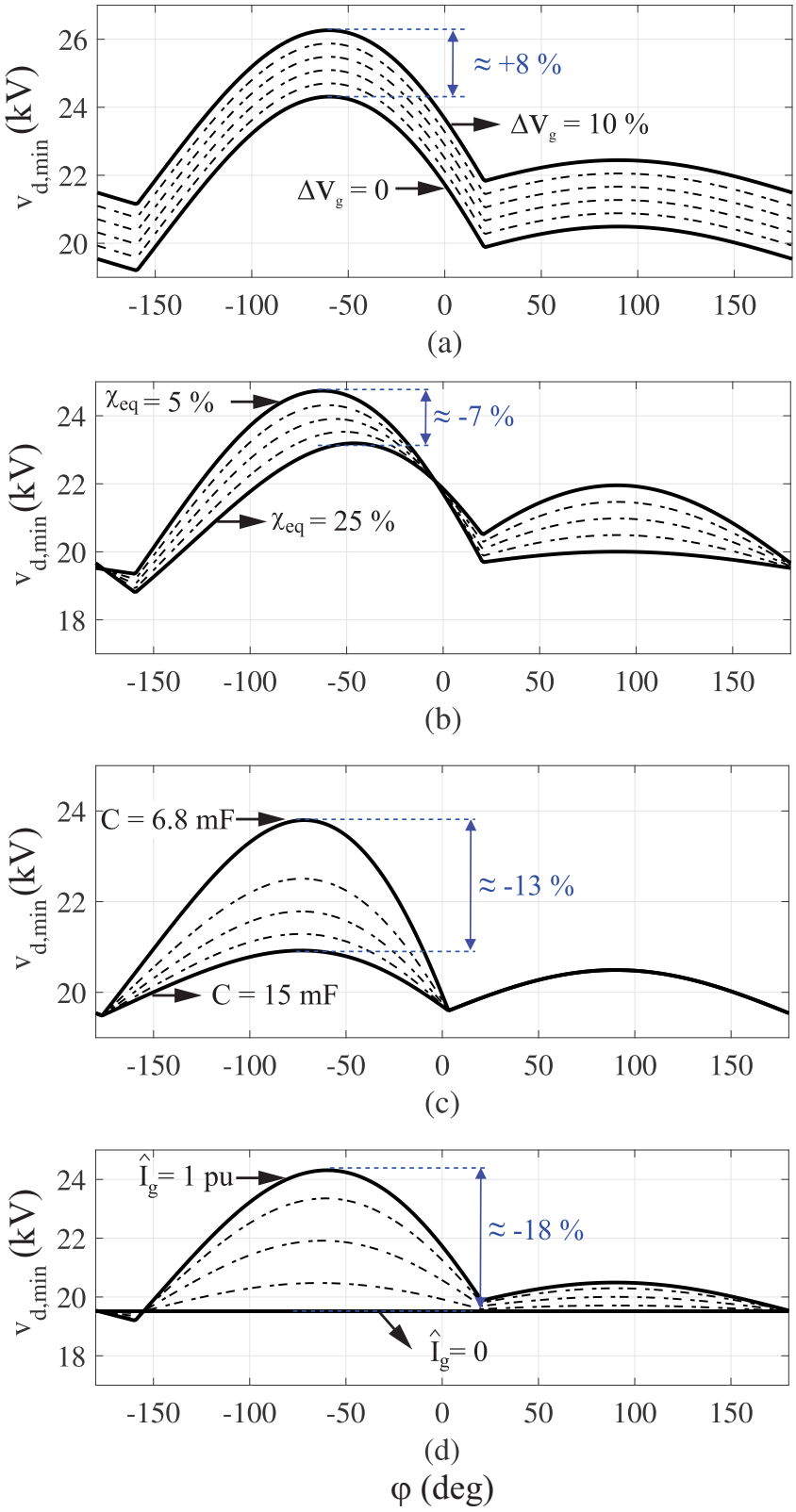

Figure 78 – Sensitivity of the minimum required output voltage as function of the operating power factor:: (a) effect of the grid voltage; (b) effect of the grid impedance; (c) effect of the cell capacitance; (d) effect of the output current amplitude.

At this point, the following conclusions can be stated:

- the non-negligible ripple in the capacitor voltages reduces the linear region of the converter in some operation conditions (mainly in the inductive region);
- for 2-level converters the boundary between linear and non-linear region is usually defined in terms of modulation index. In case of DSCC-MMCC, the modulation index can be interpreted as the minimum sum of capacitor voltages for given grid voltage conditions. Therefore, the value of the dc voltage indicated in Fig. 75 is an alternative interpretation of the boundary between linear and nonlinear region;
- the definition of the boundary in terms of minimum sum of capacitor voltages is interesting from the design point of view. Designing the converter in the boundary conditions will result in the minimum number of cells. The sensitivity of the boundary with respect to the converter and grid parameters was evaluated to indicate what are the acceptable converter design margins.

Since the STATCOM must be able to operate at rated power for both inductive and capacitive conditions, the dc-link voltage is defined by the inductive operation. For the adopted parameters, $v_{dc,2Y} \approx 23.7$ kV at rated inductive reactive power. In order to deal with the variation of the grid voltage and circulating current control, 5 % of voltage margin is included. Therefore, the rated dc-link voltage is $v_{dc,2Y} \approx 25$ kV. Under such conditions, for N = 26, the voltage per cell is $v_c^* \approx 962$ V and 1.7 kV power switches can be employed [2].

6.4 Effect of Failures

Normally, some redundant cells are included in the converter structure to increase the fault tolerance (Chen et al., 2017; Guo et al., 2018). However, redundant cells mean an increase in the converter cost. Therefore, this chapter discusses the operation in the overmodulation region as a fault tolerance strategy. Thereby, when some cells fail, the sum of capacitor voltages in the converter arm reduces and overmodulation is expected.

Figure 79 presents the per unit minimum required dc-link voltage as function of the number of failures. Here, the parameters of Tab. 17 and rated current are considered. The base value is the required dc-link voltage when the converter is in normal operation, i.e., F = 0. As observed, when failures occur, the minimum required dc-link increases,

[2] In this chapter, the 1.7 kV power devices were intentionally employed to obtain a design with a higher number of cells. As explained in chapter 5, inherent redundancy strategies are limited by physical constraints. Therefore, if N_{2Y} is higher, each cell has a lower contribution in the output voltage and the overmodulation is totally explored for a high number of failures.

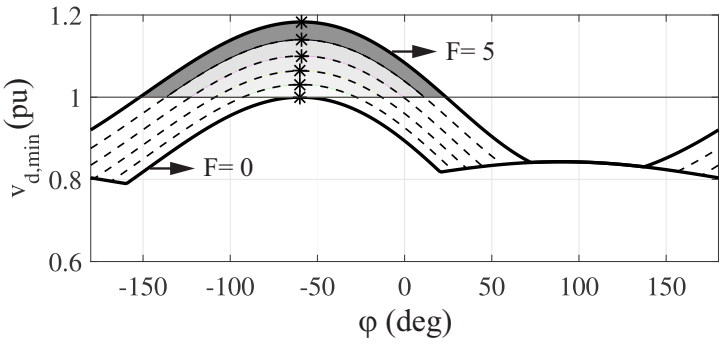

Figure 79 – Effect of failures in the minimum required dc-link voltage.

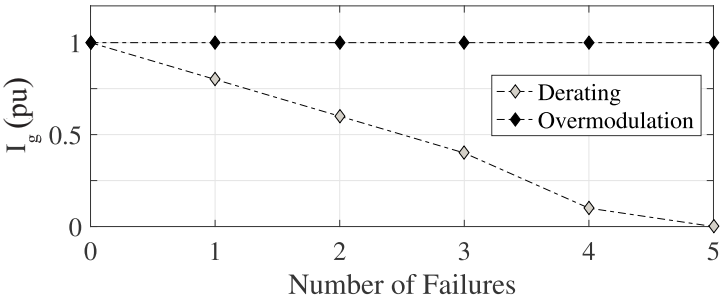

Figure 80 – Comparison of the injected current for derating and overmodulation strategies.

because there is a smaller number of cells available. Therefore, the voltage of each cell must be increased to guarantee the operation in the linear region.

Nevertheless, a cost-effective design will not consider large margins to increase the capacitor voltages. Therefore, when failures occur, the converter will overmodulate. The hatched areas in Fig. 79 indicate the power factors where the converter operates in the overmodulation. Considering the operation as STATCOM, this phenomenon occurs only for inductive operation.

Figure 80 compares the per unit current injected in the grid when the overmodulation and the derating strategy mentioned in Section 6.1 are employed. After 3 failures, the converter controlled in derating mode cannot inject 50 % of the initial power. This reduction will limit the capacity of the STATCOM to provide services to the utility. On the other hand, the operation in the overmodulation region can, theoretically, ride through faults without resulting in lost of power capability.

6.5 Results

In order to show the operation of a DSCC-MMCC STATCOM in the overmodulation region, simulations were implemented in the PLECS environment. Initially, the converter is connected to the grid without any power transfer. At the time 0.1 seconds, the reactive power increases in ramp up to the rated value. When the converter reaches

steady-state, five consecutive failures are simulated to exemplify the converter operation in the overmodulation region.

Figure 81 (a) illustrates the instantaneous active and reactive power delivered to the grid. As observed, even after the failures, the converter can deliver the rated power to the grid. Figure 81 (b) shows the circulating current dynamics. The average value of the circulating current is zero, since no active power is transferred from the dc-link to the grid. Up to the failure number 4, it can be observed a slightly increased ripple in instantaneous power and circulating current. Nevertheless, when F= 5, the ripple increases significantly, due to the increased low order harmonics synthesized by the converter.

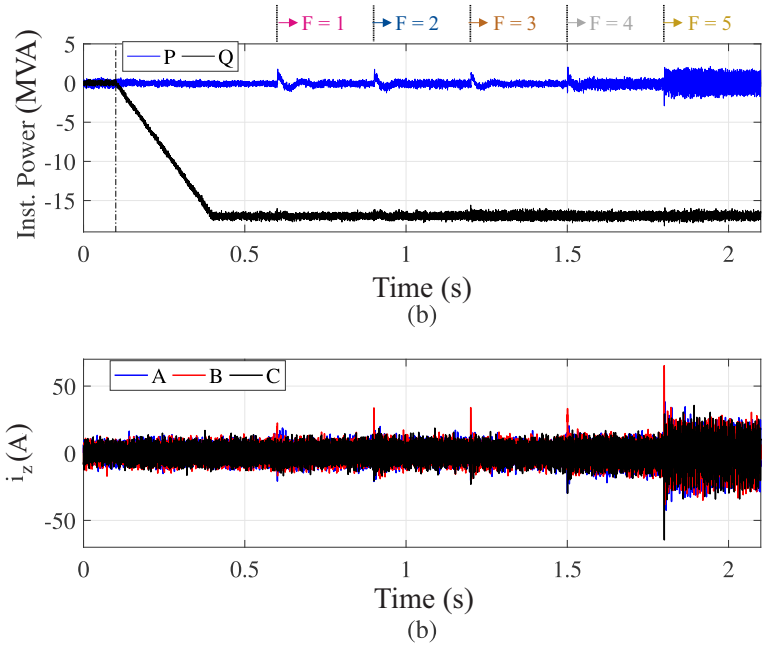

Figure 81 – Effect of the failures in DSCC-MMCC STATCOM operation: (a) instantaneous active and reactive power; (b) circulating currents.

The cell capacitor voltages are illustrated in Fig. 82. Due to symmetry, only phase A is shown. The zoomed views in Fig. 82 (b)-(d) show the average capacitor voltages are well controlled and balanced, even in the overmodulation region. The tolerance band control guarantees that the capacitor voltages are within the upper limit (defined as 110 % of the rated voltage). The voltage of the faulty cells decreases due to the bleeder resistors connected in parallel with the cell capacitors [3].

Figure 83 illustrates the DSCC-MMCC dc-link voltage $v_{dc,2Y}$ after failures in per unit values. As observed, when the failures occur, the voltage is reduced since less converter cells are operating.

[3] In the presented simulation results, small bleeder resistors are used to show the discharge process of faulty cells in a short time period. Small bleeder resistors lead to high steady-state losses. It is important to remark that in practical applications, bleeder resistors are computed to discharge completely the cells after some minutes, which leads to higher resistance values than those used in the simulations.

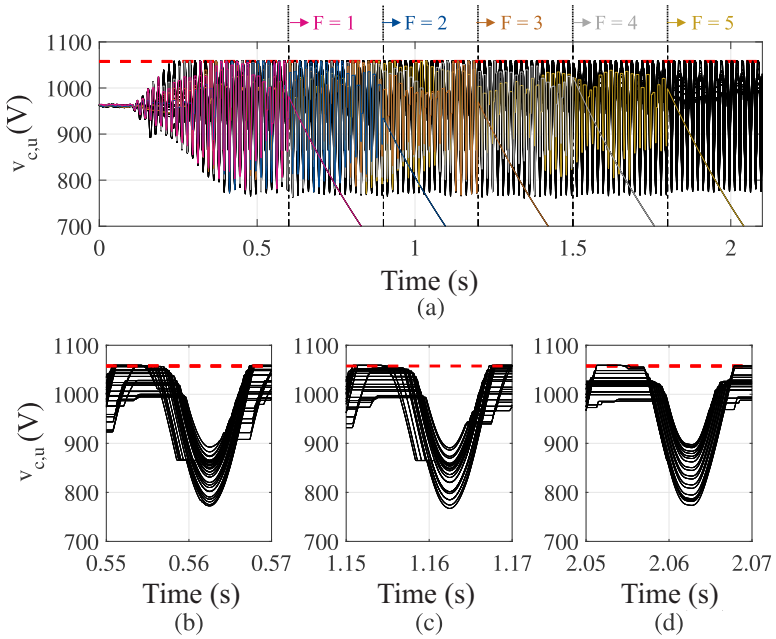

Figure 82 – Effect of the failures in DSCC-MMCC operation: (a) capacitor voltages in upper arm of phase A; (b) zoomed view for F = 0; (c) zoomed view for F = 2; (d) zoomed view for F = 5.

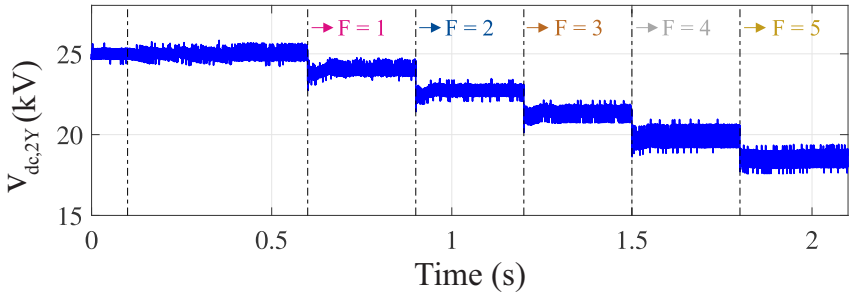

Figure 83 – Effect of the failures in DSCC-MMCC operation: dc-link voltage.

The line-to-line voltages and the converter output currents are shown in Figs. 84 and 85, respectively. As observed, the converter can deliver rated current to the grid. At normal conditions, the waveforms are almost sinusoidal, since the converter presents 53 levels ($2N_{2Y}+1$) in the output voltage. Figure 86 presents the total harmonic distortion of line-to-line voltage and output current. As observed, for the first failures (beginning of the overmodulation region), the harmonic content increases slightly. This can be also noted in the waveforms presented in Figs. 84 (c) and 85 (c). Nevertheless, when F = 5, the output current THD increases fast and exceeds 6 %. This value exceed the 5% recommended by the IEEE.

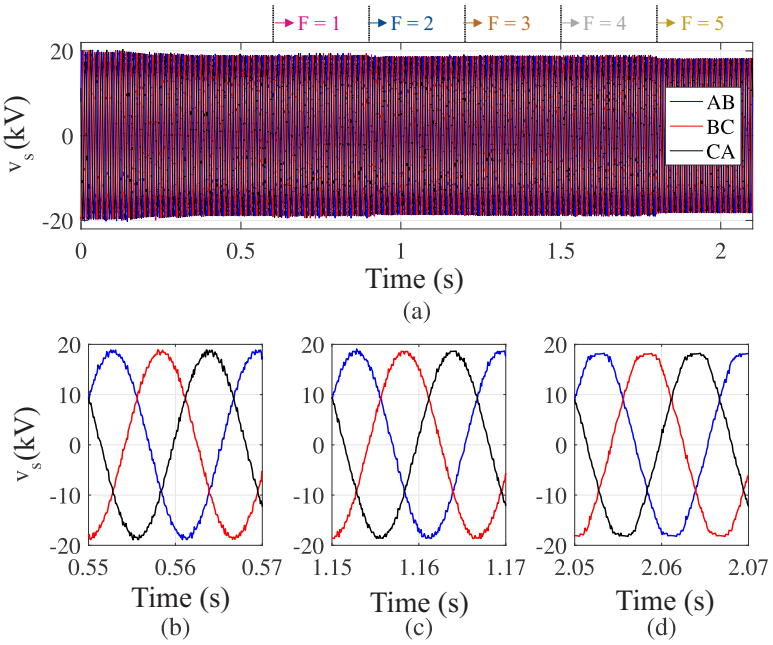

Figure 84 – Effect of the failures in the DSCC-MMCC operation: (a) converter line-to-line voltage; (b) zoomed view for F = 0; (c) zoomed view for F = 2; (d) zoomed view for F = 5.

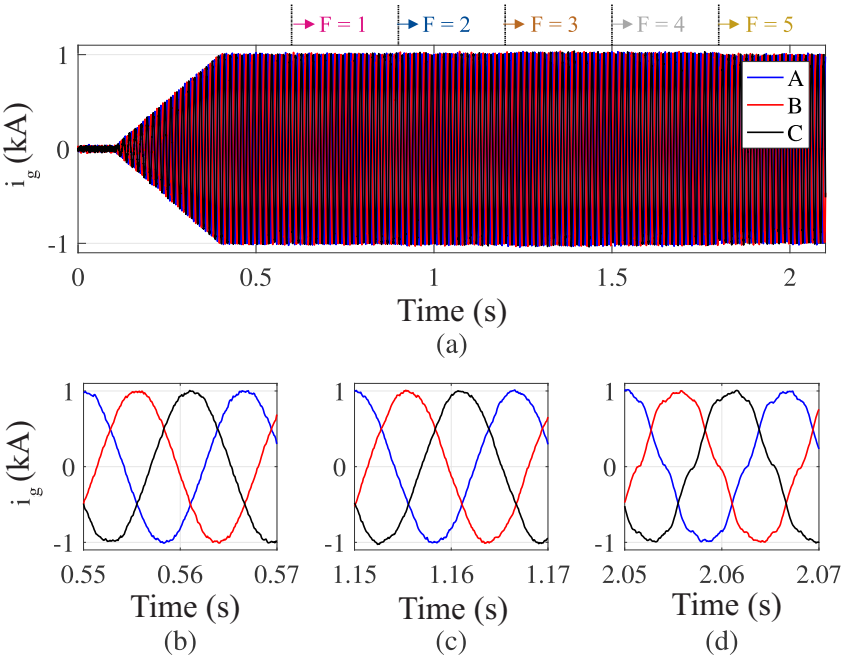

Figure 85 – Effect of the failures in the DSCC-MMCC operation: (a) grid current; (b) zoomed view for F = 0; (c) zoomed view for F = 2; (d) zoomed view for F = 5.

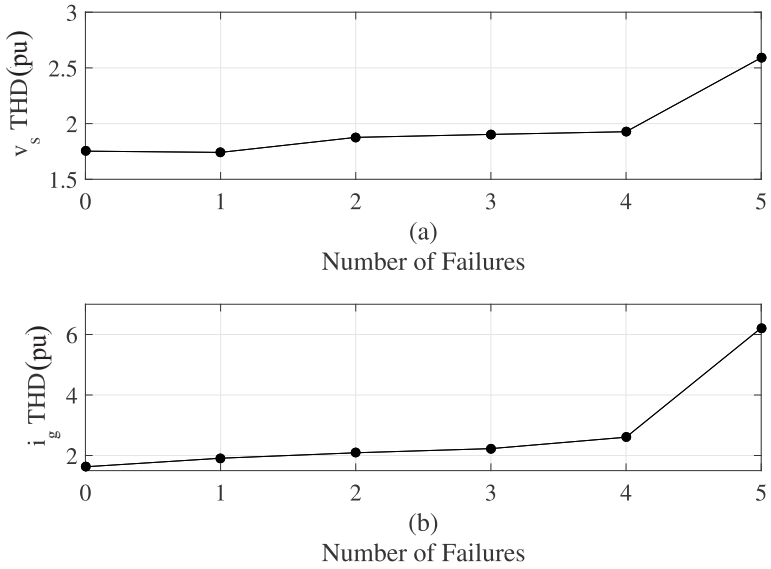

Figure 86 – Total harmonic distortion (THD) as function of the number of failures: (a) line-to-line voltage; (b) grid current.

The behavior of the output THD can be justified by the number of inserted cells, which are presented in Fig. 87. When the STATCOM operates properly (F = 0), the insertion index varies in a staircase waveform, as illustrated in Fig. 87 (a). When failures occur, the insertion index saturates in the upper limit (limited by the capacitor voltage ripples), as shown in Fig. 87 (b). This effect slightly increases the THD when more failures occur. Finally, when the number of failures increases even more, the insertion indexes are saturated in the upper and lower limits. Therefore, the output THD increases significantly in this region.

6.6 Conclusions

This chapter discussed the inherent redundancy of DSCC-MMCC in the overmodulation region. Initially, analytical expressions for the boundary of the converter linear region were developed to define the minimum required dc-link voltage. Since the ripple voltages in DSCC-MMCC are not negligible, the boundary between linear and overmodulation regions is strongly dependent on the cell capacitance.

Sensitivity analyses were implemented to show the effects of the grid voltage variations, different output impedances, power factors and injected currents. The dc-link voltage value was selected based on these analyses. Then, the effect of failures were evaluated.

The results indicated that the operation in overmodulation region has a significant inherent redundancy. For a DSCC-MMCC-based STATCOM with 26 cells per arm, the

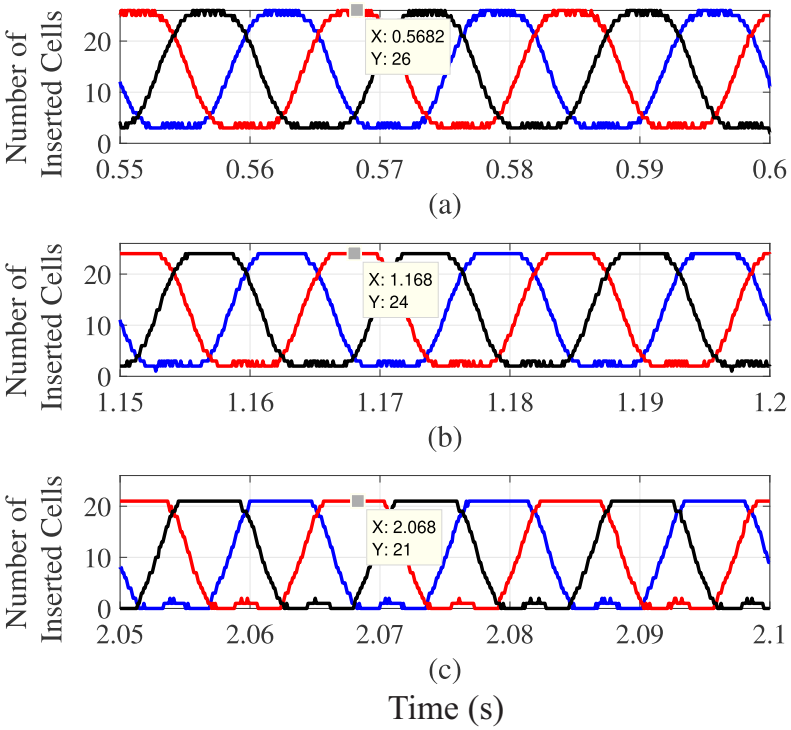

Figure 87 – Insertion number in steady-state for the lower arm: (a) F = 0; (b) F = 2; (c) F = 5.

converter can ride through 4 failures without significantly increasing the output THD or applying some derating strategy in the converter. Furthermore, the fault tolerance was reached without increase the converter cost.

The next chapter draws the conclusions and future developments of this Ph.D dissertation.

7 Summary and Research Perspectives

Modular Multilevel Cascaded Converter-based STATCOMs have important challenges related to design, control and reliability, which directly affect the system overall cost. Previous chapters explored the control, design and fault-tolerant strategies for MMCC-based STATCOM systems. This chapter summarizes the main findings of this Ph.D dissertation and the possible future developments.

7.1 Conclusions

The present Ph.D dissertation have discussed important issues of the modular multilevel cascaded converters, mainly focused in STATCOM application. The conclusions can be divided into three categories: benchmarking of MMCC topologies; reliability-oriented design for DSCC-MMCC; and fault-tolerant strategies.

7.1.1 Benchmarking of MMCC Topologies (Chapters 2 and 3)

1. DSCC-MMCC and SDBC-MMCC topologies are the most suitable for STATCOM application when negative sequence current compensation is necessary.

2. If zero sequence injection is employed in DSCC-MMCC, both SDBC-MMCC and DSCC-MMCC require the same number of cells.

3. The energy storage requirement for the SDBC-MMCC topology is approximately half of the DSCC-MMC. This situation happens because DSCC-MMCC presents energy storage variations at the line frequency and second harmonic while SDBC-MMCC presents only energy storage variations at the second harmonic. This energy storage requirements were validated through simulation models.

4. The current rating of SDBC-MMCC topology is 54 % higher than DSCC-MMCC when negative sequence compensation is taken into account. This higher current rating directly affects the costs, becoming SDBC-MMCC topology more expensive.

5. SDBC-MMCC is more sensible to unbalanced voltage conditions, since this topology presents a singularity when the voltage unbalance factor is unitary.

7.1.2 Reliability-Oriented Design for DSCC-MMCC (Chapter 4)

1. The relation between the power module current rating and unreliability is not straightforward since the mission profile plays an important role in the life consumption of the power devices.

2. The relation between the energy losses and unreliability is not straightforward, due to the nonlinear characteristics of the components power losses.

3. When the rated blocking voltage of the power modules increases, the energy losses increase. This fact can lead to higher life consumption and unreliability. On the other hand, when devices with lower rated blocking voltage are employed, the number of cells increases. Conversely, the higher the number of components, the higher the converter unreliability. Therefore, the selection of the most suitable voltage class depends on the mission profile and converter rated power.

4. The $U_x - cost$ map was introduced as a tool to compare different designs with respect to the unreliability requirement and cost. The methodology can be adapted to different cost evaluation models and reliability models. The proposed methodology indicates 3.3 kV as the most suitable voltage class for a 13.8 kV/17 MVA DSCC-MMCC-based STATCOM.

7.1.3 Fault-Tolerant Strategies for DSCC-MMCC (Chapters 5 and 6)

1. Redundancy strategies based on additional cells increase the control complexity as well the energy losses. Nevertheless, the dynamic performance is improved during failures. Redundancy strategies based on spare cells present the worst dynamic performance due to the charging process. However, this strategy presents lower power losses in steady-state.

2. Inherent redundancy strategies explore some inherent characteristics of the converter to reach fault tolerance. For standard redundancy, the redundancy factor is limited by maximum absolute cell voltage. For the operation in overmodulation region, the redundancy factor is limited by the maximum output voltage which can be reached. These approaches are suitable when the converter initial cost is prioritized.

3. The boundary between linear and non-linear region for DSCC-MMCC is not straightforward due to the non negligible ripple in the cell capacitor voltages. The proposed analytical model can predict the boundary with errors lower than 4 % and can be used to obtain a cost-effective design for DSCC-MMCC-based STATCOM.

4. The inductive operation of the DSCC-MMCC-based STATCOM will define the minimum required dc-link voltage. Therefore, after failures, the overmodulation will be observed only in inductive region.

7.2 Research Perspectives

Although many aspects were studied and documented in the present Ph.D dissertation, there are still a lot of improvements which can be implemented. From the author point of view, the following topics can be approached in further works:

- Improvement of the MMCC reliability model. The constant failure rate region can be included. Additionally, the effect of redundancy strategy and the computation of the correct redundancy factor can be approached;
- Computation of the maximum redundancy factor in overmodulation region for DSCC-MMCC STATCOM;
- Experimental validation of the proposed analytical model for the boundaries of linear region. The extension of this model for other MMCC family members can also be approached;
- Integration of battery energy storage systems in MMCC-based STATCOMs. Such kind of systems can provide both voltage and frequency regulation, and black start capability;
- Discussion of the multifunctional operation for MMCC-based STATCOMs: Frequency regulation, harmonic compensation, etc;
- Development of high performance simulation models for grid integrations studies of MMCC-based STATCOMs.

As observed, the possibilities of future work are many. The author really expects this research project does not stop in the present Ph.D dissertation.

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Appendix

APPENDIX A – Controllers Gains

A.1 SDBC-MMCC Topology

Table 19 – Controller gains for SDBC-MMCC topology.

Parameter	Symbol	Value	unit
Sampling frequency	f_s	7140	Hz
Proportional gain of average control	$k_{p,avg}$	8.8	Ω^{-1}
Integral gain of average control	$k_{i,avg}$	151	$(\Omega\cdot$ s$)^{-1}$
Proportional gain of cluster control	$k_{p,cl}$	3	Ω^{-1}
Integral gain of cluster control	$k_{i,cl}$	30	$(\Omega\cdot$ s$)^{-1}$
Proportional gain of grid current control	$k_{p,g}$	2.6	Ω
Resonant gain of grid current control	$k_{r,g}$	1000	Ω
Proportional gain of circulating current control	$k_{p,c}$	13.7	Ω
Proportional gain of individual balancing control	$k_{p,c}$	$5 \cdot 10^{-4}$	Dimensionless
Moving average filter frequency	f_{ma}	120	Hz

A.2 DSCC-MMCC Topology

Table 20 – Controller gains for DSCC-MMCC topology.

Parameter	Symbol	Value	unit
Sampling frequency	f_s	7140	Hz
Proportional gain of average control	$k_{p,avg}$	8.1	$(\Omega)^{-1}$
Integral gain of average control	$k_{i,avg}$	151	$(\Omega\cdot$ s$)^{-1}$
Proportional gain of grid current control	$k_{p,g}$	5.3	Ω
Resonant gain of grid current control	$k_{r,g}$	1000	$\Omega\cdot$s
Proportional gain of circulating current control	$k_{p,z}$	2.25	Ω
Resonant gain of circulating current control	$k_{r,z}$	1000	$\Omega\cdot$s
Circulating current LPF cut-off frequency	ω_c	8	Hz
Proportional gain of individual balancing control	k_b	$4 \cdot 10^{-4}$	Dimensionless
Moving average filter frequency	f_{ma}	120	Hz

APPENDIX B – Mathematical Developments - Chapter 6

B.1 Derivation of (6.16)

In linear region the insertion index must be higher than zero. From (6.11), it is possible to write:

$$0 < \frac{N_{2Y}-F}{N_{2Y}}\frac{v_{dc,2Y}}{2} + \overbrace{\widehat{V}_s\cos(\omega_n t) - \frac{1}{6}\widehat{V}_s\cos(3\omega_n t)}^{v_s^*}. \tag{B.1}$$

The peak of the reference voltage v_s^* is obtained by doing $\omega_n t = \pi/6$ (Sharifabadi et al., 2016). Replacing $\omega_n t = \pi/6$ in (B.1) leads to:

$$0 < \frac{N_{2Y}-F}{N_{2Y}}\frac{v_{dc,2Y}}{2} - \widehat{V}_s\frac{\sqrt{3}}{2}. \tag{B.2}$$

Solving (B.2) to $\widehat{V}_s$:

$$\widehat{V}_s < \frac{N_{2Y}-F}{N_{2Y}}\frac{v_{dc,2Y}}{\sqrt{3}}. \tag{B.3}$$

This solution is denoted by $\widehat{V}_{s0}$.

B.2 Derivation of (6.17) and (6.25)

In the linear region, the insertion index must be lower than 1. The maximum insertion index is expected when the reference voltage is maximum, which means $\omega_n t = \pi/6$ (Sharifabadi et al., 2016). Substituting (6.12) in (6.11) yields:

$$n_l = \frac{\frac{N_{2Y}-F}{N_{2Y}}\frac{v_{dc,2Y}}{2} + \widehat{V}_s\cos(\omega_n t) - \frac{1}{6}\widehat{V}_s\cos(3\omega_n t)}{v_{dc,2Y}\left(\frac{N_{2Y}-F}{N_{2Y}}\right) + \frac{N_{2Y}}{2C_{2Y}v_{dc,2Y}}(\Delta W_\Sigma - \Delta W_\Delta)} < 1. \tag{B.4}$$

Substituting (6.13) and (6.14) in (B.4) and replacing $\omega_n t = \pi/6$ yields:

$$\frac{N_{2Y}-F}{N_{2Y}}\frac{v_{dc,2Y}}{2} + \widehat{V}_s\frac{\sqrt{3}}{2} < \frac{N_{2Y}-F}{N_{2Y}}v_{dc,2Y} + \frac{N_{2Y}\widehat{I}_g}{4\omega_n C_{2Y}}[f_1(\varphi)+f_2(\varphi)], \tag{B.5}$$

where

$$f_1(\varphi) = -\frac{\widehat{V}_s}{2v_{dc,2Y}} \sin\left(\frac{\pi}{3} - \varphi\right) + \frac{\widehat{V}_s}{12v_{dc,2Y}} \sin\left(\frac{\pi}{3} + \varphi\right) + \frac{\widehat{V}_s}{24v_{dc,2Y}} \sin\left(\frac{2\pi}{3} - \varphi\right), \tag{B.6}$$

$$f_2(\varphi) = -\frac{N_{2Y} - F}{N_{2Y}} \sin\left(\frac{\pi}{6} - \varphi\right) + \frac{8}{9} \frac{N_{2Y}}{N_{2Y} - F} \frac{\widehat{V}_s^2}{v_{dc,2Y}^2} \cos(\varphi). \tag{B.7}$$

Relation (6.17) is obtained solving (B.5) to $\widehat{V}_s$. On the other hand, relation (6.25) is obtained solving (B.5) to $v_{dc,2Y}$.

Biography

Allan Fagner Cupertino was born in Visconde do Rio Branco - MG, Brazil in 1992. He received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV) in 2013 and the M.S. degree in Electrical Engineering from the Federal University of Minas Gerais (UFMG) in 2015. Since 2014, he has been with the Materials Engineering Department at the Federal Center of Technological Education of Minas Gerais (CEFET), teaching in the area of electric machines. Currently, he conducts researches in the Gerência de Especialistas em Eletrônica de Potência (GESEP), where he is responsible for the MMC research group since 2016. His main research interests include renewable power generation systems, multifunctional inverters, modular multilevel cascaded converters and reliability of power electronic converters.

Prof. Cupertino was a recipient of the President Bernardes Silver Medal in 2013. He is member of IEEE Power Energy Society, IEEE Power Electronics Society and Brazilian Power Electronics Society (SOBRAEP).

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