

UNIVERSIDADE FEDERAL DE MINAS GERAIS

Escola de Engenharia

Programa de Pós-Graduação em Engenharia Elétrica

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**MODELING, DESIGN AND PERFORMANCE
EVALUATION OF BATTERY ENERGY STORAGE
SYSTEMS BASED ON MODULAR MULTILEVEL
CONVERTER**

Belo Horizonte

2022

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Modeling, Design and Performance Evaluation of Battery Energy Storage Systems based on Modular Multilevel Converter

Tese de doutorado submetida à banca examinadora designada pelo Colegiado do Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Minas Gerais, como parte dos requisitos necessários à obtenção do grau de Doutor em Engenharia Elétrica.

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Belo Horizonte, MG

2022

P659m

Pinto, Jonathan Hunder Dutra Gherard.

Modeling design and performance evaluation of battery energy storage systems based on modular multilevel converter [recurso eletrônico] / Jonathan Hunder Dutra Gherard Pinto. - 2022.

1 recurso online (149 f. : il., color.) : pdf.

Orientador: Seleme Isaac Seleme Júnior.

Coorientador: Allan Fagner Cupertino.

Coorientador: Heverton Augusto Pereira.

Tese (doutorado) - Universidade Federal de Minas Gerais, Escola de Engenharia.

Bibliografia: f. 141-149.

Exigências do sistema: Adobe Acrobat Reader.

1. Engenharia elétrica - Teses. 2. Baterias – Teses.
I. Seleme Júnior, Seleme Isaac. II. Cupertino, Allan Fagner. III. Pereira, Heverton Augusto. IV. Universidade Federal de Minas Gerais. Escola de Engenharia. V. Título.

CDU: 621.3(043)



UNIVERSIDADE FEDERAL DE MINAS GERAIS
ESCOLA DE ENGENHARIA
COLEGIADO DO CURSO DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA

FOLHA DE APROVAÇÃO

"Modeling, Design And Performance Evaluation Of Battery Energy Storage Systems Based On Modular Multilevel Converter"

JONATHAN HUNDER DUTRA GHERARD PINTO

Tese de Doutorado defendida e aprovada, no dia 6 de junho de 2022, pela Banca Examinadora designada pelo Colegiado do Programa de Pós-Graduação Engenharia Elétrica da Universidade Federal de Minas Gerais constituída pelos seguintes professores:

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Belo Horizonte, 06 de junho de 2022.



Documento assinado eletronicamente por **Seleme Isaac Seleme Junior, Membro de comissão**, em 06/06/2022, às 18:45, conforme horário oficial de Brasília, com fundamento no art. 5º do [Decreto nº 10.543, de 13 de novembro de 2020](#).



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*À minha mãe,
À minha família,
À minha esposa, Leticia,
Aos meus mentores e amigos.*

Agradecimentos

Agradeço a Deus por me iluminar e permitir a conclusão de mais uma importante etapa da minha vida. À minha mãe, por toda dedicação e apoio, e pelo incentivo constante para a realização dos meus objetivos. Obrigado, mãe! Você é um exemplo! Esta conquista é para você. Aos meus irmãos Iá, Érika, Patrão e Melas, obrigado por sempre estarem ao meu lado e cuidando de mim. Vocês são as minhas referências!

Aos poucos a família foi crescendo e vocês são essenciais para mim. Obrigado, Danilo pela amizade. Nat e Tets, obrigado pelo carinho e por me acompanharem ao longo desta trajetória. Amo vocês! Marta e Márcio, obrigado por tudo que fazem por mim. Agradeço também aos meus sobrinhos: Arthur, Maria Teresa, Ana Laura e Rafa. Vocês alegam cada vez mais nossa família!

À Letícia, obrigado meu amor por me apoiar e sempre estar ao meu lado. Essa conquista é nossa. Te amo muito! Você é o melhor presente que o destino me deu!

Agradeço ao Professor Seleme, pelos ensinamentos e por aceitar meu convite para ser meu Orientador. Professor, obrigado pela disponibilidade e compreensão. Você é muito importante na minha formação! Ao Professor Heverton, pelas orientações e por sempre me ajudar no que é preciso. Obrigado, por me proporcionar fazer parte de uma equipe tão qualificada! Ao Professor Allan, meus agradecimentos pela amizade e por todo apoio ao longo do trabalho. Por maior a complexidade que existisse no trabalho sempre encontrava uma solução ou uma palavra de conforto. Obrigado por tudo, você é um exemplo.

Agradeço e dedico este trabalho a todos os membros do GESEP. Estou muito feliz por fazer parte de um grupo de profissionais tão competente! Independente da distância, todos sempre estiveram dispostos a contribuir com este trabalho. Em especial agradeço ao William pela amizade e ensinamentos que muito contribuíram para a realização deste trabalho. Muito obrigado, William! Além disso, quero agradecer aos meus companheiros de BH, Renata e João Víctor pelo companheirismo e amizade.

Por fim, gostaria de agradecer à UFMG, ao CEFET-MG e a FAPEMIG pelo apoio financeiro.

Resumo

O sistema de armazenamento de energia de bateria baseado em conversor modular multinível (*MMC-based BESS*) pode desempenhar um papel importante quando aplicado a sistemas de energia, por exemplo, estabilizando e melhorando a qualidade da energia. A associação das baterias com o MMC pode ocorrer de duas formas: centralizada ou distribuída. Na configuração centralizada, o banco de baterias é conectado no barramento cc do MMC. Já na configuração distribuída, o banco de baterias é conectado em cada submódulo (SM) do MMC. Neste trabalho, o foco é na configuração distribuída. Dentro da configuração, distribuída o banco de baterias pode ser associado ao SM de duas formas: estágio único e dois estágios. Para a abordagem de único estágio, as baterias são conectadas diretamente aos SM do MMC. Já na abordagem de dois estágios, o conversor cc-cc realiza a interface entre as baterias e o MMC. Essas duas configurações já estão consolidadas na literatura. No entanto, existe uma lacuna em termos de projeto, otimização de custos e estratégia de controle dos sistemas MMC-based BESS. A metodologia é baseada em determinar um valor ideal de tensão para os SM para que em um determinado intervalo de tempo, os custos do MMC-based BESS sejam mínimos. Além disso, de forma a diminuir o sobredimensionamento de energia disponível em um projeto, este trabalho propõe duas soluções: a padrão (do inglês, *standard*) que são os projetos realizados com banco de baterias comerciais e as customizadas (do inglês, *customized*) que são os projetos com banco de baterias formado por células. O estudo de caso proposto analisa um sistema de 10.9 MVA/5.76 MWh conectado à uma rede de 13.8 kV, que fornece serviços auxiliares, principalmente nos horários de ponta. Diferentes tensões de bloqueio nominais são assumidas para os dispositivos semicondutores. Além disso, diferentes estados de carga máximos e mínimos permitidos (SOC) são adotados no projeto do conversor. A metodologia proposta também pode ser usada para encontrar a combinação ótima dos números de bateria e do transistor bipolar de porta isolada (IGBT) com base em um determinado conjunto inicial. Desta forma, esta tese de doutorado visa preencher esta lacuna, fornecendo as seguintes contribuições: (i) comparação de topologias mais adequadas para a associação de baterias; (ii) proposta de uma metodologia para estimar as perdas de energia do sistema; (iii) análise da vida útil das baterias (iv) análise comparativa dos custos para as duas abordagens e (v) metodologia para realizar o controle e os ajustes nos ganhos dos controladores para MMC-based BESS de um e dois estágios. Para o projeto em estudo os resultados apontaram a melhor opção de um estágio composto de baterias na solução customizada.

Palavras-chaves: Baterias; Conversor Modular Multinível; Otimização de custos; MMC-based BESS; Tensão de referência do submódulo; Vida útil das baterias.

Abstract

Modular Multilevel Converter-based Battery Energy Storage System (MMC-based BESS) can play an important role when applied to power systems, for example, stabilizing and improving power quality. The association of batteries with the MMC can occur in two ways: centralized or distributed. In the centralized configuration, the battery bank is connected to the MMC dc-link. In the distributed configuration, the battery bank is connected to each submodule (SM) of the MMC. In this work, the focus is on the distributed configuration. Within the distributed configuration, the battery bank can be associated with the SM in two approaches: single-stage and two-stage. For the single-stage approach, the batteries are connected directly to SM of the MMC. For the two-stage approach, the batteries are decoupled from the SM via a dc/dc converter. These two topologies are already consolidated in the literature. However, there is a gap in terms of design, cost optimization and control strategy of MMC-based BESS. The methodology identifies what is the optimum SM voltage reference which minimizes the MMC-based BESS total cost for a given target of operating time. Furthermore, in order to reduce project energy oversizing, this work proposes two solutions: standard, which are projects carried out with a commercial battery bank, and customized, which are projects with a battery bank formed by cells. The case study is based on a 10.9 MVA/5.76 MWh connected to a 13.8 kV power system, which provides ancillary services, especially at peak hours. Different rated blocking voltages are assumed for the semiconductor devices. Moreover, different maximum and minimum allowed state-of-charge (SOC) is adopted in the converter design. The proposed methodology can also be used to find the optimum combination of the battery and insulated-gate bipolar transistor (IGBT) part numbers based on a given initial set. This PhD thesis work aims to fill this gap, providing the following contributions: (i) comparison of configurations more appropriate to the association of batteries; (ii) proposal of a methodology to estimate the power losses of the system; (iii) battery lifetime analysis; (iv) comparative analysis of costs for the two approaches and (v) methodology for tuning the controllers for the MMC-based BESS single-stage and two-stage approach. For the case study, the results showed the best option is the single-stage approach composed of batteries in the customized solution.

Keywords: Battery; Converter Design; Cost Optimization; Lifetime battery; MMC-based BESS; Modular Multilevel Converter; Submodule reference voltage.

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List of Abbreviations and Acronyms

- ABB** Asea Brown Boveri
- BESS** Battery Energy Storage System
- BMS** Battery Management System
- BBO** Big Battery Old
- CAPEX** Capital Expenditure
- Cd** Cadmium
- CPE** Constant-Phase-Element
- DAB** Dual Active-Bridge Converter
- DOD** Depth-of-Discharge
- EIS** Electrochemical Impedance Spectroscopy
- EMS** Energy Management System
- EOL** End-of-Life
- ESS** Energy Storage System
- EU** European Union
- FC** Flying Capacitor
- GVEA** Golden Valley Electric Association
- HB** Half-Bridge Converter
- IGBT** Insulated-Gate Bipolar Transistor
- H₂SO₄** Sulfuric-Acid
- KOH** Potassium Hydroxide
- LiCoO₂** Lithium Cobalate
- LiCoO₄** Lithium Perchlorate
- Li-ion** Lithium-Ion

LiNiO₂ Lithium Nickel Oxide

LiPOF₄ Lithium Iron Phosphate

LiPF₆ Lithium Hexafluorophosphate

MAF Moving Average Filter

MMC Modular Multilevel Converter

M5BAT Modular Multiple Megabit Storage and High-Voltage Multitechnology and Technology

Na Sodium

NaS Sodium Sulphur

Ni Nickel

NiCd Nickel Cadmium

NiFe Nickel-Iron

NiH₂ Nickel-Hydrogen

NiMH Nickel Metal Hydride

Ni(OH)₂ Nickel Hydroxide

NiZn Nickel-Zinc

NPC Neutral Point Clamped

OCV Open Circuit Voltage

OPEX Operational Expenditure

OPEX_L Operational Expenditure-Losses Cost

OPEX_R Operational Expenditure-Replacement Cost

Pb Lead

Pb-acid Lead-Acid

PbC Lead Carbon Batteries

PbO₂ Lead Dioxide

PCS Power Conversion System

PI Proportional-Integral

PLL Phase-Locked Loop

PV Photovoltaic

PR Proportional Resonant

PS-PWM Phase-Shifted Pulse Width Modulation

PSB Polysulfide Bromide

pu Per Unit

RES Renewable Energy Sources

RMS Root Mean Square

SEI Sumitomo Electric Industries

SM Submodule

SOC State-of-Charge

STATCOM Static Synchronous Compensators

SPWM Sinusoidal Pulse Width Modulation

THD Total Harmonic Distortion

UPS Uninterruptible Power Supply

USA United States of America

VRFB Vanadium Redox Battery

WPPs Wind Power Plants

ZnBr Zinc Bromide

List of symbols

C	SM Capacitance
C_n	Battery Capacity
C_r	Discharging Rate
e_a	Error in Phase- a
e_b	Error in Phase- b
e_c	Error in Phase- c
E_B	Total Energy of the Batteries
E_c	Total Energy Losses
E_n	Total Energy Storage Requirement
$E_{n,bat}$	Battery Rack Energy Storage Requirement
E_O	Energy Oversizing
E_R	Energy Requirement
f_c	Switching Frequency of MMC
f_g	Grid Frequency
f_{sw}	Switching Frequency of dc/dc Converter
\hat{I}_g	Peak of Grid Current
ΔI_{bat}	Current Ripple
i_{bat}	Battery Current
$i_{bat,RMS(SS)}$	The Effective Current in the Battery in the Single-Stage Approach
$i_{bat,RMS(TS)}$	The Effective Current in the Battery in the Two-Stage Approach
$i_{c,a}$	Circulating Current of Phase- a
$i_{c,b}$	Circulating Current of Phase- b
$i_{c,c}$	Circulating Current of Phase- c

$i_{c,n}$	Circulating Current of n -Phase
i_{dc}	Dc-link Current
i_g^*	Grid Current Reference
$i_{g,a}$	Grid Current of Phase- a
$i_{g,b}$	Grid Current of Phase- b
$i_{g,c}$	Grid Current of Phase- c
$i_{g,n}$	Grid Current of n -Phase
I_{IGBT}	Power Module Rated Current
$i_{g\alpha\beta}$	Grid Current Stationary Frame
$i_{g\alpha\beta}^*$	Reference Grid Current Stationary Frame
$i_{l,a}$	Lower Arm Current of Phase- a
$i_{l,b}$	Lower Arm Current of Phase- b
$i_{l,c}$	Lower Arm Current of Phase- c
$i_{l,n}$	Lower Arm Current of n -Phase
i_{SM}	SM Current
$i_{u,a}$	Upper Arm Current of Phase- a
$i_{u,b}$	Upper Arm Current of Phase- b
$i_{u,c}$	Upper Arm Current of Phase- c
$i_{u,n}$	Upper Arm Current of n -Phase
$k_{I,L}$	Integral Gain of Leg-Balancing Control
$k_{I,R}$	Integral Gain of the Voltage the dc/dc Control
$k_{I,S}$	Integral Gain of Global SOC Control
$k_{I,W}$	Integral Gain of the Current the dc/dc Control
K_o	Price per kWh
$k_{P,C}$	Proportional Gain of Circulating Current Control
$k_{P,G}$	Proportional Gain of Grid Current Control

$k_{P,L}$	Proportional Gain of Arm-Balancing Control
$k_{P,R}$	Proportional Gain of the Voltage the dc/dc Control
$k_{P,S}$	Proportional Gain of Global SOC Control
$k_{P,W}$	Proportional Gain of the Current the dc/dc Control
$k_{R,C}$	Ressonant Gain of Circulating Current Control
$k_{R,G}$	Ressonant Gain of Grid Current Control
$k_{R,W}$	Ressonant Gain of the Current the dc/dc Control
L_{Arm}	Arm Inductance
L_{dc}	Inductance of dc/dc Converter
L_{dc}	Equivalent Arm Inductance
L_{Grid}	Grid Inductance
m	Modulation Index
N	Number of SM
$N_{energy,bat}$	Number of Batteries Based on Energy Storage Requirement
$n_{l,n}$	Insertion Index Lower Arm
$N_{p,bat}$	Number of Batteries of Parallel Battery Strings
$N_{power,bat}$	Number of Batteries Based on Rated Power Converter
$N_{s,bat}$	Number of Series Battery Strings
$n_{u,n}$	Insertion Index Upper Arm
$P_{Arm,ind}$	Ohmic Losses in the Arm Inductor
$P_{bat,min}$	Minimum Battery Rack Power
P_{cond}	Conduction Losses
$P_{dc,ind}$	Ohmic Losses in the dc/dc Converter Inductor
P_L	Power the Load
$p_{l,n}$	Instantaneous Active Power in Lower Arm of n -Phase
$P_{losses-SM}$	Total Power Losses of SM

P_N	Rated Active Power
P_{pv}	Power Relative to Photovoltaic Solar Production
P_{ref}	Active Power Reference
p_{SM}	Power of SM
P_{sw}	Switching Losses
$p_{u,n}$	Instantaneous Active Power in Upper Arm of n -Phase
Q_n	Reactive Power Reference
Q_{ref}	Rated Reactive Power
R_{Arm}	Arm Inductor Resistance
R_{Grid}	Grid Equivalent Resistance
$SOC_{\Sigma,n}$	Average SOC per n -Phase
SOC_{Σ}^*	SOC Reference in Leg-Balancing
$SOC_{diff,n}$	Difference SOC per n -Phase
SOC_g^*	Reference Average Global SOC
SOC_g	Average Global SOC
$SOC_{l,i}$	SOC for the i - SM in Lower Arm
SOC_{max}	Maximum Allowed SOC
SOC_{min}	Minimum Allowed SOC
S_n	Converter Rated Apparent Power
$SOC_{u,i}$	SOC for the i - SM in Upper Arm
T_j	Temperature of the Semiconductor Devices
$\Delta T_{bat(SS)}$	Temperature Variation in the Batteries in the Single-Stage Approach
$\Delta T_{bat(TS)}$	Temperature Variation in the Batteries in the Two-Stage Approach
ΔV	The Maximum ac Grid Voltage Variation in pu
V_{100FIT}	Blocking Voltage of IGBT
v_{bat}	Battery Rack Voltage

$v_{bat,max}$	Maximum Battery Rack Voltage
$v_{bat,min}$	Minimum Battery Rack Voltage
v_c^Σ	Sum of the Capacitors
$v_{c,n}$	Internal Voltage of n -Phase
v_{dc}	Nominal dc-Link Voltage
$v_{dc,min}$	Minimum dc-link Voltage
\hat{V}_g	Peak of the ac-Grid Voltage
$v_{g,n}$	Grid Voltage of n -Phase
$v_{g\alpha\beta}$	Grid Voltage Stationary Frame
$v_{g\alpha\beta}^*$	Reference Grid Voltage Stationary Frame
$v_{l,a}$	Voltage Upper Arm of Phase- a
$v_{l,b}$	Voltage Upper Arm of Phase- b
$v_{l,c}$	Voltage Upper Arm of Phase- c
$v_{l,n}$	Voltage Upper Arm of n -Phase
V_{ps}^*	Rated Blocking Voltage
\hat{V}_s	Peak of Line-to-Neutral Voltage
v_{SM}^i	The i -th SM Voltage
v_{SM}^*	Reference SM Voltage
$v_{SM,max}^*$	Maximum SM Voltage
$v_{SM,min}^*$	Minimum SM Voltage
$v_{s,n}$	Line-to-Neutral Voltage
$v_{u,a}$	Voltage Upper Arm of Phase- a
$v_{u,b}$	Voltage Upper Arm of Phase- b
$v_{u,c}$	Voltage Upper Arm of Phase- c
$v_{u,n}$	Voltage Upper Arm of n -Phase
W_{conv}	Energy Storage Requirements

x_{Arm}	pu Value of Arm Reactance
x_{pu}	pu Equivalent Output Reactance of the Converter
Y	Number of Operating Years
Z_{h-a}	Heatsink-to-Ambient Thermal Impedance
Z_{j-c}	Junction-to-Case Thermal Impedance
Z_{c-h}	Case-to-Heatsink Thermal Impedance
δ	Phase of the Output Voltage
θ_v	Phase Angle of Each Grid Phase
ω	Angular Frequency
σ	Duty Cycle of dc/dc Converter
ϕ	Grid Current Angle

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1 Introduction

1.1 Energy Storage Technology

Economic and population growth together with technological advances have contributed to the increase in electricity consumption (Babatunde; Munda; Hamam, 2019). Renewable Energy Sources (RES) have been widely used to supply this demand. Photovoltaic (PV) and Wind Power Plants (WPPs) have reached high levels of penetration in several countries. Moreover, the production of electricity using RES has already reached or exceeded demand in some countries. According to (Eurostat, 2021), in 2020, the RES represents 37,5% of the total energy consumed in the European Union (EU). Among EU countries, Sweden (56.4%) and Finland (43.1%) stand out as the largest producers of RES. In addition, WPPs (36%) and hydro (33%) accounted for more than two-thirds of the total electricity generated from RES. The remaining third of the electricity generated was from PV (14%), solid biofuels (8%) and other renewable sources (8%) (Eurostat, 2021; Twidell, 2021; Sadorsky, 2021). However, a part of this renewable energy production is wasted, due to forecasting errors ¹ (Komarnicki; Lombardi; Styczynski, 2017). Therefore, Energy Storage System (ESS) become strategic to store this unused energy. In addition, it cooperates to perform other services for the system, especially at the distribution level.

ESS is a technology that has been used since the beginning of electric power systems (Sigrist; Lobato; Rouco, 2013). In general, this system is used to assist in technical problems and overcosts resulting from the time variation of load and generation. Nowadays, ESS is being used to stabilize the power system or to the development of local power systems based on RES (Komarnicki; Lombardi; Styczynski, 2017). ESS has played two different roles:

1. Time Shifting: Electric energy time-shift is carrying out storage at times when energy is less expensive, and using it at peak times when the price is higher. Consequently, this action can increase efficiency and reduce electricity costs through energy arbitrage (Rivera et al., 2022; Shamim; Subburaj; Bayne, 2019; Argyrou; Christodoulides; Kalogirou, 2018).
2. Ancillary Services: Energy storage can improve stability and reliability of the power grid by forcing: grid frequency control, voltage control, and spinning reserve (Rebours et al., 2007). In addition, as a consequence of the increase in the use of nonlinear loads, the power quality has been compromised. Thus, supply interruptions, voltage

¹ According to Ma et al. (2018), the average error in forecasting renewable energy generation is estimated at approximately 3% per year. In some situations, the actual error may be greater.

sags, and flicker have become more common (Denholm et al., 2010). Under such conditions, ESS are able to provide energy to circumvent these grid supply problems (Rancilio et al., 2020; Shamim; Subburaj; Bayne, 2019; Argyrou; Christodoulides; Kalogirou, 2018).

The energy can be stored in the following ways:

- gravitational potential energy with water reservoirs;
- compressed air;
- electrochemical energy in batteries and flow batteries;
- chemical energy in fuel cells;
- kinetic energy in flywheels;
- magnetic fields in inductors and
- electric fields in capacitors.

According to Argyrou, Christodoulides e Kalogirou (2018) the energy storage technology choice depends on the power and energy ratings, response time, operating cycles, weight, volume, and temperature. Figure 1 shows the categories mentioned above according to the load duration time. Systems that need energy storage to last for hours or days, while those that last for minutes or hours. Finally, short-term ones have storage capacity for seconds or minutes.

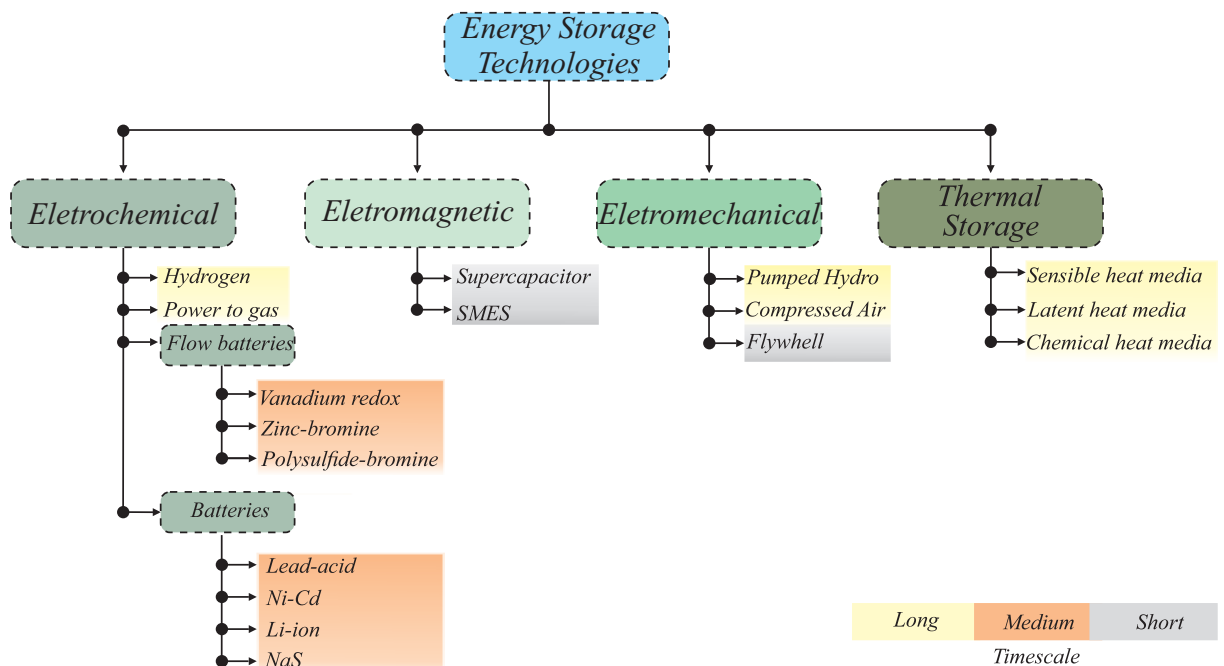


Figure 1 – Energy storage systems technologies. Adapted from (Díaz-González; Sumper; Gomis-Bellmunt, 2016).

The performance of energy storage technologies can be defined through efficiency and energy density. The technology choice is defined according to the service provided

and the time of use. Figure 2 presents the efficiencies and life cycle of energy storage technologies, which are important figures of merit to compare different technologies. According to Figure 2(a), electromechanical and electromagnetic elements show more cycles and higher efficiencies. Traditional and modern battery technologies exhibit good energy efficiency, but they are penalized with reduced lifetime, which makes them a determining factor in the field of renewable energy sources.

Figure 2(b) exhibits Ragone Diagram ² of energy storage technologies. In this graph, power density (W/kg) is compared with energy density (Wh/kg). The higher the energy density, the greater the amount of energy available per unit of mass or volume. Besides that, the lower the power density, the lower the speed of energy transfer per unit of mass or volume. Figure 2(c) presents the costs related to different energy storage technologies. It is important to remark that the selection of a particular technology must be assessed against technical performance and application requirements.

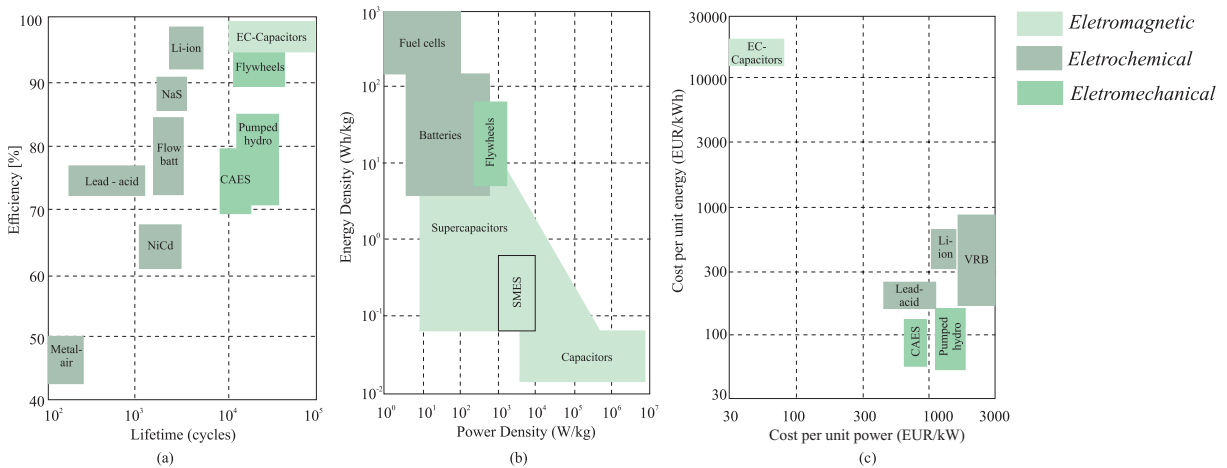


Figure 2 – Benchmarking of energy storage technologies: (a) Efficiency and lifetime; (b) The Ragone chart; (c) Capital costs. Adapted from (Rufer, 2017).

ESS that uses batteries as an energy storage source are called Battery Energy Storage System (BESS). This system is the most widespread for applications in the grid (Gyuk et al., 2005; Joseph; Shahidehpour, 2006; Divya; Østergaard, 2009). According to ??, BESS associated with the electrical grid are increasingly mentioned due to the fact that a strong continuous growth in the deployment of batteries is expected, either as independent arrays or as a distributed system. The use of BESS presents benefits such as flexibility in location for installation, shorter construction time of the facilities, and quick response time to system events. In the electric power market, BESS is gaining more and more space, due to the numerous applications in systems related to generation, transmission, and distribution. In recent years, there has been an increase in BESS facilities worldwide, totaling over 17 GW at the end of 2020 (IEA, 2021).

² Graphical representation used to compare energy storage sources according to energy density and power density (Bagotsky; Skundin; Volkovich, 2015).

Figure 3 shows the schematic diagram of a BESS, which is formed by a Energy Management System (EMS), battery rack and Power Conversion System (PCS). EMS has the function of monitoring the batteries through sensors, and ensure the electrical and thermal characteristics. In addition, it monitors all operations through a supervisory system.

The battery has a basic energy storage unit, denominated cell. The series and/or parallel association of the cells constitutes a module. The Battery Management System (BMS) is responsible to monitor the electrical and thermal characteristics of the module, for example, charge level, current, voltage, and temperature. In order to maintain the system protection, all these elements mentioned above are installed in a junction box. The association of several units forms a rack.

Another important component in an energy storage system is the PCS. This is the intermediate device between the battery rack and the electrical grid. Usually, PCS is installed in larger environments, such as containers. In general, the battery technologies used in BESS systems to provide energy support are those which show deep discharge feature (Reddy, 2011). The technologies currently in use are: Lead-Acid (Pb-acid), Sodium Sulphur (NaS), Flow Batteries, Nickel Cadmium (NiCd) and Lithium-Ion (Li-ion) (Divya; Østergaard, 2009). In the following section, a brief summary is carried out among the types of batteries mentioned.

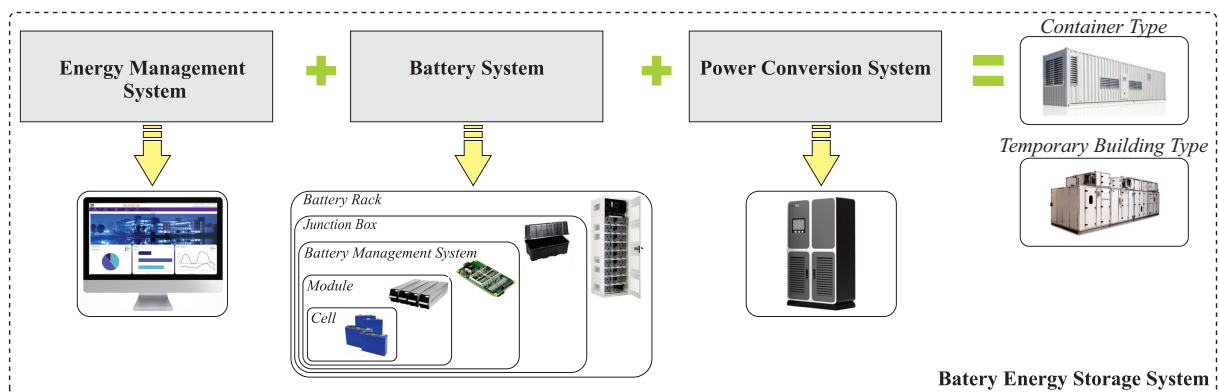


Figure 3 – Schematic of a BESS.

1.2 Battery Technology Overview

The battery converts electrical energy into chemical energy during the charging process and provides electrical energy during the discharging process, as shown in Figure 4. This process occurs through oxidation-reduction (redox) electrochemical reactions. These transformations can achieve good efficiency values, ranging from 80% to 90% (Rufer, 2017). The batteries are composed of a set of cells connected in series and/or parallel. According

to the internal material they are classified as non-refillable (primary cells) or refillable (secondary cells).

The primary cells lifetime is limited to a complete discharge. When finalized this cycle, they must be discarded. This battery type is generally used as a source in low-power applications, such as watches and calculators. On the other hand, secondary cells can be recharged with the support of an external source. Therefore, secondary cells battery can be reused, and are employed in cell phones, Uninterruptible Power Supply (UPS), electric vehicles, notebooks, and others (Pinho; Galdino, 2014). There are various rechargeable battery models available in the market. However, the main characteristics to choose are energy density, efficiency, capacity, lifetime, self-discharge rate, recyclability of materials, and costs.

The cells consist of two electrodes: positive (cathode) and negative (anode). The electrodes are inert in a solution that can be in the solid, liquid, or viscous state (Ibrahim; Ilinca; Perron, 2008; Díaz-González et al., 2013).

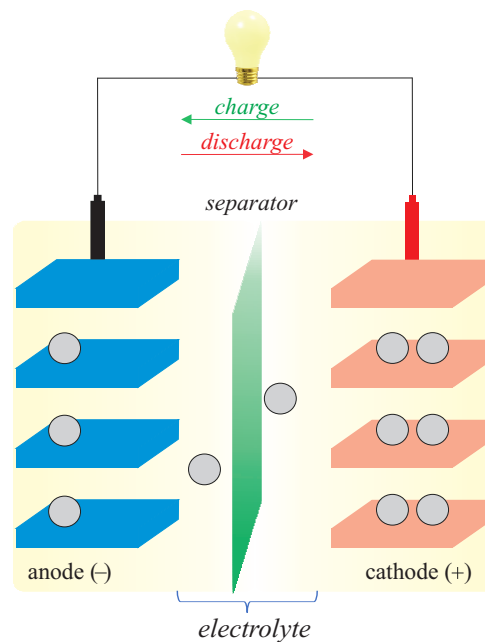


Figure 4 – Simplified sketch of the battery operation.

1.2.1 Lead-Acid Batteries

Pb-acid batteries are the oldest secondary cell technology. This technology was developed in 1859 and implemented commercially in 1880. Thenceforward, these batteries are the most widely available and used secondary batteries in the world (Moseley; Garche, 2014). A cell of this technology uses Lead Dioxide (PbO_2) as the cathode and spongy lead as the anode. Sulfuric-Acid (H_2SO_4) is the electrolyte and Lead (Pb) is used in the current collector (Ibrahim; Ilinca; Perron, 2008; Vazquez et al., 2010; Díaz-González et al., 2013). The nominal voltage of the cell is about 2 V, causing the need to make serial and parallel

connections to achieve the power and energy requirements of the application. There are two main types of **Pb-acid** batteries commonly used in the market: ventilated and sealed (or regulated) **Pb-acid** batteries.

The main advantages of lead-acid batteries are: short response time (in the range of milliseconds), low self-discharge rate (3% to 20% per month), efficiency (70% to 85%) and low cost capital (100-200 \$/kWh) (Molina, 2017). However, **Pb-acid** has disadvantages, such as short shelf life (500-1200 cycles), low energy density, reduced capacity, and poor performance at low and high temperatures. In addition, the material used to sulphate the plates exhibits restricted use (Lawder et al., 2014; McKeon; Furukawa; Fenstermacher, 2014).

An alternative among the **Pb-acid** batteries is the Lead Carbon Batteries (**PbC**). **PbC** is considered an evolution of traditional **Pb-acid** batteries (Li et al., 2022). In the design, the negative electrode, which is responsible for most of the aging, is replaced by carbon (Manjitha; Kumar; Kannan, 2017; Kollmeyer; Jahns, 2019). As advantages, **PbC** batteries have better performance, greater charging capacity, greater depth of discharge, longer life, and lower incidence of sulfation (Manjitha; Kumar; Kannan, 2017).

The main projects that use **Pb-acid** batteries were focused on management, power quality, and ancillary services to power systems, such as peak shaving, frequency and voltage control, spinning reserve, etc. However, the most recent projects aim to expand the area of operation, such as: support the integration of the grid of solar and wind systems and the realization of the smart grid. Among recent operational projects, the Yuza project shows 4.5 MW/10.5 MWh installed in 2010 in Japan and the Modular Multiple Megabit Storage and High-Voltage Multitechnology and Technology (**M5BAT**) installed in 2016 in Aachen, Germany. The **M5BAT** has a capacity of 5 MWh and a discharge time of approximately 1 h at rated power, 5 MW.

1.2.2 Nickel Chemistry Batteries

Nickel-based chemical battery technology is on the market since 1915, since nickel is a material in abundance on Earth (Molina, 2013). Among nickel batteries, there are some models to highlight:

- Nickel Cadmium (**NiCd**);
- Nickel Metal Hydride (**NiMH**);
- Nickel-Iron (**NiFe**);
- Nickel-Hydrogen (**NiH₂**);
- Nickel-Zinc (**NiZn**).

NiCd are highly advanced among batteries mentioned above. During the 90's it was the most used rechargeable battery. Its cell uses Nickel Hydroxide (Ni(OH)_2) as the cathode, metallic Cadmium (**Cd**) as the anode. In this system Potassium Hydroxide (**KOH**) is used as an electrolyte (Vazquez et al., 2010). The nominal voltage of the cell is about 1.2 V, the power specifies approximately 150 W/kg and specific energy between 40 to 60 Wh/kg. In addition, it has a useful life of close to 2000 cycles and a discharge rate of around 10% per month. These batteries have an efficiency between 70% to 90% and a capital cost of approximately 300-600 \$/kWh (Molina, 2017).

NiCd batteries are characterized by fast recharge, long lifetime, good reliability in their operation, and relatively high safety, thus, they are stable in discharge processes and deep overloads (Zhao et al., 2015; Hannan et al., 2021). Moreover, they exhibit a good performance in systems with low temperatures (-20 °C to -40°C) (Baker, 2008; Divya; Østergaard, 2009; Hadjipaschalis; Poullikkas; Efthimiou, 2009; Khaligh; Li, 2010). If this technology is recharged repeatedly after being partially discharged, it may develop a memory effect. In this way, there may be a reduction in the maximum capacity of the battery. (Chen et al., 2009; Luo et al., 2015). In addition, the use of **Cd** and Nickel (**Ni**) may trigger contamination risks to the environment and human health due to the presence of heavy metals highly toxic in their composition.

Currently, some installations **NiCd BESS** are commercially available. For instance, the Golden Valley Electric Association (**GVEA**) project, installed in 2003 in the United States of America (**USA**). The battery system can provide a nominal power of 27 MW for 15 min or 40 MW for 7 min, and its efficiency is in the range of 72% to 78%, with an expected useful life of 20 to 30 years (Holdmann; Asmus, 2019; Molina, 2017).

1.2.3 Sodium Sulphur Batteries

NaS batteries have been marketed since the early 90's. In their internal configuration, they contain molten salt constructed from liquid sulfur at the anode and liquid Sodium (**Na**) at the cathode, separated by a solid ceramic tube of beta alumina that simultaneously acts as the electrolyte and the separator (Vazquez et al., 2010; Molina, 2013; Rosewater; Williams, 2015). The cell voltage of a **NaS** battery is approximately 1.7 V. The **NaS** batteries are used to assist the power grid in large-scale non-mobile applications that require daily cycling, such as peak shaving, load leveling, emergency power supply, and support for the integration of renewable energy generation (Nourai, 2002; Rodrigues et al., 2014).

The use of this battery technology brings some advantages, such as high-specific power (150 to 300 W/kg), high-specific energy (150 to 240 Wh/kg), and high efficiency (approximately 80% to 90%). Its lifetime is approximately 2500 cycles and its capital cost ranges from 250 to 500 \$/kWh (Sarasua et al., 2010; Vazquez et al., 2010; Rodrigues et

al., 2014). However, as a disadvantage, this technology requires a heat source to maintain its operating temperature (about 300°C) (Vudata; Bhattacharyya, 2021). An alternative to solve this problem is to use their own stored energy to power this source, causing the battery performance to drop.

The main projects of BESS that use the technology of NaS are installed in Japan, USA and Italy. These projects have a capacity of more than 180 MW (Molina, 2017). In 2008, a system, Village Wind Farm, was installed in the Rokkasho–Japan with a capacity of 238 MWh and a discharge time approximately of 7 h at rated power (34 MW). Another system was installed in 2016 by Mitsubishi Electric Corporation, which built the largest NaS BESS in the world (50 MW/300 MWh) for the Japanese energy supplier Kyushu Electric Power Company. In 2014, Terna SANC Project in Flumeri (BESS 1) and Misano (BESS 2), were installed in Campania, Italy. This system consists of two BESS with 12 MW and 96 MWh each, dedicated to balancing electricity demand and supply and stabilizing the transmission grid to optimize performance with the massive increase in intermittent renewable energy. Finally, in USA the Big Battery Old (BBO) is a 4 MW/32 MWh system installed in 2010 to provide backup power to the city of Presidio, Texas, USA, in case of power outages mainly associated with severe weather conditions (storms) (Molina, 2017).

1.2.4 Flow Batteries

Commercialized since the 80's, flow batteries are similar to conventional batteries. However, the electroactive material is stored in two electrolysis tanks, producing energy by a reversible electrochemical reaction between two electrolytes. The three types of flow batteries most discussed in the literature is are described below (Chalamala et al., 2014): Zinc Bromide (ZnBr), Vanadium Redox Battery (VRFB) and Polysulfide Bromide (PSB). When compared to conventional batteries (lead acid batteries), flow batteries have some advantages, such as:

- The flow battery exhibits high-energy density and large energy capacity in a single device. On the other hand, conventional batteries always have a trade-off between high-power (which requires thin electrodes) or high-energy (which requires thick electrodes) (Chalamala et al., 2014).
- Increased safety because the reagents storage assets are separated into tanks. In addition, access to the tanks facilitates a better measurement of the State-of-Charge (SOC)³.

³ The ratio between the charging capacity, available in a battery or cell, and the nominal capacity of the battery. This value is expressed as a percentage of nominal capacity.

- Flow batteries have a discharge rate (1% per day) and are tolerant of overloads and deep discharges. As a consequence, to supply the same demand, fewer flow batteries are needed than conventional batteries.
- The lifespan of the cells is between 3000 and 5000 cycles and are not dependent on the discharge depth, which is not the case with conventional batteries.

The main disadvantages of flow batteries include low energy density (75 Wh/kg to 85 Wh/kg), and complex system requirements when compared to other batteries (Chalamala et al., 2014; Perry; Weber, 2016). To work with this type of battery, a pump system, sensors, flow, and energy management, and secondary containment vessel are used. Therefore, this technology seems unsuitable to small-scale storage applications (Suvire; Molina; Mercado, 2012).

There are some BESS flow batteries installed such as Sumitomo Electric Industries (SEI), Osaka, Japan. Projects carried out that add up to 25 MW and 90 MWh. Minami Hayakita substation of 15 MW/60 MWh installed in Abira-Chou, Hokkaido, Japan (Molina, 2017). Another project is the Storage and Transmission of Wind and Solar Energy in Zhangbei, China.

1.2.5 Li-ion Batteries

Li-ion batteries started to be commercialized in 1990. Currently, they have been widely used in portable electronic devices, such as cell phones, notebooks, watches, and others. Li-ion batteries are lighter, smaller, and more powerful than other batteries, which become more attractive for consumer electronics applications (Mahlia et al., 2014).

The operation of these batteries is based on the electrochemical reactions of the anode, consisting of an analytic material (graphite) and the cathode formed by a lithium metal oxide material, for example, Lithium Cobalate (LiCoO_2) and Lithium Nickel Oxide (LiNiO_2) (Díaz-González et al., 2012; Moseley; Garche, 2014). The electrolyte is a non-aqueous organic liquid containing lithium salts, such as Lithium Perchlorate (LiClO_4) or Lithium Hexafluorophosphate (LiPF_6), dissolved inorganic carbonates.

BESS systems that use Li-ion batteries can be divided in two groups: high-power and high-energy. high-power projects are characterized as short duration and aim to perform frequency control. An example of high-power projects was installed in 2016 in Gyeongsangbuk-do, South Korea, a 48 MW/12 MWh BESS plant (discharge time of about 15 min at nominal power). On the other hand, high-energy systems aim to support the integration of intermittent renewable energy. The 36 MW/24 MWh plant with a discharge time of approximately 40 min at nominal power installed in 2013 in Goldsmith, Texas, USA is an example of the high-energy system. This demonstration technology is used to

help a 153 MW wind power system solve intermittency problems and to provide regulatory services in the ERCOT market (Molina, 2017).

The main disadvantages of Li-ion batteries are depth of discharge and high temperatures. These parameters are directly linked to the lifetime of the batteries. Furthermore, with regard to security, Li-ion technology presents serious problems. Electrodes are thermally unstable and can decompose at elevated temperatures (Aneke; Wang, 2016). Thus, the release of oxygen can lead to a thermal runaway. In order to minimize these risks, Li-ion batteries need special packaging and monitoring, and protection systems to prevent overcharges and excessive discharges (Molina, 2017).

A benchmarking of the battery technologies available in the market is presented in Table 1. The Li-ion, NaS and VRFB batteries are more promising for use in a BESS. Although these technologies are not well consolidated as Pb-acid batteries, which mainly affect their cost, they present characteristics relevant to stationary applications. In addition, which indicates that the cost of this technology will decrease in the next decades (Stroe, 2014a). Thus, in this work Li-ion batteries were used to study the BESS system.

Table 1 – Comparison of key parameters for energy storage systems.

Technology	Specific Energy (Wh/kg)	Efficiency (%)	Lifetime (years)	Cycles	Cost (\$/kWh)
Li-ion	75-265	90-97	10-15	3500	300-700
NaS	150-240	80-90	10-15	2500	250-500
VRFB	75-85	70-85	5-10	5000	200-300
NiCd	40-60	70-90	10-15	2000	300-600
Pb-acid	30-50	70-85	3-6	1200	100-200

1.3 Power converters for BESS realization

Since the batteries provide a direct voltage, power converters are commonly used to interface the batteries and the ac-grid. In current installations, in the MW/MWh range, the converters generally used are based on systems with two or three-level converters based on Insulated-Gate Bipolar Transistor (IGBT). This approach is called single-stage.

Figure 5 illustrates a single-stage BESS, which consists of the association of batteries with a dc/ac⁴ converter connected directly to the grid. There are several dc/ac converter topologies that can be used for BESS. When working with low-voltage storage applications, two-level converters are the topologies typically used. The efficiency and simplicity of its control system increase its notoriety (Trintis; Munk-Nielsen; Teodorescu, 2010). However,

⁴ The acronyms used in this work follow standards that provide the recommended abbreviations, symbols, and units for IEEE publications.

with the increase of the dc-link and grid voltages, this topology does not become more advantageous, because it requires power semiconductors connected in series. Thus, an alternative is to work with three-level converters.

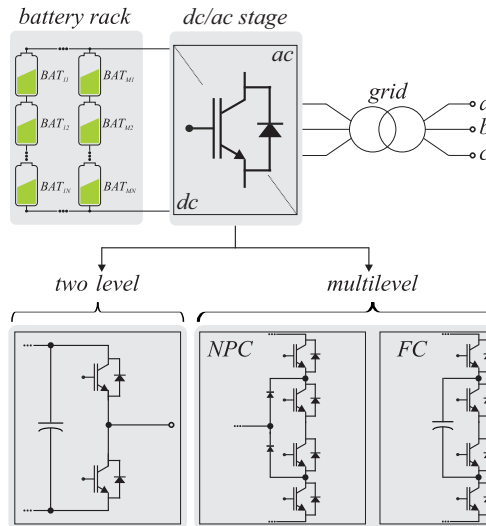


Figure 5 – Schematic for single-stage configuration with dc/ac topologies typically used for BESS.

A three-level converter typically used for BESS is the Neutral Point Clamped (NPC), (Soong; Lehn, 2014a; Wang et al., 2016). One of the advantages of the NPC is the possibility of increase the magnitude of the output voltage and improving the harmonic performance. Indeed, there is a possibility to reduce filter requirements. However, this converter requires more complex control and modulation techniques than two-level converters. Similar to NPC, the Flying Capacitor (FC) converter is a three-level topology. In these converters, flying capacitors are used to generate more levels, reducing the voltage stress on the IGBT. In addition, balancing the capacitor voltages through modulation is possible.

The direct association of the batteries with the inverter observed in single-stage systems can lead to some issues. Figure 6 shows a generic curve for Li-ion batteries. As observed, the Open Circuit Voltage (OCV) varies significantly, up to 30%, depending on the SOC range adopted. Thus, the inverter needs to accommodate these variations. One of the alternatives is to design the converter to operate with a wide voltage range in its dc-link and a wide current range in its IGBT, which could lead to high voltage and current stress and, probably, high losses. However, this approach leads to low-modulation indexes and increases the output harmonics. In addition, the wide input voltage range leads to a non-optimized design of the inverter, which may increase the costs.

One of the alternatives to mitigate the problems mentioned above is to decouple the batteries from the inverter. In this case, a bidirectional dc/dc converter is employed. This is the concept of a two-stage BESS configuration, shown in Figure 7.

Connecting a dc/dc converter between the batteries and the converter is interesting

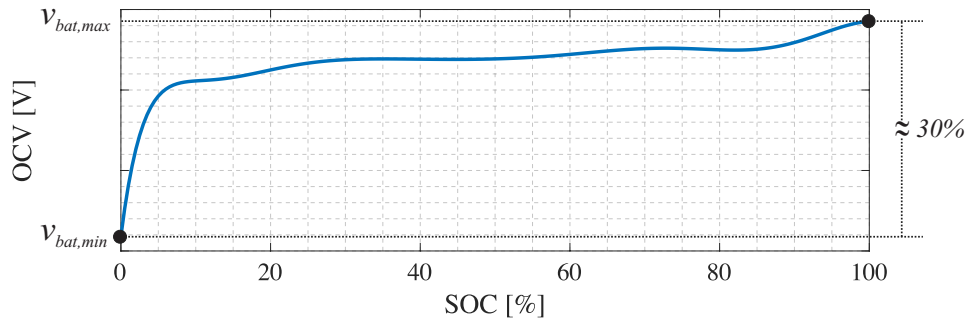


Figure 6 – Generic OCV versus SOC curve for a Li-ion battery.

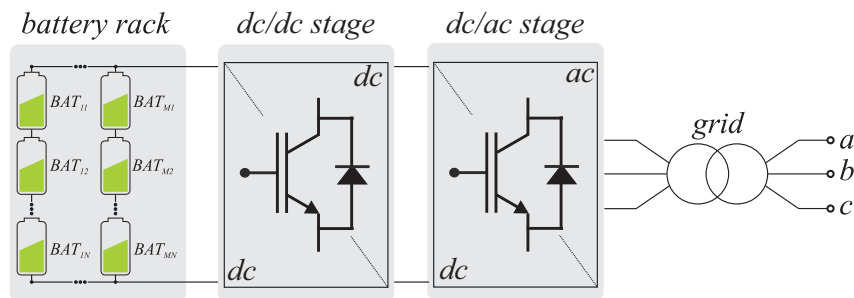


Figure 7 – Schematic of a two-stage configuration.

because it uses fewer batteries to achieve the same dc-link voltage of the inverter when compared to the single-stage. Figure 8a illustrates the parallel topology. In this configuration, the converters are connected to the same dc-link. As a consequence, to obtain higher voltage, more batteries are used or the voltage gain of the dc/dc converter increases. In addition, when faults occur, the dc/dc converter must be able to guarantee that there will be no current injection into the grid.

Figure 8b shows the series configuration. This proposal has the advantage of designing dc/dc converters with a low-voltage gain and using fewer series connected batteries. However, if a dc/dc converter fails, the system must be able to bypass the faulty unit and increase the voltage gain of the other units.

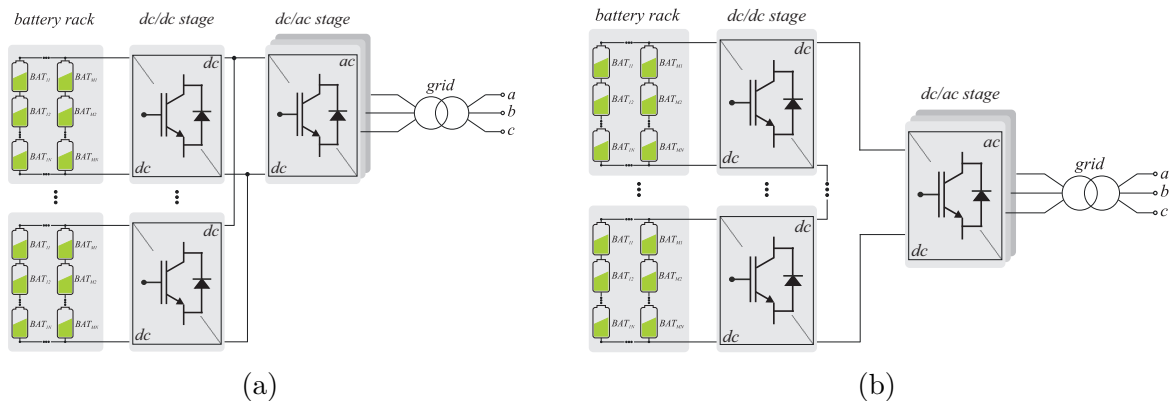


Figure 8 – Two-stage configuration topology: (a) two-stage system with parallel-connected configuration. (b) two-stage system with series-connected configuration.

Several dc/dc converter topologies are presented in the literature (Karshenas et

al., 2011). Topology selection depends on battery technology, voltage gain and the aimed efficiency (Bragard et al., 2010). Figure 9 shows examples of dc/dc converter typically used for BESS.

Soong e Lehn (2014a) and Vasiladiotis e Rufer (2015a) proposed the use of a bidirectional boost converter. This topology becomes attractive due to the extensive knowledge in the literature and its simple implementation. Another bidirectional converter proposal is presented at (Inoue; Akagi, 2007; Thomas; Stieneker; De Doncker, 2013; Everts et al., 2014). The Dual Active-Bridge Converter (DAB) features high efficiency, elevated voltage gain (adjusted by the transformer turns ratio), and galvanic isolation. Finally, Keyhani e Toliyat (2012) proposes the use of the flying capacitor dc/dc converter. In comparison with the bidirectional boost converter, the FC dc/dc converter features a higher voltage conversion rate and lower energy losses. In addition, the proposed topology can be extended to several voltage levels.

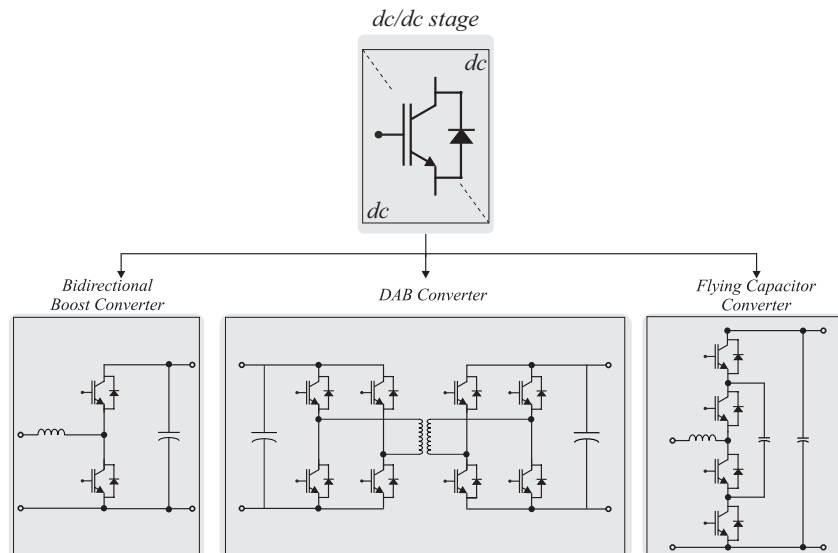


Figure 9 – Typical dc/dc converter topologies used to decouple the dc-link batteries from the inverter.

In comparison with the single-stage BESS, the two-stage BESS can reduce the number of batteries in series. In addition, the dc/dc converter inserts a degree of freedom in terms of voltage gain which leads to an optimized design of the inverter. In addition, some studies mention a possible increase in battery lifetime when dc/dc converters are employed (Abbas; Lehn, 2009; Trintis; Munk-Nielsen; Teodorescu, 2011; Soong; Lehn, 2014a).

1.3.1 Cascaded Multilevel Converters

The aforementioned approaches present limitations when the grid voltage value and rated power increases. An alternative concept which allows to mitigate this limitation is the multilevel topologies. Cascaded multilevel converters or cascaded H-bridge, CHB

use **SM**, or cells, connected in cascade order to increase the output voltage. Thus, this approach presents some advantages, such as: high voltage level, possibility to work with low switching frequencies, fault tolerance, redundancy, and flexibility to change the number of **SM**.

Two variants of the cascaded multilevel converter can be implemented, star or delta. Figure 10a and Figure 10b, respectively. Figure 10c shows the **BESS** system connection for the cascaded multilevel converter star and delta configuration. In the two-stage approach, six semiconductors are needed. Consequently, it raises project costs. Thus, for physical implementations, the star system is more economical. On the other hand, with respect to symmetrical and asymmetric grid faults, the delta configuration has better dynamics (Dekka et al., 2017).

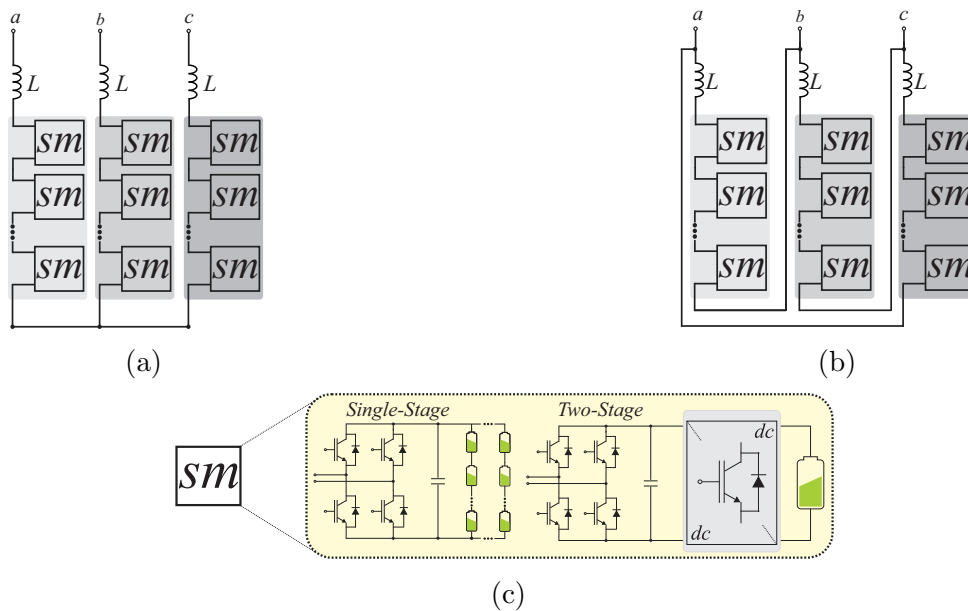


Figure 10 – Structures of the cascaded multilevel converter: (a)Star-connected; (b)Delta-connected; (c) SM configurations.

An alternative among cascaded multilevel converters is the topology patented by Marquardt (2001), called Modular Multilevel Converter (**MMC**). The **MMC** uses the same concepts as the cascade converters mentioned above, differing only in the circuit configuration. In an **MMC**-based **BESS** system the battery arrangement can be connected directly to the dc-link, as shown in Figure 11a, this configuration is called centralized. Another proposal is presented in Figure 11b, where the batteries are associated in each **SM** of the converter. This configuration is called distributed.

Centralized BESS becomes less advantageous compared to the distributed system, as it requires long battery chains to increase voltage values. Thus, to take advantage of the converter modularity, the batteries can be connected to each SM. In addition, in this configuration the batteries can be connected directly to the SM (single-stage) or interfaced by a dc/dc converter (two-stage) (Wang et al., 2016).

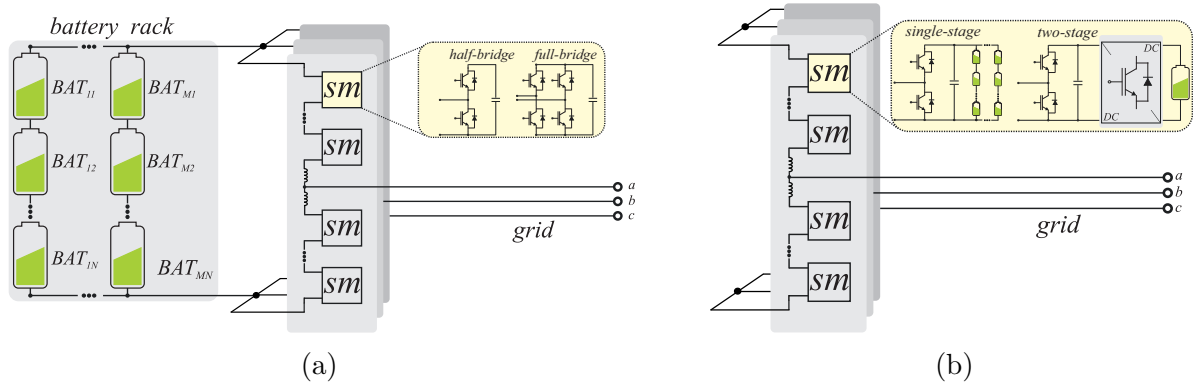


Figure 11 – MMC-based BESS:(a) Centralized BESS;(b) Single-stage and two-stage realizations of a distributed MMC-based BESS.

Finally, Table 2 presents some examples BESS around the world. As observed, most projects employ two or three-level converters. In addition, Li-ion batteries have been strongly used in recent years.

Table 2 – Major companies using BESS systems.

Manufacturer	Of Stage	Configuration	Battery Technology
ABB	1	2 and 3 level	Li-ion
DynaPower	-	2 and 3 level	Li-ion
Enercon	2	2 and 3 level	Li-ion
Extreme Power	-	2 level	Advanced Li-ion
General Electric	-	2 and 3 level	Pb-acid
Mitsubishi	-	2 and 3 level	Li-ion
Nidec	2	2 level	NaS
Parker SSD	1	2 and 3 level	Li-ion
S&C Electric	2	2 and 3 level	Pb-acid
Yunicos	-	2 and 3 level	Advanced Li-ion
AES Tiete	1	-	Li-ion
WEG	2	-	Li-ion
Akagi Testing Center ⁵	1	2 level	Li-ion

⁵ Prototype real-scale (500 kW) cascaded multilevel converter (star-connected) grid model and a 6.6-kV real-scale distribution line, (Kawakami et al., 2014).

1.4 Purpose and Contributions

As presented in the previous sections, the cascade multilevel converter becomes an alternative due to some points that can be mentioned below, such as:

- low-switching frequency;
- high-output voltage;
- fault-tolerance and redundancy.

Among the cascaded multilevel converters topologies, some comparisons are made to determine the optimal topology to use in a BESS. The star-connected topology, for a given voltage level, requires fewer semiconductor components and SM when compared to star and delta configuration. As a result, this alternative has the lowest costs (Baruschka; Mertens, 2011). However, the topology does not have a circulating current. Consequently, capacitor voltage balancing is performed by injecting zero-sequence voltage. In addition, the ability to control negative-sequence reactive current is limited by the rated voltage of the converter. Thus, the star-connected topology is not an alternative for working with systems that need to flicker compensation or unbalanced conditions (Behrouzian; Bongiorno, 2017).

The delta-connected configuration has fewer voltage levels than the star-connected. Furthermore, it needs more SM and semiconductors. On the other hand, the delta-connected configuration has a lower switching frequency and a degree of freedom in the circulating current equivalent to zero sequence (Behrouzian; Bongiorno, 2017). Similar to the star-connected configuration, the delta-connected has limitations under voltage unbalance conditions (Behrouzian; Bongiorno, 2017).

The MMC share the advantages of multilevel converters, such as low voltage harmonic content and low voltage switching devices. Compared to cascade converters, the MMC has only half the arm current at the same power rating. Also, it contains a dc-link which is not available in the cascaded topology (Wang; Lin; Ma, 2019). On the other hand, MMC topology is more expensive compared to star and delta-connected configuration. When integrating BESS to support the electric power system and/or a high-integration of renewable sources, MMC with distributed energy storage has a fixed dc-link that makes it possible to interconnect with a medium grid voltage. In this way, a single system can act as both a dc/ac interconnect and an energy storage unit (Soong; Lehn, 2014a).

According to the above considerations, and due to a gap in the literature of works to optimize design using MMC, this work chose to work with this topology. In an MMC-based BESS the single-stage and the two-stage approaches are possible. However, there are few references in the literature comparing these realizations. Therefore, this work presents

a benchmark of the two configurations, and it presents solutions to optimize the design of each of the systems. One of the optimization variables is battery energy oversizing. Indeed, this work proposes two design strategies, customized and standard solutions. In the customized solution, the projects are evaluated with battery cells, a personalized proposal for the client. In the standard solution, commercialized battery packs are used.

1.4.1 Objectives

MMC-based BESS can play an important role when applied to power systems, for example, stabilizing and improving power quality. The use of a distributed system and its configuration have already been discussed. However, a comprehensive analysis of single and two-stage approaches remains unexplored in the literature. This study evaluates metrics such as losses, volume, efficiency, and total cost for each design. Therefore, this work aims to:

- Benchmark of single-stage and two stage MMC-based BESS in terms of number of batteries, power semiconductors, efficiency and total cost.
- Evaluate single and two-stage approaches for customized and standard solution.
- Design a tool that evaluates the total costs of projects based on the lifetime of the batteries. This analysis is considered for the single-stage and two-stage approaches.
- Develop a control strategy for MMC-based BESS for single-stage and two-stage approaches.

1.4.2 Contributions

The main contributions of this work are:

- Evaluation of the MMC-based BESS systems distributed by comparing the order of magnitude of the system (batteries + IGBT) to supply the same demand. In addition, assessing the losses for an adopted load profile.
- Provide methodology to support engineers in the design and cost optimization of MMC-based BESS.
- Determine the ideal combination of battery and IGBT part numbers based on a given initial set.
- Provide the methodology to calculate the lifetime of batteries;
- Provide a methodology to perform the tuning of the controllers for the MMC.

1.5 Organization of this Ph.D. Thesis

This Ph.D. is organized into seven chapters: Chapter 1 presents a brief review of the structures adopted in this study, the motivations and objectives of this project. In Chapter 2 the design of the distributed MMC topology and SM is presented discussing its main characteristics. Next, a flowchart with the objective of optimizing the settings is discussed. After, the control strategies for MMC-based BESS single and two-stage approach are discussed in Chapter 3. In addition, the methodology used to perform the tuning of the controllers is presented. Chapter 4 presents the methodology used to calculate the losses and the total costs for the single and two-stage approaches. Based on the methodology presented, the total cost related to each approach is discussed in Chapter 5. In order to validate the controller design and analyze the dynamics of the MMC-based BESS topology, simulations for single-stage and two-stage approaches are presented in Chapter 6. Next, the results obtained in simulations are discussed. Finally, Chapter 7 presents the conclusions and future developments based on this work.

1.6 List of Publications

1.6.1 Submitted Journal Papers (under review)

- J. H. D. G. Pinto, A. F. Cupertino, H. A. Pereira and S. I. S. Junior. Modelling and Control tuning of single-stage MMC-based BESS.

1.6.2 Published Journal Paper

- J. H. D. G. Pinto, W. C. S. Amorim, A. F. Cupertino, H. A. Pereira, S. I. S. Junior and R. Teodorescu. Optimum Design of MMC-based ES-STATCOM Systems: The Role of the Submodule Reference Voltage. *IEEE Transactions on Industry Applications*, 2020.
- Pinto, J.H.D.G.; Amorim, W.C.S.; Cupertino, A.F.; Pereira, H.A.; Junior, S.I.S. Benchmarking of Single-Stage and Two-Stage Approaches for an MMC-Based BESS. *Energies* 2022, 15, 3598. <https://doi.org/10.3390/en15103598>

1.6.3 Published Conference Paper

- Castro, P. D. C., da Silva Alves, M. H., Pinto, J. H. D. G., Cardoso Filho, B. D. J., and Seleme, S. I. Desenvolvimento de um Modelo Matemático Unificado para o Conversor Boost Entrelaçado, 2018 13th IEEE International Conference on Industry Applications (INDUSCON), São Paulo, Brazil, 2018, pp. 1-6.

1.6.4 Submitted in a journal (SOBRAEP): In cooperation with the research group

- João Victor Guimarães França, Jonathan Hunder Dutra Gherard Pinto, Dayane do Carmo Mendonça, João Victor Matos Farias, Renata Oliveira de Sousa, Heverton Augusto Pereira, Seleme Isaac Seleme Júnior, Allan Fagner Cupertino. Development Of A Full-Bridge Converter Platform For Flexible Power Electronic Converters. Revista Eletrônica de Potência–SOBRAEP, 2022.

2 Main Circuit Parameters Design

This chapter begins with the presentation of the architecture of the MMC-based BESS and respective approaches: single-stage and two-stage. Then, the mathematical model of the converter is presented as well as the equations to determine the current in the battery for the single-stage and two-stage approaches. In addition, the design flowchart and the effect of roudings in the BESS oversizing is comprehensively analyzed. According to the analyses, two solutions are presented: standard and customized. In the standard solution, commercial-type battery racks are considered. On the other hand, in the customized solution, battery racks formed by battery cells are considered.

2.1 Investigated Architectures

The MMC topology is illustrated in Figure 12. This converter concept is based on the cascade connection of converters that operate at lower voltage levels, denominated SM. The upper and lower arms are connected through two inductors with arm inductance (L_{arm}). These inductors limit the current increase rate during faults and reduce the high-order harmonics in the circulating current (Harnefors et al., 2013; Perez et al., 2015; Arslan et al., 2018). L_{arm} presents an intrinsic resistance, denoted as R_{arm} . Moreover, the MMC is connected in the grid through a three-phase isolation transformer with leakage inductance L_{grid} and grid equivalent resistance R_{grid} .

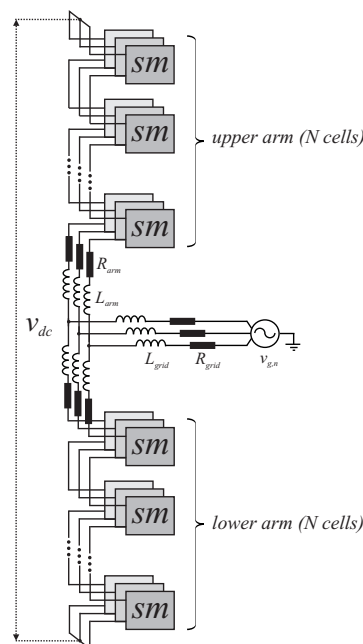


Figure 12 – Schematic of an MMC topology.

Two configurations of MMC-based BESS are investigated in this work. In the single-stage approach, the batteries are connected directly to the SM, as shown in Figure 13 (a). The use of passive filters in single-stage approach is quite controversial. Some references propose passive filters to attenuate or reduce harmonics in the battery current (Soong; Lehn, 2014a; Vasiladiotis; Rufer, 2015a). On the other hand, some references do not include a filter. Therefore, in this work, the passive filter has not been investigated yet. An example of a commercial-scale system without dc-filter is presented in (Kawakami et al., 2014).

For the two-stage approach, Figure 13 (b), a bidirectional boost converter is used to connect the batteries to the MMC. The choice of this dc/dc converter is justified by its simple control structure and reduced number of components.

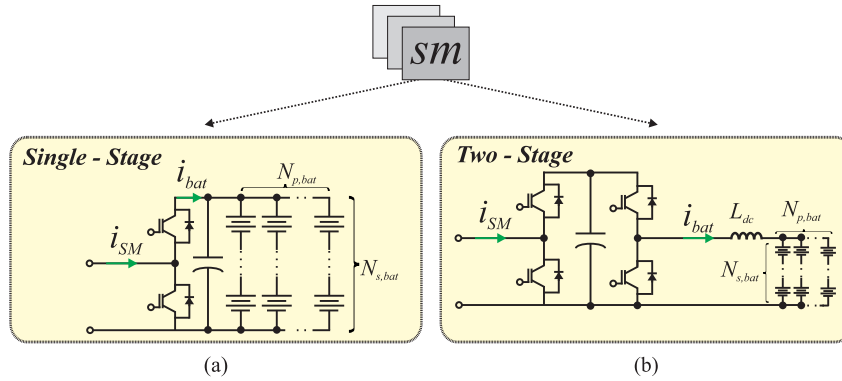


Figure 13 – Possible configurations for the distributed energy storage approach: (a) single-stage and (b) two-stage.

2.2 MMC Mathematical Model

The mathematical model presented in this section intends to define the main variables that describe the MMC dynamics. In addition, the instantaneous power flow in the MMC is modeled, which leads to some conclusions regarding the capacitor voltage balancing and voltage ripple. Voltage sources represent the voltages generated by each arm. $v_{u,n}$ denotes the voltage synthesized in the upper arm of *phase-n* while $v_{l,n}$ denotes the voltage synthesized in the lower arm of *phase-n*.

1. The effect of the switching frequency is neglected, i.e., an average model is considered;
2. The capacitor voltages are assumed to be perfectly balanced.

Under these conditions, the converter presented in Figure 12 can be represented by Figure 14. This model assumes perfect balancing capacitor voltages and negligible harmonic components.

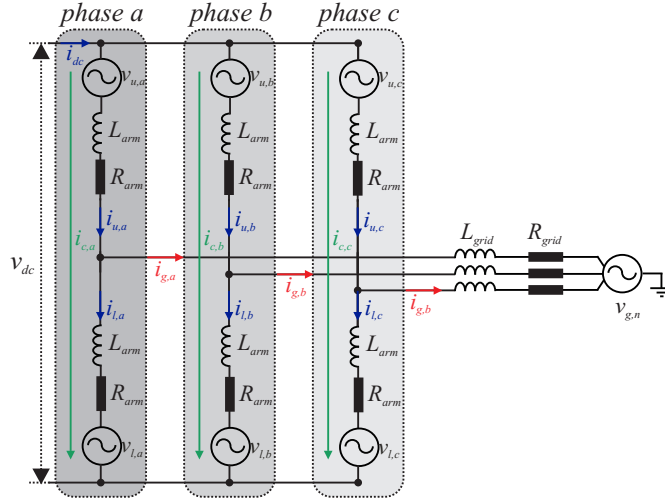


Figure 14 – MMC arm-average model for $i_{g,n}$ and $i_{c,n}$ dynamics evaluation.

In the distributed topology, the dc-link current (i_{dc}) is zero. In this way, the sum of the upper and lower arm currents must be zero. Accordingly,

$$\sum_{n=1}^3 i_{u,n} = \sum_{n=1}^3 i_{l,n} = 0, \quad (2.1)$$

where $i_{u,n}$ is the upper arm current of *phase-n* and $i_{l,n}$ is lower arm current of *phase-n*.

According to [Sharifabadi et al. \(2016a\)](#), the arm currents can be written as follows:

$$\begin{cases} i_{u,n} = \frac{i_{g,n}}{2} + i_{c,n}, \\ i_{l,n} = -\frac{i_{g,n}}{2} + i_{c,n}, \end{cases} \quad (2.2)$$

where $i_{g,n}$ is the grid current of *phase-n* and $i_{c,n}$ is circulating current of *phase-n*. The current $i_{c,n}$ can be indirectly measured through the arm currents as follows:

$$i_{c,n} = \frac{i_{u,n} + i_{l,n}}{2}. \quad (2.3)$$

Substituting Eq. (2.2) into Eq. (2.1) yields:

$$i_{c,a} + i_{c,b} + i_{c,c} = 0. \quad (2.4)$$

The superposition theorem can be employed to analyze the output current and the circulating current independently. The output current dynamics are described by the per-phase circuit shown in Figure 15.

The analysis of Figure 15 leads to:

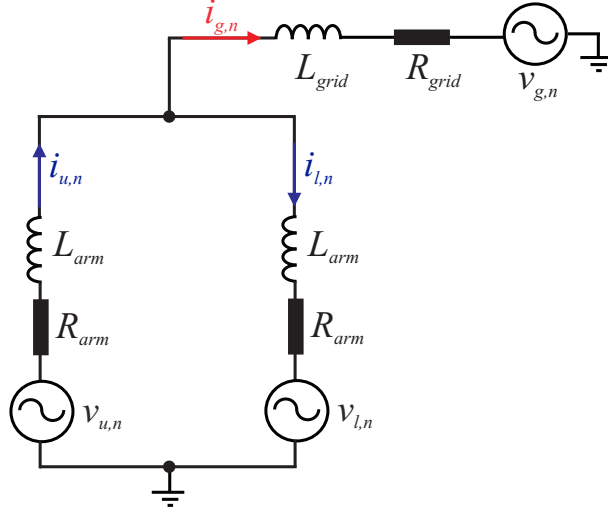


Figure 15 – Equivalent circuit of the output current dynamics.

$$v_{g,n} = v_{s,n} - \left(\frac{L_{arm}}{2} + L_{grid} \right) \frac{di_{g,n}}{dt} - \left(\frac{R_{arm}}{2} + R_{grid} \right) i_{g,n}, \quad (2.5)$$

where $v_{s,n}$ is line-to-neutral output voltage, which can be expressed by:

$$v_{s,n} = \frac{1}{2}(-v_{u,n} + v_{l,n}). \quad (2.6)$$

It is important to remark that the factor $1/2$ in the Eq. (2.5) and (2.6) is due to Millman's theorem¹.

The $i_{c,n}$ dynamics can be obtained as follows:

$$\frac{v_{dc}}{2} - v_{c,n} = L_{arm} \frac{di_{c,n}}{dt} + R_{arm} i_{c,n}, \quad (2.7)$$

where v_{dc} is dc-link voltage, R_{arm} and L_{arm} are arm resistance and inductance, respectively. $v_{c,n}$ is the common-mode voltage, which is given by:

$$v_{c,n} = \frac{1}{2}(v_{u,n} + v_{l,n}). \quad (2.8)$$

where $v_{u,n}$ is the voltage upper arm of *phase-n* and $v_{l,n}$ is the voltage lower arm of *phase-n*. These voltages can be expressed by:

$$\begin{cases} v_{u,n} = \sum_{i=1}^N n_{u,n} v_{SM,n}^i, \\ v_{l,n} = \sum_{i=1}^N n_{l,n} v_{SM,n}^i, \end{cases} \quad (2.9)$$

¹ According to Millman (1940), any association of connected voltage sources in parallel can be reduced to just one equivalent source. The same conclusion can be obtained through Thevenin's theorem.

The normalized reference signals per n-phase are given by:

$$\begin{cases} v_{u,n} = \frac{v_b^*}{v_{SM}^*} + \frac{v_{c,n}}{v_{SM}^*} - \frac{v_{s,n}}{Nv_{SM}^*} + \frac{1}{2}; \\ v_{l,n} = \frac{v_b^*}{v_{SM}^*} + \frac{v_{c,n}}{v_{SM}^*} + \frac{v_{s,n}}{Nv_{SM}^*} + \frac{1}{2}. \end{cases} \quad (2.10)$$

where v_b^* is output references of individual voltage balancing control. However, v_b^* is disregarded as it is close to zero and v_{SM}^* is the SM voltage reference and N is the total number of SM.

The insertion index for upper and lower arms, respectively, are given by:

$$\begin{cases} n_{u,n} = \frac{v_{u,n}}{Nv_{SM}^*}, \\ n_{l,n} = \frac{v_{l,n}}{Nv_{SM}^*}. \end{cases} \quad (2.11)$$

At this point, two facts must be highlighted. Firstly, the control of output current guarantees the power exchange between the batteries and the electrical grid. On the other hand, the circulating current control plays an important role in the energy balance among the converter arms. Expressions of the instantaneous power developed by each arm in steady-state are derived to explicitly show these facts. The instantaneous active power in the lower arm of *phase-n* ($p_{l,n}$) and the instantaneous active power in upper arm of *phase-n* ($p_{u,n}$) of the system can be estimated by:

$$\begin{cases} p_{l,n} = v_{l,n}i_{l,n}, \\ p_{u,n} = v_{u,n}i_{u,n}. \end{cases} \quad (2.12)$$

Using Eq (2.2) and (2.10), the Eq. (2.12) can be expanded as follows:

$$\begin{cases} p_{l,n} = \left(-v_{c,n} + v_{s,n} + \frac{v_{dc}}{2}\right) \left(-\frac{i_{g,n}}{2} + i_{c,n}\right), \\ p_{u,n} = \left(-v_{c,n} - v_{s,n} + \frac{v_{dc}}{2}\right) \left(\frac{i_{g,n}}{2} + i_{c,n}\right). \end{cases} \quad (2.13)$$

Eq. (2.13) can then be rewritten as follows:

$$\begin{cases} p_{l,n} = v_{c,n} \frac{i_{g,n}}{2} - v_{c,n}i_{c,n} - v_{s,n} \frac{i_{g,n}}{2} + v_{s,n}i_{c,n} - \frac{v_{dc}}{2} \frac{i_{g,n}}{2} + \frac{v_{dc}}{2}i_{c,n}, \\ p_{u,n} = -v_{c,n} \frac{i_{g,n}}{2} - v_{c,n}i_{c,n} - v_{s,n} \frac{i_{g,n}}{2} - v_{s,n}i_{c,n} + \frac{v_{dc}}{2} \frac{i_{g,n}}{2} + \frac{v_{dc}}{2}i_{c,n}. \end{cases} \quad (2.14)$$

Assuming the contribution of internal voltage of *phase-n* ($v_{c,n}$) small, Eq. (2.14) can be simplified. Accordingly:

$$\begin{cases} p_{l,n} \approx -v_{s,n} \frac{i_{g,n}}{2} - \frac{v_{dc}}{2} \frac{i_{g,n}}{2} + \frac{v_{dc}}{2} i_{c,n} + v_{s,n} i_{c,n}, \\ p_{u,n} \approx -v_{s,n} \frac{i_{g,n}}{2} + \frac{v_{dc}}{2} \frac{i_{g,n}}{2} + \frac{v_{dc}}{2} i_{c,n} - v_{s,n} i_{c,n}. \end{cases} \quad (2.15)$$

Different colors are employed in relation Eq. (2.13) to highlight power terms with different physical meanings. At this point, the following conclusions can be stated:

1. The product $v_{s,n} \frac{i_{g,n}}{2}$ leads to a dc component and second-harmonic power oscillation. Assuming that $v_{s,n}$ and $i_{g,n}$ are sinusoidal waves, the average value represents the active power transferred from the submodules to the grid. The oscillating component leads to a second-harmonic ripple in the battery current.
2. The product $\frac{v_{dc}}{2} \frac{i_{g,n}}{2}$ leads to a fundamental frequency oscillating power. This term results in a fundamental frequency ripple in the battery current. As observed, this term presents opposite signals in the lower and upper arms. Therefore, this power oscillation is not observed at the converter ac terminals.
3. The terms containing $i_{c,n}$ require more attention. As previously mentioned, a possible solution for Eq. (2.4) is given by:

$$i_{c,c} = -i_{c,a} - i_{c,b}, \quad (2.16)$$

with free $i_{c,a}$ and $i_{c,b}$. The term $\frac{v_{dc}}{2} i_{c,n}$ indicates that a dc-component in circulating current component can perform the energy exchange between the converter phases. Indeed, the sum of the power transfer for the three phases must be zero, which becomes evident in the energy exchange among the converter phases.

4. The term $v_{s,n} i_{c,n}$ indicates that a fundamental frequency circulating current leads to a non-zero power in the arm. Moreover, these terms present opposite signals in the upper and lower arms. Therefore, a fundamental frequency circulating current can exchange energy between the lower and upper arms.

In power systems connected to the grid, an strategy to increasing the operating range is to inject a third-order harmonic into the phase voltages (Saedifard; Irvani, 2010). Regardless of whether the system is a one-stage or two-stage approach, the variation in arm power will generate a ripple current in the battery. In addition, for the single or two-stage approach, it assumes that the system is balanced, $i_{c,n} = 0$. Thus, analyzing only the voltage of the arm, for example, Eq. (2.12) can be rewritten as follows:

$$p_{u,n} = v_{u,n}i_{u,n} = \left[\underbrace{\frac{v_{dc}}{2} - \widehat{V}_{s,n} \cos(\omega t + \theta_v) + \frac{1}{6}\widehat{V}_{s,n}(3\omega t)}_{v_{u,n}} \right] \left[\underbrace{\frac{1}{2}\widehat{I}_g \cos(\omega t + \phi + \theta_v)}_{i_{u,n}} \right]. \quad (2.17)$$

where $\widehat{V}_{s,n}$ is the peak of output voltage, \widehat{I}_g is the peak of grid current, ω is the nominal grid angular frequency, θ_v is the grid voltage angle and ϕ is the grid current angle.

Assuming negligible power losses and that the power is evenly distributed to the SM, the power of an SM can be estimated by:

$$p_{SM} = \frac{p_{u,n}}{N}, \quad (2.18)$$

where p_{SM} is the power of SM. Then, the SM current can be expressed by:

$$i_{SM} = \frac{p_{u,n}}{Nv_{sm}^*}. \quad (2.19)$$

Therefore, i_{SM} can be expressed as follows:

$$i_{SM} = \frac{1}{Nv_{SM}^*} \frac{\widehat{I}_g}{2} \left[\frac{v_{dc}}{2} \cos(\omega t + \phi + \theta_v) - \widehat{V}_{s,n} \cos(\omega t + \theta_v) \cos(\omega t + \phi + \theta_v) + \frac{\widehat{V}_{s,n}}{6} \cos(3\omega t + \theta_v) \cos(\omega t + \phi + \theta_v) \right]. \quad (2.20)$$

Considering $m = 2\frac{\widehat{V}_{s,n}}{Nv_{SM}^*}$, the Eq. (2.20) can be rewritten as²:

$$i_{SM} \approx \frac{1}{8} m \widehat{I}_g \left[\underbrace{-\cos(\phi)}_{dc \text{ component}} + \underbrace{\sqrt{3} \cos(\omega t + \theta_v + \phi)}_{1^{st} \text{ harmonic}} - \underbrace{\cos(2\omega t + 2\theta_v + \phi)}_{2^{nd} \text{ harmonic}} + \underbrace{\frac{1}{6} \cos(2\omega t - \theta_v - \phi)}_{2^{nd} \text{ harmonic}} + \underbrace{\frac{1}{6} \cos(4\omega t + \theta_v + \phi)}_{4^{th} \text{ harmonic}} \right], \quad (2.21)$$

Figure 16 illustrates the behavior of i_{SM} current for single and two-stage approach. According to the Eq. (2.21), i_{SM} has first, second, and fourth harmonic components, which can generate a ripple in the battery. In the single-stage approach shown in Figure 16a, as $v_{SM}^* = v_{bat}$, if no filter is used, the fundamental and second harmonic components flow in

² $\cos(A) \cos(B) = \frac{1}{2} [\cos(A+B) + \cos(A-B)]$.

the battery. Under such conditions, those harmonics increase the Root Mean Square (RMS) value of current and the losses in the battery. For the two-stage approach system shown in Figure 16b the dc/dc converter can be controlled to guarantee a battery current with only dc components.

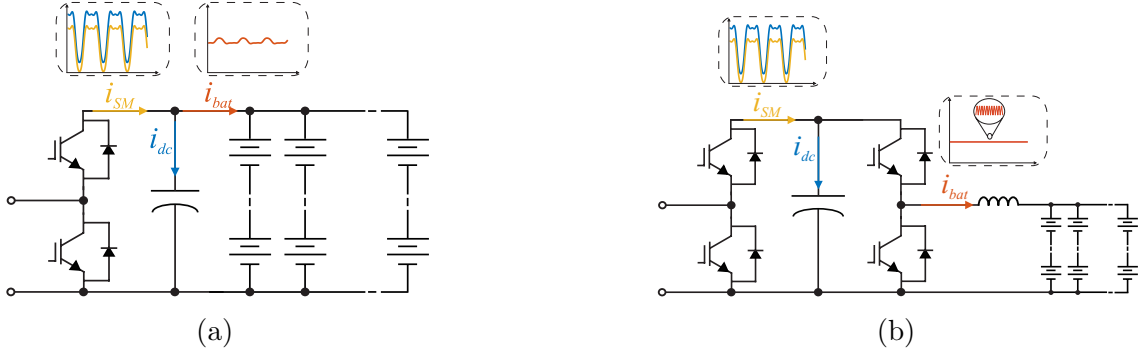


Figure 16 – Analysis of currents using an equivalent model of SM: (a) single-stage approach configuration; (b) two-stage approach configuration.

According to Eq. (2.21), the effective current in the battery in the single-stage approach ($i_{bat,RMS(SS)}$) and in the two-stage approach ($i_{bat,RMS(TS)}$) can be calculated as follows, respectively:

$$\begin{cases} i_{bat,RMS(SS)} = \frac{1}{8}m\hat{I}_g\sqrt{\cos^2(\phi) + \frac{67}{36}}, \\ i_{bat,RMS(TS)} = \delta\frac{1}{8}m\hat{I}_g|\cos(\phi)|, \end{cases} \quad (2.22)$$

where δ is the duty cycle. Furthermore, for unit power factor, $\cos^2(\phi) = 1$.

The harmonics increase the RMS value of current and consequently the temperature. Thus, increases battery losses and reduces batteries lifetime (Bragard et al., 2010; Xie; Angquist; Nee, 2008). Thus, the temperature variation in the batteries in the single-stage approach ($\Delta T_{bat(SS)}$) and in the two-stage approach ($\Delta T_{bat(TS)}$) can be calculated as follows:

$$\begin{cases} \Delta T_{bat(SS)} = \left(\frac{i_{bat,RMS(SS)}}{N_{p,bat(SS)}}\right)^2 R_s R_{TH}, \\ \Delta T_{bat(TS)} = \left(\frac{i_{bat,RMS(TS)}}{N_{p,bat(TS)}}\right)^2 R_s R_{TH}, \end{cases} \quad (2.23)$$

where, R_s and R_{TH} are the battery equivalent internal resistance and battery thermal resistance. In addition, $N_{p,bat(SS)}$ and $N_{p,bat(TS)}$ are number of batteries in parallel for the single and the two-stage approaches.

In order to compare the temperature variation in the single-stage and two-stage approaches, the power demand, and energy capacity of the SM in the single-stage and two-stage approaches should be identical. Therefore, in the two-stage approach, the duty cycle (σ) varies the current so that both approaches process the same power. Consequently, $N_{p,bat(TS)} = N_{p,bat(SS)}/\sigma$;

Finally, the relationship between $\Delta T_{bat(SS)}$ and $\Delta T_{bat(TS)}$ can be obtained as follows:

$$\frac{\Delta T_{bat(SS)}}{\Delta T_{bat(TS)}} \approx 2.86 \quad (2.24)$$

It is important to note that this temperature variation is increased by the ambient temperature of the batteries. Furthermore, this relationship is only valid if the same power synthesized by the SM in both approaches is considered. In addition, some variables can influence this relationship to be changed, such as: rounding in the design process, different designs and the type of service provided by the battery. In the next chapters, this analysis will be exemplified with the proposed case study.

2.3 MMC-based BESS Design

The flowcharts to optimize designs the MMC-based BESS in single-stage and two-stage approaches are presented in Figure 17 (a) and (b), respectively. The primary input parameters are the MMC-base BESS specifications, such as: nominal energy storage (E_s), nominal power (S_n), grid voltage (V_g), and grid frequency (f_g). Furthermore, the first step in the converter design is to calculate the minimum required output voltage which guarantees the connection to the grid. This value is computed by (Chaudhary et al., 2020):

$$\hat{V}_s \approx 1.05\hat{V}_g (1 + \Delta V + x_{pu}), \quad (2.25)$$

where \hat{V}_g is the peak of the line-to-neutral voltage, ΔV is the maximum grid voltage variation in pu and x_{pu} is the per unit equivalent output reactance of the converter. The margin of 5% is assumed to guarantee a suitable dynamic behavior in the current control (Backlund et al., 2009; Vasiladiotis; Rufer, 2015b).

The secondary input parameters are variables that can be changed for reduce purposes. For both approaches, the following parameters are considered: switching frequency (f_s), SOC interval (SOC_{max} and SOC_{min}), and per unit equivalent output reactance of the converter (x_{pu}). Furthermore, in the two-stage approach, the switching frequency of the dc/dc converter is considered (f_{sw}). In this step, the adjustment of the parameters has an influence on the reduce of the system. For example, the SOC operating range affects the volume and efficiency of the MMC and the batteries lifetime.

The MMC must be able to synthesize \hat{V}_s in the linear region of the modulator. The sum of the capacitor voltages (v_c^Σ) is calculated as a function of \hat{V}_s . This relationship depends on the topology and the modulation strategy used. In this way, the sum of the capacitor voltages of each arm when using the Sinusoidal Pulse Width Modulation (SPWM) is $2\hat{V}_s$. Another interesting approach that makes it possible to extend the linear region of the modulator is to consider 1/6 third harmonic injection (Ilves et al., 2014). Thus the sum of the capacitors, $v_c^\Sigma = \sqrt{3}\hat{V}_s$.

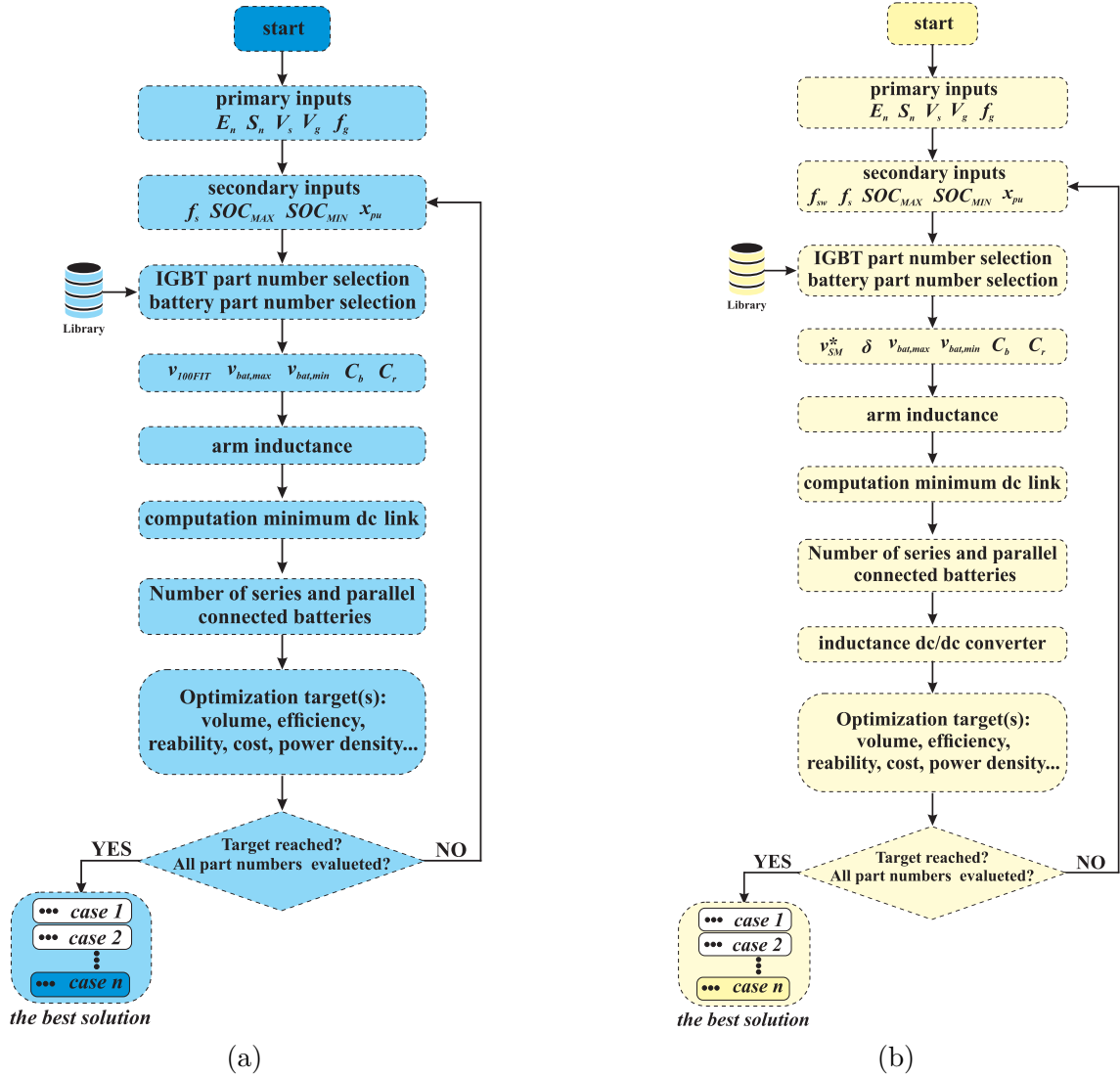


Figure 17 – Flowcharts to minimize MMC-based BESS projects: (a) single-stage approach configuration; (b) two-stage approach configuration.

In this chapter, the projects of capacitors, inductors, and number of batteries in series and parallel (including the effect of their rounding) are carried out. Regarding the variable to be optimized, this subject is addressed in Chapter 4. Finally, the results and analyzes of this optimization methodology are presented in Chapter 5.

2.3.1 Single-Stage MMC-based BESS

The SM for MMC-based BESS proposal for the single-stage approach topology is presented in Figure 18.

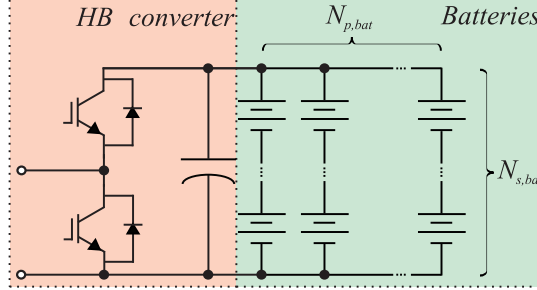


Figure 18 – Schematic of SM for single-stage approach MMC-based BESS topology.

The number of series battery strings ($N_{s,bat}$) can be calculated according to:

$$N_{s,bat} = \text{floor} \left(\frac{v_{SM}^*}{v_{bat,max}} \right), \quad (2.26)$$

where v_{SM}^* is the SM maximum voltage, the equivalent of blocking voltage of IGBT, V_{100FIT} ³. Besides that, $v_{bat,max}$ is the maximum battery voltage. The number of battery racks in series is computed using the *floor* function to avoid that the maximum battery rack voltage exceeds V_{100FIT} .

The number of SM, N , is computed by:

$$N = \text{ceil} \left(\frac{v_{dc,min}}{N_{s,bat} v_{bat,min}} \right), \quad (2.27)$$

where $v_{bat,min}$ minimum battery voltage, limited by the SOC_{min} . Under such conditions, at minimum voltage conditions the converter can connect to the grid and provide voltage \hat{V}_s .

The $N_{p,bat}$ ⁴ must fulfill two requirements. The first criterion computes the number of battery racks in parallel $N_{power,bat}$ to fulfill the MMC-based BESS rated power.

$$N_{power,bat} = \text{ceil} \left(\frac{P_n}{6N P_{bat,min}} \right), \quad (2.28)$$

where P_n is the nominal converter power and $P_{bat,min}$ is minimum battery rack power. The $P_{bat,min}$ can be estimated as follows:

³ FIT (Failure In Time) is a unit that represents failure rates and how many failures occur every 10^9 hours.

⁴ Note that in the previous section to deduce the temperature according to the battery current, the terms $N_{p,bat(SS)}$ and $N_{p,bat(TS)}$ were used to represent the number of parallel batteries in the single-stage and two-stage approaches, respectively. However, in the rest of the text, these variables will not be compared in the same calculation. Therefore, $N_{p,bat}$ will be used for the number of batteries in parallel both in the single-stage approach and in the two-stage approach. If there is a need to compare them again, the reader will be informed.

$$P_{b,min} = v_{bat,min} C_r C_n, \quad (2.29)$$

where C_r is the discharging rate and C_n is the battery capacity. The second criterion computes the number of batteries in parallel $N_{energy,bat}$ to fulfill the MMC-based BESS rated energy storage. Accordingly:

$$N_{energy,bat} = \text{ceil} \left[\frac{100E_R}{6E_{R,bat} N N_s (SOC_{max} - SOC_{min})} \right], \quad (2.30)$$

where E_R is nominal energy storage requirement, $E_{R,bat}$ is battery energy storage requirement, SOC_{max} is maximum allowed SOC and SOC_{min} is minimum allowed SOC. Finally, the number of parallel battery strings ($N_{p,bat}$) per SM is given by:

$$N_{p,bat} = \max(N_{power,bat}; N_{energy,bat}). \quad (2.31)$$

2.3.2 Two-Stage MMC-based BESS

Figure 19 shows the SM configuration of the two-stage approach. In this work, the dc/dc converter is the boost type when considering the energy flowing from the batteries to the dc-link of SM. As a consequence, the total voltage of the battery rack varies according to δ .

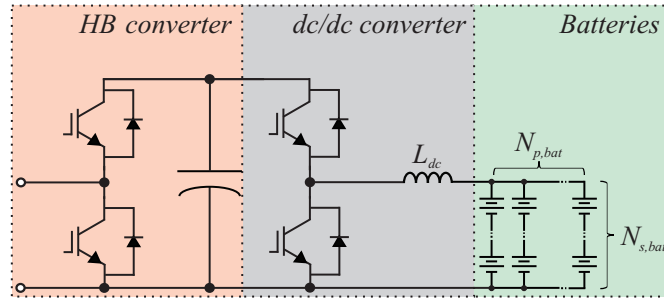


Figure 19 – Schematic of SM for two-stage approach MMC-based BESS topology.

Since the dc/dc converter decouples the batteries from SM, $N_{s,bat}$, expressed by:

$$N_{s,bat} = \text{floor} \left(\frac{v_{SM}^*}{v_{bat,max} \sigma} \right), \quad (2.32)$$

where v_{SM}^* is reference SM voltage must be higher than the battery voltage and lower than the power modules maximum voltage (recommended by the manufacturer)⁵.

The number of battery racks in series is computed using the *floor* function to avoid the maximum battery rack voltage exceeds v_{SM} . The number of SM N is computed by:

⁵ A margin may be adopted to guarantee an acceptable dynamic performance of the dc/dc converter control

$$N = \text{ceil} \left(\frac{v_{dc,min}}{v_{SM}^*} \right). \quad (2.33)$$

The Eq. (2.28)-(2.31) can be used to determine the number of batteries in parallel for the MMC with dc/dc topology.

2.3.3 Passive components

After developing the battery rack design, the next step is to perform calculations related to passive components, such as SM capacitance, inductance (arm and bidirectional boost converter), and semiconductors (IGBT and diodes).

The SM capacitance is defined as follows:

$$C = \frac{W_{conv} S_n}{3000N(v_{c,n})^2}, \quad (2.34)$$

where W_{conv} is the energy storage requirements given kJ/MVA. According to [Harnefors et al. \(2013\)](#) and [Cupertino et al. \(2018\)](#), 40 kJ/MVA guarantee a maximum capacitor voltage ripple of 10 %, which is typical for MMC. It should be noted that the cell capacitance dimensioning is performed considering that the system can operate as Static Synchronous Compensators (STATCOM) even if batteries are not available. According to ([Soong; Lehn, 2016](#)), in MMC-based BESS, shorter battery strings are preferable to increase system reliability. Therefore, it is concluded that in an MMC-based BESS up to 33% of the battery banks can be turned off without affecting the energy exchange of the MMC with the grid.

The L_{arm} aims to limit the high frequency components and perform a smooth control in the circulating current. Thus, the L_{arm} is expressed by:

$$L_{arm} = x_{arm} \frac{\hat{V}_g^2}{\omega S_n}, \quad (2.35)$$

where x_{arm} is the per unit value of arm reactance and ω is the grid angular frequency. According to [Sharifabadi et al. \(2016b\)](#), typical arm inductance values can vary in the range of 0.05 to 0.15 Per Unit (pu).

To determine the MMC semiconductor and inductor devices specifying the maximum arm current value is important, ([Cupertino et al., 2018](#)). As previously discussed, at balanced conditions, the circulating current can be neglected. Under such conditions, the maximum value of arm current is given by:

$$\max(i_{l,n}) = \max(i_{u,n}) = \frac{\max(i_g)}{2} = \frac{S_n}{\sqrt{6}\hat{V}_g}. \quad (2.36)$$

Also, the current **RMS** in semiconductor devices can be calculated as follows:

$$i_{SD,RMS} = \frac{\hat{I}_g}{4\sqrt{2}}, \quad (2.37)$$

note that the current stresses in semiconductor devices do not depend on the modulation index.

Finally, for the two-stage approach the minimum value L_{dc} for the converter to operate in continuous conduction mode can be express by:

$$L_{dc} = \frac{v_{bat,max}(v_{SM}^* - v_{bat,max})}{v_{SM}^* f_{sw} \Delta I_{bat}}, \quad (2.38)$$

where f_{sw} is the switching frequency of the dc/dc converter and ΔI_{bat} is the inductor (and battery) current ripple.

2.4 Design Optimization

After calculating the main circuit parameters, the next step is to optimize the designs for the one- and two-stage approaches. Depending on the application and the designer objective, some variables can be optimized, such as:

1. volume;
2. energy density;
3. lifetime of the battery and/or converter ;
4. operational costs;
5. losses/efficiency.

Solutions are presented in the literature to minimize some variables above. In (Hillers; Stojadinovic; Biela, 2015; Huber; Kolar, 2017), the authors found solutions to minimize the number of **SM**, considering the trade-off between energy conversion efficiency, passive component size, and transistor blocking voltages.

Indeed, the reference voltage v_{SM}^* has an important role in the reduce of **MMC**-based **BESS**, as illustrated in Figure 20. Thus, some considerations are highlighted:

- The minimum and maximum battery voltage range $[v_{bat,min}, v_{bat,max}]$ depend on the minimum and maximum allowed **SOC** adopted in the converter design, Figure 20 (a);

- For the adopted dc/dc converter topology, Figure 20 (b), the v_{SM}^* must be higher than the $v_{bat,max}$ and lower than the power modules maximum voltage (recommended by the manufacturer)⁶;
- SM power losses increase according to v_{SM}^* . This fact is justified by 2 factors:
 1. The increase in the switching losses with the blocking voltage;
 2. The increase of the dc/dc converter duty-cycle, which increases the conduction losses.
- For different SOC, the dc/dc converter duty-cycle is different. Therefore, the MMC global efficiency is a function of the converter mission profile;
- The value of v_{SM}^* affects the converter total cost.

The most suitable design will consider the SM voltage reference which minimizes the converter cost. A technical reference describing the reduce of MMC systems based on the SM voltage reference is still missing in the literature. Thus, this work aims to fill this gap. The next chapter discusses the methodology for finding the optimal value for v_{SM}^* .

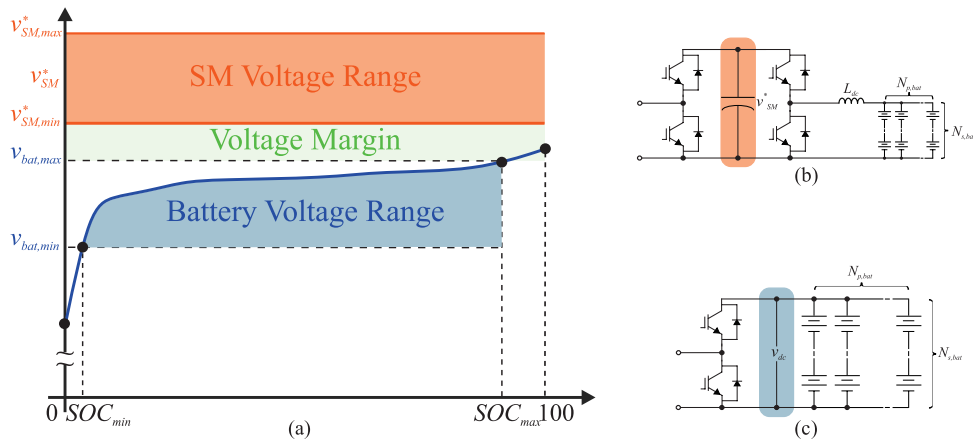


Figure 20 – Comparison of the SM reference voltage: (a) Operating intervals for approaches; (b) single-stage approach; (c) two-stage approach.

According to the flowchart in Figure 17, an iterative process calculates the most suitable design for the selected topology. The secondary inputs can be manipulated for reduce purposes. Different IGBT and battery part numbers can be evaluated.

2.4.1 Effects of rounding functions on BESS design

As discussed earlier, due to the use of *floor* and *ceil* rounding function in the MMC-based BESS sizing, the required nominal energy storage capability and the actual

⁶ A margin may be adopted to guarantee an acceptable dynamic performance of the dc/dc converter control.

energy storage capability can differ significantly. This difference can be measured through the energy oversizing, given by:

$$E_O = E_B - E_R, \quad (2.39)$$

where E_B is the total energy of the batteries. The magnitude of E_O is a function of the design ratings and the battery rack characteristics. This work investigates standard and customized solutions.

Standard solution is sized with commercially available battery rack. These battery rack have high values of voltage, energy storage, and Ah-capacity. On the other hand, the customized solution uses the battery cell to carry out the project, with lower voltages, energy, and capacity.

Two battery racks were selected in order to exemplify the consequences of rounding in the sizing for the single and two-stage approaches. For the standard case study, a battery rack was chosen, and for the customized alternative, a battery cell is adopted. Table 3 presents the parameters of battery rack and battery cell needed to carry out this study.

Table 3 – Parameters of the battery rack P3-R070 ([Samsung, 2018](#)) and the battery cell A123 26650 ([A123 Systems, 2012](#)).

Parameters	Standard	Customized
Total energy storage [E_R]	70 kWh	7.6 Wh
Power capacity [C_n]	78 Ah	2.5 Ah
C-Rate [1/h]	3	1
Maximum voltage [SOC = 100 %]	992 V	3.4 V
Minimum voltage [SOC = 0 %]	750 V	2.5 V

According to the parameters defined for the batteries, BESS sizing is carried out considering different values of grid voltage (11 kV to 69 kV) and energy requirements (1 MWh to 100 MWh). In order to exemplify the behavior of the system, IGBT blocking voltage 4.5 kV is used for the single-stage and two-stage approach. In addition, the dc-link voltage on the SM used for the tests is 2.25 kV. Note that these values are just for example, they are not necessarily the best options for the single-stage and two-stage approaches.

Figure 21 presents an analysis of energy oversizing for different voltage and energy required values. Figure 21 (a) the values for the standard solution. Note that projects with less energy oversizing are shown diagonally in the darkest color. For the selected case study, the energy oversizing is approximately 50%. On the other hand, in the customized solution, shown in Figure 21 (b), note that more areas have less energy oversizing. Furthermore, the range of energy oversizing in the standard solution is up to 30 times higher than in the customized solution.

Figure 22 (a) and Figure 22 (b) analyze the energy oversizing for the two-stage approach in the customized and standard solution, respectively. In the two-stage approach,

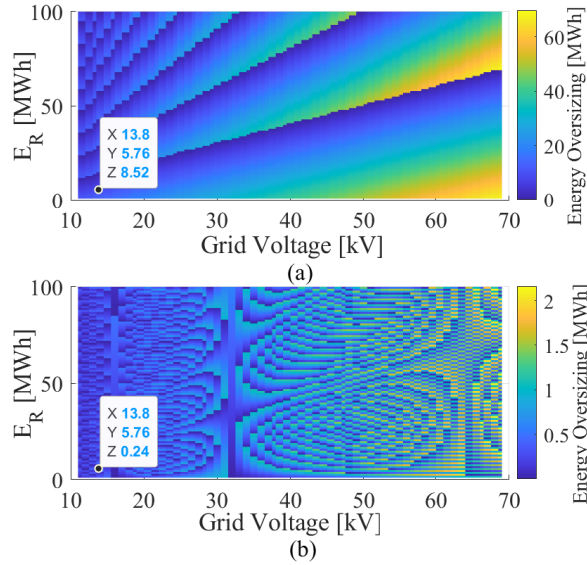


Figure 21 – Energy oversizing map for IGBT blocking voltage 4.5 kV for (a) single-stage approach standard solution (b) single-stage approach customized solution.

the dc/dc converter adds a degree of freedom which makes the magnitude of energy oversizing decrease compared to the single-stage approach. Also, in Figure 22 (b) there are more regions with less energy oversizing. Finally, the highlighted points in Figure 21 and Figure 22 refer to the case study that will be discussed in the next sections. Note that the chosen parameters E_R and mains voltage do not lead to designs optimized for the standard solution.

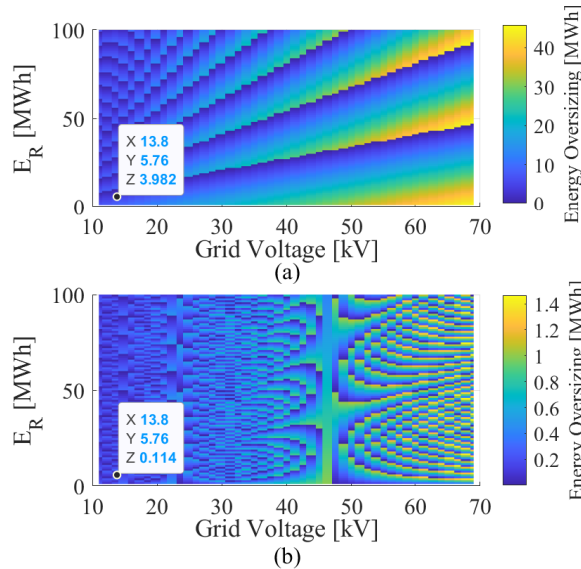


Figure 22 – Energy oversizing map for IGBT blocking voltage 4.5 kV for (a) two-stage approach standard (b) two-stage approach customized.

Figure 23 selects the designs from Figure 21 that have a maximum of 10% energy oversizing. In the standard solution shown in Figure 23 (a), note that the point selected in Figure 21 (a) is not within the applied limit. As for the customized solution shown in

Figure 23 (b) it shows that the point selected in Figure 21 (b) is within the stipulated 10% limit.

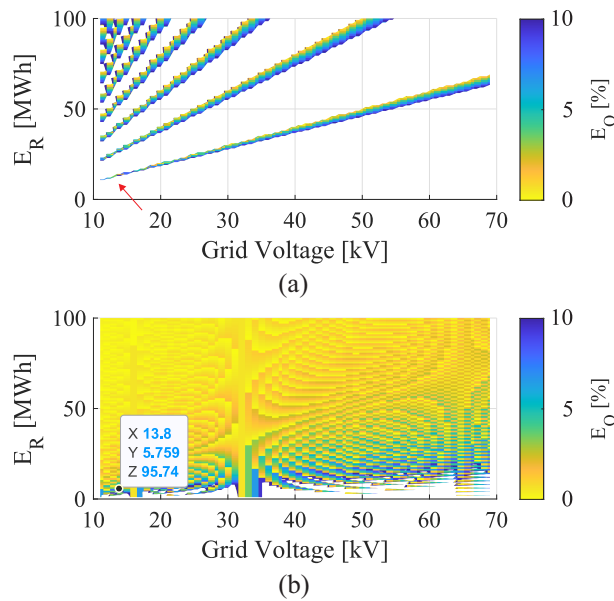


Figure 23 – Selection of optimal designs with up to 10% energy oversizing to IGBT of 4.5 kV blocking voltage for single-stage approach (a) standard solution (b) customized solution.

Figure 24 (a) presents the projects selected for the two-stage approach in the standard solution. Note that the project selected in Figure 22 is not contained within the established limit. Considering the two-stage approach customized solution presented in Figure 24 (b) the projects contemplate the desired value closer to 100%. However, in the same way as in Figure 23 (b), for low values of required energy, few projects are selected.

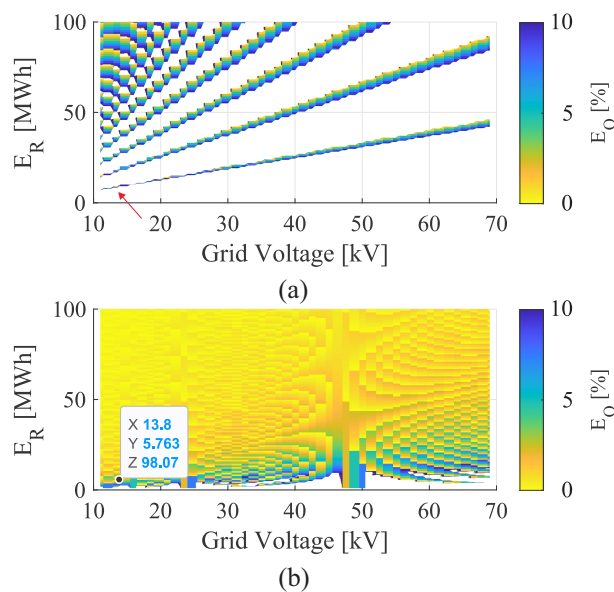


Figure 24 – Selection of optimal designs with up to 10% energy oversizing to IGBT of 4.5 kV blocking voltage for two-stage approach (a) standard solution (b) customized solution.

As noted, battery characteristics play an important role in the design. For a standard solution, the designs are more limited due to the size of the racks. As a consequence, in some designs, the energy oversizing can be double the energy required. On the other hand, in the customized solution, the rack sizes are smaller, allowing for lower energy oversizing due to rounding.

In the following chapters, the consequences of using a system with greater energy oversizing, as in the standard solution, or systems with less energy oversizing as in the customized solution, will be evaluated. In this analysis, the costs per project and the lifetime of the batteries are evaluated.

2.5 Conclusions

In this chapter, the mathematical model for the MMC-based BESS and the design calculations for the single-stage and two-stage approaches are presented. In addition, a flowchart to assist in project optimization is presented. Several variables can influence project reduce, including energy oversizing. Chapter 3 the MMC-based BESS control strategy for the single-stage and two-stage approaches. Finally, the methodology used for control tuning is discussed.

3 Control Strategies and tuning for MMC-based BESS

This chapter is divided into two parts: the first part presents the control strategy for the MMC-based BESS in the single-stage and two-stage approaches. Next, the methodology to calculate the gains related to the controllers is discussed.

3.1 MMC-based BESS control strategy

The control strategy used in MMC-based BESS, shown in Figure 25, can be divided as follows: grid current control, SOC balancing control, circulating current control and dc/dc converter control (for two-stage approach).

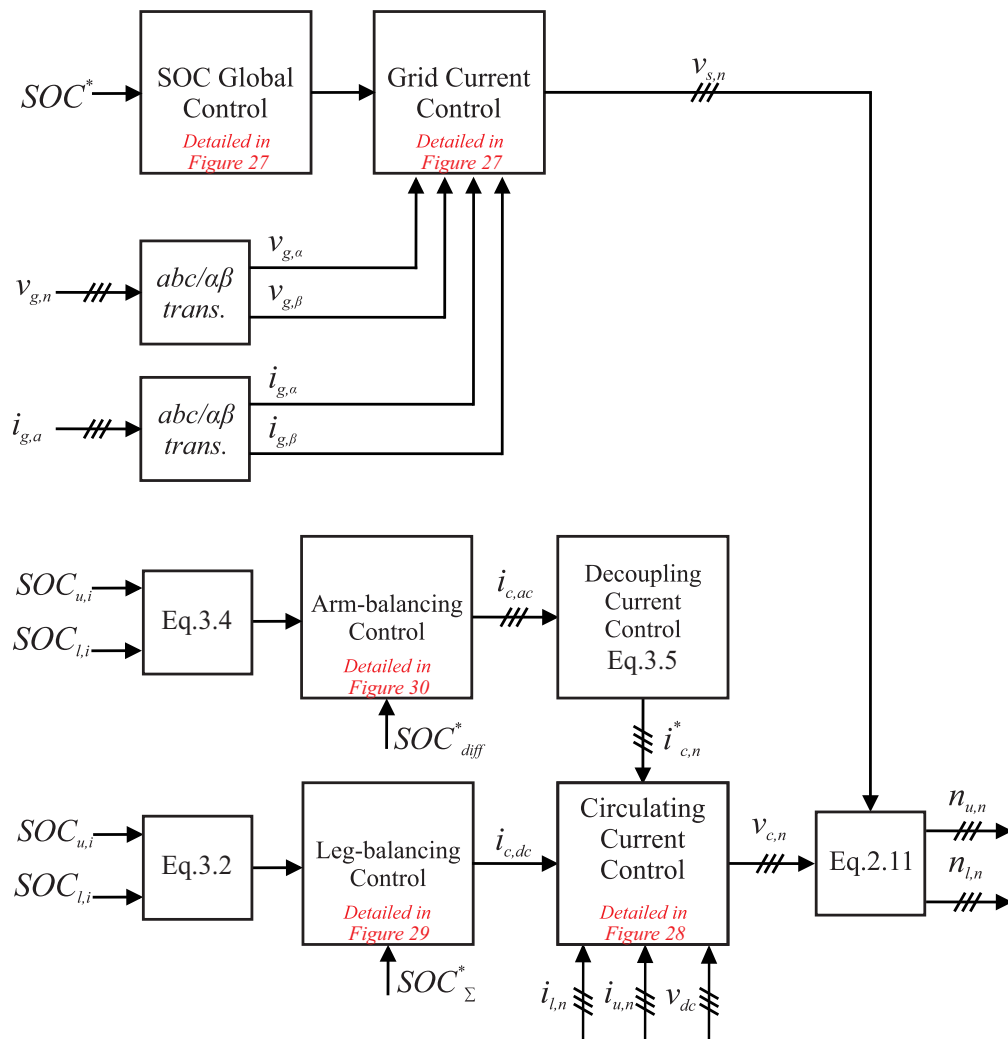


Figure 25 – Overview of the MMC-based BESS control strategy.

Figure 25 shows the complete control strategy of a MMC-based BESS. The grid current control is implemented in stationary reference frame ($\alpha\beta$) coordinates (Sharifabadi et al., 2016b). Proportional Resonant (PR) controllers are used to control the active power exchange with the grid.

The active power reference, in grid current control, depends on the operating status of MMC topology. In the process of charging or discharging the batteries, the reference is derived from the global SOC control. Therefore, P_{ref} is obtained based on the Proportional-Integral (PI) controller. On the other hand, in the case of an external power reference, the current reference is computed by:

$$i_g^* = \frac{2}{3} \frac{P_{ref}}{\widehat{V}_g^2} v_g(t), \quad (3.1)$$

where \widehat{V}_g is the peak of the line-to-neutral voltage.

The leg-balancing control guarantees that all converter phases present the same average SOC. The average SOC of each phase n is computed by the:

$$SOC_{\Sigma,n} = \frac{1}{2N} \left(\sum_{i=1}^N SOC_{u,i} + \sum_{i=1}^N SOC_{l,i} \right), \quad (3.2)$$

where $SOC_{u,i}$ are the SOC of i -th SM battery rack in upper arm of phase n and $SOC_{l,i}$ is the SOC of i -th SM battery rack in lower arm of phase n . The SOC reference in leg-balancing control is computed by the average SOC among the converter phases:

$$SOC_{\Sigma}^* = \frac{1}{3} \sum_{n=1}^3 SOC_{\Sigma,n}. \quad (3.3)$$

The leg-balancing controller computes the dc circulating current component responsible for the exchange of energy among the converter phases. Therefore, it ensures that all legs have the same average SOC.

For the arm-balancing control, the average SOC balancing in the upper and the lower arms is performed. The SOC difference in each converter phase, ($SOC_{diff,n}$), is computed through proportional controller. The $SOC_{diff,n}$ is expressed as follows:

$$SOC_{diff,n} = \frac{1}{N} \left(\sum_{i=1}^N SOC_{u,i} - \sum_{i=1}^N SOC_{l,i} \right). \quad (3.4)$$

In the arm-balancing control, the SOC_{diff}^* is set to zero, to guarantee a SOC balancing in arms of each phase. This controller computes the fundamental frequency circulating current responsible for energy exchange among the upper and lower arms. Since the leg-balancing control (or horizontal balancing) and arm-balancing control (or vertical

balancing) compute different components of circulating current, these controllers can have a similar bandwidth. The arm energy control can be designed with a bandwidth similar to the leg energy control (Soong; Lehn, 2014b).

The circulating current of one phase must be the linear combination of the other two. This work uses the decoupling network discussed in (Tsolaridis et al., 2017). This proposal injects active current in the unbalanced phase and reactive current in the balanced phases. Thus, the averages of the SOC are not displaced and the difference in average energy is not affected.

Consider the following example: if phase A has an SOC error ($e_a \neq 0$) the SOC error in phases B and C are zero ($e_b = 0$ and $e_c = 0$), a fundamental frequency component in phase with the grid voltage must circulate in phase A, to guarantee active power exchange. On the other hand, the fundamental frequency circulating currents are selected to be 90 degrees lead (or lag) to the grid voltage. Phases B and C led to now active power exchange. It is important to remark that the sum of the circulating currents will be zero if the amplitude of the circulating currents is properly computed. In this way, the circulating current references computed by the arm balancing control are given by:

$$\begin{cases} i_{c,a}^* = k_{P,A} \left[e_a \cos(\omega t) + \frac{1}{\sqrt{3}} e_b \cos\left(\omega t + \frac{\pi}{2}\right) + \frac{1}{\sqrt{3}} e_c \cos\left(\omega t - \frac{\pi}{2}\right) \right], \\ i_{c,b}^* = k_{P,A} \left[e_b \cos\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{\sqrt{3}} e_a \cos\left(\omega t - \frac{7\pi}{6}\right) + \frac{1}{\sqrt{3}} e_c \cos\left(\omega t - \frac{\pi}{6}\right) \right], \\ i_{c,c}^* = k_{P,A} \left[e_c \cos\left(\omega t + \frac{2\pi}{3}\right) + \frac{1}{\sqrt{3}} e_a \cos\left(\omega t + \frac{7\pi}{6}\right) + \frac{1}{\sqrt{3}} e_b \cos\left(\omega t + \frac{\pi}{6}\right) \right]. \end{cases} \quad (3.5)$$

where $k_{P,A}$ is the proportional gain of arm balancing control and ω is the fundamental angular frequency obtained by Phase-Locked Loop (PLL).

It is important to remark that the global SOC control and the leg-balancing control do not operate at the same time. When the MMC-based BESS is operating in the charging/discharging mode, global SOC control computes the current reference of each phase, which leads to a balance of the average SOC of the three-phases. Under such conditions, the leg-balancing control is disabled. However, when the MMC-based BESS is providing ancillary services, the global SOC balancing control is disabled. Under such conditions, the leg-balancing control is enabled and the leg-balancing control is obtained based on a dc circulating current.

The insertion index is applied in the modulation strategy. Regarding the modulation strategy, the Phase-Shifted Pulse Width Modulation (PS-PWM) is employed. For PS-PWM method, an extra individual balancing control loop, presented in Figure 25, is necessary to reach the overall balancing in each converter arm (Hagiwara; Akagi, 2009). The injection of 1/6 of the third harmonic is considered to extend the linear region of the modulator.

Based on the parameters presented, the next section discusses the control strategy and the methodology for control tuning.

3.2 Control Tuning

The main control objectives of MMC-based BESS are: each objective is reached through different control loops aforementioned. In this section, the control tuning is presented. Thus, the strategies for the respective controllers are discussed and their respective results are presented.

In order to validate the methodology for control tuning, after each control, the analysis of the frequency and step response is performed. It is worth mentioning that all controllers were discretized by the Tustin method (trapezoidal). Also, the delay of digital implementation is included in the model.

Finally, the gains for all controllers were calculated neglecting the sensor gains. This inherently assumes that, in practice, the sensor presents a higher bandwidth than the control loop requirements.

3.2.1 Grid Current

Figure 26 shows the block diagram with closed control loop for the grid current control.

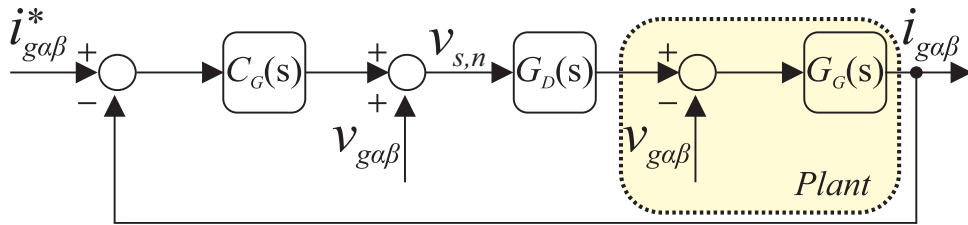


Figure 26 – Block diagram for the strategy for controlling the grid current.

In this system a PR controller is used. Then, the transfer function $C_G(s)$ is given by:

$$C_G(s) = k_{P,G} + \frac{k_{R,G}s}{s^2 + \omega_n^2}, \quad (3.6)$$

where $k_{P,G}$ is the proportional gain and $k_{R,G}$ the resonant gain. In this control loop, the resonance frequency is the grid frequency. The effect of the implementation delay and the zero-order hold can be represented by the following transfer function, (Yao et al., 2017):

$$G_D(s) = \frac{1 - e^{-T_{sw}}}{T_{sw}s} e^{-T_{sw}} \approx \frac{1}{1.5T_{sw}s + 1}, \quad (3.7)$$

where T_{sw} is the sampling time. Finally, the plant grid current transfer function $G_G(s)$ can be represented by:

$$G_G(s) = \frac{I_s}{V_s} = \frac{1}{sL_{eq} + R_{eq}}, \quad (3.8)$$

where $R_{eq} = \frac{R_{arm}}{2}$ and $L_{eq} = \frac{L_{arm}}{2}$.

The open-loop transfer function for the grid current control can be written as follows:

$$G_{G(OL)}(s) = \left(k_{P,G} + \frac{k_{R,G}s}{s^2 + \omega_n^2} \right) \left(\frac{1}{1.5T_{sw}s + 1} \right) \left(\frac{1}{sL_{eq} + R_{eq}} \right). \quad (3.9)$$

The control tuning of the current loop follows the methodology discussed in (Sharifabadi et al., 2016b). The objective is to maximize the current control bandwidth. Based on this methodology, the following tuning formulas are obtained:

$$\begin{cases} k_{P,G} = \alpha_{gc}L_{eq}, \\ k_{R,G} = 2\alpha_{hg}k_{P,G}, \end{cases} \quad (3.10)$$

where α_{hg} is resonant part bandwidth and α_{gc} is the desired closed-loop-system bandwidth. Thus, there is a upper limit to α_{gc} for the closed-loop system to remain stable with sufficiently large. In this work, consider α_{hg} at least $\frac{1}{10}$ of the grid frequency. In order to simplify the closed loop transfer function, consider $\alpha_{hg} \ll \alpha_{gc}$. In this work, $\alpha_{gc} = \frac{1}{20T_{sw}}$.

The $k_{P,G}$ gain is obtained considering the transfer function of Eq. (3.8) in a closed-loop with a pure proportional gain. According to (Sharifabadi et al., 2016b), the bandwidth of the closed-loop system is an important parameter. From it determines the exponential convergence rate for transients of the closed-loop system. The gain $k_{R,G}$ is the product of angular frequency and impedance, or equivalently, angular frequency squared times inductance.

3.2.2 Global SOC Control

The plant transfer function can be obtained by neglecting the converter losses and assuming an even distribution of the energy among the converter cells. Under such conditions, the following expression can be obtained for the battery current:

$$i_{bat} = \frac{\hat{V}}{\underbrace{4NN_sN_p v_{bat}}_{K_s}} \hat{I}_g, \quad (3.11)$$

where \hat{V} is the peak of output voltage of the SM, v_{bat} is battery voltage, \hat{I}_g is the peak of the converter output current, N_s and N_p are the number of series and parallel battery strings, respectively.

In addition, the battery SOC can be obtained as:

$$SOC(s) = SOC(0) + \frac{i_{bat}}{C_n s}. \quad (3.12)$$

where C_n is the battery capacity.

Therefore, substituting Eq. (3.11) in Eq. (3.12) obtains the following relationship:

$$\frac{SOC(s)}{\hat{I}_g(s)} = \frac{K_S}{s}, \quad (3.13)$$

In this system a PI controller is used. Then, the transfer function $C_S(s)$ is given by:

$$C_S(s) = K_{P,S} + \frac{K_{I,S}}{s}. \quad (3.14)$$

The block diagram of the SOC global control is presented in Figure 27.

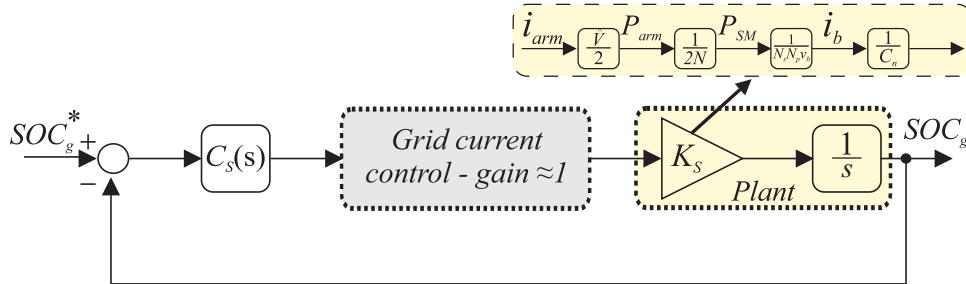


Figure 27 – Block diagram of the global SOC control.

The open-loop transfer function is given by:

$$G_{s(OL)}(s) = \left(k_{P,S} + \frac{k_{I,S}}{s} \right) \left(\frac{K_s}{s} \right). \quad (3.15)$$

The closed-loop transfer function can be written as follows:

$$G_{s(CL)}(s) = \frac{K_s k_{P,S} s + K_s k_{I,S}}{s^2 + K_s k_{P,S} s + K_s k_{I,S}}. \quad (3.16)$$

Note that Eq. (3.16) is equivalent to the following expression:

$$G_{s(CL)}(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}. \quad (3.17)$$

The tuning of the controllers is carried out by the poles placement method. This proposal, discussed in (Cupertino, 2015), defines the gains for the poles of the transfer

function in closed-loop to be real and allocated in the left semi plane. Considering the closed loop poles as p_1 and p_2 . Also, assume that $p_1 = -2\pi f_{c1,s}$ and $p_2 = -2\pi f_{c2,s}$. Soon:

$$\begin{cases} -2\pi f_{c1,s} - 2\pi f_{c2,s} = -\frac{K_s k_{P,S}}{1}, \\ (-2\pi f_{c1,s})(-2\pi f_{c2,s}) = \frac{K_s k_{I,S}}{1}. \end{cases} \quad (3.18)$$

Thus, the following tuning formulas are obtained:

$$\begin{cases} k_{P,S} = \frac{2\pi (f_{c1,s} + f_{c2,s})}{K_S}, \\ k_{I,S} = \frac{4\pi^2 f_{c1,s} f_{c2,s}}{K_S}, \end{cases} \quad (3.19)$$

where $f_{c1,s}$ and $f_{c2,s}$ are the poles of the closed-loop transfer function. Typically, the poles are separated by a decade. In addition, the value of the largest of them must be allocated at least a decade below the cutoff frequency of the grid current. In this way, it guarantees the proper functioning of the cascade control.

3.2.3 Circulating current control

The circulating current control block diagram is presented in Figure 28. In this control project $C_C(s)$ is the PR controller, represented by:

$$C_C(s) = k_{P,C} + \left(\frac{k_{R,C}s}{s^2 + \omega_n^2} + \frac{k_{R,C}s}{s^2 + (2\omega_n)^2} + \frac{k_{R,C}s}{s^2 + (4\omega_n)^2} \right), \quad (3.20)$$

where $k_{P,C}$ and $k_{R,C}$ refer to the proportional and resonant gains of the circulating current controller.

The plant transfer function of the circulating current controller $G_C(s)$ is given by:

$$G_C(s) = \frac{i_g}{v_c} = \frac{1}{sL_{arm} + R_{arm}}, \quad (3.21)$$

According subsection 3.2.1, the gains of the PR controller can be calculated according to the formula:

$$\begin{cases} k_{P,C} = \alpha_{cc} L_{arm}, \\ k_{R,C} = 2\alpha_{hc} k_{P,C}, \end{cases} \quad (3.22)$$

where α_{hc} is resonant part bandwidth and α_{cc} is the desired closed-loop-system bandwidth. Consider α_{hc} at least $\frac{1}{10}$ of the grid frequency. In order to simplify the closed loop transfer function, consider $\alpha_{hc} \ll \alpha_{cc}$. In this work, $\alpha_{cc} = \frac{1}{20T_{sw}}$.

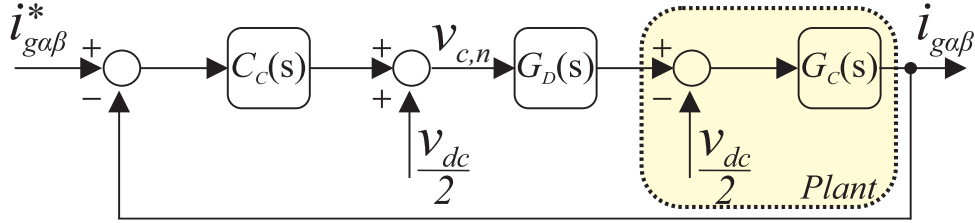


Figure 28 – Block diagram of the circulating current control.

3.2.4 Leg - Balancing Control

In order to obtain the system transfer function, the converter losses are disregarded and uniform energy distribution is assumed between the converter cells. With this, the dc portion of the current in the battery can be calculated as follows.

$$i_{bat} = \frac{\hat{V}_s}{2NN_sN_p v_{bat}} \hat{I}_g, \quad (3.23)$$

In addition, the battery SOC can be obtained as:

$$SOC(s) = SOC(0) + \frac{i_{bat}}{C_n s}. \quad (3.24)$$

Therefore, the following transfer function is obtained:

$$\frac{SOC(s)}{I_{c,dc}(s)} = \frac{K_L}{s}, \quad (3.25)$$

where $I_{c,dc}$ is the dc component of the peak current and K_L is given by:

$$K_L(s) = \frac{\hat{V}_s}{2Nv_{bat}N_sN_pC_n}. \quad (3.26)$$

In this system a PI controller is used. Then, the transfer function $C_L(s)$, is given by:

$$C_L(s) = K_{P,L} + \frac{K_{I,L}}{s}. \quad (3.27)$$

The block diagram of the leg-balancing control is presented in Figure 29. The open-loop transfer function is given by:

$$\frac{SOC(s)}{I_{c,ac}(s)} = \frac{K_A}{s}, \quad (3.32)$$

where K_A is given by:

$$K_A(s) = \frac{\hat{V}}{2Nv_{bat}N_sN_pC_n}. \quad (3.33)$$

In this system a proportional gain is used. Then, the transfer function $C_A(s)$ is given by:

$$C_A = K_{P,A} \quad (3.34)$$

The block diagram of the arm-balancing control is presented in Figure 30. The open-loop transfer function is given by:

$$G_{a(OL)}(s) = (K_{P,A}) \left(\frac{K_A}{s} \right). \quad (3.35)$$

The closed-loop transfer function is represented by:

$$G_{a(CL)}(s) = \frac{K_A K_{P,A}}{s + K_A K_{P,A}}. \quad (3.36)$$

Analyzing $G_{a(CL)}(s)$, the closed-loop poles must be located in the left semi plane for the system to be stable, (Cupertino, 2015). In effect, the gain to adjust the proportional controller can be calculated as follows:

$$k_{P,A} = \frac{2\pi f_{c,A}}{K_A}, \quad (3.37)$$

where $f_{c,A}$ is the location of the closed-loop pole. Thus, Figure 30 represents the block diagram for arm - balancing control.

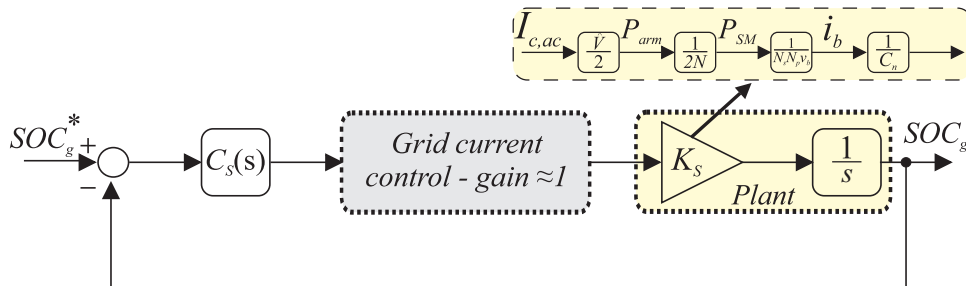


Figure 30 – Block diagram for arm-balancing control.

3.2.6 Individual SOC Balancing Control

The block diagram of the individual SOC balancing control is presented in Figure 31. The individual SOC balancing control aims to reduce the difference between the reference SOC and the i th SOC converter SM. Consider ΔSOC the difference between the average value of the SOC in an arm and the value of the SOC^* in the n th cell of the converter in the respective arm.

$$\Delta SOC = SOC^* - SOC \quad (3.38)$$

The value of ΔSOC can decrease in the process of charging and discharging the battery in the SM batteries of a given arm. For this process to take place properly, an ac-voltage is superimposed to minimize the difference. The voltage v_{bat} can be calculated as follows:

$$v_{bat} = K_{b,i} \Delta SOC \sin(\omega t) \quad (3.39)$$

where $K_{b,i}$ is a proportional gain. Note that the expression considers phase A. However, for the other phases it can be applied without loss of generality.

The active power required to perform SOC balancing in an SM is given by:

$$p_{bat} = v_{bat} \frac{\hat{I}_s}{4} - D_i \quad (3.40)$$

where D_i represents a loss or a disturbance in the converter cell. An active power, p_{bat} , is extracted or released from the SM in order to vary the SOC so that $\Delta SOC = 0$.

$$\Delta SOC \approx -\frac{1}{v_{bat} N_s N_p C_n} \int p_{bat} dt \quad (3.41)$$

$C_{ib}(s)$ is a proportional controller. Furthermore, the plant transfer function of the individual SOC balancing control G_{ib} is given by:

$$G_{ib} = \left(\frac{1}{v_{bat} N_s N_p C_n} \right) \left(\frac{1}{s} \right). \quad (3.42)$$

Therefore, the closed loop transfer function can be obtained as follows:

$$\frac{\Delta SOC(s)}{D_i(s)} = \frac{1}{s v_{bat} N_s N_p C_n + K_{i,b} \frac{\hat{I}_s}{4}} \quad (3.43)$$

Finally, the transfer function has the function of rejecting disturbances. In fact, the project uses the dynamic stiffness method. Therefore, the proportional gain can be calculated as follows.

$$K_{I,B} = \frac{8\pi f_{c,b} C_n}{\hat{I}_s} \quad (3.44)$$

where $f_{c,b}$ is the location of the closed-loop pole.

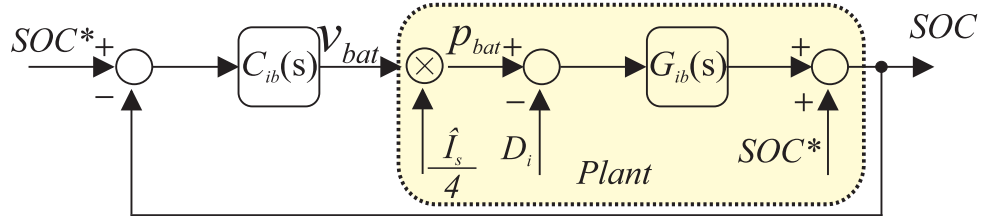


Figure 31 – Block diagram for individual SOC balancing control.

3.2.7 Dc/dc Control

The control strategy used for the dc/dc converter is an internal current loop and an external voltage loop. Figure 32 shows the block diagram of the complete control of the dc/dc converter.

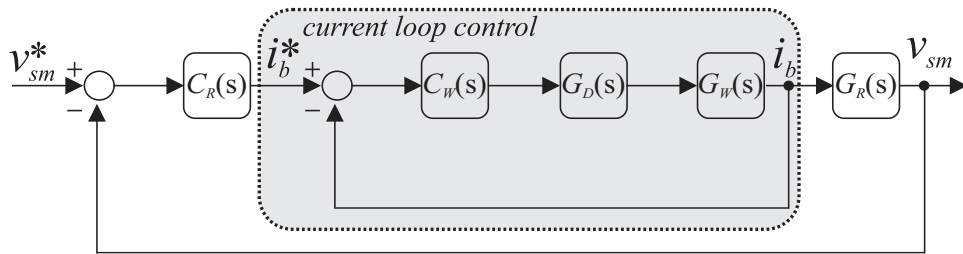


Figure 32 – Block diagram of the dc/dc converter control.

Initially, in the internal current loop, $C_W(s)$ represents the PI represented by:

$$C_W(s) = k_{P,W} + \frac{k_{I,W}}{s}, \quad (3.45)$$

where $k_{P,W}$, $k_{I,W}$ are the proportional and integral, respectively. The plant function of the dc/dc converter $G_W(s)$ is given by:

$$G_W(s) = \frac{i_b}{\delta} = \frac{1}{L_{dc}s + R_L}. \quad (3.46)$$

where L_{dc} and R_L are the inductance and resistance of dc/dc converter, respectively.

Thus, the open-loop transfer function for controlling the current of the dc/dc converter can be represented by:

$$G_{W(OL)}(s) = \left(k_{P,W} + \frac{k_{I,W}}{s} \right) \left(\frac{1}{1.5T_{sw}s + 1} \right) \left(\frac{1}{L_{dc}s + R_L} \right). \quad (3.47)$$

The gains are adjusted so that the closed-loop poles are allocated to the left semi plane, (Cupertino, 2015). In this way, the earnings of the PI are adjusted as follows:

$$\begin{cases} k_{P,W} = 2\pi f_i L_{dc}, \\ k_{I,W} = 2\pi f_i R_L. \end{cases} \quad (3.48)$$

where f_i is the frequency relative closed-loop pole.

To determine the voltage on the SM capacitor, assume that the power in the SM is equal to the power supplied by the batteries. With that, the following relationship is obtained:

$$i_{SM} = \frac{i_b v_{bat} N_s}{v_{SM}}, \quad (3.49)$$

where i_{SM} is the SM current.

Therefore, the gain K_k is given by:

$$K_k = \frac{v_{bat} N_s}{v_{SM}} \quad (3.50)$$

In voltage control, the bandwidth must be lower than current loop. Indeed, $C_R(s)$ is the transfer function of the PI controller:

$$C_R(s) = k_{P,R} + \frac{k_{I,R}}{s} \quad (3.51)$$

where $k_{P,R}$ and $k_{I,R}$ are the proportional and integral gains of the dc/dc converter voltage control. $G_R(s)$ is the plant transfer function.

$$G_R(s) = \frac{1}{sC}. \quad (3.52)$$

Furthermore, to attenuate the ripples in the capacitor voltages, a filtering technique is employed. A Moving Average Filter (MAF) with the 2/120 window is used. However, as the voltage control poles are allocated below the cutoff frequency of the MAF, it can be disregarded.

The dynamics of current control are faster than that of voltage control. In effect, the gain applied to the current loop is 1. Thus, the open-loop transfer function for the voltage control of the dc/dc converter can be expressed by:

$$G_{R(OL)}(s) = \left(k_{P,R} + \frac{k_{I,R}}{s} \right) \left(\frac{v_{bat} N_s}{v_{SM} C s} \right). \quad (3.53)$$

Finally, the tuning of the controllers can be done by applying the following formula:

$$\begin{cases} k_{P,R} = \frac{2\pi (f_{c1,d} + f_{c2,d})}{K_k}, \\ k_{I,R} = \frac{4\pi^2 f_{c1,d} f_{c2,d}}{K_k}, \end{cases} \quad (3.54)$$

where $f_{c1,d}$ and $f_{c2,d}$ are the closed-loop poles. These poles must be allocated at least 1 decade below the passband of the current control. In addition, they must be allocated 1 decade below the **MAF**.

Note that the gains for all controllers were calculated disregarding the sensor gains. In practical development, it is important to consider these gains so that the **MMC-based BESS** works as in the simulations.

3.3 Conclusion

This chapter presents the control strategy for the **MMC-based BESS**. Basically, the strategies for the single-stage and two-stage approaches are similar. The difference between the controls is the addition of the dc/dc converter control in the two-stage approach. The methodology used to calculate controller gains is based on poles placement. In a system with many control loops, this strategy makes it possible to minimize interference between the loops. Among the control loops discussed, an approach to be highlighted is the use of independent control of the energy levels of each arm. The decoupling of the system allows a better balance of the **SOC** between the arms. Finally, in Chapter 4, presents the methodologies used to obtain the costs related to each project. Among these techniques are the calculation of power losses and battery lifetime. In addition, the case study proposed for this work is presented.

4 Cost-oriented Design Methodology

As seen in the previous chapter, some design parameters for single and two-stage approaches can be used for optimization purposes. This section presents the cost-optimization methodology of MMC-based BESS for both single-stage and two-stage approaches. The total costs composed of two parts: Capital Expenditure (CAPEX) and Operational Expenditure (OPEX). The first one is related to the system expenditures (e.g. batteries, semiconductors, capacitors, and inductors). On the other hand, OPEX is the sum of two parts: Operational Expenditure-Losses Cost (OPEX_L) is associated with power losses and Operational Expenditure-Replacement Cost (OPEX_R) is associated with battery replacement over time. Finally, this chapter presents the case study, which is based on a BESS which provides peak-shaving for an industrial plant.

4.1 Power Losses Evaluation Methodology

The MMC has advantages when compared to two and three-level topologies, including the possibility of providing a substantial increase in output voltage with a low switching frequency. In fact, the switching frequency is an important factor for the design of the MMC topology, as it can affect power losses and efficiency of the converter (Cupertino et al., 2019).

The power losses in semiconductor devices are divided into conduction (P_{cond}) and switching losses (P_{sw}). P_{cond} occurs when the semiconductor device is in full conduction. In this case, the current flowing through the semiconductor is that required by the circuit and the voltage at the terminals is the voltage drop of the device itself. In this way, it can be concluded that P_{cond} has a direct relationship with the duty cycle of the converter (Jones; Davidson, 2013).

P_{sw} occurs when the semiconductor device is changing state: blocking to conduction or conduction to blocking. At this moment, energy dissipation occurs at each transition. In the case of the IGBT modules, the losses are related to the IGBT and the anti-parallel diode. In addition to P_{cond} and P_{sw} , other losses are observed in the passive elements of the converter, i.e., capacitors and inductors. Some variables can compensate for others, causing total losses to decrease. For example, the decrease in the amount of SM can compensate for the number of IGBT. Therefore, the methodology for obtaining losses for the MMC approach based on BESS is one of the important steps in this work.

4.1.1 Losses Estimations

The power losses estimation is computed by the PLECS and MATLAB/Simulink. PLECS is used to obtain the look-up tables of power losses. On the other hand, MATLAB/Simulink is used to simulate the one-year mission profile and compute the total losses.

The power losses estimation is based on the following assumptions:

- The losses are evenly distributed throughout the SM;
- The closed-loop control ensures that the SM voltage is controlled to v_{SM}^* ;
- The effect of the arm inductor current ripple in the power losses is negligible;
- The losses in the capacitors were neglected;
- The magnetic losses (in the core) of the inductors were neglected.

4.1.2 Look-up Table Generation

The following components are considered in the power losses estimation:

1. single-stage approach
 - a) semiconductor devices losses of the Half-Bridge Converter (HB);
 - b) ohmic losses in the arm inductors.
2. two-stage approach
 - a) semiconductor devices losses of the SM;
 - b) ohmic losses in the arm inductors;
 - c) ohmic losses in the dc/dc converter.

The MMC output current is given by:

$$i_g = \hat{I}_g \cos(\omega t - \phi), \quad (4.1)$$

where \hat{I}_g is the output current amplitude and ϕ is the current angle. Thus, \hat{I}_g can be expressed as follows:

$$\hat{I}_g = \frac{\sqrt{2(P_{ref}^2 + Q_{ref}^2)}}{\hat{V}_g \sqrt{3}}, \quad (4.2)$$

where P_{ref} and Q_{ref} are active and reactive power references, respectively.

The MMC output voltage v_s which drives i_g can be expressed as (Mendonça et al., 2020):

$$v_s = \widehat{V}_s \cos(\omega t + \delta), \quad (4.3)$$

where \widehat{V}_s and δ are the amplitude and phase of the output voltage. These variables can be expressed by:

$$\begin{cases} \widehat{V}_s = \sqrt{\left[\widehat{V}_g (1 + \Delta V_g) + \omega L_{eq} \widehat{I}_g \sin(\phi)\right]^2 + \left[\omega L_{eq} \widehat{I}_g \cos(\phi)\right]^2}, \\ \delta = \tan^{-1} \left(\frac{\omega L_{eq} \widehat{I}_g \cos(\phi)}{\widehat{V}_g (1 + \Delta V_g) + \omega L_{eq} \widehat{I}_g \sin(\phi)} \right), \end{cases} \quad (4.4)$$

where $L_{eq} = L_{arm}/2 + L_{grid}$.

A model equivalent is implemented to obtain the lookup table with power losses in the HB converter as shown in Figure 33 (a). Due to symmetry, only the upper arm is considered. The reference voltage for the upper arm is given by (Son et al., 2012).

$$v_{u,n} = \frac{1}{2} - \frac{m}{2} \cos(\omega t) + \frac{m}{12} \cos(3\omega t), \quad (4.5)$$

where m is the modulation index, calculate as follows:

$$m = \begin{cases} 2 \frac{\widehat{V}_s}{N v_{bat}}, & \text{for single-stage,} \\ 2 \frac{\widehat{V}_s}{N v_{SM}^*}, & \text{for two-stage.} \end{cases} \quad (4.6)$$

The reference voltage computed based on equations (4.1)-(4.6) is compared with the carrier, which generates the gate pulses. As noted, the arm current is represented by a current source, while the dc-link voltage is represented by a voltage source. Therefore, this approach emulates the current loading of a single SM without simulating the whole MMC.

The power losses are obtained for different values of P_{ref} , Q_{ref} , v_{bat} (single-stage) v_{SM}^* (two-stage) and junction temperature of the semiconductor devices (T_j). The obtained data are used to build a look-up table.

Finally, the ohmic loss in the arm inductor is computed by:

$$P_{arm,ind} = R_{arm} \left(\frac{\widehat{I}_g}{2\sqrt{2}} \right)^2, \quad (4.7)$$

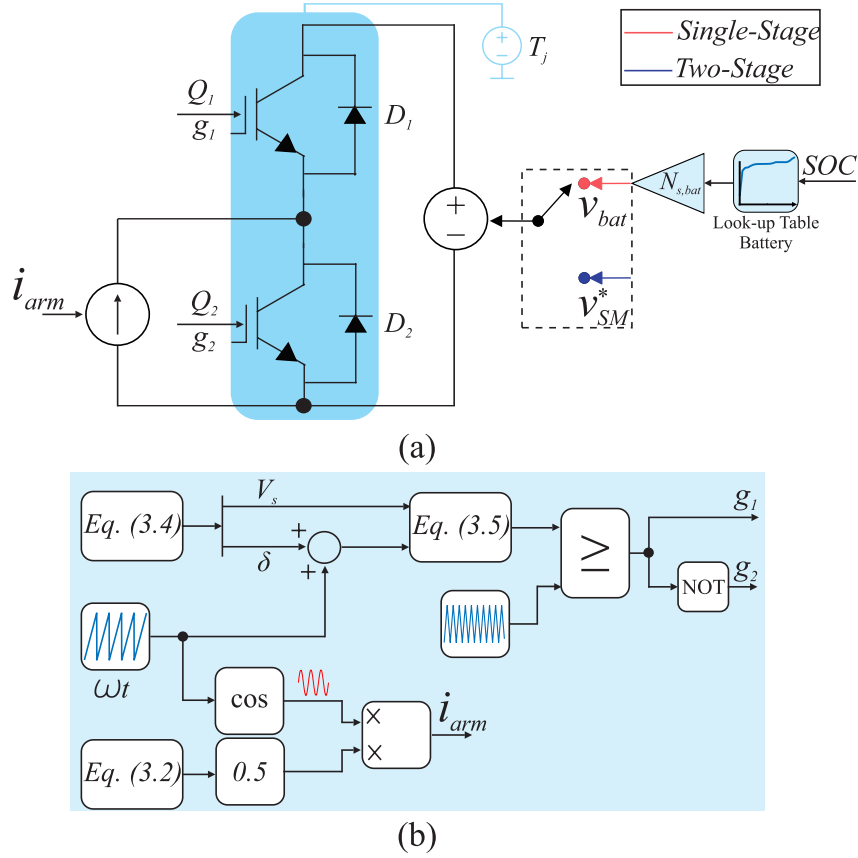


Figure 33 – Simplified model for computation of the SM Converter power losses look-up table:(a) Simplified SM model (b) modulation strategy.

where R_{arm} is the inductor resistance.

As shown in Figure 34 (a), an equivalent model is implemented to obtain the power losses lookup table in the dc/dc converter. The modulation strategy considers a simple current control with a PI controller¹ to generate the reference modulation signal, as shown in Figure 34 (b). The reference current I_{ref} can be approximated by:

$$I_{ref} = \frac{P_n}{6N_{s,bat}v_{bat}}, \quad (4.8)$$

where v_{bat} is the battery voltage, which changes according to the SOC.

The power losses are obtained for different values of SOC, v_{SM}^* and T_j . The obtained data are used to build a look-up table. The behavior of the semiconductor in relation to temperature variation, as well as all its internal parameters are obtained through the curves provided by the manufacturer.

The ohmic loss in the dc/dc converter inductor is computed by:

$$P_{dc,ind} = R_{dc}I_{ref}^2, \quad (4.9)$$

¹ The controller structure and its respective gains will be presented in Chapter 3.

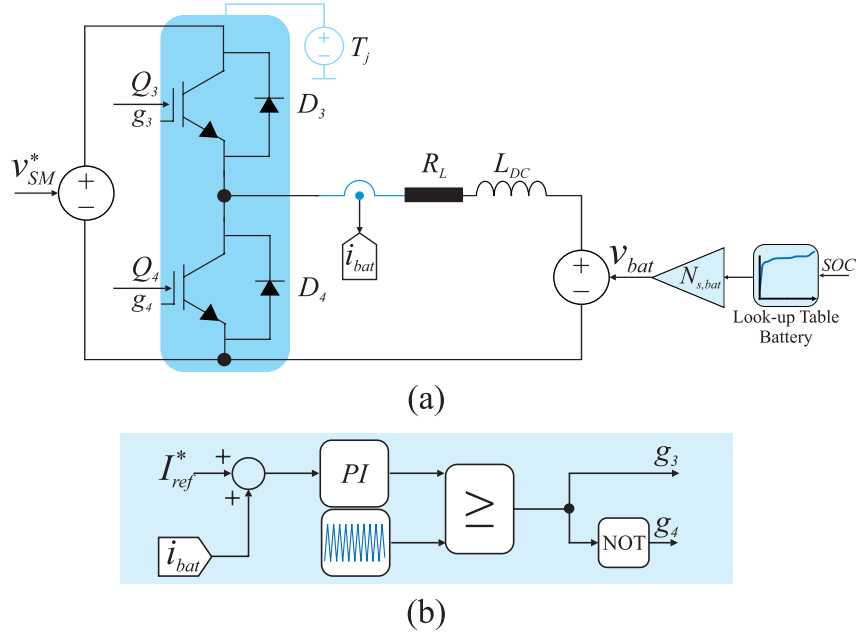


Figure 34 – Simplified model for obtaining look-up table the dc/dc converter (a) equivalent dc/dc model (b) modulation strategy.

where R_{dc} is the resistance of dc/dc converter inductor.

Finally, in order to summarize the loss calculation methodology, we have: In the single-stage approach for each reference voltage and each SOC range, the SM and N_s numbers are updated. Thus, for each simulation, the SM output voltage value is updated to the SOC interval and the P_{ref} value. In the two-stage approach, the simulation process is longer due to the need to sweep the entire reference voltage range of the dc/dc converter. In this sense, the values already mentioned are updated, as well as the N .

4.1.3 Mission Profile

The power losses are estimated for some operational conditions and look-up tables are generated as a function of the processed power. Then, a one-year mission profile for the MMC-based BESS is used to compute the total energy consumption. The methodology is illustrated in Figure 35.

The semiconductor device losses are computed based on a junction temperature estimation, active power mission profile, and SOC mission profile, as illustrated in Figure 35. Look-up tables are obtained for both conduction and switching losses. The data to generate the look-up table are obtained from the semiconductor datasheet. The switching losses are evaluated according to the SM reference voltage. In addition, the temperature dependence of the power losses is considered.

The junction temperature is estimated based on the methodology discussed in (de Sousa et al., 2017). The multilayer Foster model parameters of semiconductor devices are

extracted from the datasheets, which are composed of junction-to-case thermal impedance (Z_{j-c}) and case-to-heatsink thermal impedance (Z_{c-h}). It is assumed that the dc/dc converter and SM HB share the same heatsink. The heatsink-to-ambient thermal impedance (Z_{h-a}) is determined by simulations to guarantee that the maximum steady-state junction temperature (T_j) is in the safe operating area of the power devices.

As in the dc/dc converter inductor, the calculation of the power losses in the dc/dc power semiconductors are challenging, since both losses depend on the batteries SOC. This fact is observed because the SOC affects the instantaneous battery voltage. For enhancing the power losses estimation in the dc/dc converter stage, an electrical model of the battery is used to estimate the SOC mission profile, as shown in Figure 35. In the SOC estimation model, the input parameter is P_{ref} . It assumes that the power is divided in all SM. Thus, the current reference to be injected into the battery model is calculated. Consequently, the SOC changes. Finally, the total power losses generated by the mission profile are obtained.

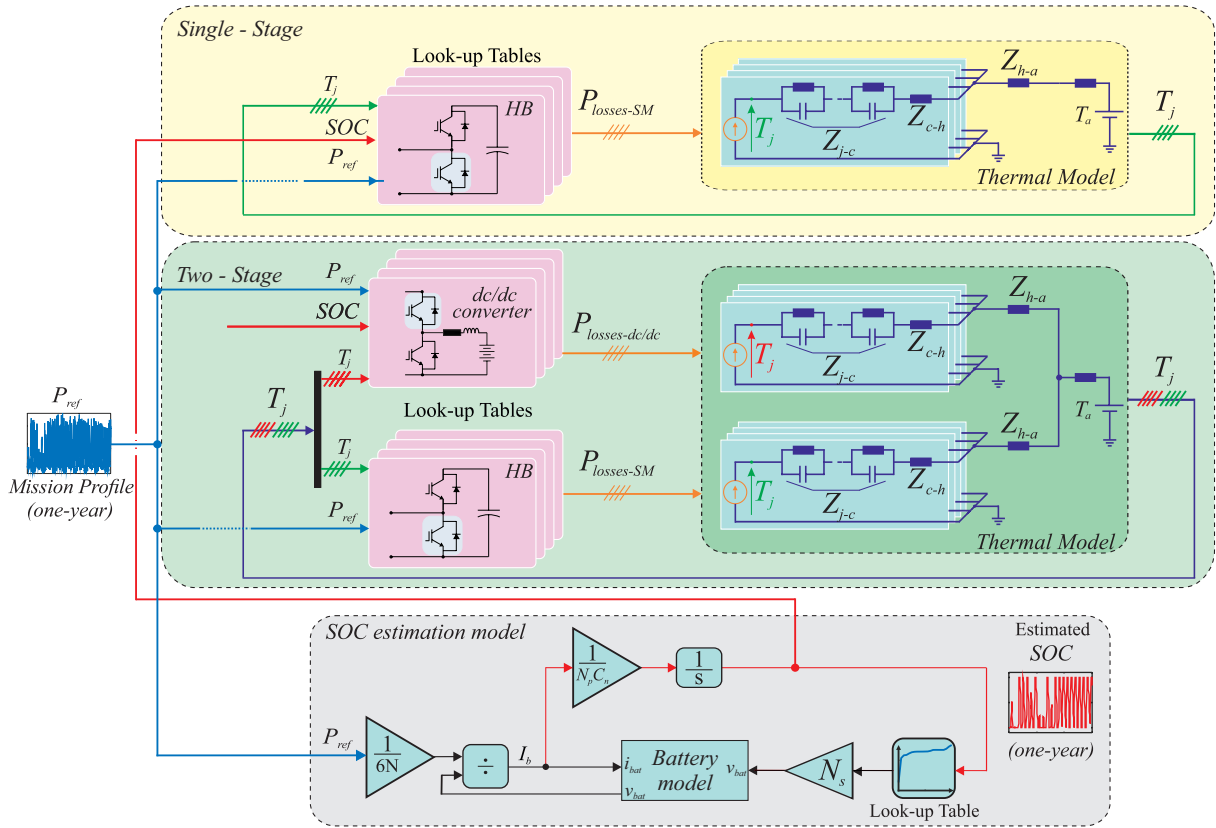


Figure 35 – Methodology for power losses computation: block diagram of the semiconductor devices power losses estimation and block diagram of the total energy consumption estimation.

4.2 Battery Model

The development of the battery model makes it possible to determine the main characteristics and predict the performance throughout the operation. In addition to performance, the battery model has to be able to predict electrical performance for different operating conditions (SOC, temperature, and current). In this way, running simulations and developing operational strategies in order to improve battery performance becomes possible.

Basically, battery modeling processes vary depending on the project and what characteristics one wants to evaluate. These approaches have different degrees of complexity and can be divided into three categories: electrochemical, mathematical, and electrical models. Electrochemical models have high precision, however, they are difficult to parameterize because the data is not provided by the manufacturers (Swierczynski, 2012). In this sense, specialized equipment would be needed to obtain this data. Mathematical models are considered to be of low precision (Chen; Rincon-Mora, 2006; Li; Ke, 2011; Shepherd, 1965). Finally, electrical models become an interesting alternative for presenting a relatively high accuracy and moderate parameterization complexity (Swierczynski, 2012).

Figure 36 presents the detailed model of the battery. Two models are used in this system: electric and thermal. In the electrical model, the current source receives updated values at all times obtained from the division between the power of an SM and the OCV of the battery. Through the battery current and other parameters with C_n , N_p , N_s , and the battery mission profile it is possible to obtain the SOC over time. Finally, the impedance of the battery at this moment is represented by Z_{bat} .

With the electrical model of the battery, the next step is to represent the thermal model. This equivalent model presents some simplifications so that several experimental measurements are not necessary. The battery surface temperature is assumed to be uniform. In this sense, three parameters are considered: internal heat transfer resistor (R_i), external heat transfer resistor (R_o), and heat capacity (C_C). These parameters were estimated from experimental data (Forgez Christophe and Do, 2010). P_L is the power of each battery and T_{amb} the ambient temperature in Kelvin. Finally, the internal temperature of the battery (T_I) is variable to be analyzed during battery operation. In addition, the battery temperature is used in the lifetime estimation procedure.

Electrical circuit-based modeling is performed by combining voltage sources with passive elements (capacitors, resistors, and inductors). In this way, it achieves an accuracy between 1% to 5% of electrical quantities, for example, voltage and current (Chen; Rincon-Mora, 2006). It is important to note that, unlike electrochemical modeling, the Li-ion battery model cannot be used in other projects or different chemistries (Swierczynski, 2012). The estimation of parameters is made from the frequency response of the battery

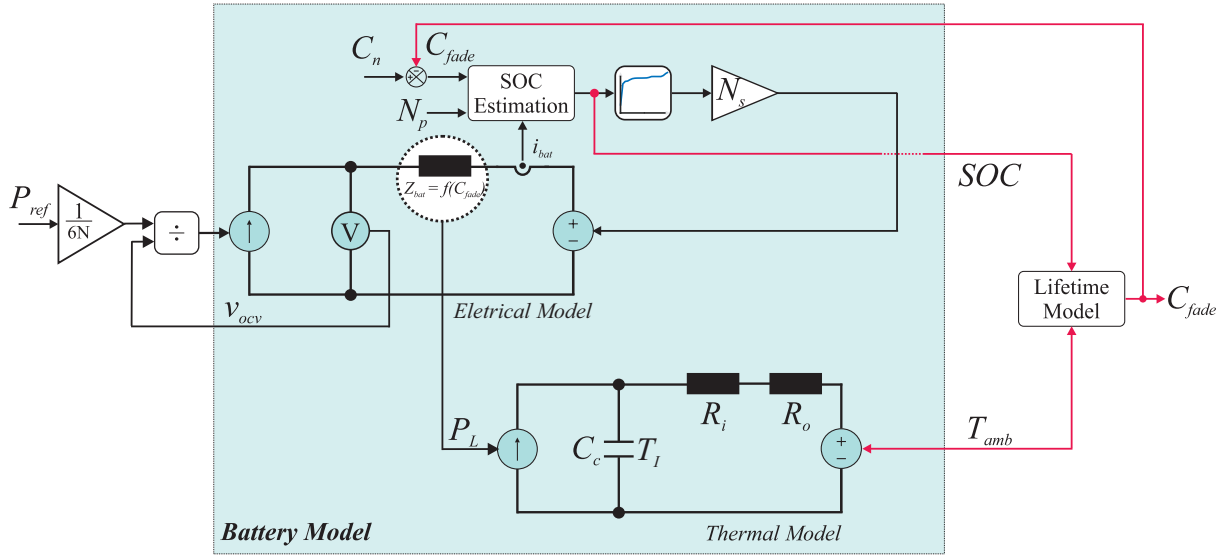


Figure 36 – Structure of the battery model

equivalent circuit. Typically, these data are obtained through Electrochemical Impedance Spectroscopy (EIS) tests. Through the EIS it is possible to obtain the complex impedance for a range of ac frequencies. The general principle of the EIS method is based on the application of a sinusoidal signal, then measuring the characteristic of the battery response, which depends on the impedance (Swierczynski, 2012).

Figure 37(a) shows in detail the Z_{bat} . In this approach, ZARC² elements are used. As shown in Figure 37(b) the ZARC element consists of an impedance and a constant phase element, which describes a semicircle in the Nyquist diagram.

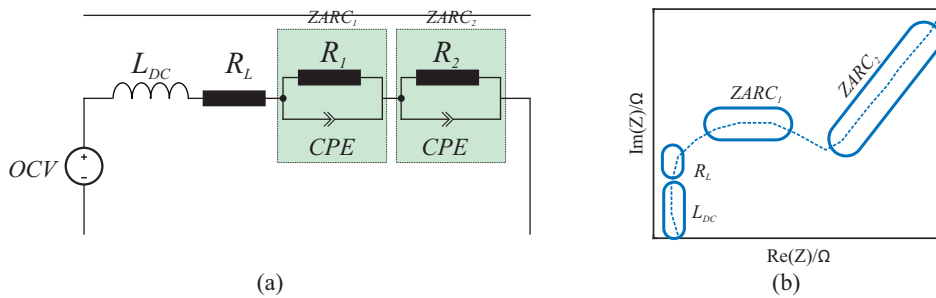


Figure 37 – Structure of the electrical-lifetime model for the Li-ion battery.

As illustrated in Figure 38, each ZARC component can be expanded by its impedances, represented by a resistor and capacitor connected in parallel. This connection forms a block. Altogether there are 5 blocks connected in series, thus forming a ZARC element.

The Constant-Phase-Element (CPE) is approximated by a generalized capacitance and a depression factor ξ which can be any value between 0 and 1. The closer to 0 it

² According to (Macdonald J Ross and Barsoukov, 2005), the name ZARC is due to the circuit elements that represent the depressed arcs in the Z plane, that is, the impedance plane.

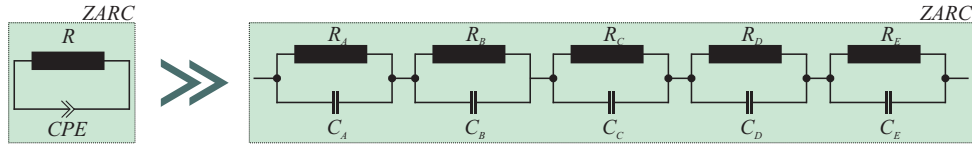


Figure 38 – Structure of the electrical-lifetime model for the Li-ion battery.

becomes the more purely resistive and the closer to 1 it becomes purely capacitive. (Wu, 2016) show the optimization factor values for the RC circuit approximation and how to calculate the parameters for the ZARC circuit.

4.2.1 Battery Lifetime Evaluation

In MMC-based BESS application, the batteries lifetime is expected to be shorter than the lifetime of others converters components, as capacitors, inductors and semiconductors devices (Stroe et al., 2014). In addition, the batteries replacement can significantly increase the system total cost.

Reference (Stroe, 2014b) proposes a lifetime evaluation methodology for Li-ion batteries. This approach considers the cycling and the calendar aging mechanisms, which are related to the battery power cycling and idle operation modes. In addition, the damage caused by the calendar and cycling aging mechanisms is employed to update the battery electrical parameters, as illustrated in the flowchart shown in Figure 39.

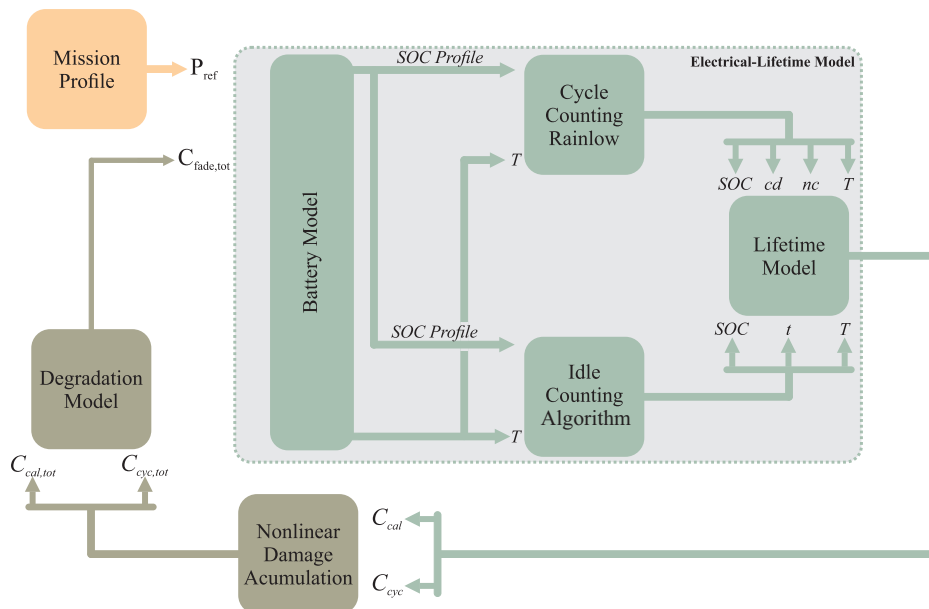


Figure 39 – Structure of the electrical-lifetime model for the Li-ion battery.

For each one-month mission profile of P_{ref} , a one-month mission profile of SOC is derived from the battery electrical model. The SOC profile and battery temperature are used in the cycle counting rainflow and idle counting algorithm to extract the main

parameters of each cycle and idle period. Then, based on the parameters of cycling and idling mode, the capacity fade for each degradation mechanism is obtained. The capacity fade caused by the cycling aging (C_{cyc}) is given by (Stroe, 2014b):

$$C_{cyc} = 2.6418e^{-0.01943SOC} 0.004e^{0.01705T} 0.0123cd^{0.7162} nc^{0.5}. \quad (4.10)$$

where nc is the number of cycles, SOC is the the average SOC in each cycle, in percentage, cd is the Depth-of-Discharge (DOD), in percentage, and T is the battery temperature, in Kelvin. The rainflow counting algorithm is employed to extract the parameters of Eq. (4.10) from the SOC mission profile.

In addition, the capacity fade caused by the calendar aging (C_{cal}) is given by (Stroe, 2014b):

$$C_{cal} = 1.9775 \cdot 10^{-11} e^{0.07511T} 1.639e^{0.007388SOC} t^{0.8}. \quad (4.11)$$

where t is the time that the battery stays in idling mode, in months and the SOC stationary in each idle period, in percentage. These parameters are obtained, based on an idle counting algorithm. Basically, the algorithm considers that the state of charge is constant if variations lower than 1 % are observed in the SOC mission profile.

The ambient temperature where the batteries are installed is assumed to be 303 K (29,5°C) (in cycling and calendar analysis)³. The lifetime models compute the capacity fade for each cycle detected in the mission profile. Then, a non-linear damage accumulation strategy is employed to compute the total damage for the one-month mission profile.

Thereafter, for each one-month mission profile of SOC , one value of C_{cyc} and C_{cal} is obtained and accumulated with the last month capacity fade. The total cycling capacity fade ($C_{cyc,tot}$) is obtained from the accumulation of the actual month cycling capacity fade ($C_{cyc,actual}$) and the previous month cycling capacity fade ($C_{cyc,previous}$), as follows:

$$C_{cyc,tot} = \sqrt{C_{cyc,actual}^2 + C_{cyc,previous}^2}. \quad (4.12)$$

The total calendar capacity fade ($C_{cal,tot}$) is obtained from the accumulation of the actual month calendar capacity fade ($C_{cal,actual}$) and the previous month calendar capacity fade ($C_{cal,previous}$), as follows:

$$C_{cal,tot} = \left[(C_{cal,actual})^{\frac{10}{8}} + (C_{cal,previous})^{\frac{10}{8}} \right]^{\frac{8}{10}}. \quad (4.13)$$

Note that in Eq. (4.12) is the square root of the sum of the parameters. Likewise in Eq. (4.13) where the parameters are raised to 10/8 and their sum is raised to 8/10. This

³ Usually, temperatures in the range from 293 K to 303 K degrees are employed (Stroe, 2014b).

algebraic compensation aims to perform a non-linear damage accumulation due to the non-linearity of the service life model.

Thus, the total capacity fade ($C_{fade,tot}$) of battery is computed by the sum of the total calendar capacity fade and total cycling capacity fade:

$$C_{fade,tot} = C_{cal,tot} + C_{cyc,tot}. \quad (4.14)$$

Finally, the battery lifetime model updates the battery electrical model parameters every month, together with the capacity in Ah of the battery, following the degradation model proposed by (Stroe, 2014b). Thus, when the Ah-capacity reaches a loss of 20 % in relation to the nominal capacity, the battery have reached its End-of-Life (EOL).

4.3 Cost Evaluation Methodology

The total cost is estimated using the methodology proposed by (Abu Bakar Siddique et al., 2016). The estimation is based on two parameters, CAPEX and OPEX. The first is defined as the capital expenditure, while the second is the operational expenditure. The total cost of MMC-based BESS can be calculated as follows:

$$Total\ Cost = CAPEX + \underbrace{OPEX_L + OPEX_R}_{OPEX}. \quad (4.15)$$

The cost of power electronics (semiconductors, cabinets, instrumentation, controls, etc) is estimated as 3.5 €/kVA of the installed switching power (P_{sw}) (Engel et al., 2014):

$$P_{sw} = N_{ps} V_{ps} I_{IGBT}, \quad (4.16)$$

where N_{ps} is the amount of power semiconductors, V_{ps} is the rated blocking voltage and I_{IGBT} is the power module rated current.

According to (Engel et al., 2014), the capacitors cost is estimated as 150 €/kJ. Furthermore, the Li-ion battery system exhibits a specific cost of 450 €/kWh (Engel et al., 2014).

$OPEX_L$ is estimated based on the cost of power losses. Using the power losses analysis described in the previous section, the total energy losses per year (E_c) can be computed. Then, the $OPEX_L$ is given by:

$$OPEX_L = K_o E_c Y, \quad (4.17)$$

where K_o is the price per kilowatt-hour. Considering the penalties for losses in the transmission system, K_o is estimated to be 1.1 €/kWh (Alvarez et al., 2016). Y is the number of operating years considered in the analysis.

$OPEX_R$ refers to the cost of batteries replacement. This cost must be added to the system when the estimated battery lifetime is lower than the target defined for the MMC-based BESS. The replacement cost is approximated by the cost of batteries. Therefore, the same approach used for CAPEX is adopted.

The total cost of the MMC-based BESS is used as a figure of merit to compare different designs employing different reference voltages and allowed SOC ranges. It should be noted that other metrics can be included in the evaluation of the cost of the system. However, the evaluation of more accurate and current metrics exceeds the scope of this thesis.

4.4 Case Study

The generation of energy from renewable sources can be used with the objective of reducing costs related to electrical services. For intermittent energy sources, it is attractive to associate energy storage systems to this generation. In this sense, among the different services and applications that can be performed, one of them is Electric Energy Time Shifting (Farias; Canha, 2018). This application consists of generating and storing energy at the lowest tariff time (off-peak hours) and using it at the highest tariff interval (peak hours). In order to avoid charging demand at peak hours, the load has to be supplied throughout the entire collection time interval. This period of time and days analyzed varies by location and utility. In this work, an interval of 3 hours is considered, from 5 pm to 8 pm, excepting weekends. Figure 40 exemplifies the process of generating photovoltaic solar energy to supply the demand throughout the day and the process of charging and discharging the batteries. In addition, the variation in off-peak and peak times is analyzed.

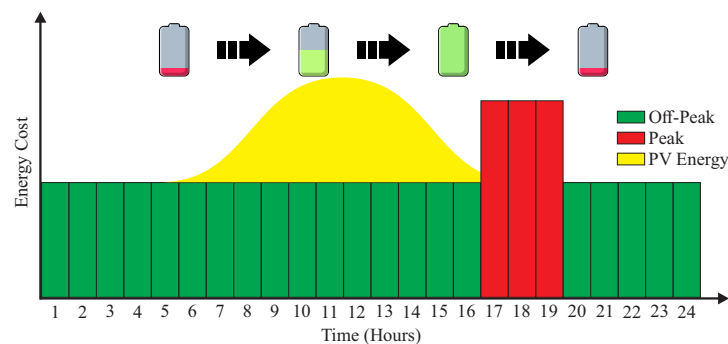


Figure 40 – Exemplification of the work case study. PV production meets the need of battery banks and consumer load. At peak hours, the batteries discharge to meet consumption.

Figure 41 displays the case study proposal over the course of a day. The production of electricity through the photovoltaic system is illustrated in Figure 41 (a). Note that the sizing of the photovoltaic system has to be able to meet the demand at peak times. Figure 41 (b) presents a load profile for a given demand. Figure 41 (c) shows the moments when the network helps in the supply of energy during off-peak hours. Finally, Figure 41 (d) exemplifies the charging and discharging processes of BESS. Throughout the day, until 5 pm, the batteries charge. When peak hours begin, all stored energy is used. After 20:00, the tariff is reduced and the utility company returns to meet customer demand.

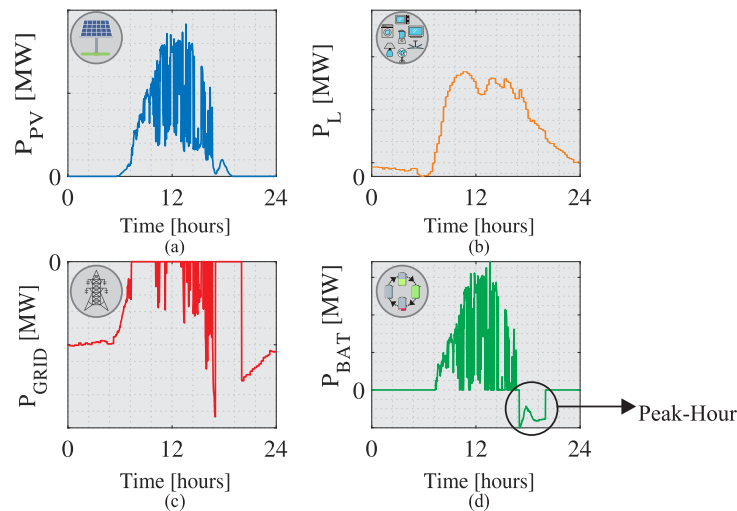


Figure 41 – Demonstration of the case study according to the power supply and/or drained from (a) the solar photovoltaic system, (b) the load, (c) the grid, and (d) the battery.

The operational mission profile considers the application a medium voltage customer. Figure 42 shows off-peak and peak-hour energy consumption over twelve months.

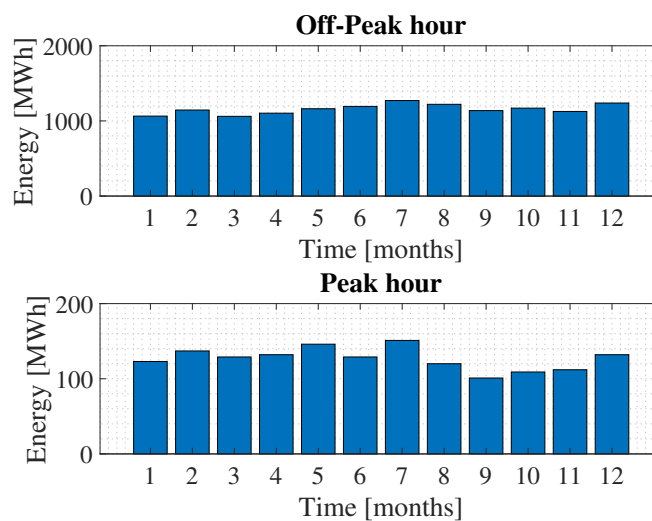


Figure 42 – Monthly energy consumption at peak and off-peak times over 12 months.

Figure 43 (a) shows the power relative to photovoltaic solar production for the city of Viçosa-MG, Brazil. The sizing of this plant was carried out using the history of energy consumption over the last 12 months. With this data and through the behavior of consumption during the course of a day, the data were expanded to fit the monthly consumption. Thus, Figure 43 (b) exhibits the customer power the load over a year.

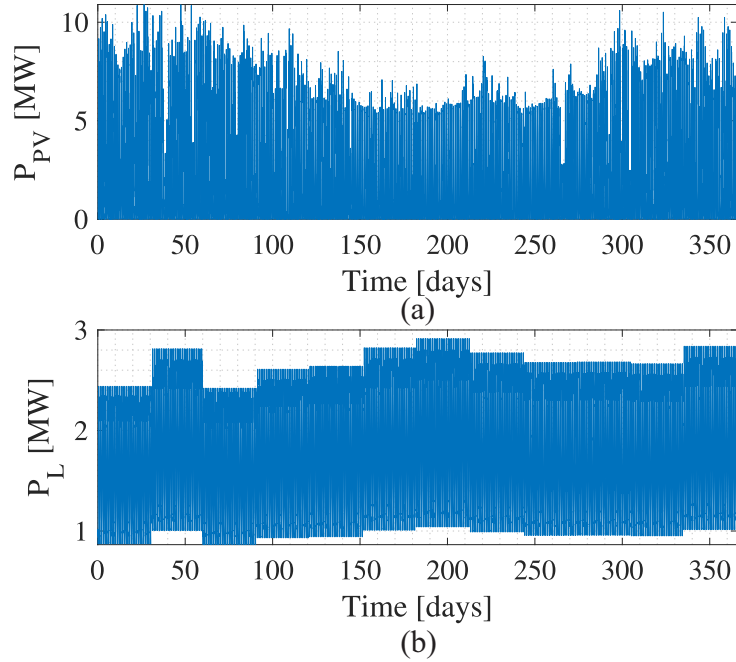


Figure 43 – Annual data referring to: (a) PV power plant and (b) load.

The MMC-based BESS input parameters studied in this work are presented in Tab. 4. It is important to highlight the determination of some parameters. The x_{arm} value is in a typical range for the MMC topology, Sharifabadi et al. (2016b). The capacitance considered is 40 kJ/MVA to guarantee a maximum capacitor voltage ripple of 10%, which is typical for MMC, (Akagi, 2017). The switching frequency of the HB (f_c) used in this work corresponds to 4.5 times the line frequency (60 Hz). This value is justified to obtain better dynamic performance and voltage balancing of the capacitor (Ilves et al., 2015). In addition, the f_{sw} value must have enough bandwidth to eliminate the second harmonic from the battery current.

As discussed above, two types of projects are considered: standard solution and customized solution. For the standard, the battery rack P3-R070 manufactured by Samsung was employed (Samsung, 2018). The battery rack parameters are presented in Tab. 5.

For the customized solution, the battery cell A123 26650 model ANR26650m1-b manufactured by A123 systems was employed (A123 Systems, 2012). The battery cell parameters are presented in Tab. 6.

Figure 44 (a) shows OCV characteristic in function of the SOC based on experimental results for a single Lithium Iron Phosphate (LiPOF_4) battery from (Meng et

Table 4 – Parameters of the MMC-based BESS.

Parameters	Symbol	Value
Rated apparent power [MVA]	S_n	10.9
Rated reactive power [Mvar]	Q_n	10.9
Rated active power [MW]	P_n	10.9
Total energy storage [MWh]	E_n	5.76
Output voltage (line to line) [kV]	V_g	13.8
Grid frequency [Hz]	f_n	60
Arm reactance [pu]	x_{arm}	0.15
Submodule Capacitance for 40 kJ/MVA [mF]	C	8
Switching frequency of the dc/dc converter [Hz]	f_{sw}	1000
Switching frequency of the HB [Hz]	f_c	270
Ripple current battery [%]	ΔI_{bat}	10

Table 5 – Parameters of the Battery Rack P3-R070.

Parameters	Symbol	Value
Power capacity [Ah]	C_n	78
Discharging rate []	C_r	0.5
Total energy storage [MWh]	E_n	0.07
Battery rack voltage @ SOC = 100 % [V]	-	992
Battery rack voltage @ SOC = 0 % [V]	-	750

Table 6 – Parameters of the Battery Cell A123 26650.

Parameters	Symbol	Value
Power capacity [Ah]	C_n	2.5
Discharging rate []	C_r	1
Total energy storage [Wh]	E_n	7.6
Battery rack voltage @ SOC = 100 % [V]	-	3.4
Battery rack voltage @ SOC = 0 % [V]	-	2.5

al., 2018). This curve is estimated based on a curve-fitting with an eleven-order polynomial. Then, these values were extrapolated to estimate the curve for the Samsung battery rack, as shown in Figure 44 (b).

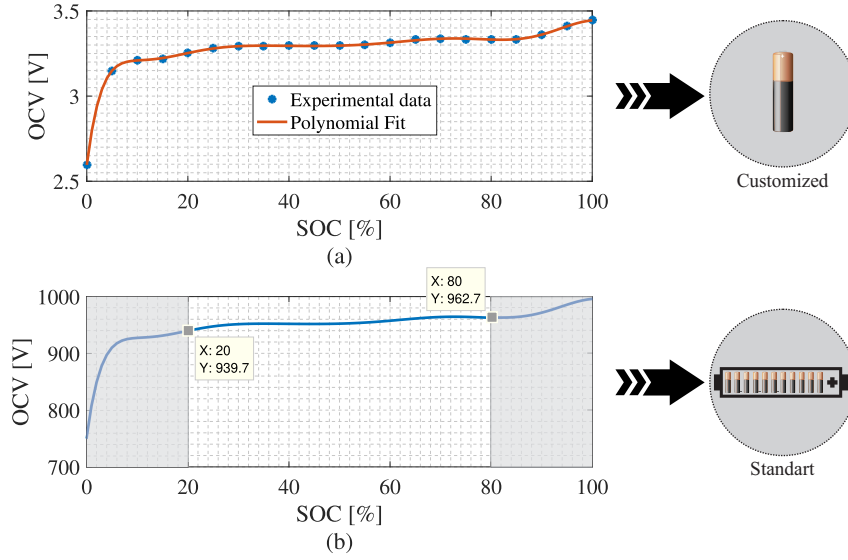


Figure 44 – Open-circuit voltage characteristics: (a) single battery cell experimental data from Meng et al. (2018) and polynomial fitting; (b) Estimated curve of the battery rack. The highlighted regions indicate the adopted range for SOC_{min} and SOC_{max} in the MMC-based BESS design.

In the case studies adopted for the MMC-based BESS, minimum and maximum SOC intervals are considered. The minimum values are between $0 \leq SOC_{min} \leq 20\%$. Three scenarios are evaluated:

- Case 1 = $SOC_{min} = 0\%$ and $SOC_{max} = 100\%$;
- Case 2 = $SOC_{min} = 5\%$ and $SOC_{max} = 95\%$;
- Case 3 = $SOC_{min} = 10\%$ and $SOC_{max} = 90\%$;
- Case 4 = $SOC_{min} = 15\%$ and $SOC_{max} = 85\%$;
- Case 5 = $SOC_{min} = 20\%$ and $SOC_{max} = 80\%$.

Regarding the SM and dc/dc converters realization, HiPak power modules manufacture by Asea Brown Boveri (ABB) are taken into account. Table 7 presents the selected part numbers. The voltages corresponding to 100-FIT values were obtained from (Isalma; Guo; Zhu, 2014). These values are defined in this work as the maximum allowed SM voltage reference for a given blocking voltage.

The same IGBT part number is used for both SM and dc/dc converter. In the thermal design, the SM and the dc/dc converter power modules are assumed to be installed in the same heatsink. The heatsink-to-ambient thermal impedance (Z_{h-a}) is computed by simulations to guarantee a maximum temperature of 120°C in the most stressed device for all analyzed part numbers. All the analyses consider a constant ambient temperature of

Table 7 – Possible candidates for the SM realization.

Part Number	Blocking Voltage	Current rating	V_{100FIT}
5SND 0800M170100	1.7 kV	800 A	0.90 kV
5SND 0500N330300	3.3 kV	500 A	1.80 kV
5SNA 0650J450300	4.5 kV	650 A	2.25 kV
5SNA 0600G650100	6.5 kV	600 A	3.60 kV

40°C. For the inductors, ohmic losses evaluation, a X/R ratio of 40 (at the fundamental frequency) is used for both arm and dc/dc converter inductors.

4.5 Conclusion

This chapter presents the cost-oriented design methodology and its respective stages. First, the concept and procedures for calculating the power losses of the systems are discussed. In this work, power losses are divided into two stages: look-up table generation and mission profile application. After, the losses of MMC-based BESS are quantified and divided into two factors: CAPEX and OPEX. Finally, the methodology presented in this chapter will be applied in simulations to be shown in Chapter 5.

5 Power Losses, Battery Lifetime and Costs Analyses

In this chapter, the designs of single-stage and two-stage approaches in customized and standard solutions are discussed. According to each project, the costs related to the power electronics for each converter are obtained. The indicator used to calculate these costs is **CAPEX**. In addition, the operating costs of the converter are analyzed. In this case, the **OPEX** methodology is used. The **OPEX** variable, in this work, is divided into two parts: **OPEX_L** and **OPEX_R**. The first is related to operating losses such as conduction and switching losses in semiconductors, for example. The second is associated with cells or batteries replacement cost. In this way, the lifetimes for each system are displayed. In this work, the period analyzed is 25 years. Finally, the total cost for each approach is obtained and its respective models are performed.

5.1 Single-Stage Approach

As discussed in Chapter 2, to maximize the number of batteries in series v_{SM}^* is assumed to be V_{100FIT} . In the case studies four classes of **IGBT** are used: 1.7 kV, 3.3 kV, 4.5 kV and 6.5 kV. In the next two subsections, the designs for the customized and standard solutions, respectively, are analyzed.

5.1.1 Customized Solution

Figure 45 (a) shows the $N_{s,bat}$ per string for each blocking voltage of the **IGBT** and for each case study. Once the blocking voltage increases, the association of batteries cells in series increases. On the other hand, the $N_{p,bat}$ decreases, as shown in Figure 45 (b).

Compared to the same **IGBT** blocking voltage, the total number of the series battery cells is the same in all case studies. However, to obtain the energy requirements of **BESS**, the number of batteries cells in parallel increases. For example, for **IGBT** of the 3.3 kV, Case 5 needs more batteries cells in parallel than Case 1.

Figure 46 (a) exhibits the total number of battery cell for each case study and for each v_{SM}^* . As discussed in Figure 45 (b), case studies with a smaller **SOC** range need more batteries to fulfill energy requirements. Figure 46 (b) shows the amount of **SM** for each design. As seen previously, the N depends on the $N_{s,bat}$ and the $v_{bat,min}$. According to Figure 46 (a), the **IGBT** of 3.3 kV uses fewer batteries in series than the others. Furthermore, in Case 1 $v_{bat,min} = 2.6$ V and for Case 5 $v_{bat,min} \approx 3.2$ V. Consequently, Case 1 and **IGBT**

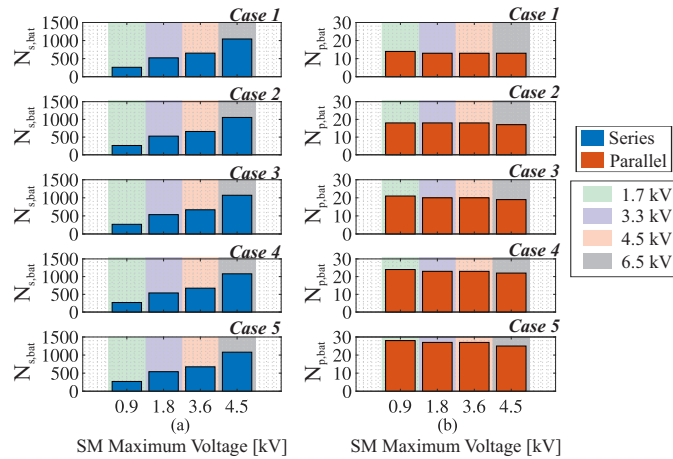


Figure 45 – Battery cell design for customized single-stage approach for the five case studies: (a) series and (b) parallel.

of 3.3 kV designs need more SM. The other cases had quantities close to SM due to the rounding of the *ceil* function used in equation (2.27).

Figure 46 (c) shows the nominal energy of each project. All cases are designed for a target of 5.76 MWh. However, due to sizing rounding, some cases are penalized with energy oversizing. Finally, Figure 46 (d) compares battery lifetime for each case study and for each v_{SM}^* . The case studies with the most energy oversizing shown in Figure 46 (c) are the ones with the longest battery lifetime.

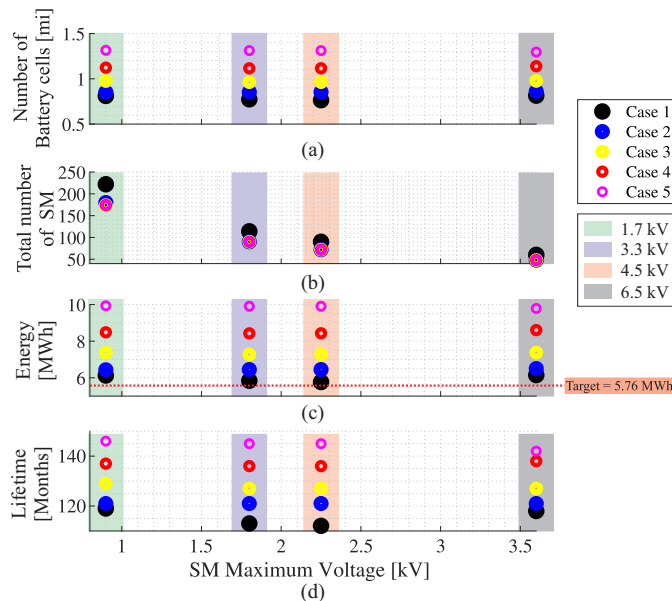


Figure 46 – System configuration according to the reference voltage variation and SOC, for single-stage approach and customized solution: (a) number of batteries cells; (b) total number of SM and; (c) total energy storage and (d) Battery lifetime.

Figure 47 (a) shows the CAPEX. Note that the behavior is similar to Figure 46 (a). Therefore, it is concluded that the cost related to energy storage is the largest portion of

CAPEX. The costs related to $OPEX_L$ are shown in Figure 47 (b). Reflecting the behavior of Figure 46 (b), designs with more SM have higher losses. The $OPEX_R$ is shown in Figure 47 (c). According to the battery lifetime shown in Figure 46 (d), the replacement estimate is considering an operation period of 25 years.

Figure 47 (d) presents the total costs for each design. The **CAPEX** and $OPEX_R$ variables determined the final cost. In this sense, all case studies and all blocking voltage of IGBT required only one battery replacement. Finally, Case 1 for IGBT of the 3.3 kV presents the best overall total cost, being the best option for the single-stage approach customized solution.

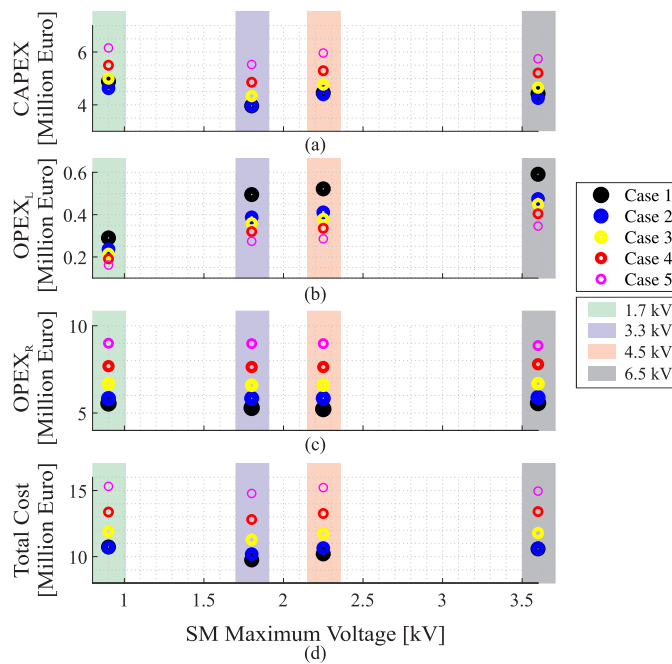


Figure 47 – Estimated costs for all cases studies evaluated for the customized single-stage approach: (a) CAPEX; (b) $OPEX_L$; (c) $OPEX_R$; (d) Total Cost.

Table 8 highlights the designs with the lowest total costs.

Table 8 – Best Cases for Each Blocking Voltage (Single-Stage customized solution)

Rated Blocking Voltage [kV]	SM Reference Voltage [kV]	Case Study	Total Cost [mi Euros]
1.7	0.9	2	10.69
3.3	1.8	1	9.74
4.5	2.25	1	10.2
6.5	3.6	1	10.58

Figure 48 shows the separate costs for the best option. The costs per class are considered: **CAPEX**, $OPEX_L$ and $OPEX_R$. Note that the cost of $OPEX_R$ represents more than half of the cost of 9.74 million Euros. This is justified by the need for two battery replacements.

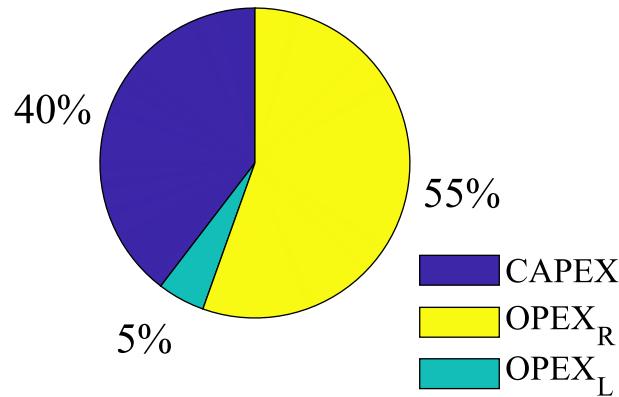


Figure 48 – Separate costs for best design.

5.1.2 Standard Solution

All analyzes performed in the previous section are made for the standard solution. Note, that in the standard solution, due to rounding, designs for the IGBT of 1.7 kV are not performed. The $N_{s,bat}$ increase with the blocking voltage of the IGBT as shown in Figure 49 (a). On the other hand, the SOC range does not change $N_{s,bat}$.

Figure 49 (b) exhibit the $N_{p,bat}$ for different IGBT blocking voltage and SOC ranges. The number of strings in parallel is the same for all blocking voltages and case studies. This is justified by the fact that these are commercial battery models with a predetermined voltage, capacity, and energy parameters. Thus, all designs are within a range of values and in rounding have the same final value.

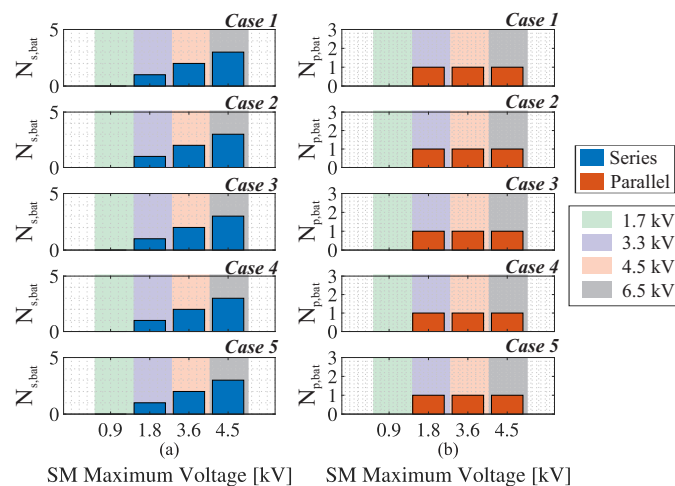


Figure 49 – Battery rack design for customized single-stage approach for the five case studies: (a) series and (b) parallel.

Figure 50 (a) shows the number of battery rack for each case study. For any IGBT blocking voltage, note that the N_s is the same. Furthermore, the value of $N_{p,bat}$ is repeated for all cases. Thus, the number of batteries in each project is different due to the number of SM shown in Figure 50 (b). As a result, Case 1 needs more SM than other designs.

Figure 50 (c) shows the amount of energy available in each project. Note that in all cases the values are greater than the target. This is a consequence of using the standard solution. Finally, Figure 50 (d) shows the lifetime of the batteries for the projects. Note, that the smaller the SOC range, the longer the battery lifetime.

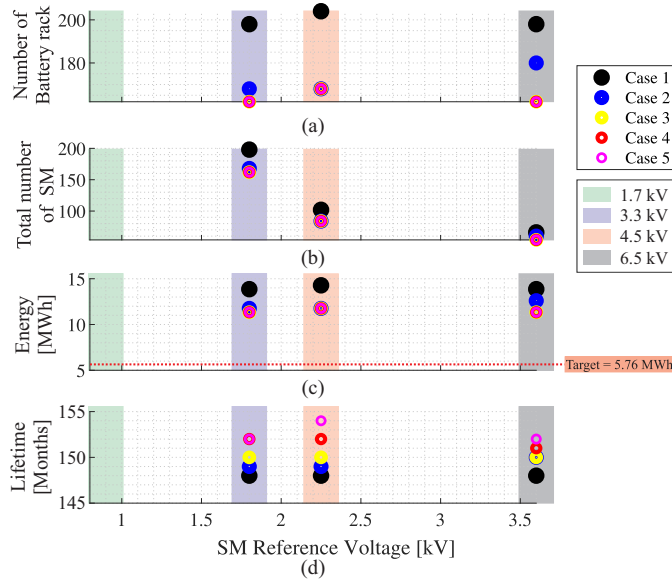


Figure 50 – System configuration according to the reference voltage variation and SOC, for single-stage approach and standard solution: (a) number of batteries rack; (b) total number of SM; (c) total energy storage and (d) Battery lifetime.

Figure 51 presents a comparison of battery lifetime between the single-stage approach, customized and standard. These results are from Case 1 for the IGBT blocking voltage of 4.5 kV. In the customized solution, projects are closer to the required energy target. Consequently, the batteries tend to cycling more as shown in Figure 51 (a). On the other hand, in the standard solution, as the projects present greater energy oversizing, the batteries have a smaller cycling mechanism.

Another effect that impacts battery degradation is calendar ageing. In this analysis, the intervals of inactivity of the batteries are considered. According to Figure 51 (b), this degradation mechanism is more impacting than cycling in the customized and standard solution. This is justified by the fact that the batteries assist the system only during peak hours. In addition, as the standard solution has higher energy oversizing, so the inactivity intervals are longer. Finally, 51 (c) shows the lifetime of the batteries for each model. This time is counted after reaching a total capacity fade of 20%.

Figure 52 (a) shows the CAPEX for each project. Regarding the customized solution, CAPEX was higher, mainly due to two factors: increase in the number of SM and energy oversizing of battery racks. Figure 52 (b) shows the OPEX_L for the cases under analysis. The costs for battery replacements is shown in Figure 52 (c). Finally, the total costs are shown in Figure 52 (d). CAPEX and OPEX_R costs are determinants for the optimized

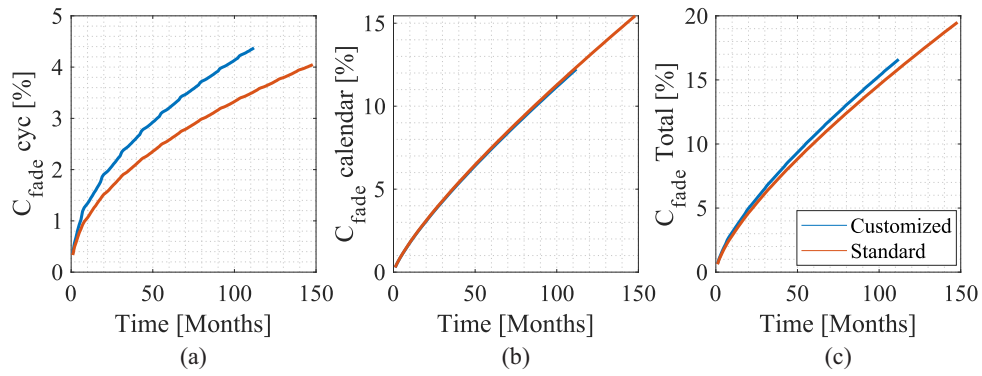


Figure 51 – Comparison between customized and standard solutions in the single-stage approach according to fading: (a) Cycling (b) calendar (c) total.

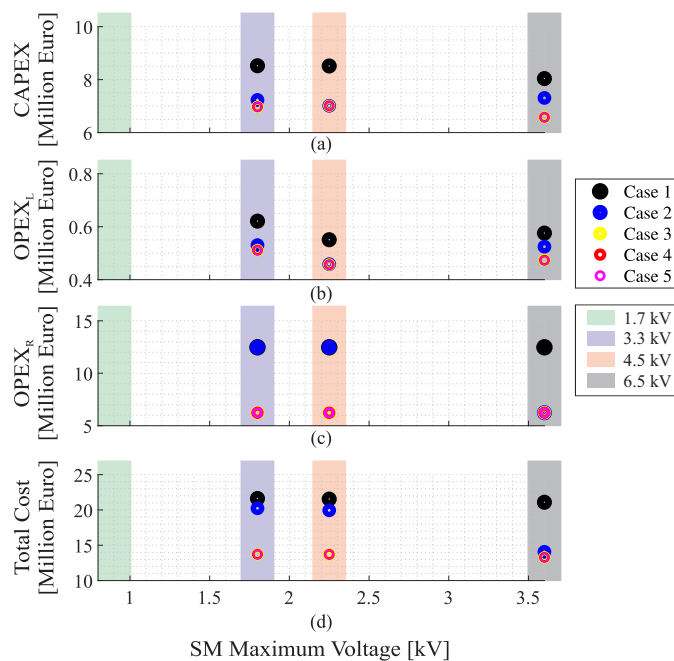


Figure 52 – Estimated costs for all cases studies evaluated for the customized single-stage approach: (a) CAPEX; (b) $OPEX_L$; (c) $OPEX_R$ (d) Total Cost

option. In this sense, Case 3, Case 4, and Case 5 were the optimal options for the three classes of IGBT.

Table 9 shows the total costs for the optimal cases for each IGBT case. Also, highlight the best overall: Case 3, Case 4, and Case 5, for the IGBT of 6.5 kV, result in 13.29 million euros. Compared with the customized solution, the best options for the standard solution are approximately 34% more expensive.

Table 9 – Best Cases for Each Blocking Voltage - (Single-Stage standard solution)

Rated Blocking Voltage [kV]	SM Reference Voltage [kV]	Case Study	Total Cost [mi Euros]
3.3	1.8	3,4 and 5	13.72
4.5	2.25	3,4 and 5	13.70
6.5	3.6	3,4 and 5	13.29

5.2 Two-Stage Approach Customized Solution

Figure 53 (a) shows the $N_{s,bat}$ according to the variation of the SM reference voltage. This is because of the association of the dc/dc converter that varies the duty cycle to reach the same voltage value on the dc-link. On the other hand, as shown in Figure 53 (b), the $N_{p,bat}$ increases or decreases according to the SM reference voltage. As $N_{s,bat}$ increases, $N_{p,bat}$ adjusts to fulfill the energy requirements.

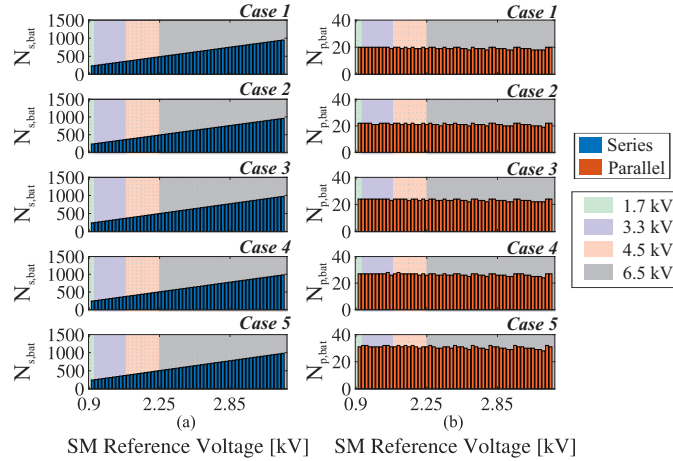


Figure 53 – Battery rack configuration in a single SM according to the variation of the v_{SM}^* and the allowed SOC range for the two-stage approach customized solution. (a) number of battery in series (b) number of strings

Figure 54 (a) shows the number of battery cells for each SM reference voltage value and for each IGBT blocking voltage. Cases with a longer SOC range need fewer battery cells to achieve the power requirement. In addition, the distance between the number of batteries between Cases 3, 4 and 5 is justified by the rounding for that value range.

For the SM reference voltage, the SM number is the same for the 5 case studies as shown in Figure 54 (b). The two-stage approach allows for a variation of the duty cycle in order to keep the dc/dc converter input voltage at V_{100FIT} . Note that in the two-stage approach the number of batteries and SM decreases compared to the single-stage approach customized solution. This way, as shown in Figure 54 (c), the designs are closer to the energy target. Projects with less energy oversizing tend to cycle more. Consequently, the lifetime of the batteries gets shorter, Figure 54 (d).

In the two-stage approach as all cases have the same number of SM for a given reference voltage, the number of battery cells is the determining factor for CAPEX. Thus, according Figure 55 (a), cases with a larger SOC range shown lower CAPEX. Furthermore, as shown in Figure 55 (b) the $OPEX_L$ are close among all cases. This small difference is due to the size of L_{dc} which varies between cases.

Figure 55 (c) shows the $OPEX_R$. As seen in Figure 55 (d), the lifetime of the battery cells got shorter. As such, most cases required more than one replacement. Finally,

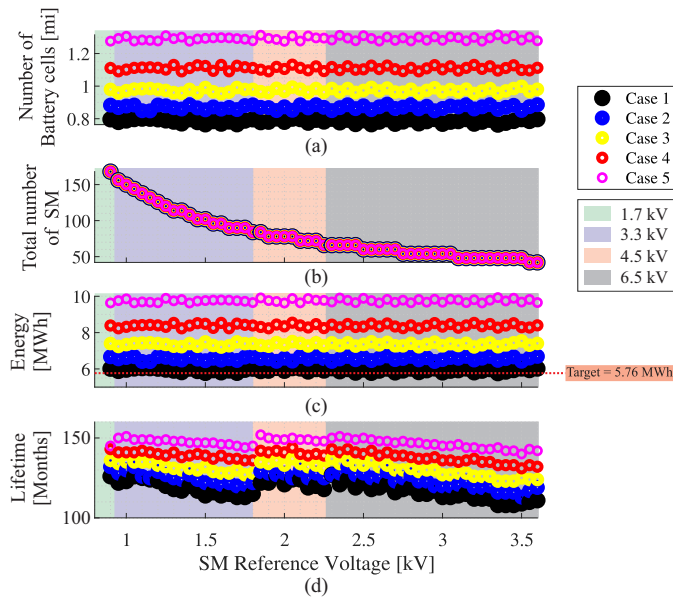


Figure 54 – System configuration according to the variation of the reference voltage and SOC for two-stage approach for customized solution: (a) Number of battery rack; (b) Number of SM; (c) Total system energy and (d) Battery lifetime.

the total cost is displayed in Figure 55 (d). For the IGBT of 1.7 kV and 3.3 kV, Case 1 presented the lowest costs. As for the IGBT of 4.5 kV and 6.5 kV, Case 5 is the ideal cost option.

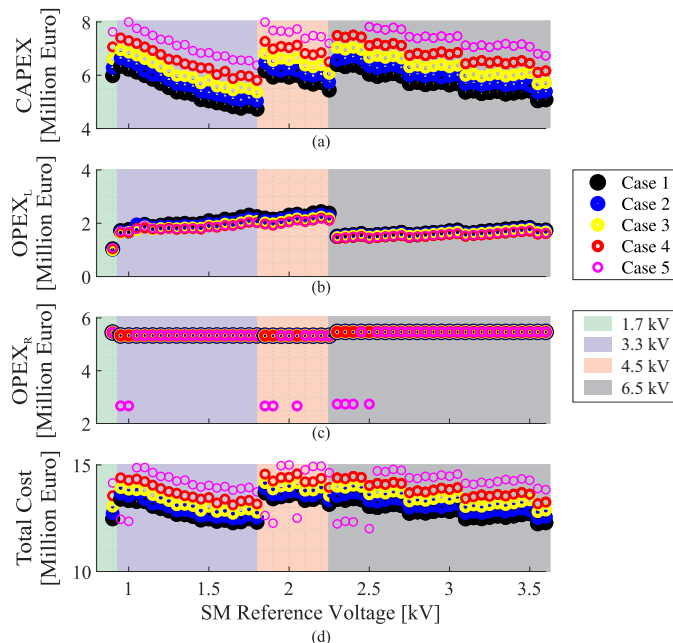


Figure 55 – Estimated costs for all case studies evaluated for the customized two-stage approach: (a) CAPEX; (b) OPEX_L; (c) OPEX_R (d) Total costs

Table 10 presents the designs that have the lowest costs for each IGBT blocking voltage. In addition, the design considered the overall great is highlighted. For the IGBT of 6.5 kV, Case 5 shows an estimated cost of €12.01 million.

Table 10 – Best Cases for Each Blocking Voltage - (Two-Stage customized solution).

Rated Blocking Voltage [kV]	SM Reference Voltage [kV]	Case Study	Total Cost [mi Euros]
1.7	0.9	1	12.47
3.3	1.65	1	12.29
4.5	1.9	5	12.27
6.5	2.5	5	12.01

Figure 56 shows the percentage of each item in the total cost of the best design for a two-stage approach in the custom solution. CAPEX occupies the largest share of the total cost and, moreover, is higher when compared to single-stage. This is due to the increase in the number of semiconductors, the IGBT blocking voltage (in the two-stage it is higher) and the number of batteries.

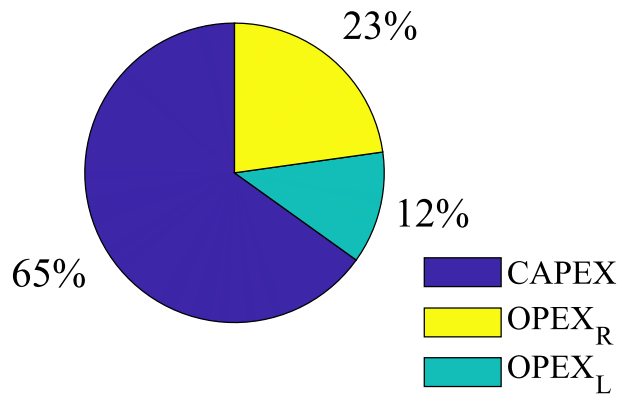


Figure 56 – Separate costs for best design.

5.2.1 Two-Stage Approach Standard Solution

According to Figure 57 (a), as the reference voltage increases, $N_{s,bat}$ remains constant until the quantity is rounded to the next integer. In the same way $N_{p,bat}$ shown in Figure 57 (b). The $N_{p,bat}$ varies depending on the need to fulfill the power and energy requirements.

In the standard solution, rounding in $N_{s,bat}$ and $N_{p,bat}$ is more evident. According to Figure 58 (a), the number of batteries, in an SM reference voltage, is the same for different case studies. Also, as discussed in customized, the SM total is the same across all case studies, Figure 58 (b).

In the two-stage approach, the degree of freedom provided by the dc/dc converter allows to analysis of different SM reference voltages. In this way, some designs are close to the energy target, as seen in 58 (c). Finally, 58 (d) shows the lifetime of the batteries. Note that some projects already have a longer lifetime than the customized solution.

The costs of all case studies for two-stage approach were estimated, as shown in Figure 59. The costs related to CAPEX are shown in Figure 59 (a). As the number of SM

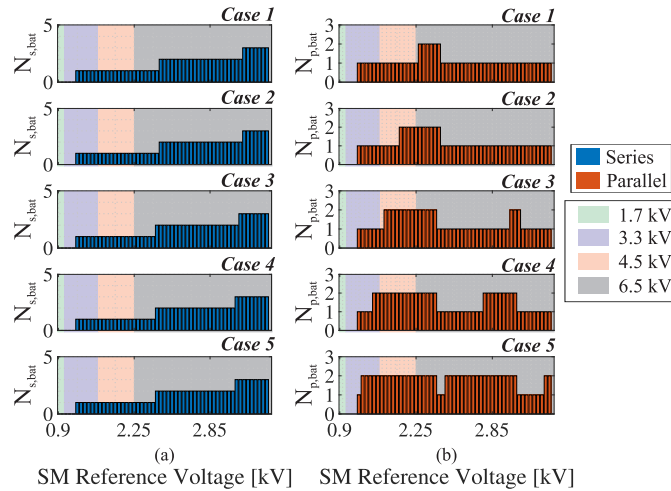


Figure 57 – Battery rack configuration in a single SM according to the variation of the v_{SM}^* and the allowed SOC range for the two-stage approach and standard solution. (a) number of battery in series (b) number of strings

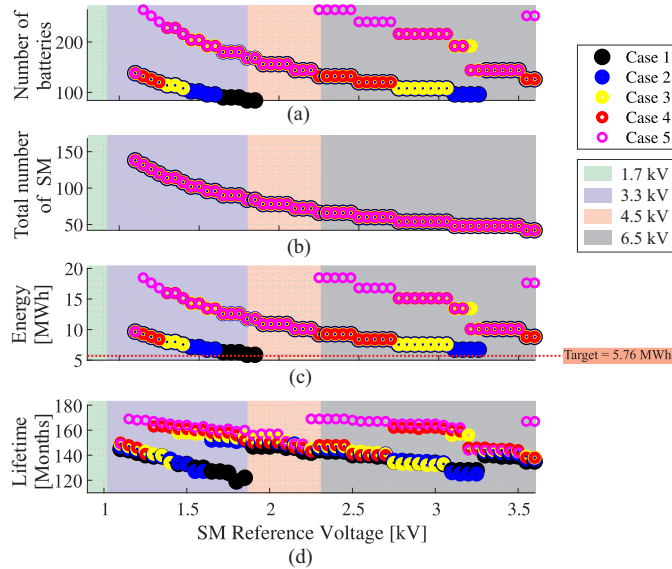


Figure 58 – System configuration according to the variation of the reference voltage and SOC for two-stage approach and standard solution: (a) number of battery rack; (b) number of SM and (c) total system energy.

is equal between the cases, the number of battery rack is the variable that differentiates the costs between the cases.

The $OPEX_L$ of each project is shown in Figure 59 (b). When compared to the custom model, costs are more adjusted between cases. One of the reasons is the size of the dc/dc converter inductor. Because of rounding, the inductor size is the same for cases with the same reference voltage.

The costs for replacing the battery rack, $OPEX_R$, are shown in Figure 59 (c). Note that most Case 5 designs required only one battery replacement. This balance between the number of battery racks and replacements is important for the total cost of projects.

Thus, Figure 59 (d) presents the total costs for the projects analyzed.

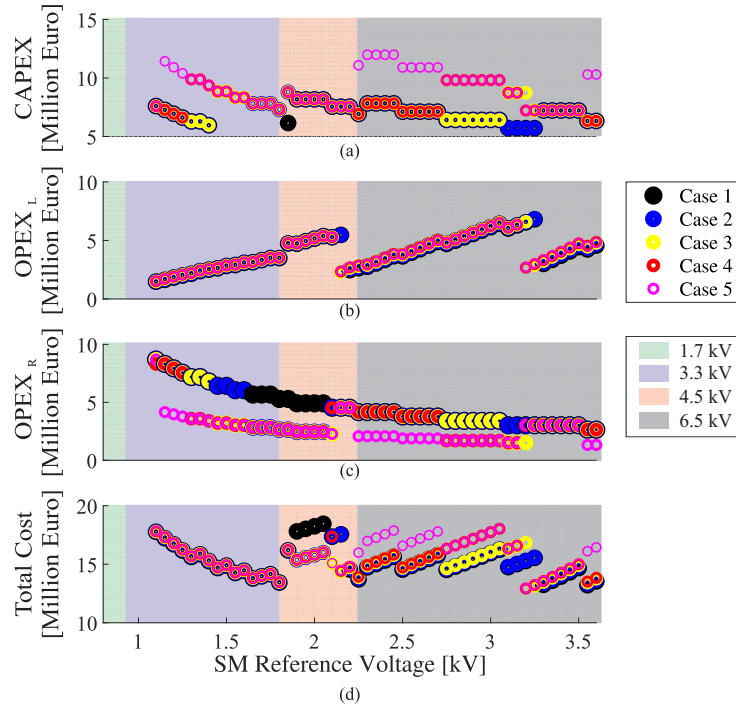


Figure 59 – Estimated costs for all evaluated case studies: (a) CAPEX; (b) OPEX; (c) Total Costs and (d) The best designs (lowest cost).

Figure 60 presents an analysis of the mechanisms that cause battery degradation. These results are from Case 1 for the IGBT blocking voltage of 4.5 kV ($v_{SM}^* = 2.25$ kV). The same behavior for the customized and standard solution seen in the single-stage approach can be analyzed for the two-stage approach. However, some models in the two-stage approach may have a shorter lifetime than the single-stage one because the dc/dc converter allows for more simplified designs.

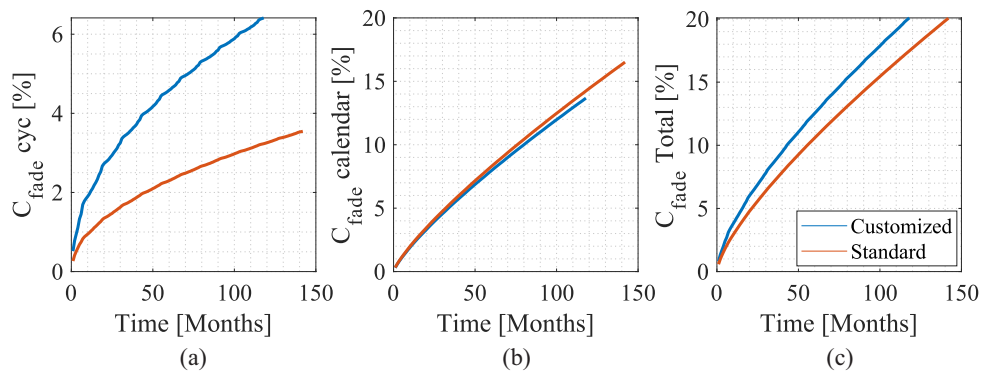


Figure 60 – Comparison between customized and standard solutions in the two-stage approach according to fading: (a) Cycling (b) calendar (c) total.

Table 11 presents the designs that have the lowest costs for each IGBT blocking voltage. In addition, the design considered the overall great is highlighted. For the 6.5 kV IGBT, Case 4 shows an estimated cost of €12.93 million.

Table 11 – Best Cases for Each Blocking Voltage - (Two-Stage standard solution).

Rated Blocking Voltage [kV]	SM Reference Voltage [kV]	Case Study	Total Cost [mi Euros]
3.3	1.8	1	13.44
4.5	2.25	1	13.71
6.5	3.2	4	12.93

5.3 Discussions

Table 12 presents the best design of the customized and standard solutions for the single-stage and two-stage approaches. In the customized solution, the single-stage approach has the lowest total cost. The blocking voltage and the higher number of semiconductor devices contributed to the two-stage approach presenting a cost of approximately 34 % higher. In both approaches, the project with the lowest total cost, called in this work the best project, are the cases that present greater energy oversizing. Consequently, a higher cost for projects. However, energy oversizing influences the lifetime of batteries. Therefore, cases with higher energy oversizing require fewer battery replacements.

The standard solution uses IGBT with a higher blocking voltage than the customized solution, and the selected case studies are the ones with the smallest SOC range. Unlike the customized solution, the optimized options are for cases that have the lowest energy oversizing. Also, due to rounding, some cases have the same number of batteries and/or SM. For example, in the standard single-stage approach, the best options are Cases 3, 4, and 5.

Finally, as discussed in Chapter 4, the temperature rise in the two-stage approach is smaller than in the single-stage approach, which can affect battery lifetime. However, in the standard solution, the selected results of the two-stage approach present a lower battery lifetime than the single-stage approach. This fact is justified by the two-stage approach having less energy oversizing. This fact shows that the comparison of both systems is not straightforward. Therefore, the proposed methodology can support the decision-making procedure.

Table 12 – Cost and energy losses analysis for the best cases.

Customized solution			
Approach	V_{ps} [kV]	Total Cost [mi Euro]	E_O [MWh]
Single-stage	3.3	9.74	0.082
Two-stage	6.5	12.01	4.12
Standard solution			
Single-stage	6.5	13.29	5.58 *
Two-stage	6.5	12.93	4.32

*Battery lifetime for case studies 3,4 and 5.

5.4 Conclusion

In this chapter the figures of merit related to the designs for the two approaches: single-stage and two-stage. In addition, two project solutions were considered: customized and standard solutions. For all projects, five case studies were considered, which were defined by SOC ranges. After calculating all projects, cell and battery lifetime analyses were performed. In addition, the power losses of each project were estimated, considering an operating period of 25 years. In this way, the total costs for each design were obtained. Finally, in Chapter 6 presents the simulation of the designs with the lowest costs for each approach. In this way, the selected cases are for the customized solution.

6 MMC-based BESS Simulation Analysis

In Chapter 3, the control strategy for the single-stage and two-stage approaches was presented. The concepts acquired in Chapter 3 were fundamental to calculating the losses in the converters, which are directly linked to the total costs of each design. Indeed, in Chapter 5 the lowest cost designs are presented. Therefore, this Chapter aims to validate the control tuning and simulate the operation of the MMC-based BESS for the optimal cases presented in Chapter 5. The results for the charging and discharging of the batteries are evaluated.

6.1 Case Study

As discussed in Chapter 5, the optimized designs are from the customized solution. The parameters of single-stage and two-stage approaches are shown in Table 13.

Table 13 – Design parameters for simulation

V_{ps} [kV]	v_{SM}^* [kV]	Total number of SM	$N_{s,bat}$	$N_{p,bat}$	Total number of IGBT	Case Study
Single-Stage Approach						
3.3	1.8	114	512	13	228	1
Two-Stage Approach						
6.5	2.5	60	682	32	240	5

The main battery cell ANR26650M1-B manufactured by A123 systems is presented in Table 14.

Table 14 – Parameters of the battery cell ANR26650M1-B (A123 Systems, 2012).

Parameters	E_n	C_n	C-Rate	SOC_{MAX} [100 %]	SOC_{MIN} [0 %]
Value	0.0076 MWh	2.5 Ah	1	3.4 V	2.5 V

The MMC-based BESS input parameters studied in this work are presented in Table. 15.

Table 15 – Parameters of the MMC-based BESS.

Parameters	Value
Rated apparent power (S_n)	10.9 MVA
Total energy storage (E_n)	5.76 MWh
Output voltage (line to line) (V_g)	13.8 kV
Grid frequency (f_n)	60 Hz
Arm reactance (x_{arm})	0.15 pu
Switching frequency of the HB (f_c)	270 Hz
Sampling time (T_{sw}) - Single-Stage	123.45 μ s
Sampling time (T_{sw}) - Two-Stage	185.19 μ s

6.2 Dynamic performance analysis of controllers

In order to validate the methodology applied in Chapter 3, this section performs frequency analysis (Bode Diagram) and step response for the controller designs of the single-stage and two-stage approaches. Note that for each control strategy the results for the single-stage and for the two-stage are presented. This analysis aims to show that the presented methodology applies to different MMC-based BESS projects.

6.2.1 Frequency Analysis

Figure 61 shows the open-loop Bode diagram for output current control. In Figure 61 (a) shown the Bode plot for single-stage approach. The control features a gain margin of 9.93 dB at 1.33 kHz and a phase margin of 57.6° at 409 Hz. Furthermore, we can see the effect of using the resonant controller in the 60 Hz range, as shown in Eq. (3.6).

Figure 61 (a) shows the Bode plot for two-stage approach. The control features a margin gain of 9.86 dB at 878 Hz and a phase margin of 54.8° at 274 Hz. Note that the phase margin is smaller than that of the single-stage approach, this is because the bandwidth depends on the number of SM.

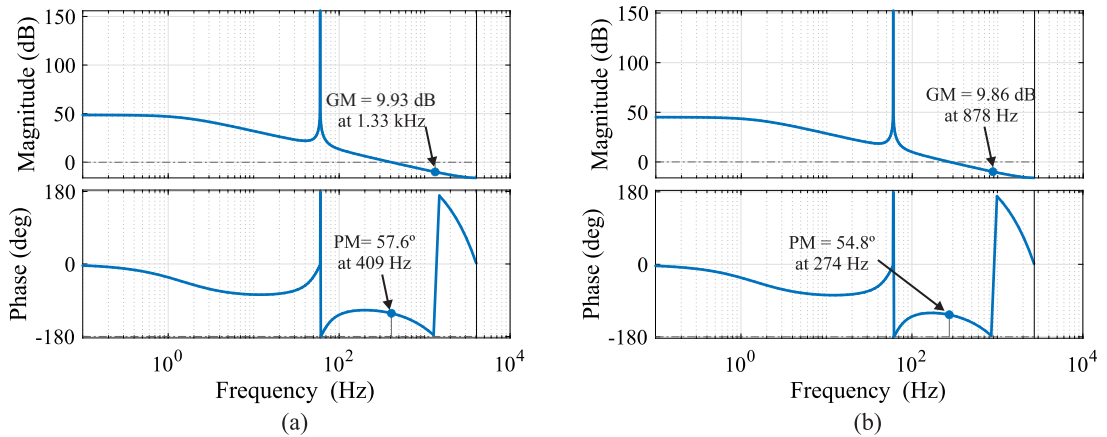


Figure 61 – Output current controller open loop Bode diagram plot: (a) single-stage approach and (b) two-stage approach.

According to Figure 27, in the global SOC, the control strategy used considers the internal loop of the output current and the external loop of the global SOC control. According to Figure 62 (a), in the single-stage approach, the control has a gain margin of 75.4 dB at 4.05 kHz and a phase margin of 85.3° at 0.441 Hz. In the two-stage approach, shown in Figure 62 (b), the control has a gain margin of 77.9 dB at 2.7 kHz and a phase margin of 85.3° at 0.221 Hz. Two Bode diagrams are presented: in the solid line, considering the ideal internal current loop (gain = 1), and, in the dashed line, considering the insertion of the internal current loop. Note that for high frequencies the curves are not similar. This is due to the fact that it is above the current loop cutoff frequency.

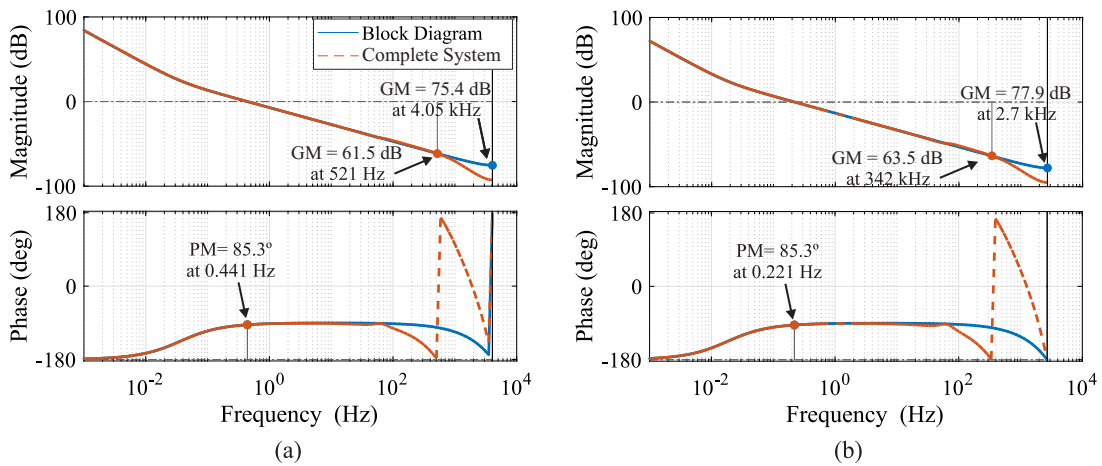


Figure 62 – Output global SOC controller open-loop Bode plot: (a) single-stage approach and (b) two-stage approach.

The open loop Bode diagram of the circulating current control for the single-stage approach is shown in Figure 63 (a). The system frequency response has a stable response at 241 Hz. The two-stage approach presented in Figure 63 (b) the system response frequency has a stable response at 121 Hz. Furthermore, according to Eq. (3.20), the resonant control used is allocated at 60 Hz, 120 Hz and 240 Hz.

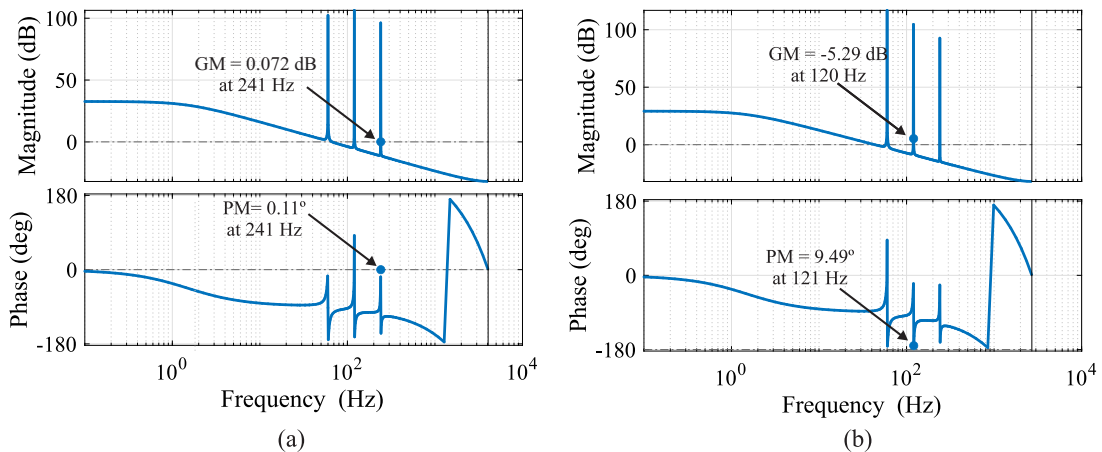


Figure 63 – Circulating current controller open-loop Bode diagram: (a) single-stage approach and (b) two-stage approach.

In the leg-balancing control, the external loop has the total SOC per phase as input. The controller output sends a current reference to the internal circulating current loop. Considering that the external loop has slower dynamics than the circulating current loop, the leg-balancing control is allocated to four decades of the circulating current control. The system has a gain margin of 95.4 dB at 4.05 kHz and a phase margin of 85.3° at 0.0442 Hz. Figure 64 (a) show the Bode diagram for the ideal and non-ideal system for single-stage approach. Note that for low frequencies the behavior is the same. However, for frequencies greater than the current loop cutoff frequency, the behavior does not follow the ideal loop. In two-stage approach, shown in Figure 64 (b), a gain margin of 97.9 dB at 2.7 kHz and a phase margin of 85.3° at 0.0221 Hz.

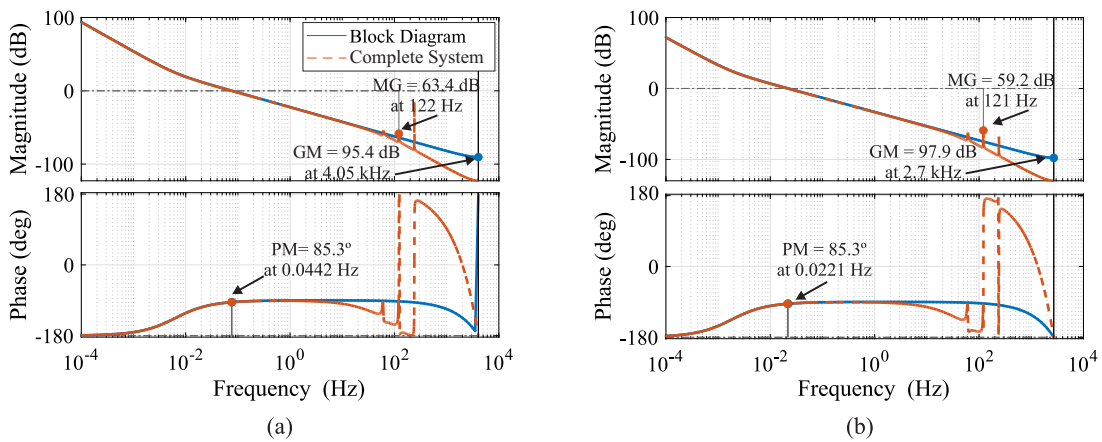


Figure 64 – Leg-balancing controller open-loop Bode plot: (a) single-stage approach and (b) two-stage approach.

The control strategy considers an internal loop of circulating current with the fastest dynamics and the SOC external loop with the slower dynamics. The open-loop frequency response of the arm-balancing control is shown in Figure 65. Considering that the external loop has slower dynamics than the circulating current loop, the arm-balancing control is allocated to three decades of the circulating current control.

According to the Bode plot in Figure 65 (a), the single-stage approach has a gain margin of 76.2 dB at 4.05 kHz and a phase margin of 90° at 0.4 Hz. In the two-stage approach, in Figure 65 (b) a gain margin of 78.7 dB at 4.05 kHz and a phase margin of 90° at 0.2 Hz. Comparing the frequency response of ideal and non-ideal systems, we observe similar behavior within the frequency range of the controllers.

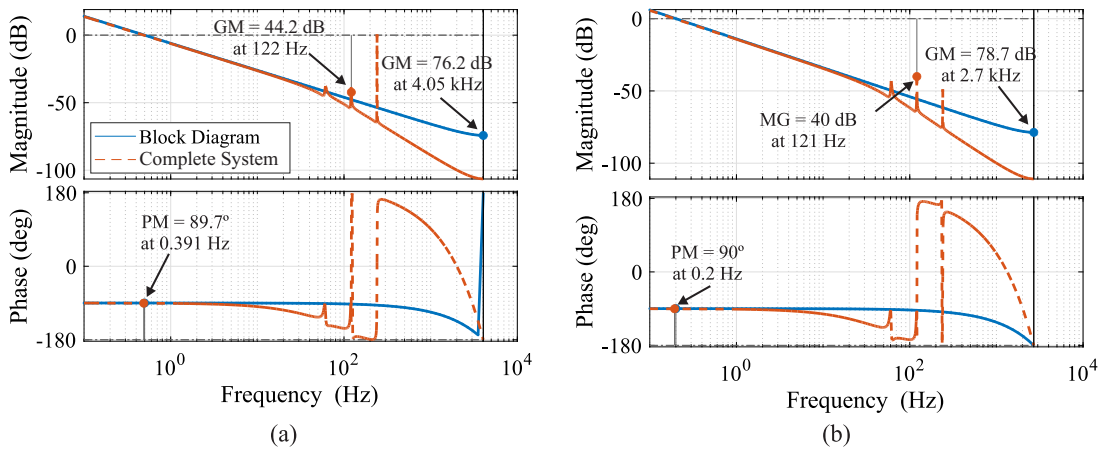


Figure 65 – Arm-balancing controller open-loop Bode diagram: (a) single-stage approach and (b) two-stage approach.

Figure 66 (a) shows the frequency response for the open-loop transfer function of the individual SOC balancing control in single-stage approach. The system has a gain margin of 44 dB at 1.35 kHz and a phase margin of 0° at 0 Hz. In Figure 66 (b) is show the Bode plot for the two-stage approach. The system has a gain margin of 64 dB at 900 Hz and a phase margin of 0° at 0 Hz.



Figure 66 – Individual SOC balancing controller open-loop Bode diagram: (a) single-stage approach and (b) two-stage approach.

The two-stage approach, in addition to the MMC strategies, adds the dc/dc converter. The control strategy is performed with an internal current loop and an external voltage loop. The switching frequency of the converter is 1000 Hz. Therefore, the converter is designed with a bandwidth of 50 Hz. Usually, values around $f_{sw}/20$ are employed (Gomes; Cupertino; Pereira, 2018). Figure 67 shows the Bode plot for the internal current loop of the dc/dc converter.

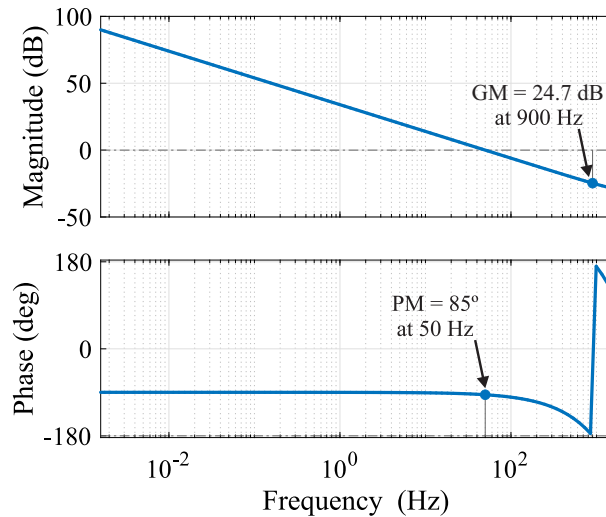


Figure 67 – Current controller open-loop Bode diagram.

The external voltage loop of the dc/dc converter is designed for 6 Hz. This loop must be slower than the current loop. Furthermore, to improve steady-state response, **MAF** is used. Figure 68 presents the Bode plot comparing the frequency response of the system considering the ideal and non-ideal internal current loop. Note that for frequencies below 21.6 Hz the systems have the same behavior.

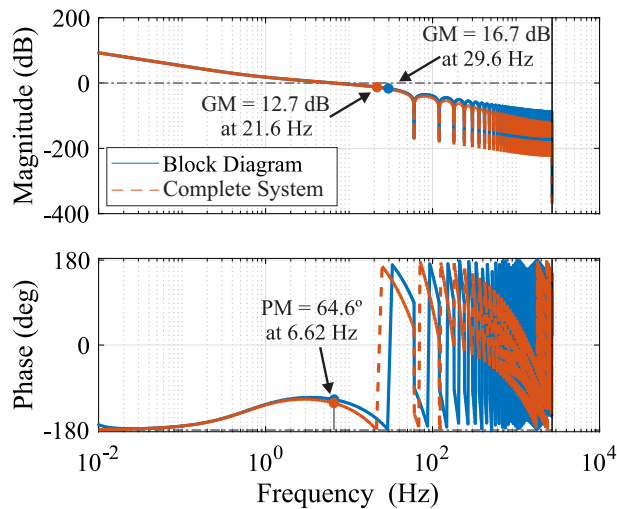


Figure 68 – Voltage controller open-loop Bode diagram.

6.2.2 Dynamic Response

The performance of the output current controller in tracking a sinusoidal reference is evaluated in a 0.30 s simulation. According to Figure 69, up to 0.15 s, the reference is zero, after which a unit reference is given. In Figure 69 (a) the behavior of the single-stage approach is presented. Figure 69 (b) presents the dynamics of the two-stage approach. Note that both approaches need, approximately, 0.02 s to follow the reference.

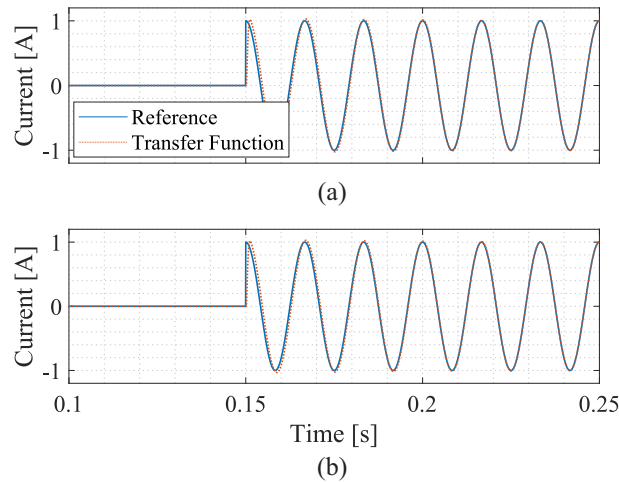


Figure 69 – Output current controller step response: (a) single-stage approach and (b) two-stage approach.

Figure 70 presents the step response for the closed-loop global SOC system considering the ideal and non-ideal systems. With slower dynamics than the output current control, the global SOC control needs approximately 2.5 s to reach the reference in single-stage approach, Figure 70 (a), and 3.5 s in two-stage approach, Figure 70 (b).

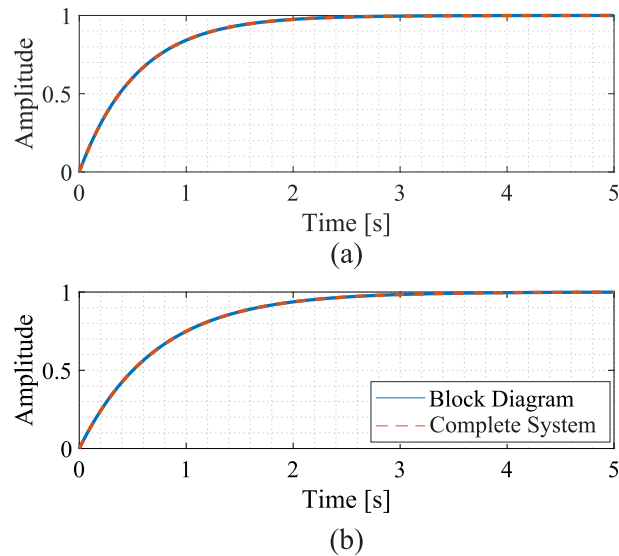


Figure 70 – Global SOC controller step response: (a) single-stage approach and (b) two-stage approach.

The performance of the circulating current controller in tracking a sinusoidal reference is evaluated for the single-stage and two-stage approaches respectively in Figures 71 (a) and Figures 71 (b). The sinusoidal reference below presents the fundamental, second and fourth order harmonic components with unity amplitudes and 0 phase. Note that the control tuning allows the circulating current to follow the reference as desired.

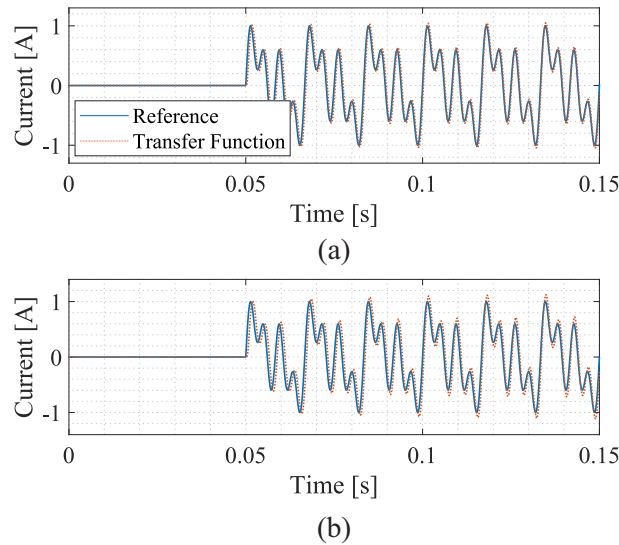


Figure 71 – Circulating current controller step response: (a) single-stage approach and (b) two-stage approach.

Figure 72 (a) and Figure 72 (b) the closed-loop response of the leg-balancing control to a step reference for the single-stage and two-stage approaches, respectively. Note that with slower dynamics than circulating current control, in the single-stage approach it takes 15 s to reach the reference. In the two-stage approach, 30 s is required.

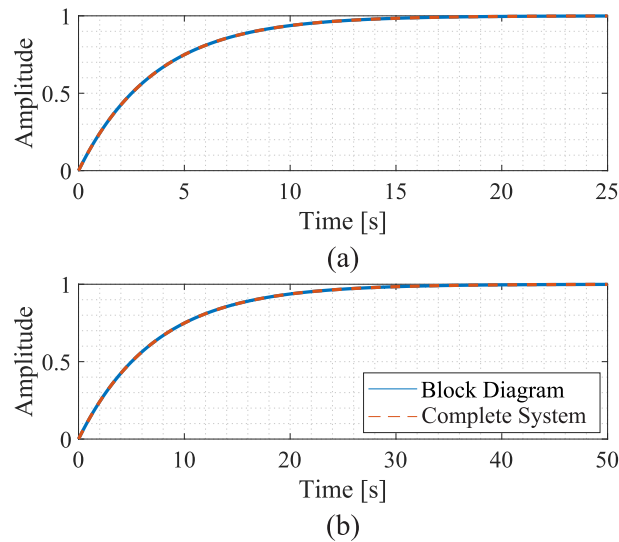


Figure 72 – Leg-balancing controller response: (a) single-stage approach and (b) two-stage approach.

The step response for the closed-loop transfer function comparing ideal and non-ideal systems in arm-balancing control is shown in Figure 73. Note that the behavior for both systems is the same. According to Figure 73 (a), in the single-stage approach, it takes 1.5 s, while in the two-stage approach, Figure 73 (b), it takes 3.5 s to reach the reference.

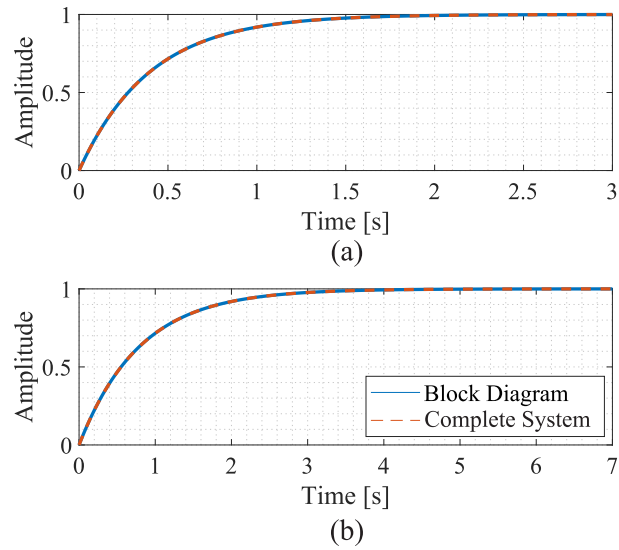


Figure 73 – Arm-balancing controller step response: (a) single-stage approach and (b) two-stage approach.

Figure 74 shows the step response for the closed-loop of the individual balance control SOC. In the single-stage approach, Figure 74 (a), needs approximately 0.8 s to reach the unit reference. In the two-stage approach, Figure 74 (b), 1.2 s is required.

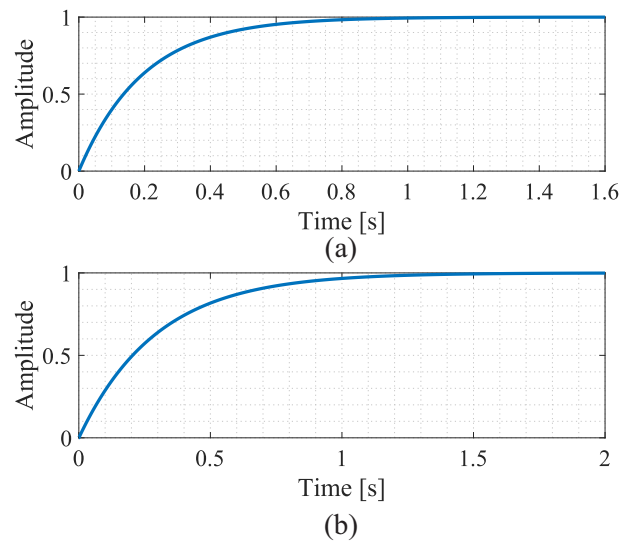


Figure 74 – Individual SOC balancing controller step response: (a) single-stage approach and (b) two-stage approach.

Figure 75 shows the step response for the current control of the dc/dc converter. Note that the system needs 0.02 s to reach the reference.

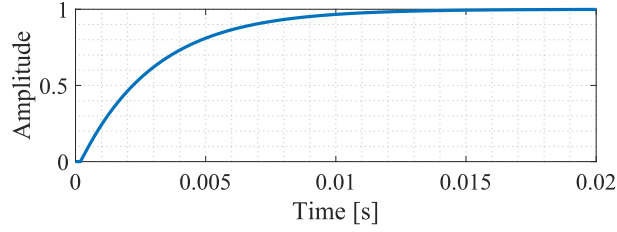


Figure 75 – Current controller step response in dc/dc converter.

Figure 76 shows the step response of closed loop voltage control. The system needs approximately 60 ms to reach the reference.

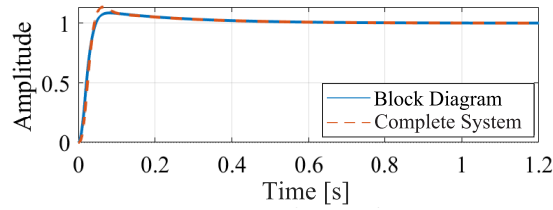


Figure 76 – Current controller step response in dc/dc converter.

In order to summarize the results above, Table 17 presents the frequencies chosen for each control in the single-stage and two-stage approaches.

Table 16 – Frequency bandwidth for the MMC-based BESS.

Frequencies	Single-Stage	Two-Stage
$f_{c1,s}$	0.4 Hz	0.2 Hz
$f_{c2,s}$	0.04 Hz	0.02 Hz
α_{gc}	405 Hz	270 Hz
α_{hg}	37.69 Hz	37.69 Hz
α_{cc}	405 Hz	270 Hz
α_{hc}	37.69 Hz	37.69 Hz
$f_{c1,l}$	0.04 Hz	Hz 0.02
$f_{c2,l}$	0.004 Hz	Hz 0.002
$f_{c,b}$	0.81 Hz	0.54 Hz
$f_{c,A}$	0.4 Hz	0.2 Hz
f_i	-	50 Hz
$f_{c1,d}$	-	6 Hz
$f_{c2,d}$	-	0.72 Hz

Finally, the gains of the controllers used in the simulations for the single-stage and two-stage approaches are shown in Table 17.

6.3 Results

Based on the above parameters, the simulation results of the MMC-based BESS will be presented in the next subsections. All analyses were performed using the PLECS software. The results of the simulations are divided into two process: charge and discharge batteries.

Table 17 – Controller parameters of the MMC-based BESS.

Control Tuning	Parameter	Single-Stage	Two-Stage	Units
$k_{P,G} = \alpha_{gc}L_{eq}$	$K_{P,G}$	5.8972	3.9315	Ω
$k_{R,G} = 2\alpha_{hg}k_{P,G}$	$K_{R,G}$	1396.9	148.21	Ω/s
$k_{P,S} = \frac{2\pi(f_{c1,s} + f_{c2,s})}{K_S}$	$K_{P,S}$	1202.7	922.37	A
$k_{I,S} = \frac{4\pi^2 f_{c1,s} f_{c2,s}}{K_S}$	$K_{I,S}$	274.80	105.37	A/s
$k_{P,C} = \alpha_{cc}L_{arm}$	$K_{P,C}$	1.8771	1.2514	Ω
$k_{R,C} = 2\alpha_{hc}k_{P,C}$	$K_{R,C}$	7.50	5.0057	Ω/s
$k_{P,L} = \frac{2\pi(f_{c1,l} + f_{c2,l})}{K_L}$	$K_{P,L}$	27.50	21.090	A
$k_{I,L} = \frac{4\pi^2 f_{c1,l} f_{c2,l}}{K_L}$	$K_{I,L}$	0.628	0.24094	A/s
$k_{P,A} = \frac{2\pi f_{c,A}}{K_A}$	$K_{P,A}$	546.70	419.26	A
$K_{I,B} = \frac{8\pi f_{c,b} C_n}{\hat{I}_s}$	$K_{I,B}$	0.0272	0.181	V
$k_{P,W} = 2\pi f_i L_{dc}$	$K_{P,W}$	-	10.497	Ω
$k_{I,W} = 2\pi f_i R_L$	$K_{I,W}$	-	0.31416	Ω/s
$k_{P,R} = \frac{2\pi(f_{c1,d} + f_{c2,d})}{K_k}$	$K_{P,R}$	-	0.375	S
$k_{I,R} = \frac{4\pi^2 f_{c1,d} f_{c2,d}}{K_k}$	$K_{I,R}$	-	1.51	S/s

6.3.1 Charging Procedure

In the battery charge process, the simulation time is 250 s. In the beginning, the arm-balancing control is disabled. Then, at $t = 20$ s, this controller is activated. To validate the SOC arm-balancing control, the upper arms of each phase start with a SOC 1 % greater than those of the lower arm. At $t = 130$ s, a step in the SOC is applied from 52 % to 55 %. Furthermore, in the loading process, the balance control of the leg is deactivated, because the global SOC control is responsible for the balance of the battery SOC.

6.3.1.1 Single-Stage Approach

Figure 77 (a) presents the SOC behavior in phase A and the average SOC for the three phases. The SOC in the arm are not spread out and within the tolerance range of 1

%. Figure 77 (b) shows the average SOC of the arms of each phase. As observed, before 20 s, there is no balancing of the arms. After, the energy balance control is activated and the SOC average become balanced.

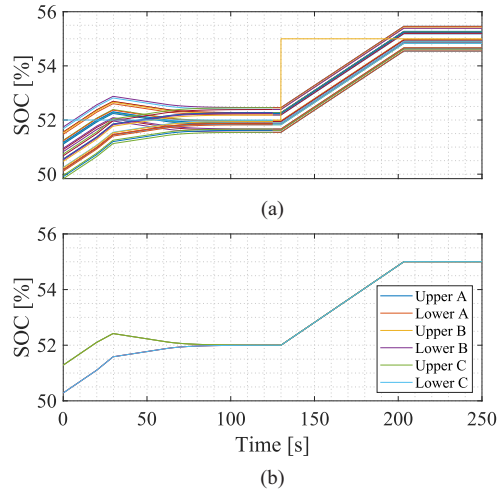


Figure 77 – SOC behavior during the charging process: (a) SOC phase A and (b) average SOC.

Active and reactive powers during the charging process are analyzed in Figure 78 (a). As observed, the reactive power is controlled to zero, while active power is defined by the global SOC control. When the SOC reaches the reference value, the active power reduces to a value close to zero. The grid current follows the behavior of the active power, as shown in Figure 78 (b). According to Figure 78 (c) shows a zoomed view of the grid current, which is practically sinusoidal. The Total Harmonic Distortion (THD) at this operating point is 0.1 %.

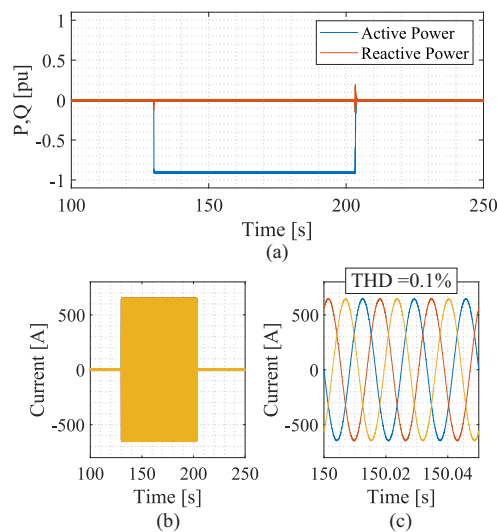


Figure 78 – Dynamic behavior during the battery charging process: (a) Active and reactive power, (b) grid current and (d) zoomed view of the grid current.

As seen in the previous Figure 77, before the SOC balance control operates, the current and the variation in the current reference of one phase affects the others, as shown

in Figure 79. Figure 79 (b) shows the transient in the circulating current. Due to imbalances between the SOC, ac components can be visualized. Finally, Figure 79 (c) shows a zoom in on the circulating current at steady-state instants.

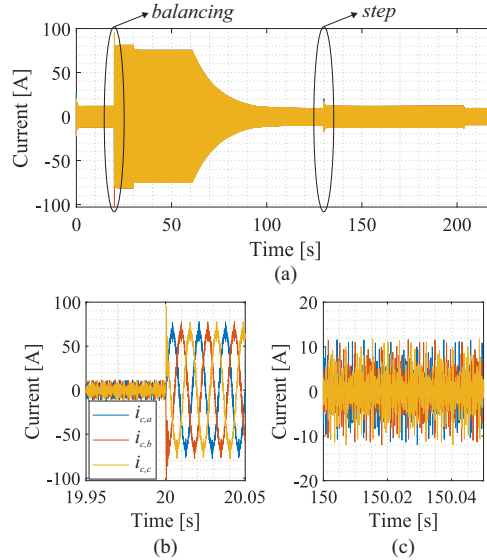


Figure 79 – Dynamic behavior of the circulating current during the charging process: (a) circulating current; (b) zoomed view on transitory state; (c) zoomed view on steady state.

6.3.1.2 Two-Stage Approach

For the development of two-stage topology simulations, the same initial conditions of the single-stage approach are considered. As seen in Figure 80 (a), a step of is applied to the SOC. The response time is actually slower than in the single-stage approach. However, it is important to note that in the two-stage the v_{SM} is controlled to a reference value, in the single-stage the v_{SM} is equivalent to the voltages of the associated batteries.

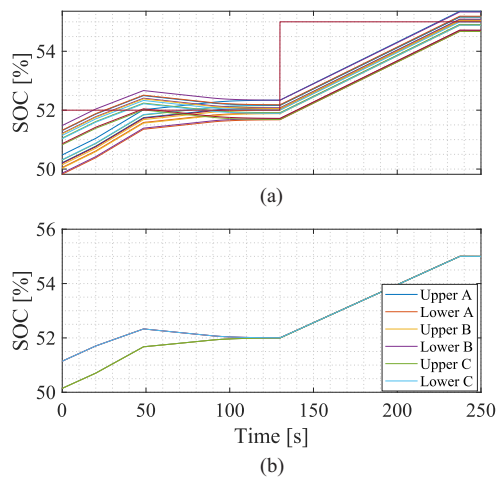


Figure 80 – SOC behavior during the charging process: (a) SOC phase A and (b) average SOC.

In addition, Figure 80 (b) shows the average SOC of each arm. When controlling the balance of the arms, the average value of all arms is in the reference value. Comparing with the single-stage approach, the amount of SM is smaller, requiring less energy to be controlled. With this, a faster balance of SOC is observed, without many variations.

Figure 81 (a) shows active and reactive powers during the charging process. The reactive power is controlled to zero, while active power is defined by the global SOC control. When the SOC reaches the reference value, the active power reduces to a value close to zero. Figure 81 (b) show the grid current follows the behavior of the active power. According to Figure 81 (c) shows a zoomed view of the grid current, which is practically sinusoidal. The THD at this operating point is 1 %.

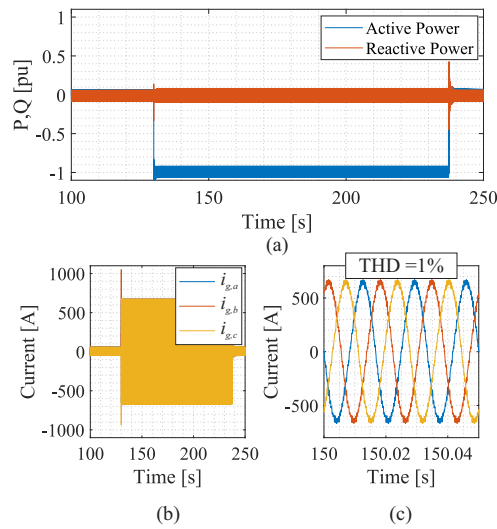


Figure 81 – Dynamic behavior during the battery charging process: (a) Active and reactive power, (b) grid current and (d) zoomed view of the grid current.

Figure 82 (a) shows the behavior of the circulating currents of the three phases of the MMC-based BESS. The transient in 20 s is due to the independent control of the energy levels of each arm. Figure 82 (b) shows a zoomed-in on the simulation transient. By not having balanced the SOC, ac-components can be visualized in the transient. Finally, in Figure 82 (c) a zoomed-in the steady-state instant is shown. Note that the average change in current in the three phases tends to zero.

The dynamic voltage response in the upper arm capacitors of phase A is shown in Figure 83. The reference voltage for the dc/dc converter is 2.5 kV. According to Figure 83 (a), the voltage is close to the reference until the instant of 130 s in which a variation of SOC is applied to the system. After the system reaches the SOC reference, the voltage stabilizes at the 2.5 kV reference. In Figure 83 (b) the transient is zoomed when the SOC step is applied. Finally, Figure 83 (c) shows a zoomed-in voltage when entering a steady state. Note that the average voltage is within the reference value. A transient is observed during the active power step. As observed, a slow response is observed in the

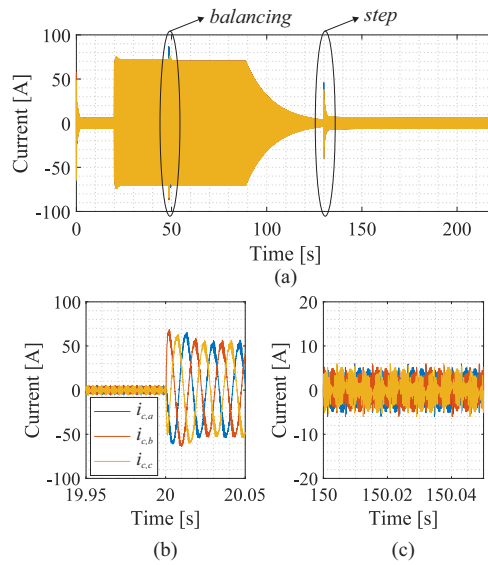


Figure 82 – Dynamic behavior of the circulating current during the charging process: (a) circulating current; (b) zoomed view on transitory state; (c) zoomed view on steady state.

voltage control, probably due to the moving average filter, which limits the voltage-loop bandwidth.

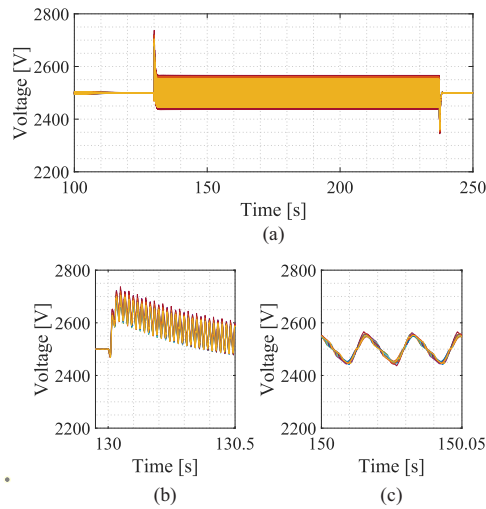


Figure 83 – Dynamic response to the dc/dc converter voltage controller: (a) During the charging process, (b) zoomed in transient voltage (d) zoomed view in steady state.

6.3.2 Discharge Procedure

In the battery discharge process, the simulations started with the initial conditions of the previous tests. However, for the discharge process, global SOC control is disabled, while leg-balancing control is enabled. At the instant $t = 130$ s, the negative step is applied after the system reaches steady-state. Therefore, the grid current reference is computed based on equation (3.1).

6.3.2.1 Single-Stage Approach

In the battery discharge process, the simulations started with the initial conditions of the previous tests. However, for the discharge process, global SOC control is disabled, while leg-balancing control is enabled. At the instant $t = 130$ s, the negative step is applied after the system reaches steady-state. Therefore, the grid current reference is computed based on equation (3.1).

Figure 84 shows the behavior of the SOC of the MMC-based BESS in the battery discharge process. The individual SOC of phase A maintains the same behavior presented before the discharge. Because the SOC control is disabled, small mirroring can be seen in the average SOC of the converter, Figure 84 (b).

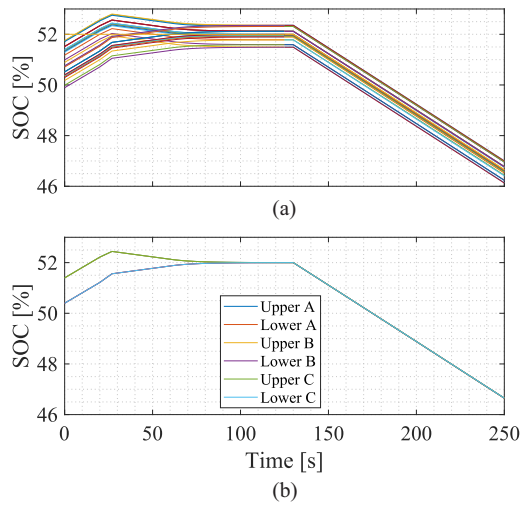


Figure 84 – SOC behavior during the discharging process: (a) SOC phase A and (b) average SOC.

Figure 85 (a) shows the dynamic behavior of the instantaneous active power injected into the grid for the single-stage approach. As observed, the converter injects 1 pu of active power during the discharge process. Figure 85 (b) shows the output current response. As noted in Figure 85 (c), during battery discharge the peak current is, approximately, 600 A.

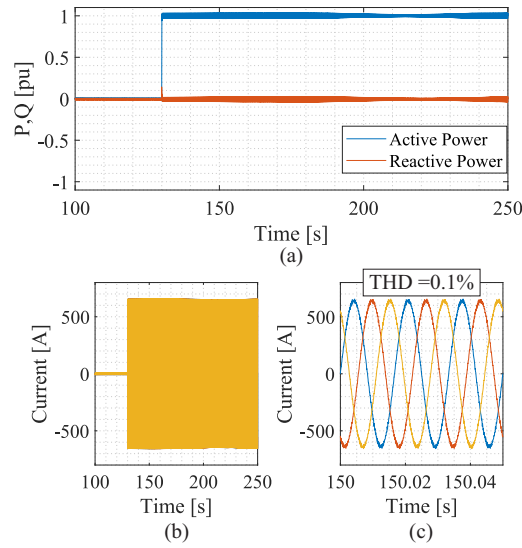


Figure 85 – Dynamic behavior during the battery discharging process: (a) Active and reactive power, (b) grid current and (d) three phases grid current.

6.3.2.2 Two-Stage Approach

In the discharging process for the two-stage approach, the SOC starts more spread out when compared to the single-stage approach. However, they get closer when starting the discharge process, as seen in Figure 86 (a). In addition, the average SOC of each arm can be analyzed using Figure 86 (b). When comparing with single-stage, the discharge rate of the two-stage is higher. This is because the battery current reference is controlled by the dc/dc converter.

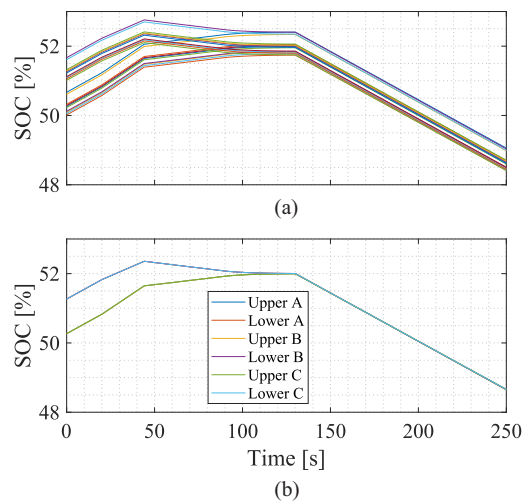


Figure 86 – SOC behavior during the discharging process: (a) SOC phase A and (b) average SOC.

As previously mentioned, when disabling the global SOC control for the discharge process, the current reference for the system is the one that allows to obtain the maximum reference of active power (1 pu). Thus, Figure 87 (a) shows the behavior of the active and reactive powers during the discharge of the batteries. Finally, Figure 87 (b) shows

the output current of the converter. The moment the batteries are being charged, the amplitude of the currents reaches 580 A, as seen in the zoom in Figure 87 (c).

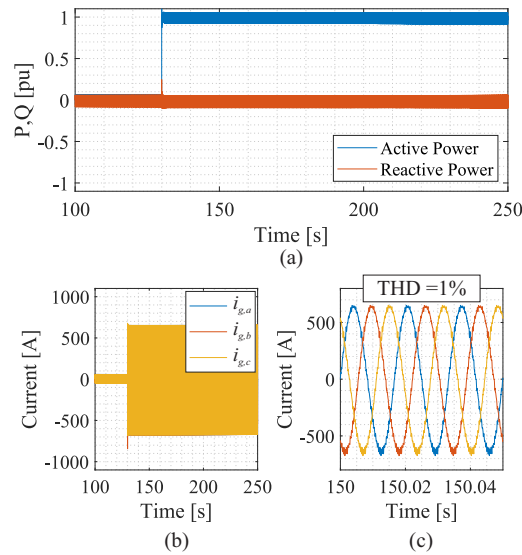


Figure 87 – Dynamic behavior during the battery discharging process: (a) Active and reactive power, (b) grid current and (d) three phases grid current.

6.3.3 Current Behavior in the Batteries

An important analysis for comparing topologies is the current behavior in the batteries. Figure 88 (a) shows the current behavior during the charging process for the single-stage approach. Analyzing the current spectrum in Figure 88 (c), low-frequency components with high amplitudes are observed. The fundamental and second harmonic components are the most significant in the battery current harmonic spectrum.

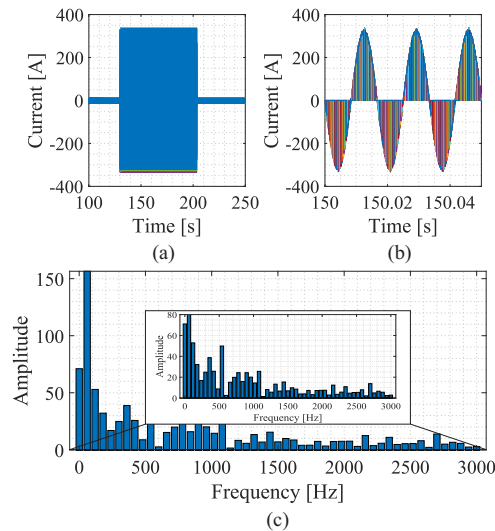


Figure 88 – Current in the batteries for single-stage approach: (a) dynamic behavior (b) current in the charging process (c) spectral analysis.

Figure 89 (a) shows the current behavior in the batteries for the two-stage approach in the charging process. As the dc/dc converter performs the decoupling of the batteries with the SM, the current shows less oscillations, Figure 89 (b). According to the spectral analysis presented in Figure 89 (c), the low-order harmonic components are strongly attenuated. Compared to the single-stage approach, the fundamental and second-order harmonics have been reduced considerably. In addition, harmonic components are observed near the frequency of 1 kHz. These components are derived from the switching of the dc/dc converter. In addition, the RMS battery current is less in the two-stage approach.

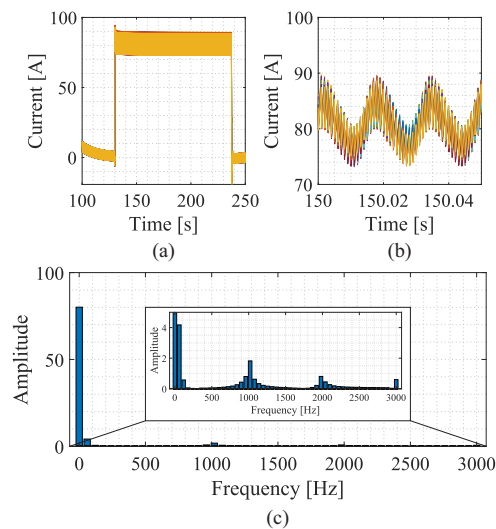


Figure 89 – Current in the batteries for two-stage approach: (a) dynamic behavior (b) current in the charging process (c) spectral analysis.

6.4 Conclusion

In this chapter, simulations are performed for one- and two-stage topologies to validate the design of the controllers. The analysis of the systems dynamics considers the charge and discharge process. Finally, the battery steady-state current is evaluated for both single-stage and two-stage approaches. The next chapter draws the conclusions of this thesis.

7 Closure

MMC-based BESS presents important challenges related to design, control, and operation. These can directly impact the total cost of the system. Previous chapters explored design, cost analysis, and control for MMC-based BESS. This chapter summarizes the main conclusions of this Ph.D. thesis and future developments.

7.1 Conclusions

This thesis presents a methodology to minimize the design of two approaches to the MMC-based BESS topology: single-stage and two-stage. In the minimization process, several variables can be evaluated, for example, volume, efficiency, cost, weight, and size, among others. Thus, in this work, the variable chosen to be minimized is the cost related to the MMC-based BESS. Analyses such as power losses, lifetime battery, and battery replacement are considered to obtain the total cost over a given period.

In addition, in the sizing of the MMC-based BESS, rounding is used to supply the voltage, energy, and power demand of the system. Indeed, depending on the type of battery characteristic, energy oversizing can occur in projects, which would result in a higher project cost. Thus, this work presents two solutions: customized and standard. Thus, some conclusions can be highlighted in this thesis.

- The single-stage approach leads to a higher number of SM than two-stage approach. However, the number of power semiconductor devices is higher in two-stage, because of the dc/dc converter.
- In all case studies, the two-stage approach has higher energy losses than the single-stage approach. This is justified by the presence dc/dc converter.
- In the two-stage approach, the dc/dc converter increases design flexibility. Furthermore, it allows defining the optimal SM reference voltage. This fact reduces the energy oversizing in most cases;
- In the single-stage topology, the battery current presents low-order harmonics (especially first and second order). These components, increase the battery RMS current and, consequently, the battery internal losses.
- In the MMC-based BESS design, some roundings are present in its design calculations. In this way, designs based on commercial battery racks (standard solution) can

present high energy oversizing. On the other hand, when using custom battery racks (customized solution) energy oversizing can be reduced.

- In the two-stage approach, the dynamic response is slower than in the single-stage approach. This is justified by the fact that in the two-stage approach the output voltage of the **SM** is defined by a nested control with two loops. In the single-stage approach, the output voltage of the **SM** is defined by the associated batteries.
- The allowed **SOC** range plays an important role in the cost optimization. The higher the **SOC** range, the lower the **CAPEX**. Therefore, the optimum **SOC** range depends on the mission profile and the **SM** reference voltage.
- The **CAPEX** were similar for single and two-stage approaches. On the other hand, **OPEX** were decisive for choosing the design with the lowest cost.
- The cost analysis presented in this work involves different approximations. Carrying out cost analysis is a difficult task because costs depend on several factors. However, the proposed methodology is perfectly adaptable to other cost or power losses evaluation models.
- For the case study presented in this paper, calendar aging degradation is the major factor for the battery aging. As the customized two-stage designs have more compact designs, degradation by cycles increases. Consequently, the battery life is shorter. In the single-stage approach, due to rounding in the **BESS** sizing, the energy oversizing is higher, which leads to longer battery lifetime.
- The two-stage approach presents a dynamic behavior with less ripple in the battery current compared to the two-stage approach.
- In one of the tests carried out, the **THD** for the single-stage averaged 0.1% for the three phases and, 1% for the two-stage.

According to the results obtained comparing the single-stage and two-stage approaches, some points can be highlighted in Table 18. Note that the notation **✓** is used for the most advantageous options and **✗** for the less advantageous ones.

Table 18 – Summary of results obtained for the MMC-based BESS.

	Single-Stage	Two-Stage
N for the same v_{SM}^*	×	✓
Energy oversizing	×	✓
Number of Semiconductors	✓	×
Power Losses for the same v_{SM}^*	✓	×
Flexibility for reference voltage	×	✓
Number of batteries for the same v_{SM}^*	✓	×
Harmonic Component (fundamental and low-order harmonic)	×	✓
THD	✓	×
Number of control loops	✓	×

7.2 Research Perspectives

After the studies carried out and documented in this Ph.D thesis, the author understands that there are still the following topics to be addressed and deepened:

- Experimental validation of an [MMC-based BESS](#) converter in single-stage and two-stage approaches;
- Experimental validation of the battery lifetime model used in simulation;
- Experimental validation the impact of harmonic components on battery lifetime in single-stage and two-stage approaches and;
- Use the optimization tool evaluating other metrics (e.g. volume, efficiency, etc). In this Ph.D thesis the general metric was the total cost.

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Biography



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