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**POSTFAULT RELIABILITY IMPACT ANALYSIS OF MODULAR DESIGN IN
MEDIUM VOLTAGE IGBT-BASED CONVERTERS**

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MEDIUM VOLTAGE IGBT-BASED CONVERTERS**

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GUILHERME SALVADOR FERREIRA

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Abstract

Modular design is largely applied to Medium Voltage Converters and provides a simple way to replace a set of damaged devices after failure events, allowing a fast return to operation. Arranging the power semiconductors into converter phase modules for instance, allow the system to be taken out of operation only for the defective phase module replacement, which can be sent to the supplier for repair. However, the indication of the failed power semiconductors inside the phase module is usually only given by the gate driver and simple in-circuit tests performed with the aid of a multimeter during the downtime. In this master thesis, it is demonstrated that a failure occurring in one flat-pack IGBT power semiconductor of any phase can cause escalated consequences and basic tests may not be enough to spot degraded devices in other phase modules. This is performed by the modeling, simulation, and analysis of two consecutive faults in a real case application of a three-level medium voltage converter. Furthermore, post-fault offline tests are performed in flat-pack IGBT samples that apparently survived the real case fault. The results reveal a relevant parameter shift in the leakage current between Collector and Emitter that support questioning the benefits of the modular design. The deteriorated power devices might not fail immediately, but they will have a shorter lifetime expectancy impacting the overall reliability leading to a subsequent fault of likely larger significance.

Keywords: fault analysis; IGBTs; post-fault diagnosis; degradation; parameter shift; failure prognosis; reliability.

Resumo

O projeto modular é amplamente aplicado em Conversores de Média Tensão e proporciona uma maneira fácil de substituir um conjunto de dispositivos danificados após eventos de falha, permitindo um rápido restabelecimento da operação. A disposição dos semicondutores em módulos de fase, por exemplo, permite que o sistema seja retirado de operação apenas para a substituição do módulo de fase defeituoso, que pode ser enviado ao fornecedor para reparo. Porém, a indicação dos semicondutores em falha dentro do módulo de fase geralmente é dada apenas pelo gate driver e por testes simples, com os dispositivos conectados no circuito, realizados com o auxílio de um multímetro durante o tempo de inatividade. Nesta dissertação de mestrado, é demonstrado que uma falha que ocorre em um módulo de potência IGBT de qualquer fase pode causar maiores consequências e os testes básicos podem não ser suficientes para detectar dispositivos degradados em outros módulos de fase. Isto é realizado através da modelagem, simulação e análise de duas faltas consecutivas em um caso real de aplicação de um conversor de média tensão de três níveis. Além disso, testes pós-falha com os semicondutores desconectados, offline, são realizados em amostras de IGBTs flat-pack que aparentemente sobreviveram ao caso real de falta. Os resultados revelam uma alteração relevante do parâmetro corrente de fuga entre Coletor e Emissor, o que suporta o questionamento dos benefícios do design modular. Os dispositivos de energia deteriorados podem não falhar imediatamente, mas terão uma expectativa de vida mais curta, impactando a confiabilidade geral, levando a uma falha subsequente de, provavelmente, maiores proporções.

Palavras-chave: análise de falta; IGBTs; diagnóstico pós-falha; degradação; alteração de parâmetros; prognóstico de falhas; confiabilidade.

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Abbreviations

0V (zero-volt potential in the converter)	36
AFE (Active Front End)	36
ANPC (Active Neutral Point Clamped).....	20
CM (Conditioning Monitoring)	130
DT (Dead Time).....	68
DUT (Device Under Test).....	100
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HSF (Hard Switching Fault)	39
IEGT (Injection-Enhanced Gate Transistor).....	39
IGBT (Insulated Gate Bipolar Transistor)	16
MB (Machine Bridge).....	36
MOS (Metal-Oxide Semiconductor).....	89
MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor).....	21
MTBF (Mean Time Between Failures)	21
MTTR (Mean Time to Repair).....	16
MV (Medium Voltage)	16
NPC (Neutral Point Clamped).....	20
NPP (Neutral Point Piloted)	32
PHM (Prognostic and Health Management).....	25
PoF (Physics of the Failure)	17
RBSOA (Reverse Bias Safety Operating Area)	44
SCFM (Short Circuit Failure Mode)	39
SCSOA (Short-Circuit Safe Operating Area).....	46
SHE (Selective Harmonic Elimination).....	38
SILC (Stress Induced Leakage Current).....	89
SOA (Safe Operating Area)	24
STO (Self-Turn-Off).....	45
TIM (Thermal Interface Material).....	102

VSC (Voltage Source Converter).....	16
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Chapter 1.Introduction

The use of MV (Medium Voltage) Converters is commonly associated with critical loads, i.e., those necessary to sustain production or to reach the main mission of an application. Therefore, the downtime caused by failures or unplanned maintenance in the converters will inherently have a high impact and cost in the plant operation.

For marine applications for instance, a failure in the MV converter can lead to the loss of the propulsion system, impacting the time for the vessel to complete the mission or even leading to a crash. Another example is the steel industry, in which the MV converters are present in many parts of the production line, like mills, run-out tables, coilers, and pinch roles [1]. Since steelmaking is a continuous process, a failure in one converter can lead to the shutdown of the entire plant. The cost of the downtime can reach hundreds of thousands of dollars per day depending on the production capacity [2] [3].

One of the strategies often adopted by the converter manufacturers to reduce the MTTR (Mean Time to Repair) and the time to resume full operation, is the modular design notion in which individual components are combined into separated subassemblies or building blocks. The modules are designed to be simple to remove and reconnect, so that they can rapidly be replaced by spare ones in the event of a fault. In the case of three-level VSC (Voltage Source Converter) explored in this study, one of the main subassemblies is the Phase Module. It comprises the IGBTs (Insulated Gate Bipolar Transistors), the heatsink, the snubbers and the gate cards for each phase of the converter.

Nevertheless, this concept is based on reliability studies and prediction methods assuming that the failures are insulated and disregarding the failure interactions among components and with external factors [4]. For instance, each possible phase module fault is usually treated as an independent event such that the overall reliability is the product of each individual success probability [5]. The investigation developed in this work demonstrates that the post fault damage is not always contained inside the failed phase module as normally assumed. For that, a real case of two consecutive faults in the same converter is analyzed giving evidence that the second fault, here referenced as Main Fault, happened due to the reuse of phase modules with power semiconductors that were degraded in the first fault.

Generally, the determination of the phase module that needs to be replaced hinge on the fault indication coming from the gate driver, visual inspection and simple in-circuit

tests that are performed with the help of a multimeter. It is demonstrated that when the power semiconductors are not completely failed, those simple in-circuit tests might not be sufficient to spot degradation that will lead to a new failure within a short time frame.

This work proposes an analysis on the impacts of a fault in the converter reliability based on the PoF (Physics of the Failure). The methodology consists of evaluating the overstress in the power semiconductors of different phase modules by the study of the measured data and fault plots complemented by the results of a simulation model in which the second fault is replicated. The subsequent fault current paths created by the interaction of the motor back emf, DC link capacitors and the converter stray inductances are addressed, and the affected devices are tagged. Furthermore, offline / off-circuit tests are determined and carried out in device samples that experienced only the second fault, revealing relevant parameters shift when compared to a base line built with results from new units and data obtained from the IGBT manufacturer.

The content is organized as follows:

- Chapter 2 introduces some current strategies to improve reliability in power electronics presenting the concepts of the modular design in MV converters and how the reliability can be impacted if there is a damage spread to other phase modules after a fault. The methodology used for evaluating the damage in the power semiconductors after the real case fault is discussed, comprising a combination of the fault analysis, simulation, and off-circuit tests. The focus is not on the most damaged phase module that initiated the fault and would be replaced, but rather in the fault spread and the estimation of the stress in the devices of the other phase modules.
- Chapter 3 presents the main characteristics of the MV converter in which the fault analysis is performed. The electrical configuration, IGBT, phase module architecture, types of faults and protections available are explained to form the basis for the discussions on the fault plots, simulation and test results addressed in the next chapters.
- In Chapter 4 the first fault experienced by the converter is reviewed to understand the conditions in which the converter operation was restored before the second fault. The tests and actions taken after the fault are summarized. Traces of a possible degraded device could have passed the inspection are shown and the suspicion that the reuse of this device could have led to the second fault is discussed.

- Chapter 5 analyzes the second fault, center of this study. The most probable fault sequence is described, indicating the link of the fault start with the deteriorated IGBT reused from the previous fault. The converter under fault is modeled and the simulation results are used along with the site measurements to characterize the new overstress in all the power semiconductors over the short circuit current loops created by the effects of the motor back emf and the converter stray inductances. Initial test results and evidence of internal deterioration in IGBTs that experienced only this fault are presented.
- Chapter 6 discusses the failure modes and degradation indicators (or failure precursor parameters [6] [7]) of the flat-pack IGBTs. The internal phenomena that affect the device structure for different types of stress are detailed. The failure modes are related to the precursor parameters that could be investigated through individual offline / off-circuit tests and would be able to spot deviations, indicating a possible deterioration.
- Chapter 7 presents the results of the laboratory offline tests suggested in Chapter 6 and applied to the IGBT samples taken after the second fault according to the conclusions of Chapter 5. The signs of degradation found are shown and the risk of incurring in a new fault when reusing these devices is debated. The results are reviewed for the tests at ambient temperature and using a hot plate setup to heat up the junction close to its maximum temperature.
- Finally, in Chapter 8, the potential shortcoming of the modular design is discussed upon the main findings of this work and the conclusions are presented. Furthermore, the effectiveness and practical feasibility of the proposed tests are discussed as a tool to be used on site to support after faults analysis and help spot degraded devices whose reuse should be avoided. A proposal of future work is given, expanding the concepts of the PoF for degradation prediction to online measurements that can be added to the IGBT's gate drivers.

In summary, this work analyzes the impacts of the faults in the general converter reliability, discussing the factors that can lead to the reoccurrence of faults due to degradation of components affected by the first fault. Understanding these aspects can help users and manufactures to act in a preventive way, avoiding the reuse of degraded components.

Chapter 2. Reliability, Modular Design and Damage Prognosis

In this chapter introduces some recent strategies being explored to improve reliability in Power Electronics. The modular design is also presented as a possible way to enhance the converter reliability by reducing the maintenance time, but the risks associated with the assumption that the fault is self-contained and that the failure rates are constant when the converter is restored to operation are discussed. To overcome the difficulties of identifying the damage spread and avoid reusing degraded devices, a post-fault evaluation methodology is proposed for the impact analysis and damage prognosis of the power semiconductors of a converter. In the next chapters, this methodology is applied to flat-pack IGBT samples removed from a 3-level VSC that experienced two consecutive faults.

2.1. Reliability Strategies Under Study in Power Electronics

The reliability is the ability of an item to perform a required function under stated conditions for a certain period [8] [9]. A failure is defined as any trouble with a power component that causes a partial or complete shutdown or lead to an unacceptable performance of the user's equipment [10]. In that sense, it is important to denote the following interpretation of the terms failure and fault in this text as:

- Failure: In the sense of a Catastrophic Failure. When the component, mainly the semiconductor, loses its switching capability and stays either in open circuit or short circuit.
- Fault: An event of high energy like a short circuit that happens because of the catastrophic failure of a component.

The Reliability is an important performance factor and different strategies are currently explored to improve it in systems that use power electronic components like medium voltage converters [4]. The multi-disciplinary approaches can be divided as presented in Figure 2.1 [8] [11].

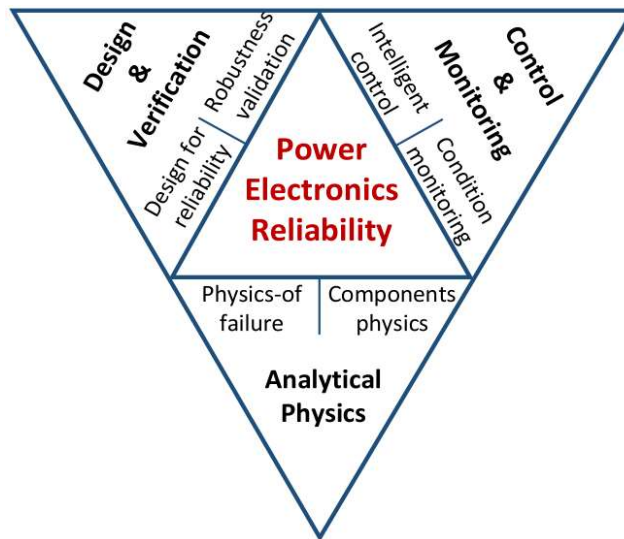


Figure 2.1 Approaches for Enhancement of the Reliability of Power Electronic Converters [8] [11]

Among the pillars of the reliability enhancement, this study explores the PoF analysis and condition monitoring, yet other research areas can be mentioned to contextualize it among other strategies.

One of the innovative design developments is to address the Availability, given by Eq. (2.1) [12], by the realization of Fault-Tolerant topologies that increase the MTBF (Mean Time Between Failures) since the converter would be able to overcome failures in its power devices without loss of functionality, before its definitive downtime [13].

$$Availability = \frac{MTBF}{MTBF + MTTR} \quad (2.1)$$

Figure 2.2 exemplifies a fault-tolerant proposition for the ANPC (Active Neutral Point Clamped) topology [14] [15] in which the clamp diodes of the conventional NPC (Neutral Point Clamped) are replaced by IGBTs. In addition to that, the FT-ANPC (Fault-Tolerant Active Neutral Point Clamped) has two extra IGBTs (S5 and S8) with their respective the FWD (Freewheeling Diode) per phase and a switch (Kc) with two reversible contacts. Kc can be implemented with simple contactors since it commutates under zero current. With these extra components, the FT-ANPC can have its configuration changed in multiple ways to maintain the operation [16] [13].

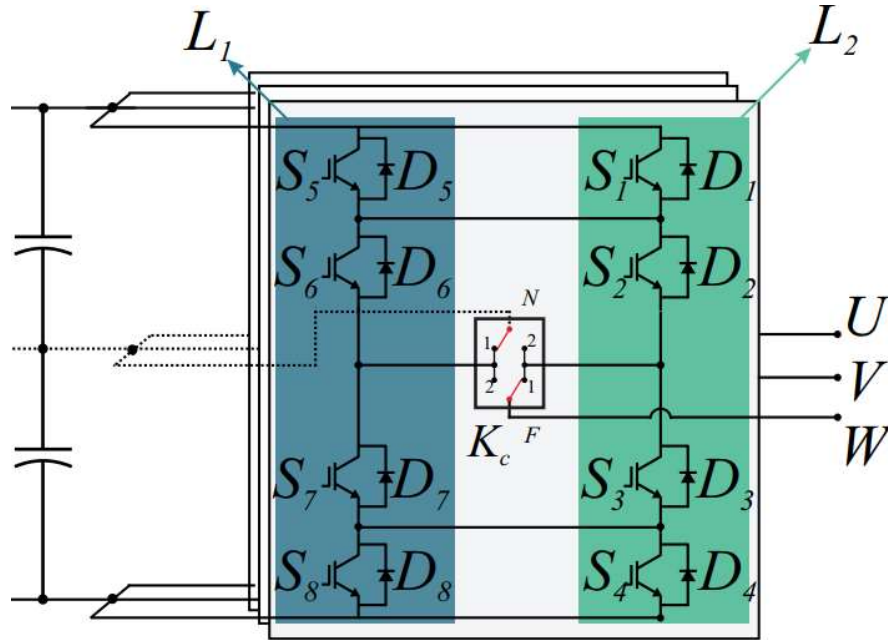


Figure 2.2 Software reconfiguration of the self-healing ANPC after a failure in the IGBT Q1A [16]

Another field that is being largely explored is the ways to improve the reliability of devices built with WBG (Wide Band Gap) semiconductor materials like silicon carbide (SiC), gallium nitride (GaN), and diamond. The WBG materials have better electrical, mechanical, and thermal properties than the Consequently, WBG devices can increase the breakdown voltages, switching frequency, and operating temperatures as well as reduce switching losses increasing efficiency, as demonstrated in Figure 2.3 [17]. However, some constructive issues still reduce its reliability with respect to Silicon (Si) ones [18].

SiC devices for instance, have reliability issues in the gate oxide channel, bias temperature instability that affects threshold voltage and lower short-circuits robustness. As detailed in Section 3.3, withstanding the short-circuit current for some μs can determine if a component failure will generate a fault inside the module. While Si-IGBT short circuit withstand duration is around $10 \mu s$, the SiC-MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) has a lower withstand duration mainly because the dies are smaller and therefore the power density to be dissipated during a short-circuit is higher [18].

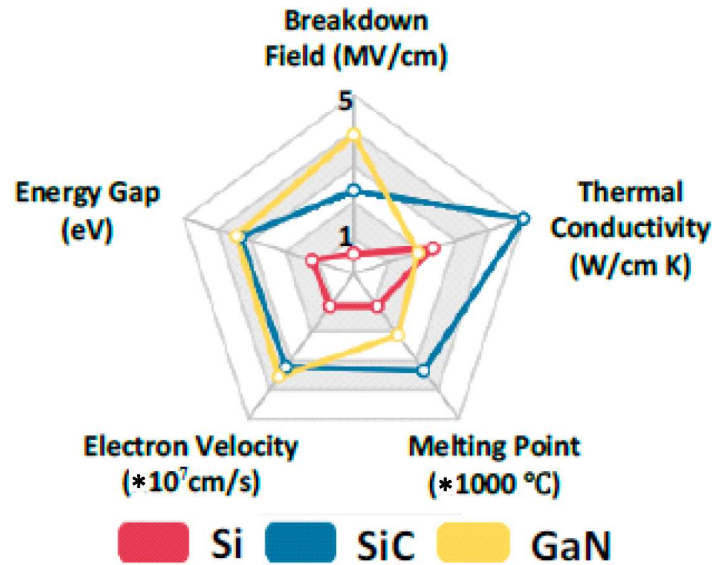


Figure 2.3 Summary of Si, SiC, and GaN relevant material properties [17]

2.2. Modular Design Reliability in MV Converters

Another way to improve the system availability is to reduce the MTTR by the application of the modular design, because a failed module can be rapidly replaced by a new unit. It consists of subdividing a complex product or system into standardized and interchangeable smaller self-contained groups of parts or modules that can be managed independently, be easily removed, swapped, or replaced by a new one [19]. The definition of what parts would constitute the modules considers many economic and strategic aspects, among which the reduction of the maintenance cost and MTTR are some of the most important ones.

Since the power semiconductors are one of the most vulnerable components of the converters and at the same time the ones of highest importance for its correct operation the basic module commonly developed for the converters are designed to have those devices and its complementary circuit [20] [21]. Examples of modules of power semiconductors in medium voltage converters are the “Power Cells” in the ROBICON Perfect Harmony Converter [22] [23], or the “Submodules” with full and half-bridge topologies used in the more recent Hybrid Modular Multilevel Converters design [24]. As stated in Chapter 1 and better detailed in Chapter 3, the main converter structure of

interest in this study is the more traditional arrangement of 3-level converters per phase called “Phase Module”.

The modules constructed with the semiconductors are therefore essential for the converter reliability. i.e., it directly impacts the probability of the converter to perform its intended function adequately for a specific period without failure [5]. This impact can be computed in the overall MTBF calculation. For a non-redundant system, like the converter object of this analysis, the overall MTBF is affected by the Failure Rate (λ) of each module as a series effect as represented by Eq. (2.2) [12].

$$MTBF_{Converter} = \frac{1}{\lambda_{module1} + \lambda_{module2} + \lambda_{module3} + \dots + \lambda_{module_n}} \quad (2.2)$$

At the same time, the failure rate of the module is mainly linked to the semiconductor failure rate, which the characteristic over time is known as the Bathtub Curve, shown in Figure 2.4.

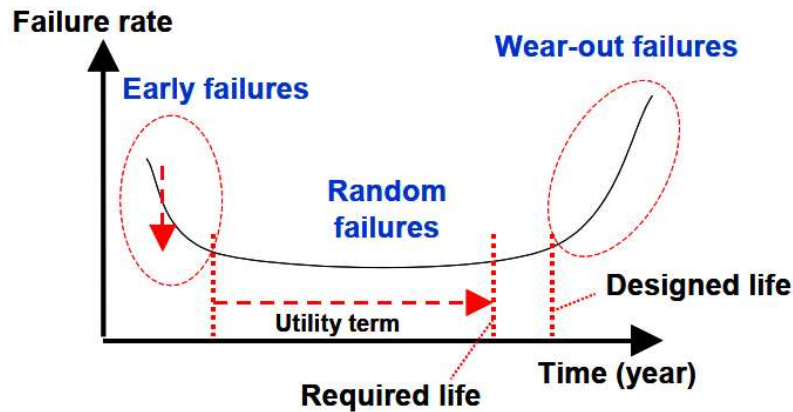


Figure 2.4 Time-dependent change of the failure rate for semiconductor devices [25]

Early failures are caused by microscopic defects in the manufacturing process of the semiconductor and can be reduced by improving the quality control and removed by disregarding defective parts after outgoing tests. The wear-out failures are caused by fatigue and can be avoided by selecting components to reach the required life before the wear-out phase. Therefore, the failure rate considered in the reliability studies is generally the random failures that are caused by excessive stresses over maximum rating such as overvoltage, overcurrent, overheat and so on. Statistically, the rate of random failures is almost constant because the failures are considered independent and self-contained [5] [25].

IGBTs, for instance, have failure rates of around 100 FIT (Failure in Time) [26], which is the expected number of units failing per billion operating hours. It can be

interpreted as 100 failures expected in 1000 devices in 1 million hours, or in 1 million devices in 1000 hours, etc. This very low failure rate is however valid for the random failure period only, if the IGBT is forced to operate out of the SOA (Safe Operating Area) or if the junction temperature surpasses the maximum limit, and the device does not fail completely, it can accumulate degradation to its internal structure. The effect will be similar to an accelerated aging, taking the device to the wear-out period in the bathtub curve, in which the constant failure rate cannot be guaranteed anymore.

Eq. (2.2) shows that the MTBF for the overall system will always be smaller than the value of the module with the smallest MTBF [12]. Although the modular design helps to improve the MTTR, the final MTBF can also be reduced by: Early Failures that can happen in the new unit; or because the effects of a fault were not contained inside the exchanged module. The latest case is the one of interest in this study. The overall MTBF can be drastically reduced if a module with a degraded component is kept in the converter.

This study shows that there is a risk of this being the case for medium voltage converters after-fault events in one phase module. Although the phase module in which the fault started is the one normally damaged and replaced, the high energy involved in the fault can make the other phase modules be affected and have its power semiconductors accumulating degradation.

The situation is worsened by the difficulty to execute a test at site after a fault that would be able to spot degradation in the remaining modules after a fault. Usually, only simple in-circuit tests are performed with a multimeter, checking if the power semiconductors are short circuited or if they respond to the firing commands by measuring the Collector and Emitter Voltage when applying a small current (multimeter in diode mode) or measuring the resistance. The evaluation of the good and bad results is done by comparison with the expected equivalent in-circuit value, e.g., the equivalent resistance of the IGBT internal Collector to Emitter structure, parallel gate driver resistance and parallel snubber resistance. This can be enough to identify evident damage but might not be sensitive enough to spot smaller parameter shift in the semiconductor due to degradation.

The damage prognosis methodology proposed next and applied in this study tries to address those two main points, the estimation of the damage spread and the tests that can give a better estimation of the state of the power semiconductors after a fault, to avoid keeping a phase module that the failure rate cannot be trusted and could lead to a new fault in a time period much shorter than the expected designed lifetime.

2.3. Post-Fault Evaluation Methodology

The normal damage accumulation can be estimated through the number of power cycles under the operation conditions of each application. Statistic models and rainflow algorithms considering temperature, frequency, and current variations in the IGBT wire bonds can evaluate the expected remaining lifetime after a period of operation hours [4] [20]. However, since it's based on the repetition of the power cycles, this methodology is adequate to estimate degradation that's associated with fatigue but it's not able to compute the acceleration in the aging process due to a single and fast external unexpected event. In this case, the device experiences a high temperature variation over a short time caused by the short circuit current. The abnormal conditions and overstress accelerate the wear-out process [27] [28].

The methodology proposed in this work is based on the PoF approach and derived from the hybrid PHM (Prognostic and Health Management) given by [7]. It explores the failure mechanisms and physical parameter variations that can lead to the fault. However, instead of accelerating the aging process in laboratory, the power semiconductors submitted to the real fault are used. The process flow is shown in Figure 2.5. The post fault evaluation is important to avoid the recurrence of faults due to the reuse of degraded power semiconductor devices.

The proposed damage evaluation can be divided into two main paths that are combined to support the identification of overstressed devices after a fault. The first path is the Fault Analysis in which the internal fault current loops are recreated through simulation allowing the determination of the most affected components. The second path is the definition and execution of offline tests in the semiconductor devices that apparently survived the fault but can present degradation not easily spot through basic in-circuit tests.

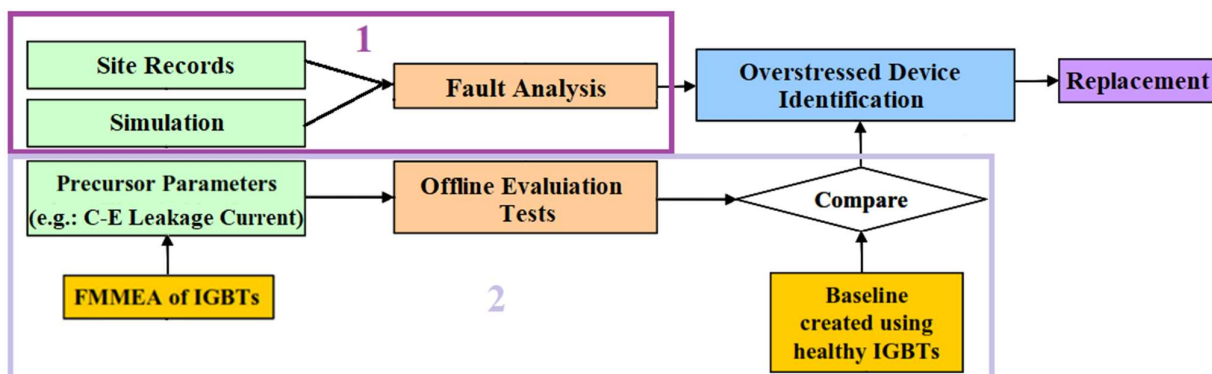


Figure 2.5 Proposed Damage Prognosis Methodology (adapted from [7])

2.3.1. Fault Analysis

The Fault Analysis is added to the original hybrid PHM approach to support the determination of the most stressed components during the fault and consequently the ones most likely to present parameter shift when submitted to the tests. It allows the estimation of the damage spread by understanding the short circuit current paths and affected components inside the converter. The site records are used to find the most probable root cause, how and at which point the fault started. Although the available measurement points in the converter are limited, the fault plots also show the magnitude, if the fault current is going to the motor, to the grid or to the converter and help reconstitute the subsequent behavior of the electrical quantities after the fault is established.

Since there is no dedicated measurement of the currents and voltages at each semiconductor device, a simulation is used to replicate the phenomena and study the internal variation of the electrical quantities. The model is built in PLECS using the parameters obtained from the as built documentation of the system under study and it is validated by comparing the values of the dc link voltage, motor currents, grid voltage and currents with the measured values. It is assumed that if the external measured electrical quantities match the simulation results, then the internal behavior of the electrical quantities are likely close to what happened.

The Fault Analysis is developed in Chapter 4 and Chapter 5 for a converter that experienced two consecutive faults. The first fault is detailed to set the converter condition and list the reused IGBTs that ended up leading to the second fault, which is the main fault of interest in this work. The second fault is deeply explored through the onsite data and simulation results. Evidence that the fault started from a failure on a reused IGBT is shown and the stress on the new units placed in the converter after the first fault is estimated. Those units that experienced only the second fault and presented signs of degradation were then further tested in laboratory.

2.3.2. Offline / Off-circuit Evaluation Tests

The power semiconductors conditions are usually verified on site by basic offline in-circuit tests performed with a multimeter, such as applying individual pulses and checking the continuity/open circuit indication in the IGBT and the FWD with the multimeter in diode mode. Although those tests would be able to spot completely damaged devices, like an

IGBT in short circuit for instance, this work demonstrates that they are not sufficient to identify degradations that will make the device fail within a short period of time.

Despite the simplicity, the normal in-circuit tests results are influenced by the connection to the gate driver and snubber circuit. The off-circuit evaluation proposed here is a combination of tests that are also executed offline and with the devices in static condition, either ON or OFF, but that require the disconnection of the semiconductor devices so that they can be tested individually, and the results can be compared with expected values in new units using a baseline formed with data obtained from interactions with the IGBT manufacturer and measurements of new IGBT units.

Due to the higher level of complexity to be performed, these tests are intended to be performed as a support for the after-fault evaluation of the components and determination of the fault spread. The detailed evaluation can take time but can also be crucial to avoid further faults and new outages. Keeping enough number of spare modules that allow the complete replacement of all modules after a fault can be an alternative to diminish the impact in the MTTR. The modules possibly affected can be analyzed separately and eventually be used to replenish the stock of spares.

In the study, the power semiconductors leakage current or equivalent insulation resistance is the main parameter investigated. It presented deviations when investigated at ambient temperature, what facilitates its verification on site or shop floor. As described in this text, during the post fault investigation, the IGBTs collector to emitter insulation were tested individually on site and the results were able to indicate a degraded IGBT after the second fault. Other precursor parameters and offline/ off-circuit tests are discussed in Chapter 6 and the results of the tests in devices removed from the converter of the real case application are presented in Chapter 7.

The hybrid PHM in [7] proposes a continuous monitoring of the failure precursors. Although this can provide a continuous estimation of the converter overall reliability during the operation, performing online and in-circuit evaluation of the semiconductor conditions is very challenging. It requires very sensitive measurement strategies to be able to spot variations of low amplitude over quantities that can reach high magnitudes, for instance finding deviations in the collector to emitter ON-state voltage while these same measurement points will rise to kilovolts when blocking the DC link. Furthermore, the sensors must be sufficiently shielded to not be influenced by surrounding noisy environment created by the switching process at high frequency of the power semiconductors [29].

2.4. Internal Device Structure Investigation

A final complementary step in understanding the fault impact and damage spread is suggested to be the decapsulation of the IGBTs and inspection of its internal structure comprising an evaluation if the damage or degradation can be visually verified and separated between the IGBT and FWD and analyzing the state of the dies and wire bonds.

Opening the device case needs to be executed carefully to no affect the internal wire bond connections, and since it is a non-reversible step, it can only be done after finishing all proposed tests. This complementary step is here proposed as a Future Work in Section 8.1.

2.5. Limitations

The methodology suggested and applied to real case faults and the IGBT samples demonstrated to be able to support the identification of degraded IGBTs that should not be reused after a fault, especially when its overall appearance and the normal multimeter tests could wrongly suggest that they are in good conditions. Its execution can be cumbersome though, because of the complexity of the fault analysis and the difficulties of disassembling the components for the offline / off-circuit tests.

Although the fault analysis and simulation allow the evaluation of the fault spread and can suggest what components are worth being replaced or further investigated because of the overstress that they experienced, it is a complex study that dives into a deep understanding of the fault conditions and the most probable fault sequence. It requires understanding of the converter main parameters values, components, and stray inductances.

The offline / off-circuit tests are reasonably simple to be performed, they only require the devices in static mode, either ON or OFF. For the real case of study explored here, the tests were able to spot variations in the failure precursor parameters even at ambient temperature, what makes it easier to be executed on site or the shopfloor. However, they still require the disassembly of the power semiconductor devices from their circuit and gate drivers. The tests also don't provide a continuous monitoring of the defined precursor parameters, but the results obtained in this work can be used to develop an

online monitoring strategy that can be included in a gate driver design in a future work, Section 8.1.2.

Finally, this approach is not able to estimate the remaining lifetime expectancy of the affected devices. The general recommendation here is to replace the devices in case of a large parameter shift identified or estimated overstress. Yet, it can be used as a basis for developing a calculation for the remaining lifetime in a future work.

2.6. Conclusions

This chapter explored the risks associated with the reliability of MV converters after a fault, failed module replacement and return to operation. It was explained that the fault may not be contained inside the most damage module, affecting other modules that would initially be considered in the constant random failure rate part of the bathtub curve. This can affect the overall converter reliability.

An adaptation of the hybrid PHM as the methodology proposed and applied in this study for the identification of the overstress and degradation of the power semiconductor devices after a fault. The strategy is based on the PoF, since the usual statistic models, constructed with recursive overload stress and removal to force the accelerated aging in the devices, are not adequate for the fast event of high energy associated with the faults. The hybrid PHM proposed is a combination of the fault analysis, performed with recorded data and simulation, and offline tests that can show deviations on the device parameters when compared to new units. The offline / off-circuit tests are simpler to execute and less susceptible to interference than the continuous online monitoring with the devices connected in the circuit, however they demand the disassembly of the components which requires controlled environment and qualified personnel.

Chapter 3. Converter Circuit, Types of Faults and Protections

The electrical characteristics and main protections of the converter under study are discussed in this chapter to give the basic support information for the Fault Analysis explored in Chapter 4 and Chapter 5.

The single line diagram and main electrical elements of the converter are shown as well as the arrangement of the power semiconductors. The main electrical parameters of the system comprising the main transformer, the converter and the motor are listed. This chapter also explores the converter control architecture and main measurements, indicating the p.u. basis and convention for the flow of the currents. Finally, the type of faults expected for the applied topology are described and the protections available from the measurements and gate drivers are presented. The protection detection and actuation times are given and the steps in the process of turning OFF the power semiconductors are described.

3.1. Converter Phase Module

The phase module is a modular arrangement containing the IGBTs, the heatsink, the snubber circuit and the gate cards for each phase of the converter. The phase modules are designed to be identical and interchangeable.

3.1.1. IGBT Type

The applied power semiconductor is the MBN750H65E2 from Hitachi [30], comprising the IGBT and FWD, and the gate driver is the Scale 1 from Power Integrations, previously Concept [31]. The IGBTs and the snubber resistors are assembled with the thermal grease over one unique heatsink per phase. PT100 is placed near the IGBT with the highest estimated temperature at full load, modulation, and speed.

The MBN750H65E2 is a Flat-pack device. This type of power semiconductor is also known as Power Module, yet this nomenclature will not be used in this text to avoid

confusion with the concept of module in the Modular Design, i.e, a subassembly built with a set of devices. An overview of the device and its internal connections are shown in Figure 3.1. IGBTs can be easily paralleled to increase the overall current capacity because manufactures have good control over the variation of the IGBT parameters from one device to another, the ON-state voltage doesn't vary much with temperature and the devices have a positive temperature coefficient [32]. This means that if one IGBT has a lower $V_{CE_{SAT}}$, the current is higher, making the losses higher and increasing the junction temperature. Consequently, due to the positive temperature coefficient, the $V_{CE_{SAT}}$ increase, decreasing the current and tending to balance the losses.

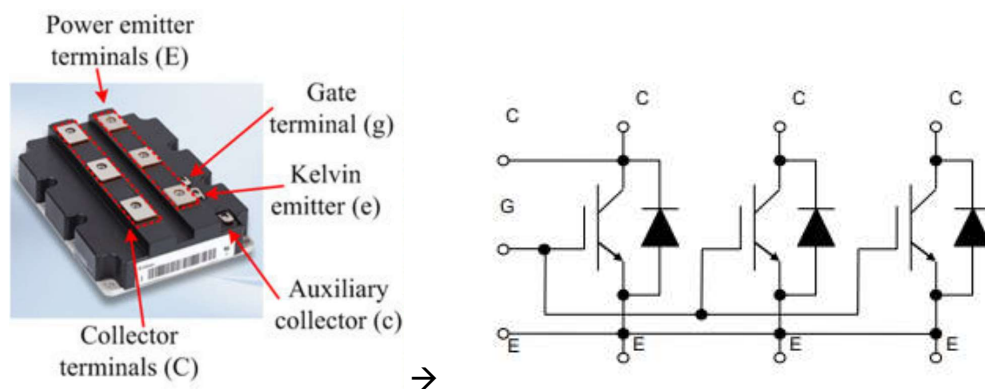


Figure 3.1: Flat-pack IGBT example (Left: Typical Appearance, Right: Internal Circuit Diagram of the MBN750H65E2 from Hitachi) [33] [30]

Figure 3.2 and Figure 3.3 show two main models of the IGBT internal structure. Figure 3.2 shows that the IGBT comprises a MOSFET at the input, n-p-n structure of the MOS layer in the gate, and a BJT at the output. The parasitic transistor formed between collector and emitter can lead to the IGBT latch-up when turned ON under fault conditions [7] [34].

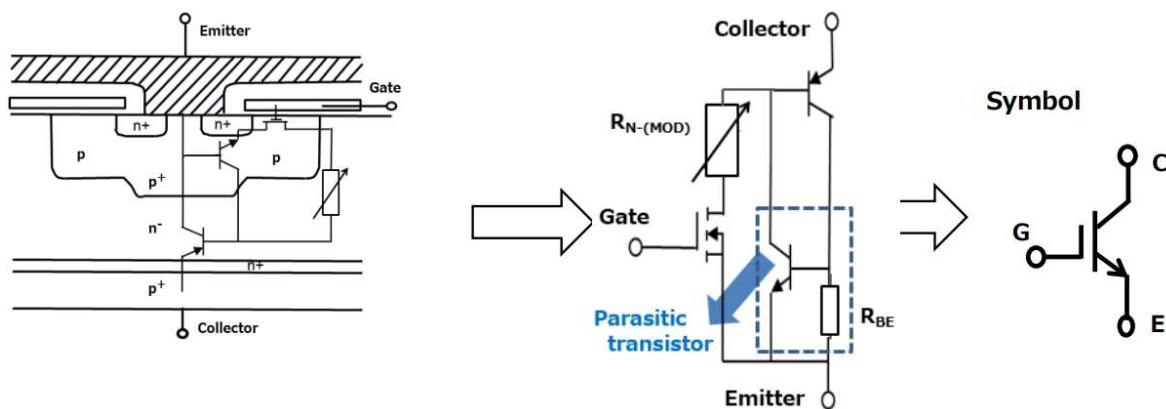


Figure 3.2 Basic Structure and Equivalent Diagram of an IGBT [34]

Figure 3.3 illustrates the internal structure, showing the main stray components that influence the behavior under fault. Further details of the IGBT internal structure are given in Chapter 6.

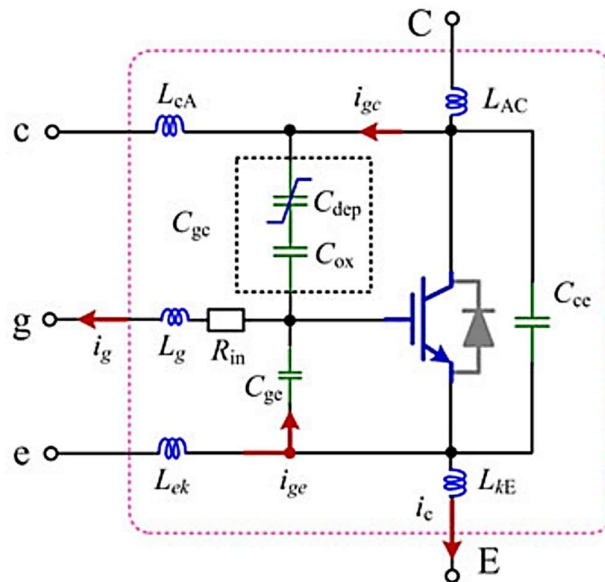


Figure 3.3: IGBT Internal Equivalent Circuit [33]

Where:

- L_{AC} , L_{cA} , L_g , L_{eK} and L_{kE} are the parasitic inductors between the external Power and Kelvin terminals and internal chips.
- R_{in} is the internal gate driver resistor which increases driver loop damping.
- C_{ge} is gate capacitor or MOS capacitor.
- C_{ce} is the parasitic capacitor across collector and emitter.
- C_{gc} is the gate collector capacitor and consists of the variable depletion layer capacitor C_{dep} and the fixed oxide capacitor C_{ox} . C_{gc} is also known as Miller Capacitance or Reverse Transfer Capacitance, due to its relation to the turn-off transition stages.

3.1.2. Phase Module Topology

The converter phase modules are arranged in 3-level, NPP (Neutral Point Piloted) topology. This topology was first presented by J. Holtz in 1977 [35], it is derived from the ANPC [14] [15] and analogous to the T-Type topology, but has series associated IGBTs

[36]. In this case 2 series IGBTs are placed in the vertical arms positive and negative per phase module, as proposed by [37].

While in the ANPC the control needs to be adapted, T1 and T2 in the NPP receives the same firing command that was sent to the T1 alone in the NPC, while T5 receives the commands that are sent to T1 in the NPC, and reciprocally for the negative arm. Therefore, the switching pattern doesn't need to be changed when converting from the conventional topology to NPP.

Figure 3.4 shows the phase module circuit and an example of switching states to apply $V_{DC}/2$ with a positive current into the load. The representation of the switching states will be here simplified by a 4 digits number taking advantage of the fact that IGBT pairs T1&T2 and T3&T4 receive the same firing commands. The letter Q will be used to reference the whole flat-pack frame comprising the IGBT (T) and the FWD (D).

The vertical switches Q1 to Q4 have a parallel resistance of high value to equalize the steady state voltage distribution and an RC snubber to reduce the surge voltages during the turn-off and to help balance the dynamic voltage distribution during the switching between the series IGBTs.

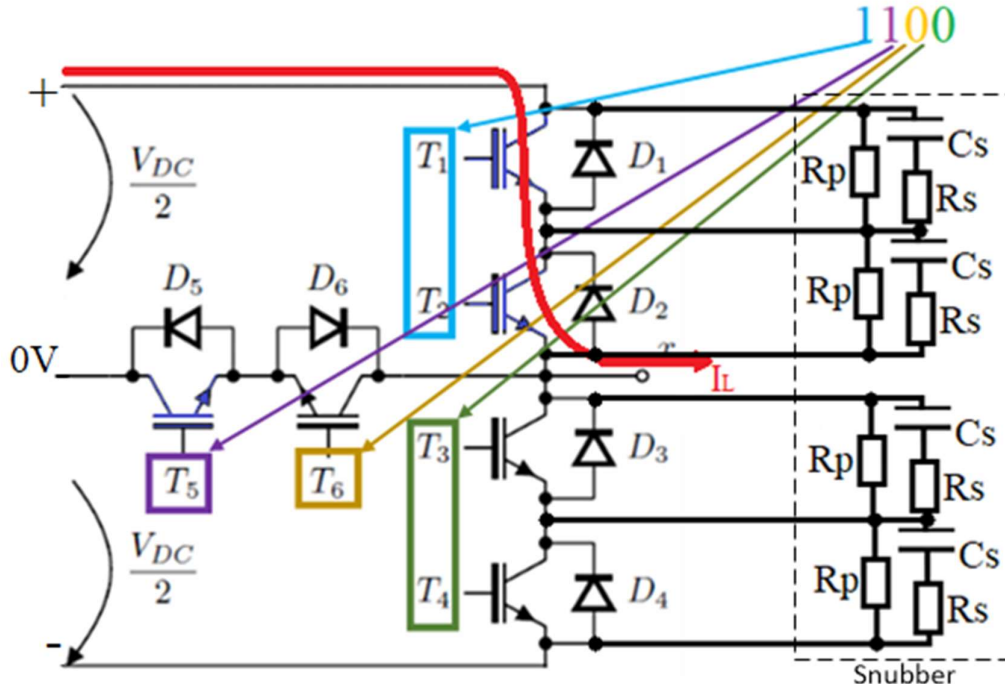


Figure 3.4: 3-level NPP topology and 4 Digits Representation for Switching States. Example of state 1100 with $i_L > 0$ (adapted from [36])

Table 3.1 summarizes the switching states and shows the devices that commute depending on the load current flow. To support the analysis in the next sections, it is important to remark that although the maximum switching voltage seen by the vertical IGBTs is half DC link divided by two or $V_{DC}/4$, the maximum blocking voltage is $V_{DC}/2$. For instance, when T3 and T4 are conducting, T1 and T2 receive the full DC link voltage. On the other hand, IGBTs T5 and T6, switch and block half DC link voltage.

Although the total power loss per phase module is the same in the NPC and the NPP, the NPP topology has a more efficient loss distribution per IGBT at high modulation. The difference is the most relevant in the switching losses of the external vertical IGBTs due to the use of series IGBTs in the NPP. This can be advantageous for high-speed applications in which the switching frequency is high and there can be a thermal overstress on the external vertical IGBTs T1 and T4 of the NPC [37] [36].

Table 3.1: Activated IGBTs versus the Desired Output (adapted from [36])

Output voltage level		$V_{DC}/2$	0	$-V_{DC}/2$
Switching signals sending on		T ₁ , T ₂ , T ₅	T ₅ , T ₆	T ₃ , T ₄ , T ₆
4 Digits Representation		1100	0110	0011
Current is leaded by	$i_L > 0$	T ₁ , T ₂	T ₅ , D ₆	D ₃ , D ₄
	$i_L < 0$	D ₁ , D ₂	D ₅ , T ₆	T ₃ , T ₄

Figure 3.5 compares each topology and the calculated power losses in a experimental test bench built as a chopper composed of one NPP commutation leg and one NPC leg [37]. The DC bus voltage was 600 V and the load current was 90 Arms, the switching frequency was 20 kHz, unit power factor, modulation index=0.8 and PWM type=H3. It is possible to notice that T1 losses are diminished in the NPP and comparing the losses of T2 on the NPC with T5 on the NPP, once those IGBTs receive the same firing commands.

The major disadvantage and a risk factor of the NPP topology is the use of series IGBTs. T1 and T2 are supposed to switch at the same time. However, due to practical differences in the two IGBT units, tolerances of the components of the snubber circuit and the $R_{g_{ON}}$ and $R_{g_{OFF}}$ resistors in the gate drivers, the voltage and current sharing between the two series IGBTs will be non-ideal and one device can dissipate more power than the

other. The phase module design considers some margin for this difference in the estimation of the junction temperature and definitions of the cooling system, yet, if one of the two IGBTs fail in short circuit the other will face higher blocking voltages and higher losses that can lead to its fault.

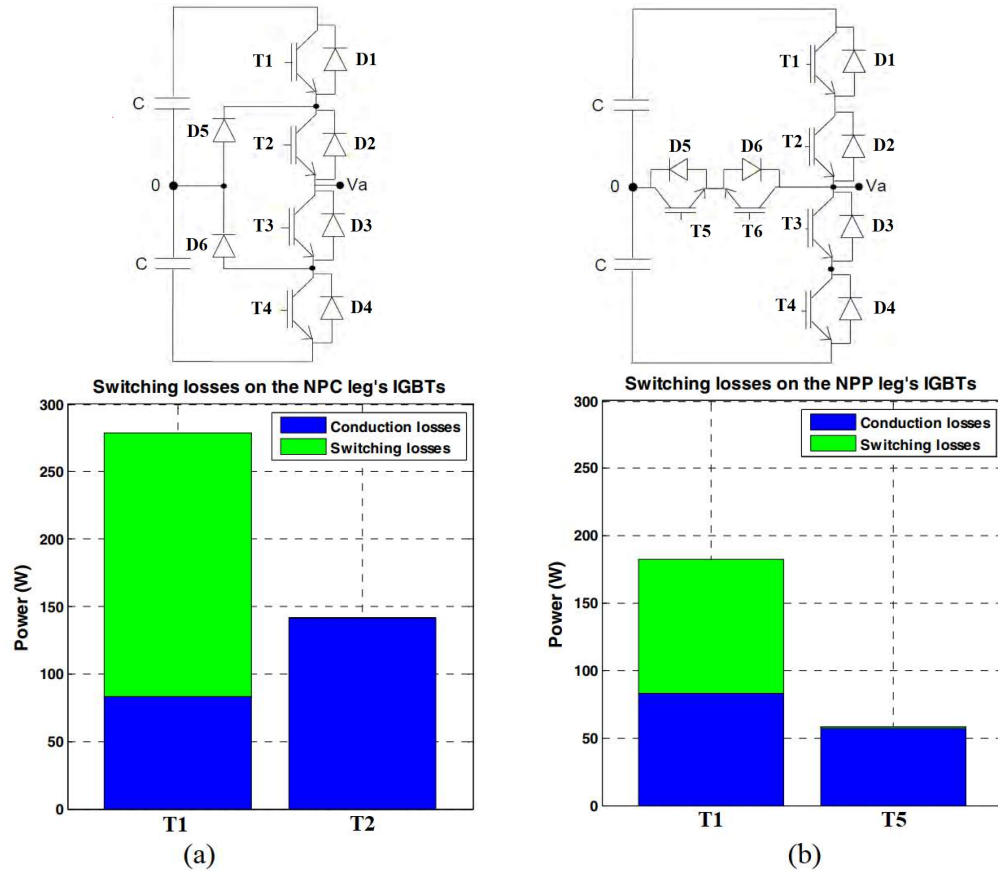


Figure 3.5: 3-level NPC vs NPP power loss comparison [37]

3.2. Converter Circuit

The converter comprises 12 phase modules placed in 2 parallel bridges at the AFE (Active Front End) input and two at the MB (Machine Bridge). The AFE input has a LCL'L filter [38], with a series reactor of 1.7 mH, and a resonant branch. The output has a dv/dt filter comprised of a smaller series reactor of 140 μ H and a RC shunt. Figure 3.6 shows the converter single line diagram with the main components, measurement points and communication interface. The DC link of the two AFEs are interconnected, as well as the DC link of the two inverter bridges. The AFE side positive and negative DC link poles are also connected to the MB side poles respectively, but not the 0V (zero-volt potential in the converter). A resistor is placed between the inverter bridge 0V and the ground to monitor the system (transformer, converter, and motor) insulation.

The drive control architecture is formed by 2 CPUs, one for the AFE and one for the inverter side or MB. The auxiliary faults and the overall control are processed in the CPUs. Each CPU is connected to two dedicated DSP boards, one for each parallel bridge. These boards are responsible for the IGBTs firing. They can monitor and fast actuate to suppress the commanded pulses in the case of critical faults.

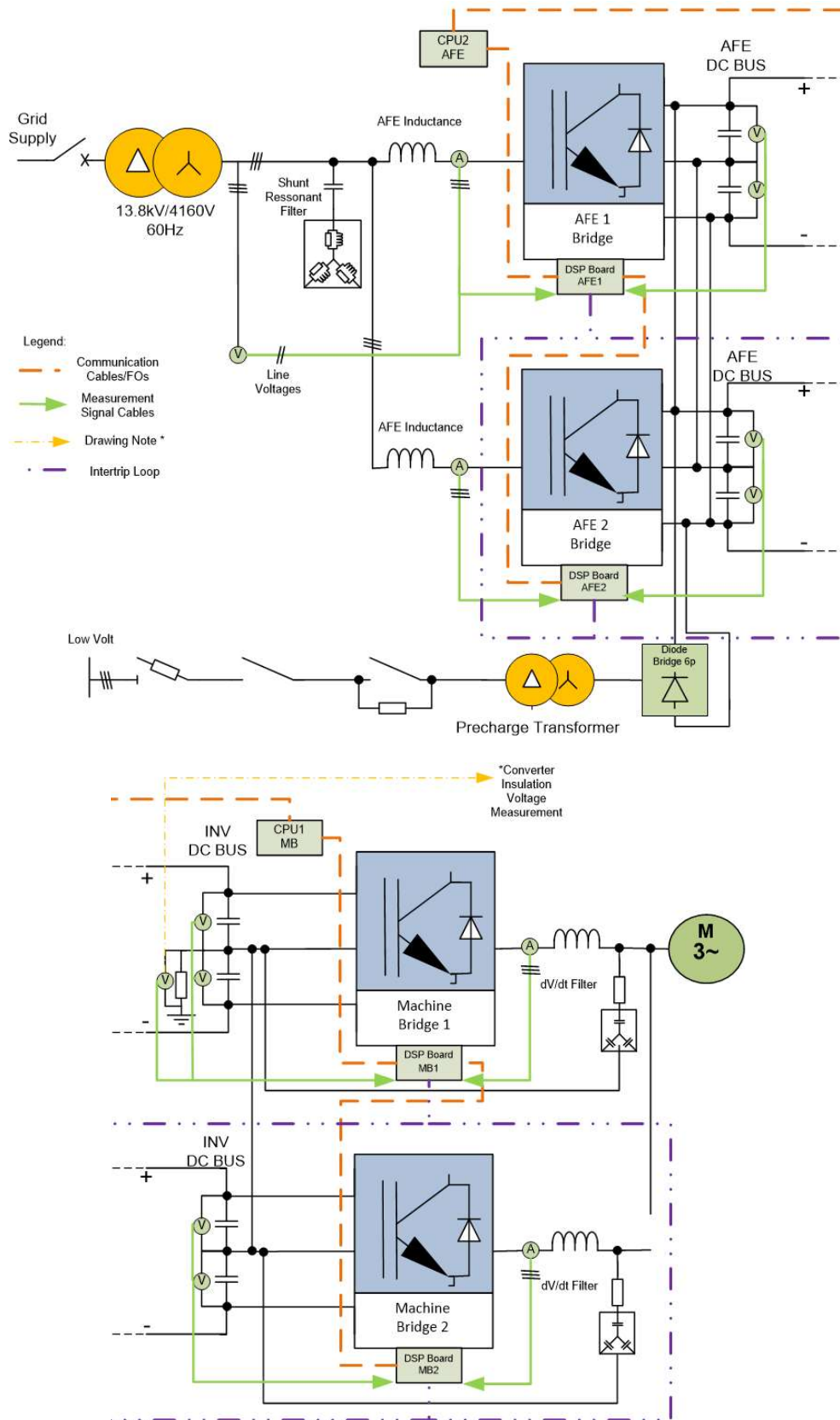


Figure 3.6: Schematics the converter under analysis (top: AFE, bottom: MB)

The synchronous SHE (Selective Harmonic Elimination)-PWM [39] [40], 5 angles, is the switching strategy of the AFE side, having a switching frequency around 600 Hz (each device sees half of this frequency). The MB side operates in H3-PWM at 660 Hz. The sampling time is twice the MB output PWM frequency, i.e, $T_s(\text{sample time}) = 1/2(F_{pwm}) = 757 \mu s$.

Table 3.2 summarizes the main parameters of the system formed by the insulation transformer, the converter, and the motor. These parameters are used in the simulations developed in Chapter 5.

Table 3.2: Main Converter Measurements and Conventions

Item	Parameter	Value	Unit
Grid	Line voltage	13.8	kV
	Frequency	60	Hz
	Short Circuit Power (Scc)	251.7	MVA
Insulation Transformer (D1Yn)	Nominal Power	6	MVA
	Primary Voltage	13.8	kV
	Secondary Voltage	4160	V
	Impedance	8	%
AFE PWM Control	PWM_type	SHE PWM – 5 angles	
MB PWM Control	Switching frequency	660	Hz
	PWM_type	H3PWM	
DC Link	DC Link Nominal Voltage	6400	V
Motor	Nominal Power	5	MW
	Primary Voltage	4	kV
	Number of Pair Poles	6	-
	Power Factor	0.85	-
	Frequency	26.5	Hz
	Nominal Load (Quadratic)	195	kNm
	Total inertia	45000	kgm2

The main measurements monitored by the converter control are shown in green in the Figure 3.6 and are summarized in Table 3.3 with the p.u. convention and protection threshold.

Table 3.3: Main Converter Measurements and Conventions

	Main measurements	Convention	Read by Controller	Protection Threshold
1	3 $\emptyset$ currents at the of the PMs to the motor, before the dv/dt filter	1 p.u.=750 A (530 Arms) positive when going to the motor	MB	1.4 p.u.
2	DC link Voltages referred to the 0V on the MB side	0.5 p.u.=3200 V*	MB	0.625 p.u.
3	0V to ground insulation voltage	1 p.u.=6400 V*	MB	0.5 p.u.
4	3 $\emptyset$ currents at the of the PMs to the grid, before the LCL'L filter	1 p.u.= 750 A (530 Arms) positive when going to the converter	AFE	1.4 p.u.
5	Input line voltages at the secondary side of the transformer, after the LCL'L filter	1 p.u.=5883 V (4160 Vrms)*	AFE	1.22 p.u.
6	DC link Voltages referred to the 0V on the AFE side	0.5 p.u.3200 V*	AFE	0.625 p.u.

Note: *DC link and input voltage readings are not in the same base.

3.3. Type of Faults and Protection

Differently from press pack IGBT, or IEGT (Injection-Enhanced Gate Transistor), that have a guaranteed SCFM (Short Circuit Failure Mode) due to its constructive characteristics [41], flat-pack devices can fail in both open and short circuit. Special attention is given to the short circuit failure mode since it can create a short circuit event and a path for the fast discharge of the DC link capacitors with a high current if another switch is turned ON with the one that failed [42]. Therefore, it is important to study the types of short circuit faults, the gate driver protection, and the actuation of the main DSP board to turn-off all the IGBTs.

Three types of short circuit fault can happen inside the NPP phase module [42] [43]:

- Type 1 or HSF (Hard Switching Fault): The IGBT is turned ON into an existing short circuit forming a path for the short circuit current.
- Type 2 or FUL (Fault Under Load): The short circuit happens while the IGBT is already turned ON and carrying the load current.
- Type 3 or FWD failure: The short circuit happens during the conducting mode of the FWD.

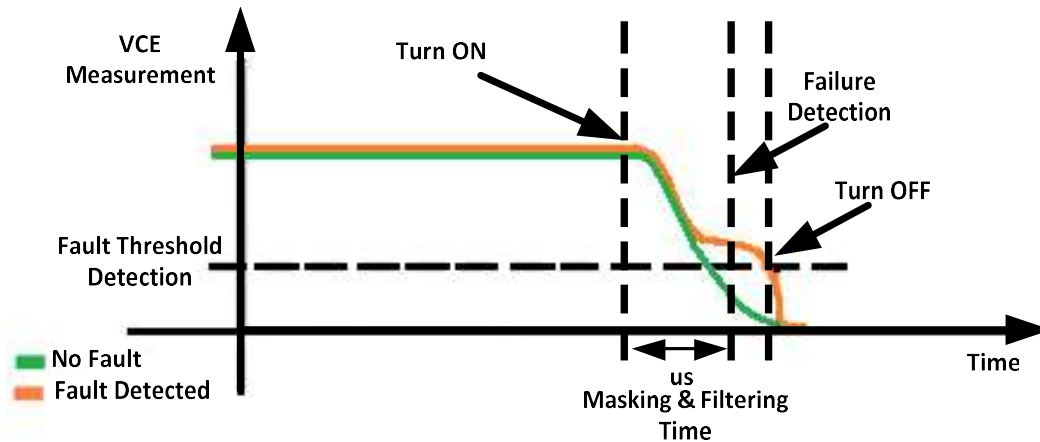
Those faults would involve a fast discharge of the DC link capacitors into the phase module internal circuit and would be only limited by the stray inductances in the short-

circuit current path, i.e, the DC capacitors stray inductances, the IGBT stray inductances as show in Figure 3.3 and mainly the stray inductances in the connection path, i.e, the connection between the DC capacitors and the phase modules and the phase module internal connections of the IGBTs. Since it is internal to the phase module, the short circuit current is not directly measure and the gate driver is the only component able to detect the fault. [44]

According to [43], another type of short-circuit can be described for the condition in which the short circuit occurs while an IGBT is turned OFF without taking any blocking voltage, like the case of redundant output states for multilevel inverters. This type of short-circuit will not be detailed here since it is not applicable to the NPP topology objective of this study.

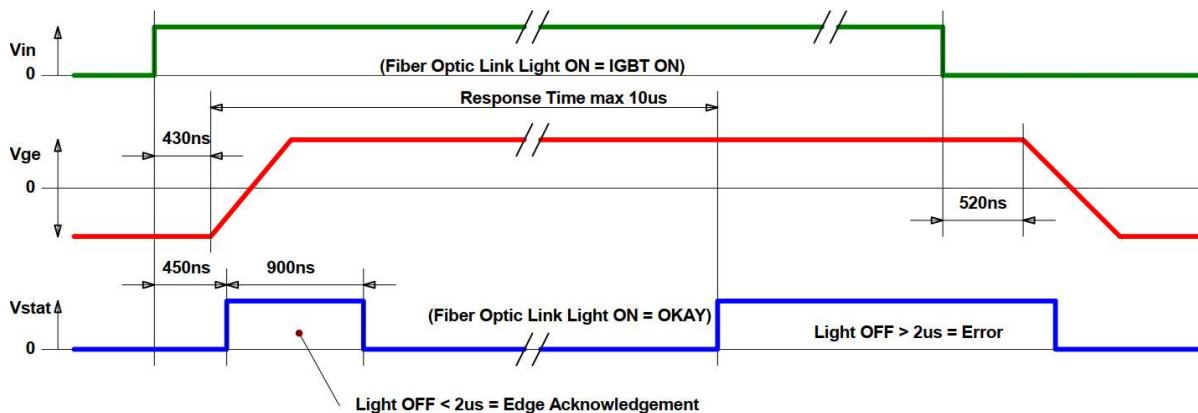
3.3.1. Gate Driver Protection

The main protection inside the converter are obtained by the gate driver direct monitoring of the IGBT and the actuation of the DSP board based on the measurements, as per thresholds shown in Table 3.3, and the status of feedback optical fiber. The gate driver has two types of protections, the undervoltage detection of its gate voltage and the short circuit protection based on the V_{CE} desaturation monitoring. For the latter, the voltage is checked after the turn-on command, a short circuit fault is considered when the V_{CE} voltage remains greater than 1.2 kV after the masking time of 10 μs , as illustrated in Figure 3.7 and Figure 3.8 [31] [45].

Figure 3.7: GD, V_{CE} Desaturation Short Circuit Protection

To avoid the effects of turning-off with a very high short circuit current, as explained in Section 3.3.3, the gate driver is configured not to turn-off immediately but rather send a failure status to the controller which will apply the hierarchical turn-off process. The IGBT is turned OFF only when the gate driver receives a light OFF signal in the firing command, as shown in Figure 3.8. The last blue line represents the IGBT status, when this signal is high the feedback fiber optic is turned OFF.

As an example, considering the Short Circuit Type I, the IGBT would turn-on, then a short circuit current would be created not letting the V_{CE} voltage to reduce to normal conduction level, as shown in Figure 3.9. The gate driver would check the voltage and turn the feedback light OFF, 10 μs after receiving the turn-on command.

Figure 3.8: Gate Driver V_{CE} desaturation Short Circuit Protection [45]

Note that in Figure 3.8, the light OFF signal of 900 ns shown when the IGBT turns ON (positive V_{GE}) is a separated functionality called Edge Acknowledge that can be used

to confirm the firing command received by the IGBT. This light OFF pulse lasts less than 2 μs , while a fault detected light OFF remains activated until the IGBT turns OFF.

It is worth mentioning that although not available in this real case application, other protections can be included in the gate driver to try to detect and interrupt the switching prior to the formation of the short circuit current. Measuring V_{CE} voltage when the device turns off and triggering a protection if the voltage doesn't rise within a certain time, is an example. Also, for devices with guaranteed SCFM with several IGBTs associated in series for each voltage level, if a device fails the expected voltage per device when the IGBTs are turned OFF will be higher what can be used to actuate a protection. This depends though on the number of series devices and DC link value, because the overvoltage that happens during the normal turn-off can cause the protection to act improperly.

3.3.2. DSP Board Actuation

Table 3.4 details the hierarchical turn-off sequence. The path after a trip and up to the OFF-state is shown with red arrows. The normal possible switching states and intermediate states (dead time) are represented with blue arrows. If the trip is detected at the null state, the decision is taken based on the previous state sequence, e.g., if it's a null state coming from the positive state, then it takes the path 0110→0100→000 and the negative path if coming from the negative state. The hierarchical turn-off process is decided by the DSP FPGA and will respect the deadtime states before turning OFF all the IGBTs in the same phase. The deadtime for the real case under analysis is 20 μs . The DSP processing time is much faster than the IGBT switching, around 33 ns.

Table 3.4: Trip Sequence from DSP board and Firing States

Final State	Trip	Intermediate State (Dead Time)	Trip	Off State
Positive 1100	→	0100	→	
Null 0110	→		→	0000
Negative 0011	→	0010	→	
Legend:				
→	Trip			
→	Normal Sw States			

The DSP boards have a loop fiber optic called Intertrip, represented in purple in Figure 3.6. When one of the boards identifies the fault, it sends the others a light off signal that commands them to cut off the firing commands of the other bridges as well.

3.3.3. Short Circuit Type 1

An example of short circuit type one is if T6 is turned ON following the state 1100 in Figure 3.4, but for some reason devices T1 and T2 are short circuited and fail to turn-off. A VDC+ to 0V short circuit inside the NPP phase module would be formed and a high current will flow through the devices T1, T2, T6 and D5.

Figure 3.9 represents the idealized internal electrical behavior in the device T6 when it is trying to turn-on and the short circuit current is formed. The analysis of the waveforms can be divided into 5 critical points [42] [46].

- Short Circuit Start: The IGBT blocks the DC link voltage. When the gate voltage rises commanding the IGBT to turn-on, a short circuit is formed, and the collector current rises steeply.

Due to the higher current, the voltage across collector and emitter will not fall to the saturation value as expected. Instead, the new value of the V_{CEON} voltage will depend on the voltage drop across the parasitic inductance in the fault loop path, or $L_{strayTotal} * di_C/dt$.

- Point I: The current stops rising at the transition to the active region at a specific gate voltage. Latch-up can occur.

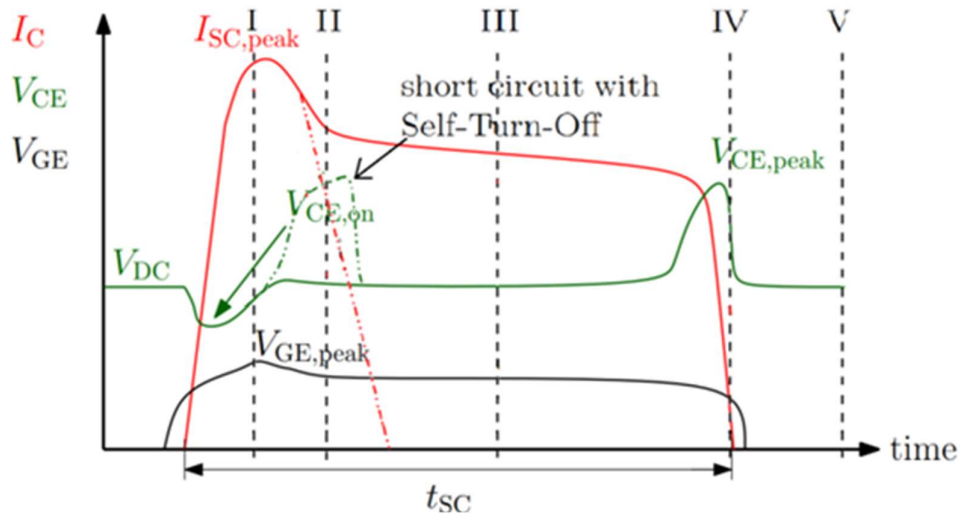


Figure 3.9: Typical current and voltage waveforms during Short Circuit Type 1 (adapted from [42] and [46])

Figure 3.10 shows the $I_c \times V_{ce}$ curve of the Hitachi MBN750H65E2 under study, combining the behavior at ambient temperature and at 125 °C. The transition from the saturation to the active current is highlighted. It is possible to notice that for 15 V of gate supply voltage the current to enter the saturation region is not shown. In fact, the only information given in [30] is the maximum allowable pulsed collector current, $I_{CP} = 1500$ A for 1 ms. This is the current limit of the RBSOA (Reverse Bias Safety Operating Area), or the current conditions over which the manufacturer guarantees that the IGBT can be turned OFF without self-damage [34]. Based on discussions with Hitachi for the performance of this study, the actual transition to the active region for 15 V of V_{GE} can be estimated as 3500 A at ambient temperature.

It is important to notice that the peak short circuit current is often higher than the saturation value because, as represented in Figure 3.9, V_{GE} rises to a peak value above the applied voltage due to a weak clamping of the gate voltage, parasitic inductances in the gate-emitter path (L_g) and displacement currents at the Miller capacitance (C_{gc}).

At this point, the maximum collector current would slightly decrease due to the self-heating during the short circuit as shown in Figure 3.9 if the IGBT survives the current rise. However, if the current becomes too large, injected electrons may turn-on the parasitic transistor shown in Figure 3.2 and the IGBT would latch-up. The IGBT controllability is lost, and the maximum current cannot be guaranteed. Further details of latch-up process in the IGBT structure are presented in Chapter 6.

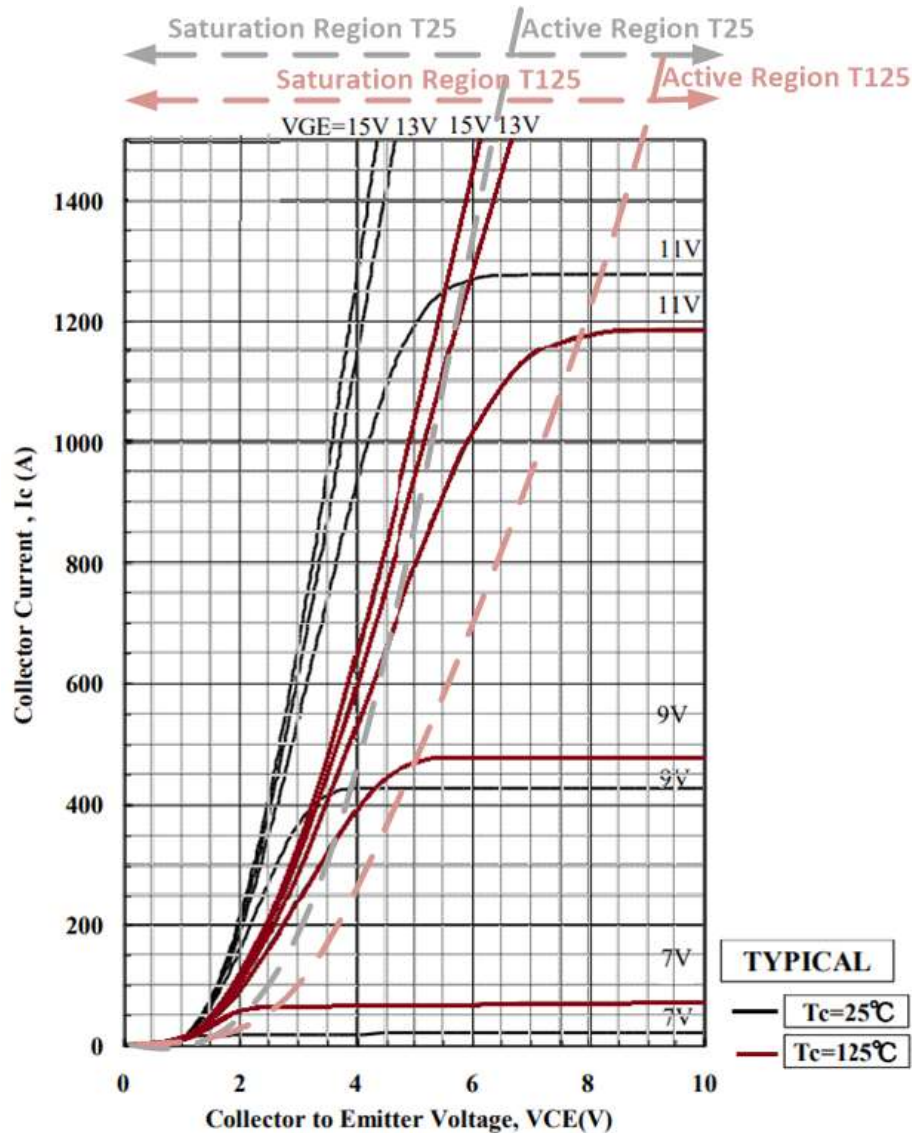


Figure 3.10 IGBT Expected ON-state Current vs Voltage [30]

- Point II: The STO (Self-Turn-Off) mechanism can occur shortly after the turn-on.

As explored by [42], the IGBT can turn itself OFF shortly after running into short circuit, thus not being controlled by the process described in Sections 3.3.1 and 3.3.2, i.e., gate driver fault detection, then feedback light OFF to advise the DSP board, which finally turn the firing command OFF. Although it is a fast phenomenon that happens after the fault, the V_{CE} overvoltage during the STO is oscillating, difficult to control and can disturb the V_{CE} -desaturation protection of the gate driver shown in Figure 3.7.

- Point III: Time under short circuit can lead to Thermal Runaway.

If the IGBT is surviving the event, it will stay with a high current and high voltage for the time under short circuit t_{SC} , which can lead to thermal runaway due to the strong self-

heating associated. t_{SC} is also known as the Short Circuit Pulse Width, in the IGBT's datasheet. For the Hitachi IGBT under this study, this time is $10 \mu s$ [30], and matches the expected time to detect and turn-off for the gate driver.

- Point IV: Short-circuit turn-off. Dielectric breakdown can happen due to the overvoltage generated by the collector current variation over the stray inductance.

Like point I, the overvoltage created by the $L_{strayTotal} * di_C/dt$ adds to the rated blocking voltage and can overpass the IGBT insulation capabilities [47].

- Point V: Normal blocking conditions if the IGBT can survive the short-circuit.

Manufactures has been improving the IGBTs characterization under short-circuit into the SCSOA (Short-Circuit Safe Operating Area), which not only accounts for the defined time in short-circuit t_{SC} related to the thermal runaway, but also the maximum allowed V_{CE} and peak saturation current I_c that can cause the immediate destruction of the IGBT during the desaturation process [48] [49].

3.3.4. Short Circuit Type 2

Figure 3.11 represents the internal electrical behavior in the IGBT for a short-circuit type 2. The waveforms are very similar to the ones for the type 1, unless for the point in which the short-circuit starts and the current I_c rises to the maximum peak. In this case, the device is already carrying the load current, thus it is flooded with charge carriers and operating in the saturation region with a correspondent V_{CEsat} . When another device fails and the short circuit occurs, the collector current rises steeply up to a maximum fault. The IGBT desaturates and now the V_{CE} voltage rises steeply to the desaturation value.

The dv_{CE}/dt can be very high and can influence the gate voltage significantly. With a higher gate voltage overshoot, the maximum current, $I_{SC,peak}$, will be higher too. Then the gate voltage decreases back to the applied level, consequently the current is lowered to the correspondent gate voltage value in the active region and there will be the overvoltage $V_{CE,peak1}$. If this peak is higher than the maximum allowed value in the SOA, the IGBT will damage. Besides, the STO phenomena will involve more energy and destruction if it happens, as observed by [42].

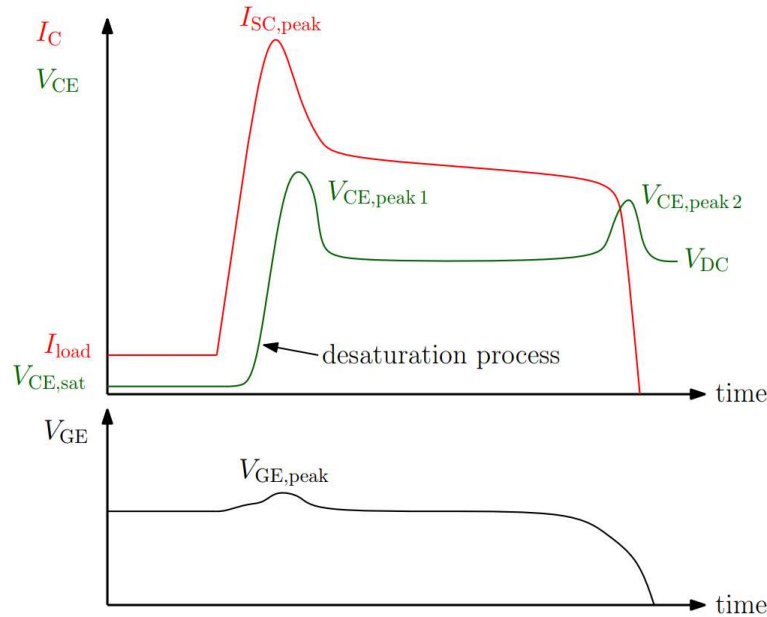


Figure 3.11: Typical current and voltage waveforms during Short Circuit Type 2 [42].

If the IGBT withstand this moment, then the rest of the idealized behavior is very similar to the short-circuit type 1 with the critical moments being the thermal withstand of the high I_c current and high V_{CE} voltages up to the turn-off point in which there will be another $V_{CE,peak}$ due to the interruption of the current.

3.3.5. Short Circuit Type 3

In this case the short-circuit starts while the FWD is conducting the current. The IGBT may or may not have already the gate voltage applied to it. The short circuit current flows from the Anode to the Cathode of the FWD.

The case in which the gate voltage is applied to the IGBTs could be for instance when the current is flowing from the load to the DC link during a deceleration for state 1100 shown in Figure 3.3. It would be passing through D1 and D2 while T1 and T2 are turned ON. If Q6 fails, there will be a short circuit current going from the DC link to the 0V, in opposite flow to the initial load current.

The FWD experiences a fast reverse recovery with a high di_c/dt when the short circuit current commutates from the FWD to the anti-parallel IGBT due to the gate voltage applied to the IGBT. At first, the IGBT should relieve the diode by taking the current, yet an

avalanche process can occur in the diode, and it would take the complete short-circuit current incurring in the risk to be destroyed [43] [50].

If the diode survives the fault, the idealized short circuit behavior will be similar to the short circuit type 2 with the same critical points in which the IGBT can fail, as shown in Figure 3.12. The passive turn-on point marks the reverse recovery and possible avalanche that can happen to the FWD.

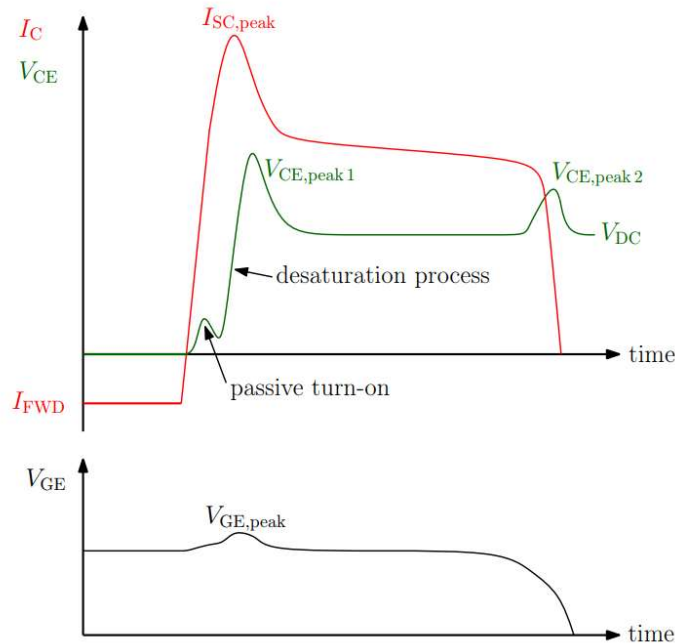


Figure 3.12: Typical current and voltage waveforms during Short Circuit Type 3 [42].

The case without gate voltage or, more commonly, at a negative value to avoid undesirable turn-on through the Miller capacitance, can happen during the dead time in the migration from state 1100 to 0110, for example. State 0100 would be applied and diode D6 would immediately turn-on to commutate the current from T1 and T2.

The current will not commute to the IGBT and the risks of damaging the FWD are even higher. The overvoltage during the reverse recovery is amplified by the negative di_C/dt which only depends on the DC link voltage and the parasitic inductances.

3.4. Conclusions

This chapter presented the phase module as the main modular subassembly of the converter under study and focus of the analysis performed in the next chapters. The phase module is built with flat-pack IGBTs arranged in NPP topology to improve the power loss distribution. A convention of 4 digits representation for the IGBTs states is introduced to facilitate the explanation of the PoF and most probable fault sequence described later in the text. Furthermore, the converter circuit containing 2 parallel AFE bridges and 2 MBs is shown, indicating the main points of measurements as the input and output currents, the DC link, and the input voltages. As usual, no visualization of the internal physical values of the electrical quantities inside the phase modules is available, unless for the gate driver monitoring which provides the main protection through its interaction with the DSP board dedicated controller. After identifying a fault, the firing pulses will be interrupted respecting the hierarchical turn-off process, which goes to the 0 state after applying the states with DT. The type of protection is based on a reaction to the short circuit current, thus depending on the SC to be established first. Therefore, even when the fault is detected and the IGBT is turned off within the maximum allowed time of 10 μ s, the device will experience overstress due to the behavior of the current I_C and voltage V_{CE} under fault and depending on the type of fault. The critical points related to the device under fault conditions that can lead to its destruction are presented and help justify the spread of the fault effects observed in the next chapters despite of the correct actuation of the protection and disabling of the firing command to all devices in the converter.

Chapter 4. Fault #1 – Input Filter Insulation Failure

The first of the two consecutive real fault events is examined in this chapter. The fault is explained, and the recorded plots are presented. The results of tests performed to investigate the state of the remaining IGBTs after the fault are listed, as well as the final converter configuration when the operation was restored. Later, a second fault was registered with evidence pointing to the failure of an IGBT that was deteriorated by the first fault. The second fault is analyzed in Chapter 5.

4.1. Fault #1 Analysis

This fault is of interest mainly to understand the converter conditions prior to the main fault that probably happened due to the reuse of a degraded device as detailed in Chapter 5. The post fault analysis of the converter showed a structural issue with the connections in the AFE input filter. This probably led to a phase to 0V short circuit at the converter input due to the loss of insulation between the terminals of the input resonant filter capacitors of phase V and its structure, referred to the 0V.

The LCL'L filter has a resonant branch syntonized to damp the H17 and H19, first predominant harmonics left by the SHE PWM switching strategy used in the AFE [38]. To achieve this resonant behavior a series-parallel arrangement of commutation capacitors, model E62, from ELECTRONICON is used. The capacitors frames were fixed on a metal plate that was connected to the 0V. This connection was made to give the capacitors metal casing a reference and guarantee that the maximum terminal to case voltage would be respected. Figure 4.1 illustrates the filter assembly highlighting the frame connection of the capacitors to the 0V reference.

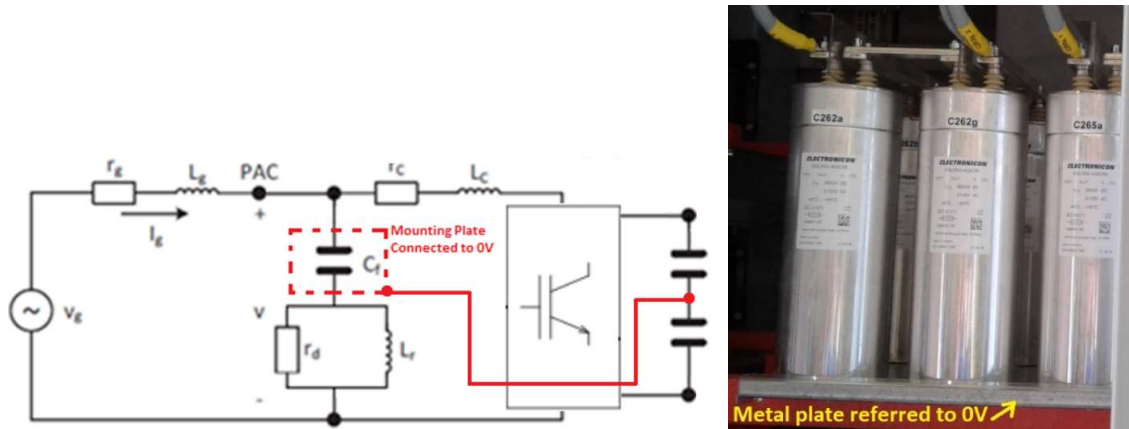


Figure 4.1: LCL with Resonant Branch (Left: AFE Input Filter Scheme. Right: Mechanical Assembly of the Resonant Filter Capacitors)

The insulation distances were in accordance with the IEC 61800-5-1 [51] and the voltage level, but mechanical issues were verified in the assembly of the capacitor connections. Rigid copper busbars were used in the terminals instead of flexible connections to allow for thermal expansion and contractions of the capacitor's cans during operation, as per supplier recommendation [52]. Furthermore, only one nut directly tightened to the capacitor insulator was used, while a counter nut would allow the application of the correct torque without damaging the insulator. The ideal terminal connection assembly is illustrated in Figure 4.2.

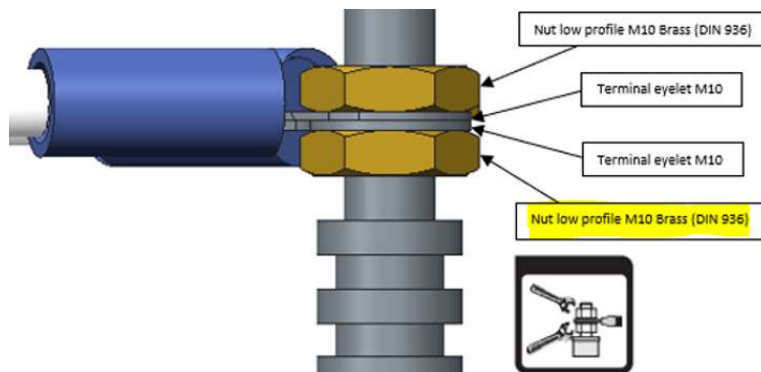


Figure 4.2: Recommendation for Capacitor's Terminal Connection using Counter Nut [52]

The post fault analysis of the converter found different points of arc flash evidence in the capacitor terminals and the casing as illustrated in the images of Figure 4.3. The capacitor connected to phase V suffered the highest overheating and the whole terminal melted. There were also signs of the arc propagation along the rigid busbars used in the terminal connections.

Therefore, it is likely that applying torque to the capacitors without the counter nut probably overstressed the connections, which were further degraded due to the rigidity

of the busbars whenever the capacitors cans would thermally dilatate and contract. Furthermore, the high frequency harmonics present in the resonant filter currents could have contributed to increase the contact resistance due to skin effect, increasing the deterioration of the contact area.

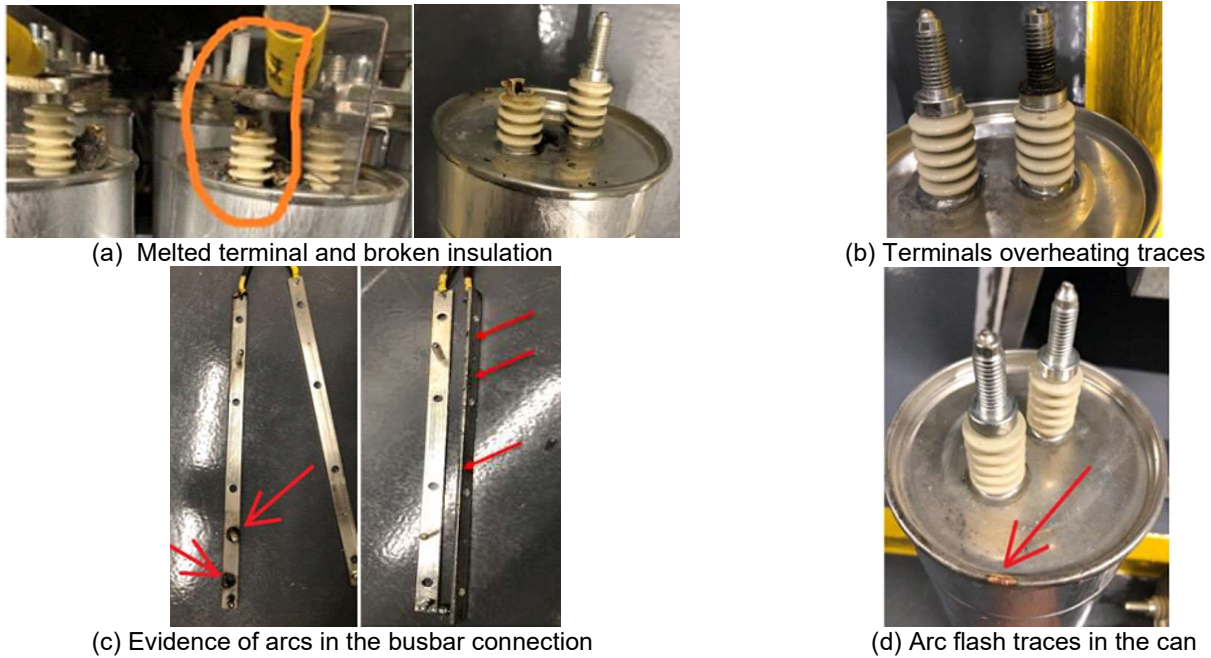


Figure 4.3: Evidence of Phase to 0V Arc Formation in the Capacitors Terminals

Figure 4.4 illustrates the filter assembly highlighting in orange the metallic frame connection of the capacitors to the 0V. The FWDs and the arc flash bypassing the line inductor of phase V form a half wave dual polarity rectifier uncontrollably charging and discharging each half DC link set of capacitors. The current of this initial stage is here called I_{sc1} (Short Circuit Current 1), shown in green.

Figure 4.5 shows the recorded fault plot with the dc link voltages on the AFE side, the six input currents per phase module (positive when going from the grid to the converter), the line voltages at the secondary side of the transformer and boolean signals of the moment in which the DSP board stop sending the firing command (shifted in the y axis to facilitate visualization).

Even with the firing commands turned OFF, marked by the red vertical line in Figure 4.5, I_{sc1} flows from phase U through the FWDs and charges the capacitors of the positive DC link while the voltage in phase U is higher than phase V. At the same time, the negative capacitors discharge through the arc back to phase V. Similarly, during the rise of the line voltage VW, the negative capacitors are charged. The current flow is positive when flowing from grid towards the DC Link, as shown in Table 3.3.

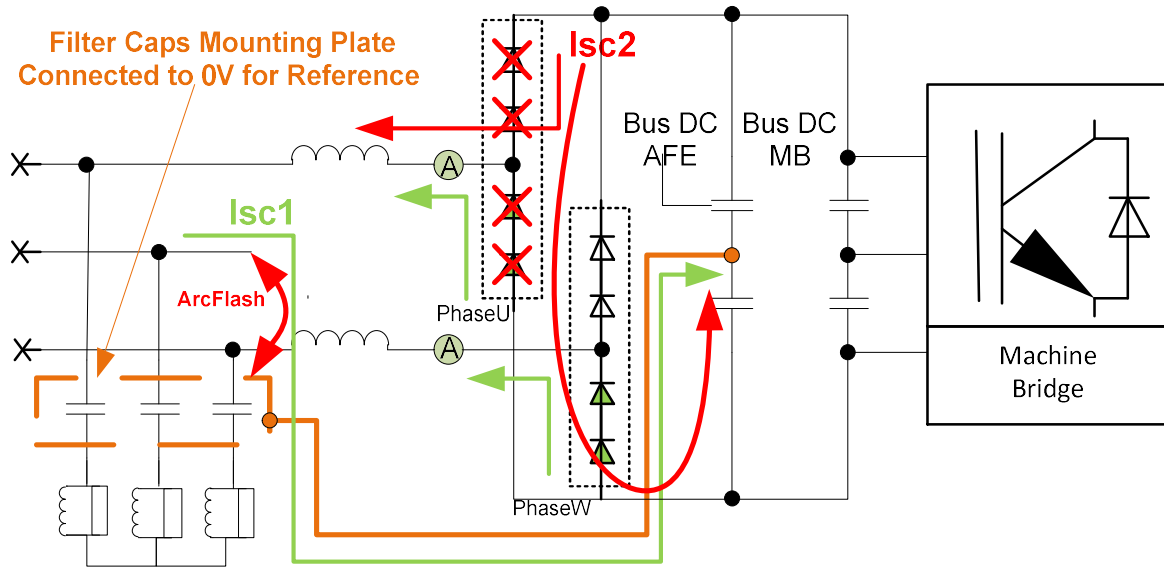


Figure 4.4: Filter Capacitor's frame reference connection and Short Circuit Current Path during Vvw Positive Semi Cycle

The DC link voltages and currents during this process are much higher than the rated values of the converter, even reaching the DSP board end of scale (flat reading in the plot), and could be only interrupted by the opening of the main breaker. Although the command to open the breaker is sent at the trip detection, the opening process takes 60 to 80 ms.

The FWDs are degraded by this current flow, and fail to sustain the higher DC voltages, collapsing and generating the positive to negative short circuit with even higher currents. This moment is represented by I_sc2 in

Figure 4.4 and the dashed red vertical line in Figure 4.5.

As mentioned in Chapter 3, the sampling time in the plot is $757 \mu s$ and therefore it is important to point out that intermediate fast variations, like IGBT transitions that happens in a few microseconds, and the exact state of the switches at all moments are impossible to determine.

Therefore, the fault event can be divided in two main stages. In the first one, the short circuit is formed in the resonant filter on the AFE side. Secondly, there is a consequent short circuit in the full DC link, positive to negative. Although the currents reach the reading end of scale, from the di/dt is possible to notice that the second stage has reached much higher short circuit currents. The detailed most probable fault sequence is listed next.

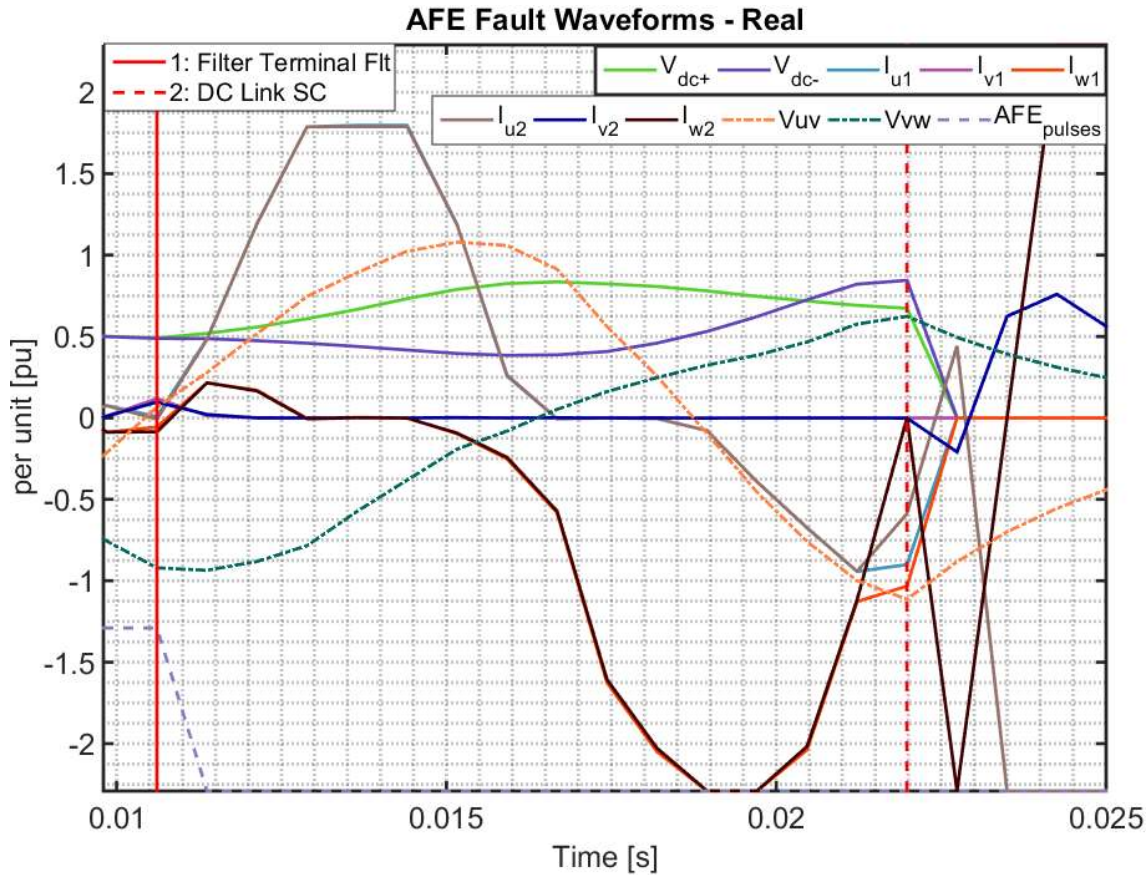


Figure 4.5: Fault #1 Plot – AFE

4.1.1. Fault #1 Sequence:

- 1) The short circuit start between the drive input phase V terminal of the resonant branch capacitors and the 0V reference to which the case is referred to.

Therefore, the 0V to ground voltage, which is used to monitor the system insulation, rises. This voltage can be seen in the MB fault plot shown in Figure 4.6. After the insulation voltage reaches ~ 0.2 p.u. the controllers identify the short circuit and stop the firing in all bridges through the fiber optic intertrip loop.

Since there is no connection from the 0V of the MB with the 0V on the AFE (see Figure 3.6), the DC link on the MB side rises evenly up to 1.6 p.u., right before the full DC link short circuit.

All measurements are frozen at around 0.04 s, this happened due to damage in the DSP controllers caused by current circulation through the 0V cabling used to give reference to the controller assembly. An improvement was later applied to the 0V reference and signal cabling going to the controller to avoid current loops and shield the

controllers from noise and fault effects. The details of this phenomenon was considered beyond the goal of this work and won't be treated in this text.

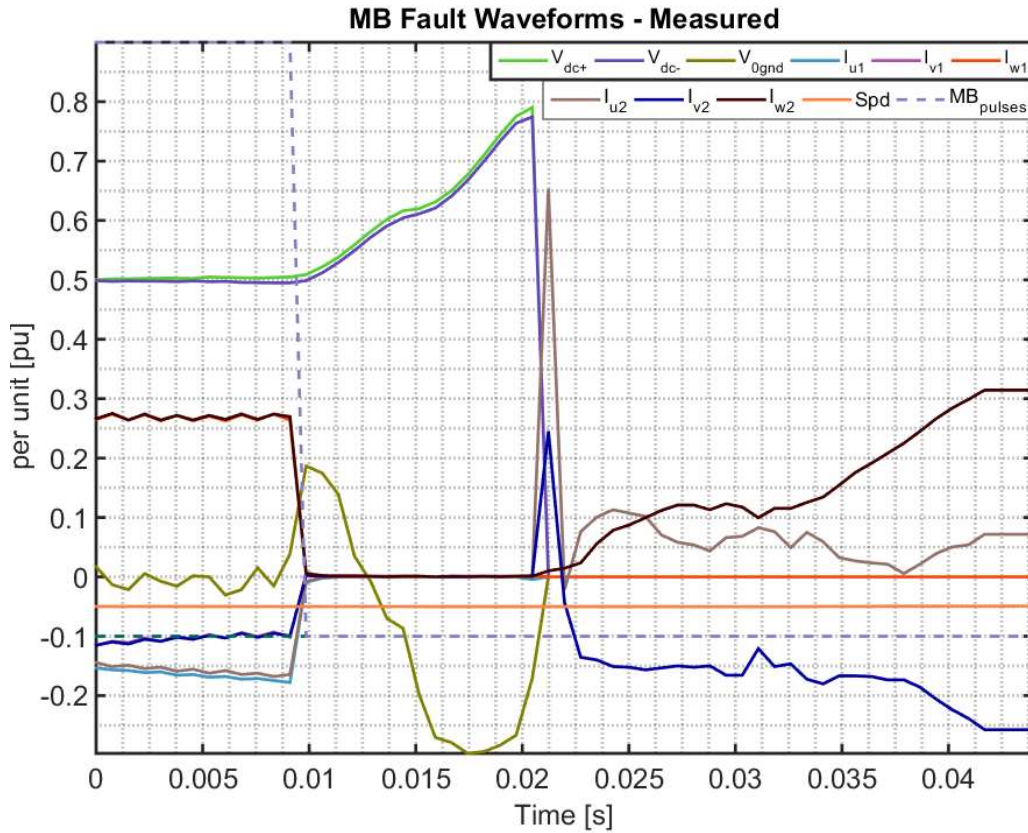


Figure 4.6: Fault #1 Plot – MB

- 2) Even with the firing of the bridges being disabled by the 0V to ground insulation detection and the intertrip loop between the DSP boards, a short circuit current path is created through the FWDs of the AFE phase modules, as shown in Figure 4.7.

The moment in which the short circuit is established between the input phase V and the 0V midpoint of the AFE can be identified by the increase of the current on phase U equally shared between AFE1 and AFE2 bridges. The increase of current is in phase with the UV voltage.

- 3) The circuit behaves as a half wave dual polarity rectifier with a direct bypass of the line inductor of phase V and its current sensor, reason why phase V measured current in Figure 4.5 for AFE1 and 2 is zero.

During the positive semi cycle of the input voltage UV, the current flows from the input through phase U and charges the capacitors of the positive DC link, returning through the arc that formed between the phase V and the 0V in the resonant branch

capacitors' assembly. The voltage of V_{dc+} increases while V_{dc-} slightly decreases with the IGBT firing pulses already disabled.

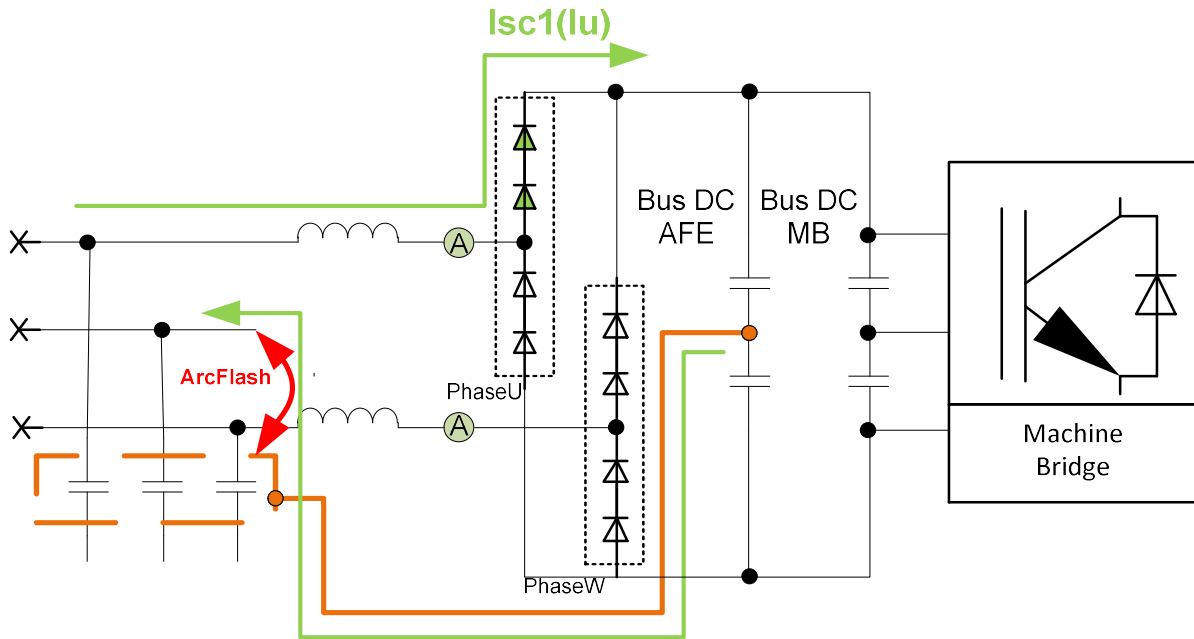


Figure 4.7: Short Circuit Current Path of Stage 1 during V_{uv} Positive Semi Cycle

- 4) The current in phase U increases up to 1.8 p.u. and then reduces to 0, as the voltage UV decreases.
- 5) Similarly, the voltage between phases V and W charge the negative capacitor during the positive semi cycle passing through the arc and returning through phase W and later phase U, as shown in
- 6) Figure 4.4.

The current of phase W increases on the negative direction up to -2.29 p.u., limit of the DSP board reading, with the voltage V_{dc-} increasing and V_{dc+} slightly decreasing.

- 7) The total V_{dc} reaches around 1.6 p.u. when both V_{dc+} and V_{dc-} drop to zero, most likely due to the short circuit of the upper FWDs.

This happens 22 ms after the pulses been disabled and is marked with the dashed red vertical line in Figure 4.5. Right before the full DC link short circuit, the current in the phases U and W are negatives, meaning that they pass in the lower vertical FWDs of each phase module. As the upper FWDs fail the full DC link short circuit is formed.

Considering the full DC link at 1 p.u as 6400 V, as per Table 3.3, the maximum voltage blocked per IGBT in the NPP topology would be around 2560 V. At first the Hitachi MBN750H65E2 flat-pack power modules would be able to sustain this voltage since they are 6500V, yet the maximum peak forward current that the FWD can conduct (I_{FRM}) is

1500 A, 2 p.u., for 1 ms [30]. For phase W the current stayed higher than 2 p.u. for around 2.5 ms and the current reading was limited at 2.29 p.u., see Figure 4.5.

8) After DC short circuit, the currents in the three phases increase and overpass the maximum measurement range again, with a higher di/dt . This second higher short circuit current is shown as I_{sc2} in

9) Figure 4.4.

After the fault it was verified that phase module W of AFE1 was the most damaged, with burnt parts, open frames and spread debris from inside the devices, indicating that the energy associated with the fault was more intense in this phase module. The vertical IGBTs of phase module L, in the MB2-W, also had cracks in the external frame, but no signs of big internal explosions.

The remaining phase modules were submitted to tests in the field before returning the converter to operation. The results are presented in the next section.

4.2. Post Fault #1 Tests

After the fault, a basic in-circuit pulse test using an external low voltage dc supply and the multimeter in voltage mode was conducted on site to evaluate the IGBTs and FWDs in blocking mode and the remaining ON-state voltage when conducting a small current from the supply.

Those are often the only tests executed before replacing the damaged phase module and reinstating the converter operation. However, to support the fault investigation, the insulation between the HV circuit and heatsink was measured as well as the Collector to Emitter insulation when applying 5kVdc with a Insulation Tester. As indicated by [25], the resistance reading would be several $M\Omega$ in normal conditions, but if the device has failed, it is seen as a short between C and E. The collector must be connected to the positive pole of the Insulation Tester (+), and the emitter to (-) to avoid energizing the FWD.

It is mandatory to avoid leaving the Gate to Emitter terminals disconnected while applying High Voltage to the IGBTs, since it can cause damage to the device, as indicated in [53]. In this initial case, the IGBTs were disconnected from the phase module circuit by removing the cables, but the GDs were kept on the IGBTs. The details of the collector to emitter insulation test are shown in Section 6.3.1.

All tests were performed at the ambient temperature. The IGBT terminal busbars were kept, so all three parallel devices assembled inside the same frame, as shown in Figure 3.1, were tested at the same time. Furthermore, each snubber resistor and capacitor assembly were checked with cables disconnected, but no relevant deviation was found.

Table 4.1. summarizes the results of the C to E insulation tests, each phase module is issued a letter representing the manufacturer serial number to facilitate the traceability in this text.

Table 4.1: Insulation Test Results After Fault #1

Phase ↓	Test ↓	Bridge→	AFE1	AFE2	MB1	MB2
		Module→	A	D	G ^{IV}	J
		Device ^{II} ↓	Result↓	Result↓	Result↓	Result↓ V _r ^{III} ↓
U	a	1	6.49MΩ	6.50MΩ	6.50MΩ	350KΩ 563V
		2	6.49MΩ	6.50MΩ	6.49MΩ	510KΩ 819V
		3	6.49MΩ	6.50MΩ	6.50MΩ	1.041MΩ 1654V
		4	6.49MΩ	6.50MΩ	6.49MΩ	312KΩ 501V
		5	6.50MΩ	6.49MΩ	6.50MΩ	6.51MΩ
		6	6.50MΩ	6.49MΩ	6.50MΩ	6.5MΩ
	b	All to Hsk	112.7GΩ	104.0GΩ	166.6GΩ	175.3GΩ
V	a	1	6.50MΩ	6.5MΩ	6.50MΩ	159kΩ 256v
		2	6.49MΩ	6.5MΩ	6.50MΩ	392kΩ 634v
		3	6.49MΩ	6.5MΩ	6.49MΩ	240kΩ 393v
		4	6.50MΩ	6.49MΩ	6.49MΩ	124kΩ 193v
		5	6.50MΩ	6.50MΩ	6.50MΩ	6.51MΩ
		6	6.49MΩ	6.51MΩ	6.50MΩ	6.50MΩ
	b	All to Hsk	97.1GΩ	173.1GΩ	174.7GΩ	175.3GΩ
W	a	1	Burst	< 10KΩ	~0V	6.49MΩ Broken Frame
		2	Burst	6.50MΩ	6.50MΩ	Broken Frame
		3	Burst	6.49MΩ	6.50MΩ	Broken Frame
		4	Burst	6.50MΩ	6.50MΩ	Broken Frame
		5	Burst	6.50MΩ	6.49MΩ	Not Measured
		6	Burst	6.50MΩ	6.50MΩ	Not Measured
	b	All to Hsk	NA	135.6GΩ	106.1GΩ	NA

Legend

Burst
Considered Bad
IGBTs Visibly Broken
Specific Problem
Considered Good

The following notes are marked in the Table 4.1:

- I. Test “a” is the C to E 5kVdc Insulation Tester and test “b” is the HV circuit insulation to the heatsink.
- II. Device number as per Figure 3.4.

- III. V_r is the maximum voltage reached by the Insulation Tester when trying to perform the 5kVdc test, i.e, the leakage current was higher than the Insulation Tester device capacity and the voltage stopped to rise.
- IV. Phase module G was considered bad not because of the results from test a, but due to lower values of V_F on the FWD when measuring with the multimeter.

Test results of new units and the IGBT manufacturer data presented in Chapter 7, establish that the expected equivalent resistance for one IGBT frame with the three internal IGBTs in parallel is around 2 G Ω , when 5 kVdc is applied. Notwithstanding, the desaturation protection circuit in the gate driver has an equivalent C to E resistance of a few M Ω , the circuit is shown in Figure 4.8. Because of that, the test was only able to spot highly damaged devices. Degraded devices that would be still able to sustain the applied voltage but with deviation in the expected leakage current would not be evidenced due to the parallel smaller resistance of the gate driver.

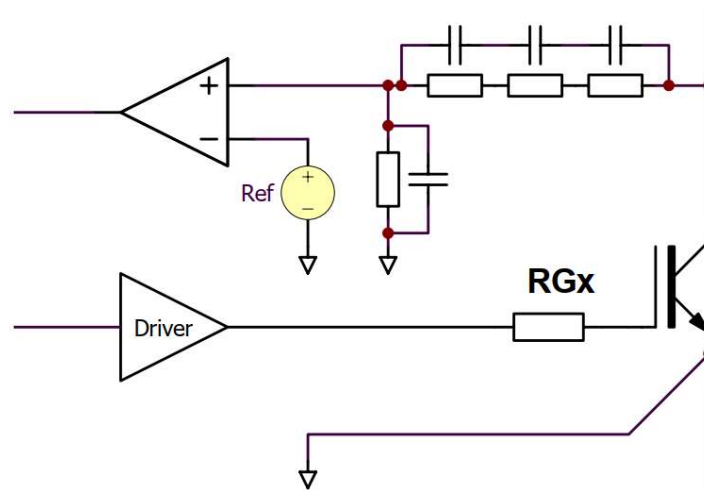


Figure 4.8: Gate Driver V_{CE} Desaturation Monitoring [45]

Chapter 5 shows that even after performing investigation tests that were more detailed than the standard IGBT evaluation in-circuit tests, it is very likely that a deteriorated device not spotted after this fault, was reused in the converter to restore operation, and ended up leading to a second fault after about a month. The details of the converter configuration to restore the operation and prior to Fault #2 are listed in Section 4.3.

4.3. Converter Configuration to Resume Operation

Phase module I was replaced by a full new unit. The new module will be given the letter M for reference in this text. The other phase modules considered damaged C, G, J, K and L were sent back to the factory to be refurbished. They are given the number 2 from now on in this text to mark the change.

- Modules J2 and K2 were rebuilt with new units of IGBTs.
- Module L2 was rebuilt with reused IGBTs.
- Module G2 was built with reused IGBTs for Q3 and Q4, while the other positions received new units of IGBTs.

For those modules, before deciding to reuse the IGBTs, they were removed from the phase modules and tests separately with a Insulation Tester, 5kVdc, at ambient temperature, C against E+G, without the gate driver. Only devices that presented an insulation resistance around the value found in new units of the MBN750H65E2, i.e. ~ 2 G Ω , were approved to be reassembled.

However, influenced by the results shown in Table 4.1 , on the phase module C2 only the IGBT Q1 was changed by a new unit. The other devices of the module were kept in the same position and a separated insulation test was not conducted only the standard factory tests.

The converter was reinstated for full power operation with the reworked phase modules. The new positions of the phase modules is shown in Table 4.2.

Table 4.2: Reconfiguration to Return to Full Capacity Operation

AFE1	AFE2	MB1	MB2	
J2	E	G2	D	New
K2	B	H	M	Reworked using new or proven high insulated IGBTs
L2	A	C2	F	Reworked with reused IGBTs, not individually tested
				Reused phase module

The system was tested for overall insulation and up to full speed. The converter operated for 25 days in this configuration before experiencing the new fault explored in Chapter 5.

4.4. Conclusions

The first fault that anticipated the main event, focal point of this study, is discussed in this chapter. The fault started due to an issue in the input LCL'L filter assembly in the AFE side. Conclusions taken from the fault analysis and test results show that IGBTs placed in different phase modules were affected by the fault spread. The post-fault tests performed were more detailed than usual, the collector to emitter insulation test was performed as per [25] and [54]. However, due to the large difference between the IGBT collector to emitter expected resistance and the gate driver parallel resistance, the fact that the test was executed with the gate drivers connected to the IGBTs could have masked degraded devices that ended up being reused and led to the second fault detailed in the next chapter.

Chapter 5. Fault #2 – Main Fault – Reuse of Degraded IGBT

The second fault and the one of most interest in this study is analyzed in this chapter. The impacts of this fault are investigated with the support of initial site test results that presented signs of degradation in some IGBTs. The most likely sequence of events that and IGBTs states prior and right after the fault are listed and the fault is simulated. The results are compared with the measurements for validation. The simulation allows the estimation of the overstress on the individual power semiconductor components inside the phase modules where no measurement was available unless for the V_{CE} voltage monitoring and protection of the gate driver. Two main phenomena, related to the motor back emf effect and the converter stray inductances, that would impact the short circuit path stressing components in other phase modules are identified and explained. Further off-circuit individual laboratory tests in brand new IGBT units submitted only to this second fault are shown in Chapter 7.

5.1. Simulated Model, Parameters and Assumptions

The study of this fault and the affected devices is developed from the site actual recordings and a simulation developed in PLECS with the circuit of Figure 3.6, the parameters of the grid, transformer, converter and motor of Table 3.2 and following the conventions in Table 3.3. The simulated model replicates the fault and provides estimation on the internal variables that are not directly measured in the site records. Figure 5.1 shows an overview of the simulated circuit. The dead time of $20\ \mu\text{s}$ was applied to the firing commands.

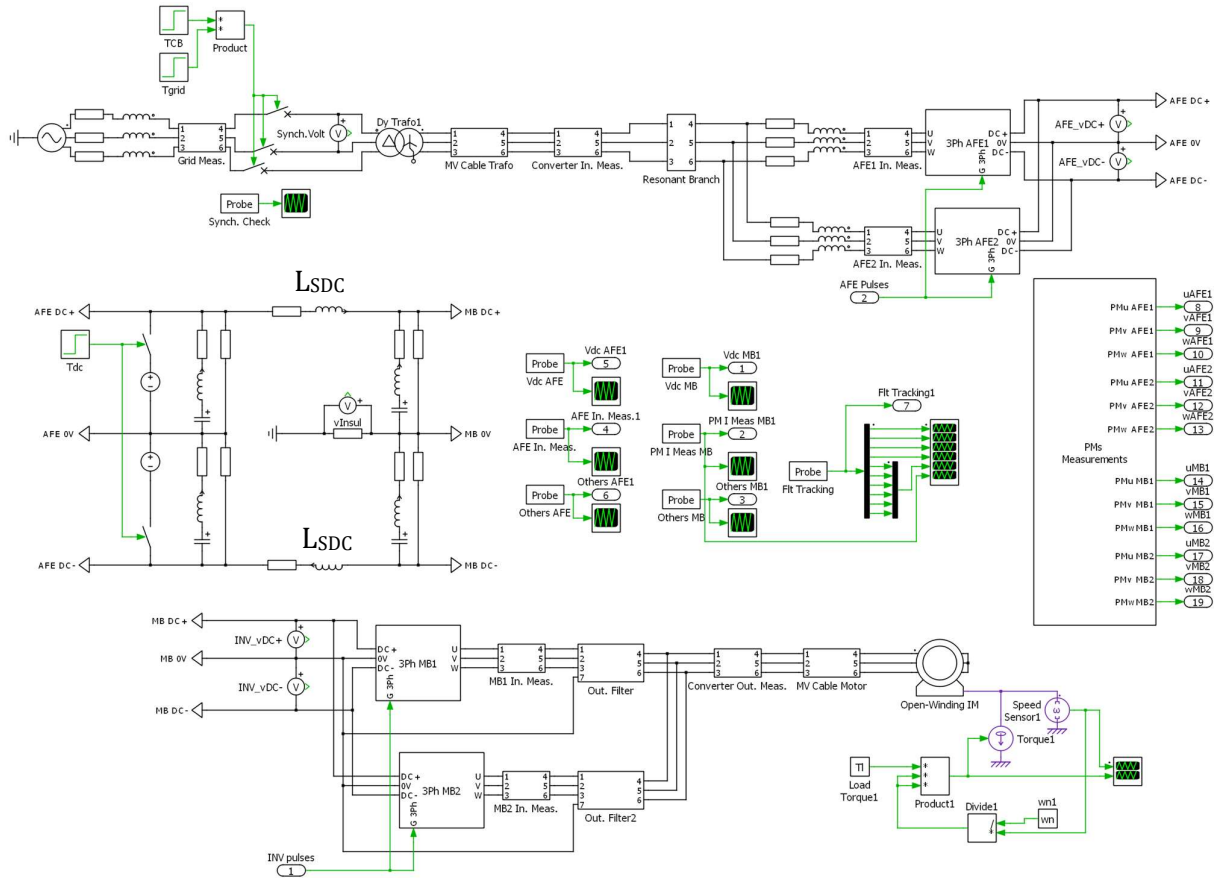


Figure 5.1: Simulated Overall Circuit

The fault will be only limited by the loop stray impedance of the DC link capacitor and in the connection to the phase module. Figure 5.2 shows the simulated phase module circuit and the connection stray inductances.

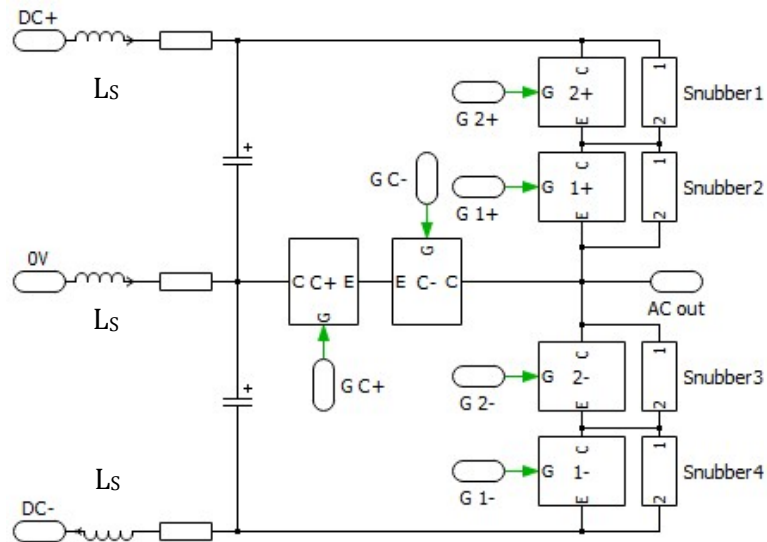


Figure 5.2: Simulated Phase Module Circuit

The following assumptions apply:

- 1) The devices are considered as always in the saturation region. The IGBT ON-state resistances is estimated from the slope in the static $I_C \times V_{CE}$ curve, Figure 3.10, when conducting with a 15 V V_{ge} , plus a forward offset voltage when the current is null. The same is applied to the FWD using the $I_f \times V_f$ curve. The curves are taken from [30]. Figure 5.3 present a close look into the IGBT model and parameters.

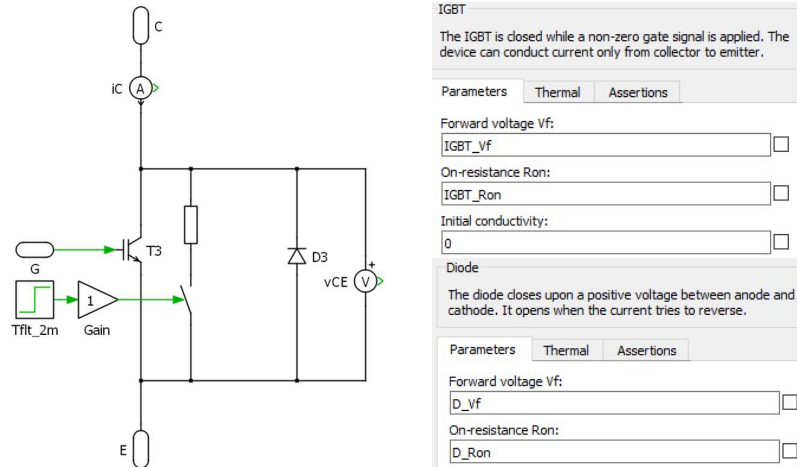


Figure 5.3: IGBT Simulated Model

- 2) The short circuit is simulated by a parallel switch in series with a SC resistance that bypasses the power semiconductor.
- 3) The DC link capacitors are modeled using the datasheet. The series stray inductance is 90 nH and the ESR (Equivalent Series Resistance) is calculated as:

$$ESR = \frac{\tan(\alpha)}{\omega C} \quad (5.1)$$

In which $\tan(\alpha)$ is the tangent of the loss angle, also called Loss Tangent, or Dissipation Factor. The manufacturer indicates $<30e^{-4}$ at 100 Hz. The final estimated value for 4 parallel capacitors on each half DC link was 1 mΩ [55].

- 4) The Capacitors to Phase Modules stray inductances is estimated in 1.2 μH, calculated from the switching tests under normal conditions.

By looking at the overvoltage during the turn-off process, the current that is being commutated and the switching OFF time, $L_{loop} = \Delta V / (di/dt)$.

This value is mostly influenced by the connection stray inductances between the DC link and the phase modules, L_s in Figure 5.2. The inductances of DC link capacitors, snubber capacitors and the IGBT internal inductances are also part

of the circuit, but its influence is less important since they are much lower than L_S . Specially for the converter under study, due to its construction and component arrangements, high voltage cables were used instead of laminated busbars in the connection of each phase module to the DC link poles and 0 V.

- 5) The IGBTs internal stray inductances, as per Figure 3.3, and the snubber inductances are neglected since the value is much lower than the connection inductances.
- 6) The AFE to MB DC link connection is also done by cables. This inductance, L_{SDC} in Figure 5.1, is estimated from the cable electrical parameters, length, and diameter as $4.2 \mu\text{H}$. When there is a full DC link short circuit the energy flows from one side of the converter to the other through this inductance.

5.2. Fault #2 Analysis

The recorded plots and the waveforms replicated in the simulation are shown in Figure 5.4 for the MB side. The plot shows the six output currents, the dc link voltages, the speed measurement from the encoder and the boolean signals to mark the firing commands OFF and when the main-circuit breaker (CB) opens. The firing pulses were interrupted by the DC link negative overvoltage protection.

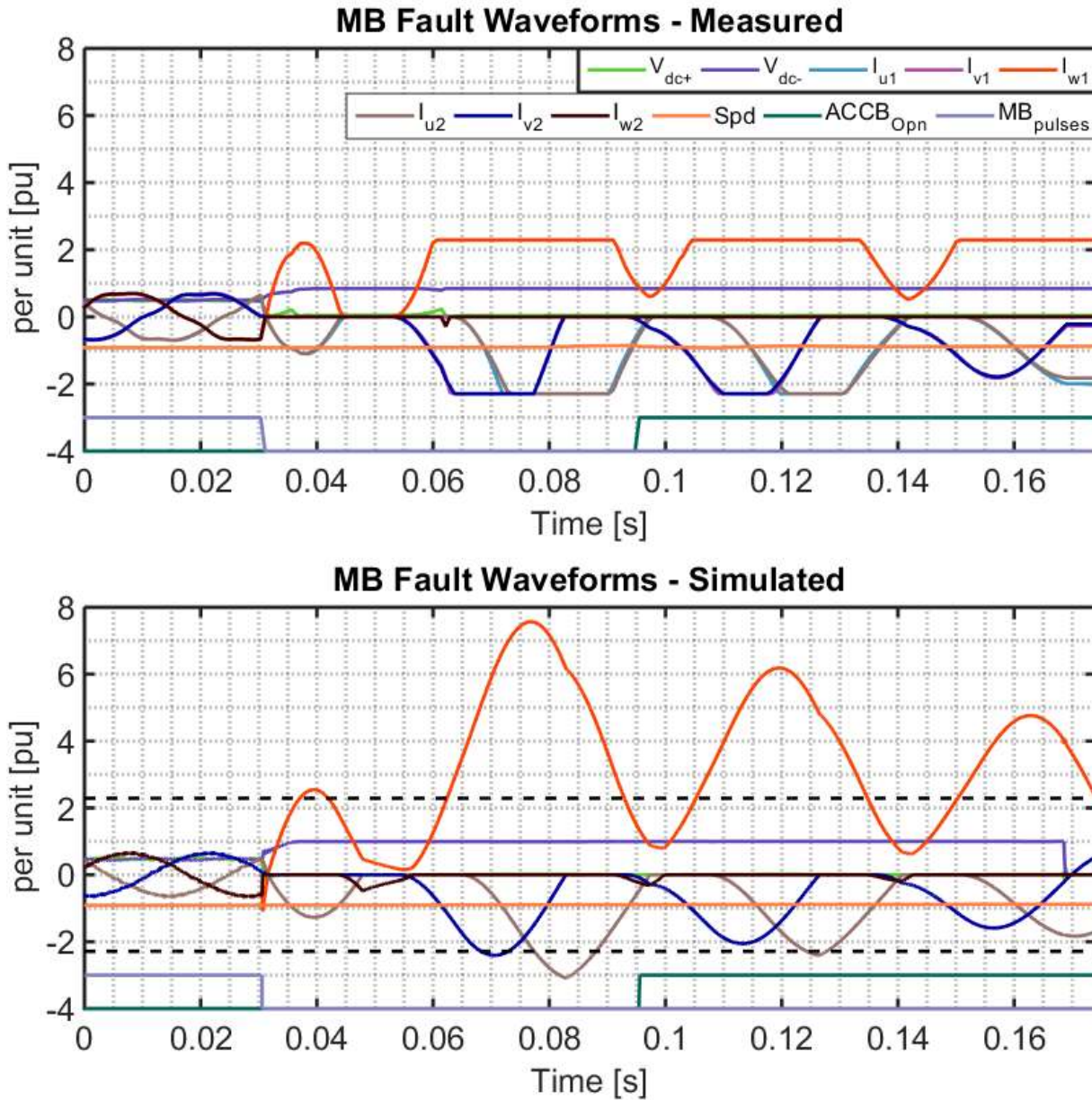


Figure 5.4: MB Fault Plot (Measured and Simulated Data)

The following notes apply to Figure 5.4:

- I. The recorded readings become flat whenever they reach the DSP board end of scale. Dashed black horizontal lines representing the reading limits of the measurements for reference.
- II. The 0V to ground insulation voltage measurement in the MB side was suppressed for better visualization.
- III. The modulated output voltage was yet to be tuned and it's possible to notice that the motor was over fluxed at this operation point, this is reflected in the shape of the peak in the output current waveforms but had no direct relation to the fault.

Right before the fault, the motor was running at 0.92 p.u. speed to the negative direction. Phase W of MB1 had a negative current, which means that the current was flowing from the motor into the drive. The reference voltage was also negative since the motor power factor is 0.85 at full load. Therefore, the possible states or transitions of the phase W IGBTs at the trip detection are the ones shown in Figure 5.5.

Phase module C2, now placed in phase W of MB1 (vide Table 4.2), was the most damaged one and probably where the fault started. It had IGBTs with broken frames and the device Q1 completely burst. This is the same module where only one device was changed and the tests were performed only with the GD installed, see Section 4.3.

At the trip detection, the vertical positive IGBTs were not conducting or switching, but its blocking voltage can vary from $V_{DC}/2$ to full V_{DC} . Q1 was a new unit while Q2 was reused after the previous fault. Besides, the Collector to Emitter insulation of Q2 was tested only with the gate driver connected and this could have masked some degradation in this device insulation after the previous fault.

Figure 5.6 illustrates the most probable fault sequence, the voltage and the currents inside the most damaged phase module, W of MB1, right before and right after the fault detection, up to the point in which the DC+ to 0V short circuit is initiated and maintained even after all IGBTs are sent to OFF-state.

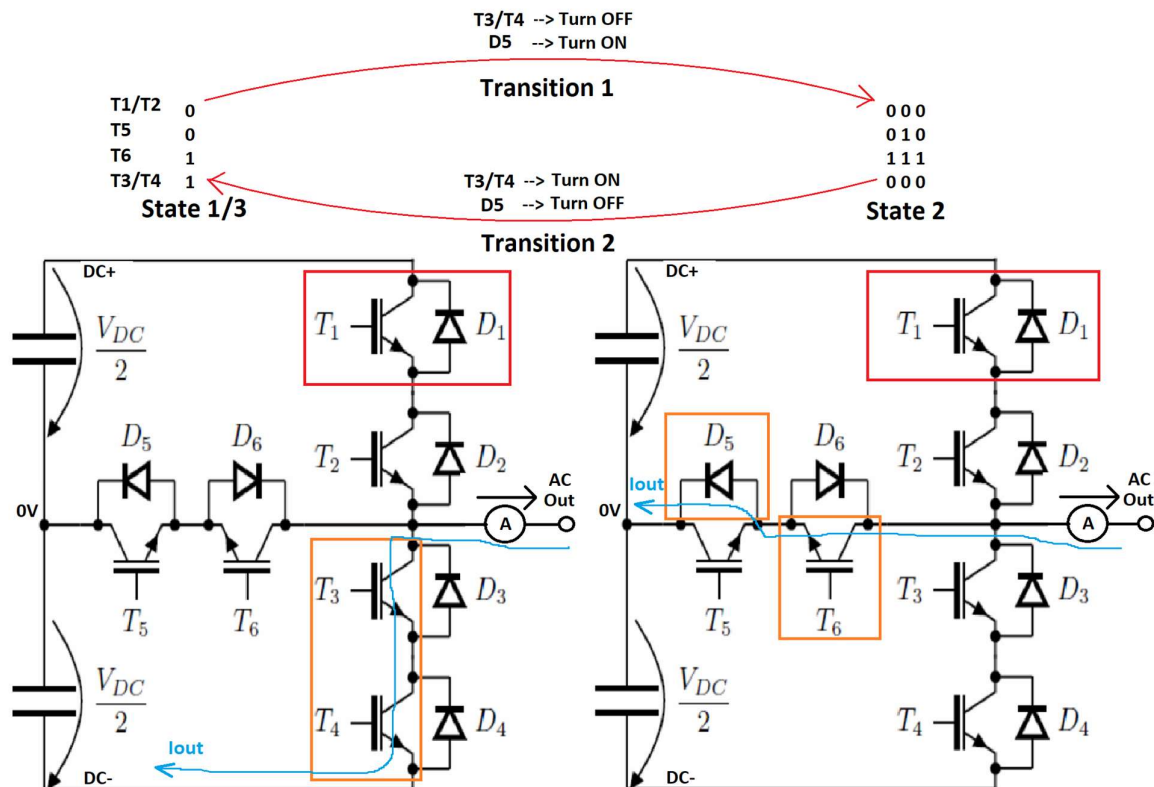


Figure 5.5: Possible States or Transitions at the Trip Moment

5.2.1. Fault #2 Sequence:

The stages of the most probable fault sequence are illustrated in Figure 5.6 and further explained next. Again, the 4-digit state representation is used according to Figure 3.4. The voltages V_{gE} , V_{CE} and the current I_C are represented as per [56].

- 1) 1100 & 0100 (DT) → With the current coming from the motor to the DC link (negative in this convention) and a negative reference voltage, state 1 is one of the possible states of the devices in the phase module W of MB1. The FWDs D1 & D2 conduct the current, even during the DT (Dead Time), until T6 is ON.
- 2) 0110 & 0010 (DT) → 0V is applied at the output and the current switches to T6 and D5.
1 & 2 are possible states or transitions prior to the fault.
- 3) 0011 (Q2 fail in SC) → When T3 and T4 turn-on, the blocking voltage is the maximum under the devices 1 and 2. Q2 fails in short circuit, due to its probable previous degradation. The collector to emitter short circuit would pass undetected at this point.
- 4) 0011 (Q1 fail in SC) → Q1 had to sustain the full DC link voltage at this blocking state. Q1 could have failed right after Q2, as illustrated on Figure 5.6, or Q1 could have still sustained the full DC link for some cycles, but the combination of a blocking voltage almost at the edge of the RBSOA, the higher than designed switching losses and junction temperature would have led to the fault.
- 5) 0011 (Full DC link SC) → Q1 & Q2 in short circuit while T3 and T4 are ON configures full DC link short circuit. In this condition the current will rise fast on those 4 devices and the gate drivers are able to detect the high V_{CE} voltage on T3 and T4 while conducting, turning the feedback light OFF. The DSP controller takes than a few nano seconds to enter the hierarchical turn-off process trying to reach OFF-state at the short circuit current level.
- 6) 0010 (Hierarchical Turn-OFF) → As presented by Table 3.4 under fault conditions and high current observed by the FPGA, the OFF-state is achieved only after the dead time. With Q1 and Q2 in short circuit the half DC link short circuit is now put in place and the current keeps rising with a lower slope since less energy is involved.
- 7) 0000 (Q6 fail in short circuit) → T6 could have failed when conducting the already established short circuit current during the DT. Most likely though, T6 tries to turn-off

after the DT, the current is very high, and it is unlikely that T6 would be able to interrupt alone the energy from flow without being damaged.

- 8) Half DC Link Short Circuit → With those three IGBTs damaged in short circuit the positive half DC link capacitors are shorted constantly independently of the devices being commanded to OFF-state. D5 will conduct the short circuit current until it is also damaged.

From this point on, the short circuit will be supplied by the source until the input circuit breaker opens in about 60 ms.

This situation configures one of the risks associated with the use of IGBTs in series. The IGBTs are expected to have a very similar switching behavior, but if Q2 was degraded, the deviations between the two IGBTs was affected, and the devices were overstressed. Furthermore, the gate driver protections as described wouldn't be able to detect Q2 in short circuit if Q1 would still switch the full voltage for a certain time. Q1 would accumulate all the losses expected for that vertical arm, besides sustaining the full DC link voltage when Q3 and Q4 are ON.

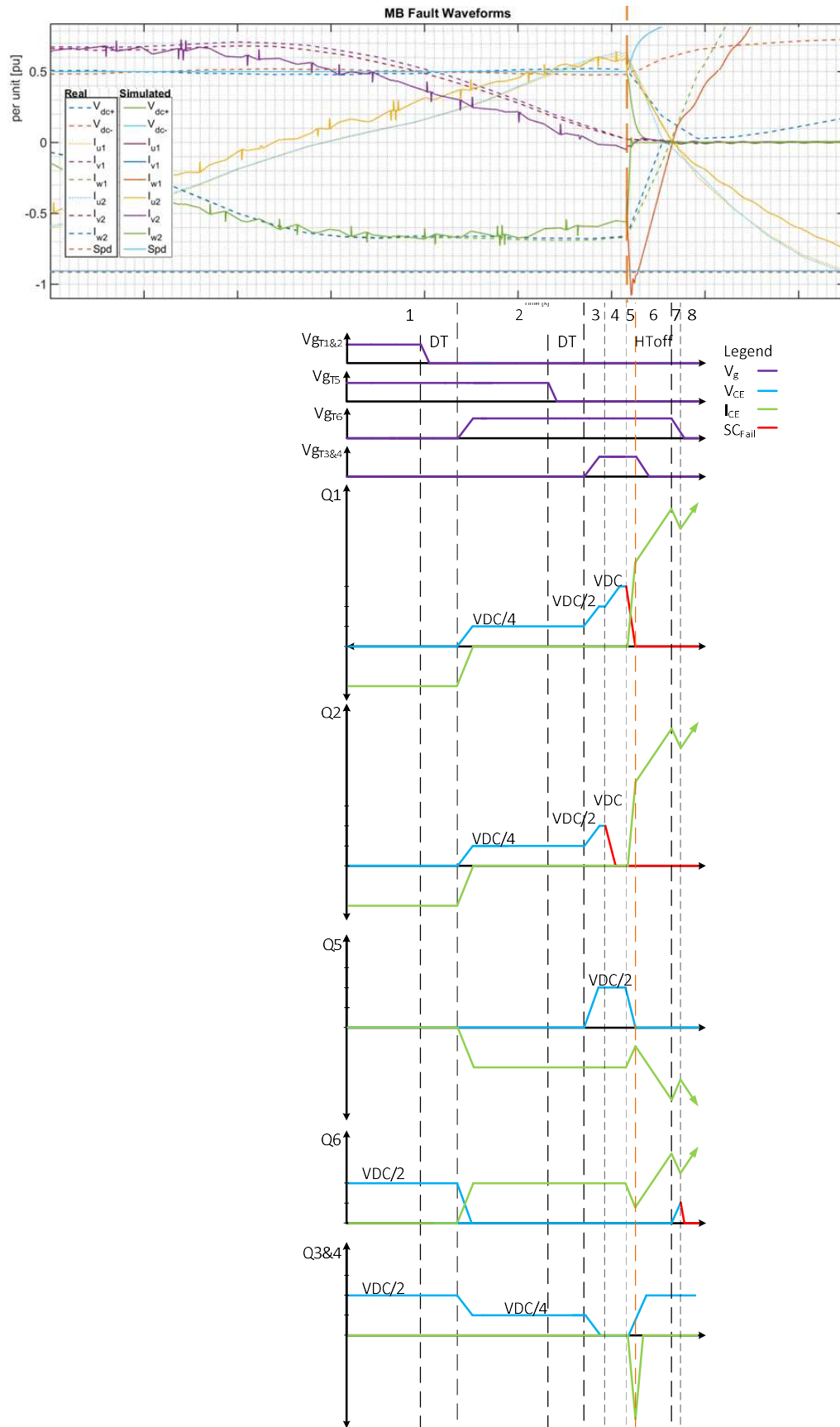


Figure 5.6: Fault Sequence inside Phase Module W of MB1

It should be noted that Figure 5.6 is only a representation of the states and transitions, the actual overvoltages and overcurrents associated to the stray inductances and the switching process of the power semiconductor devices are not shown.

5.2.2. Back EMF effect

The inertia keeps the motor running for some time after the firing pulses are removed. The residual magnetism in the rotor core maintains the back EMF voltage [57]. The oscillations of high current measured by the amperemeters positioned at the output of each phase module show that not only an inner loop is formed by the DC+ short circuit through Q1, Q2, Q6 and D5, but also an external current loop is generated, due to the back EMF, with the current flowing through the motor inductances and the FWDs D1 and D2 of the other phases.

Due to the short circuit on DC+, the motor behaves as a generator with the terminals short-circuited, feeding the fault, and tending to charge the positive capacitors. I_{sc2} will decay with time due to the winding resistance. Figure 5.7 shows the representation of this current path when the back EMF of the phase V is higher than the phase W and the current circulates through phases U of the two MBs and through phase W of MB1 [58] [59].

I_{sc1} is the inner loop current due to the positive DC link short circuit and I_{sc2} is the outer loop that passes through the motor and depends on the back EMF. The current is positive in the MB1 PM W, passing through E_w in the motor and coming back through E_u , since E_v is bigger at this moment. This corresponds to the high current semi cycle seen in Figure 5.4, right after the positive DC link short circuit.

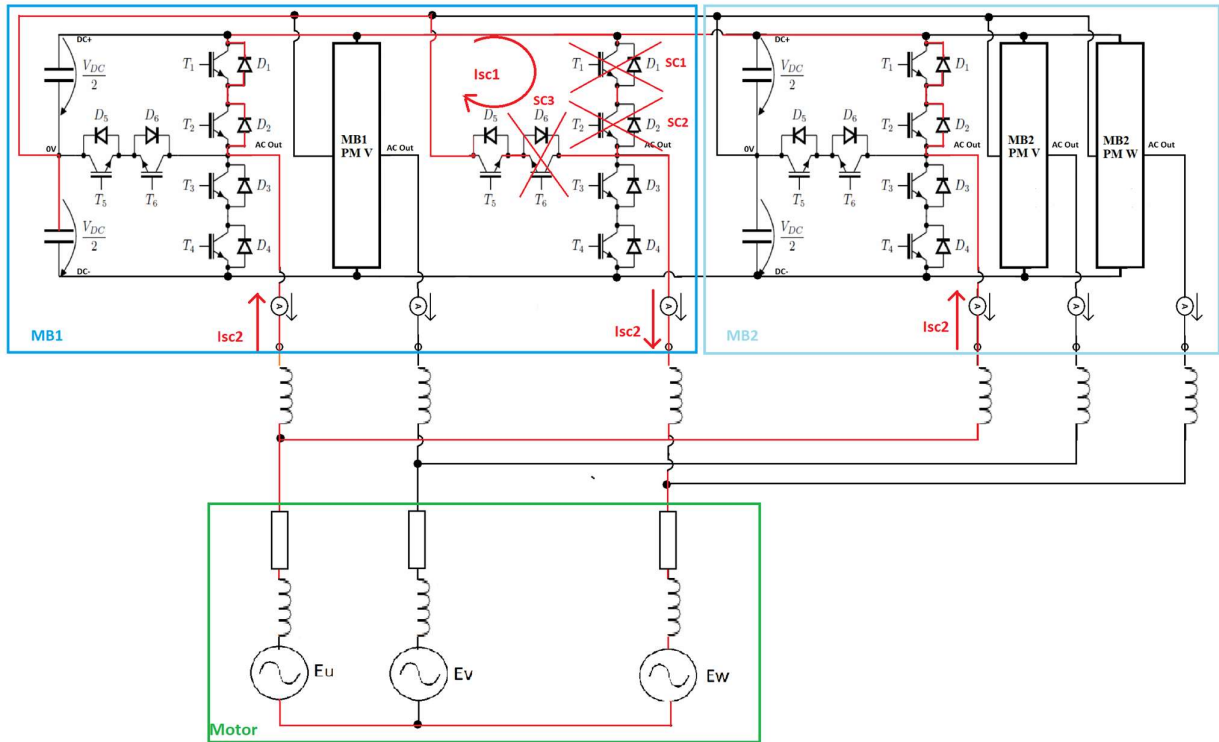


Figure 5.7: Back EMF effect and current circulation through motor ($E_v > E_w$)

There is no circulation path for the current in the MB2 PM W, because at this point T1 and T2 are healthy. In MB1 and MB2 PM U the current loop closes through the FWDs D1 and D2. This current loop stays on and oscillates between phase W and the other two phases U and V from MB1 and MB2 even after the main-circuit breaker is open, since it depends on the motor rotation due to the load inertia [58].

The voltage on the AC output will increase above the half DC link on the negative side according to the stray inductance to the 0V and the slope of the short circuit current passing across it. Since the fault current di/dt is very high, it is likely that Q3 and Q4 fail due to overvoltage. Besides, those IGBTs were probably already degraded by the high current conduction before the fault detection at stage 5 of Figure 5.6.

Figure 5.8 shows the values found on the simulation for the collector current right after the trip during the back EMF effect. The simulation confirms the overstressed in the FWDs D1 and D2 of MB1 and MB2.

Positive values mean current passing through the IGBTs and negative values are the current passing through the FWDs, unless for the Phase Module MB1 W in which the short circuit was simulated by a parallel switch. Note also that the plot was slightly offset in the vertical axes to allow the visualization of the waveforms in the devices that have close current values.

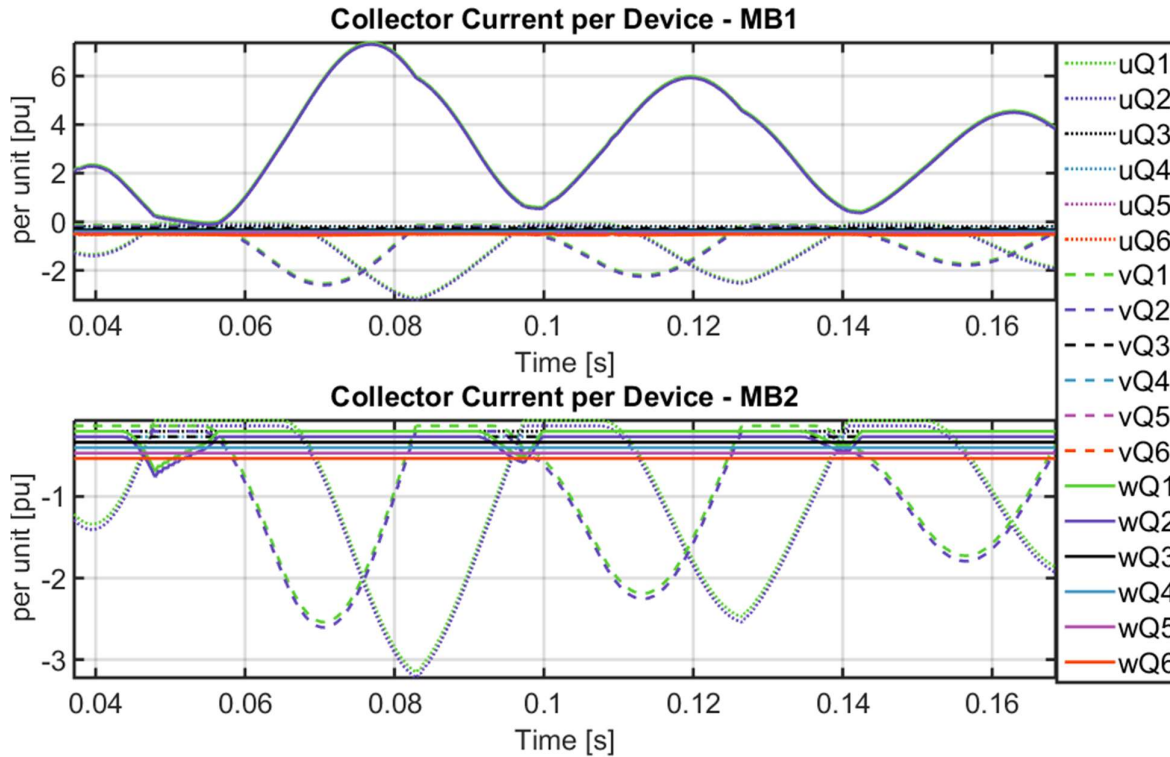


Figure 5.8: Collector Current per Device (Simulated)

5.2.3. Effect of the Stray Inductances

The stray inductances in the phase modules connection to the DC link and in the DC connection from the AFE to the MB will also create other alternative short circuit current passing through the FWDs, as illustrated in Figure 5.9 for a full DC link short circuit in the phase module W. Those currents are generated when the DC link capacitors are short circuited, and the energy is discharged fast in the stray inductances leading to LC oscillation of short duration.

The FWDs will normally block the current, but the LC oscillation can make the voltage across the capacitors to invert polarity and force the current circulation through the diodes. For the half DC link short circuit, the devices C+ and C- block the short circuit current flow in the other phase modules since they are in anti-series connection. However, the phenomenon is expressive after a full DC link short circuit with the current flowing through the vertical FWDs and affecting even the devices in the AFE side [60].

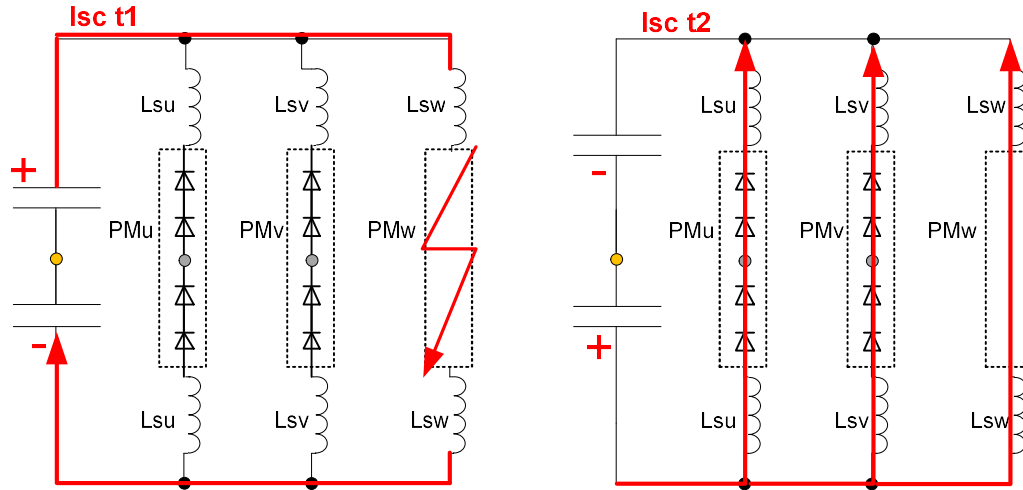


Figure 5.9: Full DC link Short Circuit Current and Currents due to the Stray Inductances

Figure 5.4 shows that the DC+ to 0V short circuit evolves to a DC+ to DC- short circuit when the devices Q3 and Q4 fail from sustaining the full DC link voltage for a long time. Due to a damage in the DSP controller board, the readings on the MB side froze at around 0.165 s, yet the DC link short circuit can be confirmed by the plot on the AFE side.

Figure 5.10 brings the records of the AFE side and the simulated results. The firing pulses are turned OFF on the AFE side right after the MB DSP board detects the fault due to the intertrip fault loop mentioned in Section 0. The main breaker opens about 60 ms later, the converter input line voltage measurements don't go directly to zero but rather have a delay to die out due to the transformer saturation. The full DC link short circuit is registered at the end of the plot.

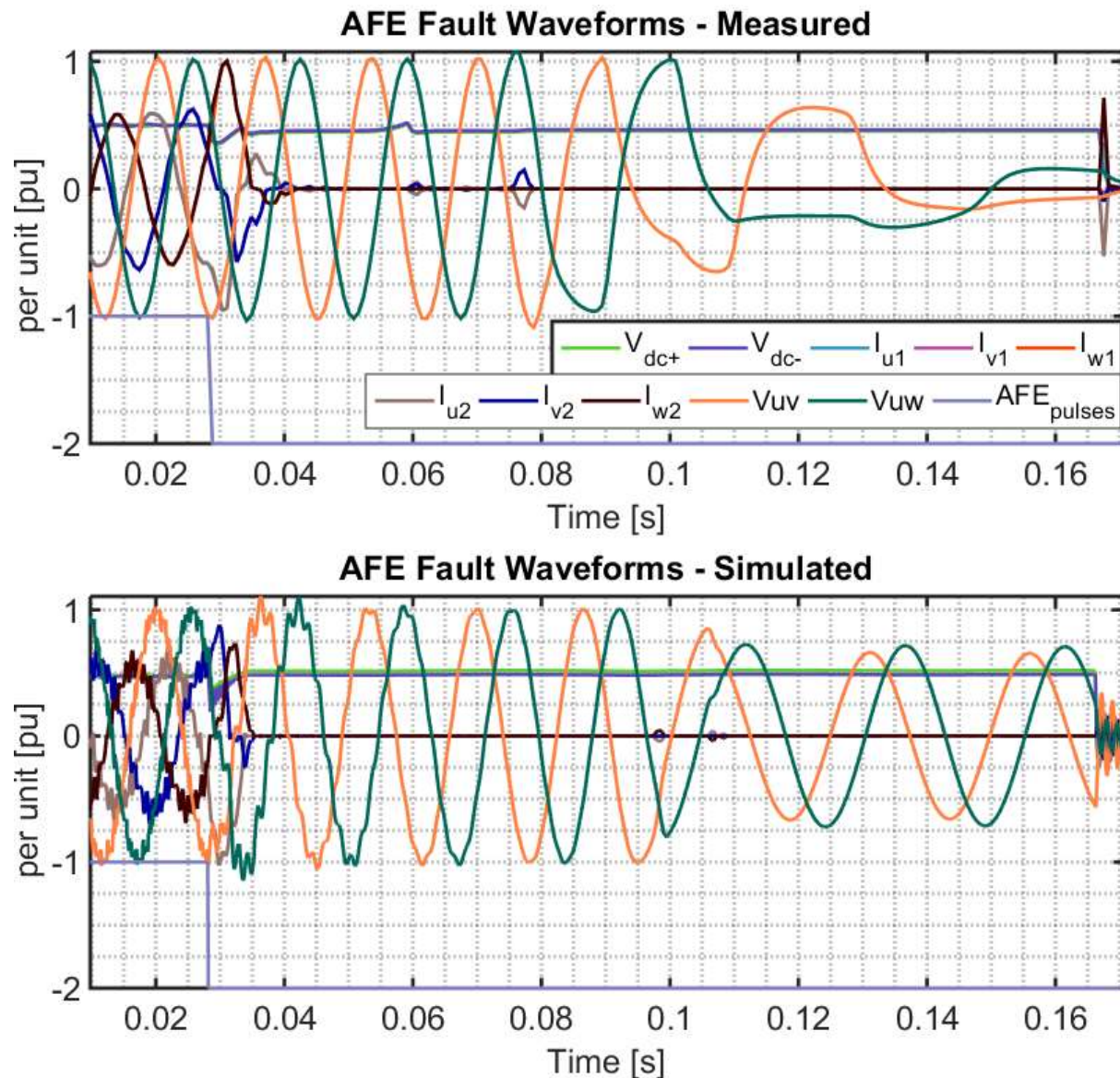


Figure 5.10: AFE Fault Plot (Measured and Simulated Data)

Figure 5.11 presents a closer look in the simulated DC link voltages and the collector currents the devices on the AFE side. Although diodes have a substantial surge rating, all the vertical FWDs are overstressed with a high overcurrent that cannot be interrupted by a protection action. The current will depend only on the DC capacitance, the loop stray inductances and the small resistances in the circuit that will dissipate the energy.

Again, the plot was slightly offset in the vertical axes to allow the visualization of the waveforms in the devices that have close current values.

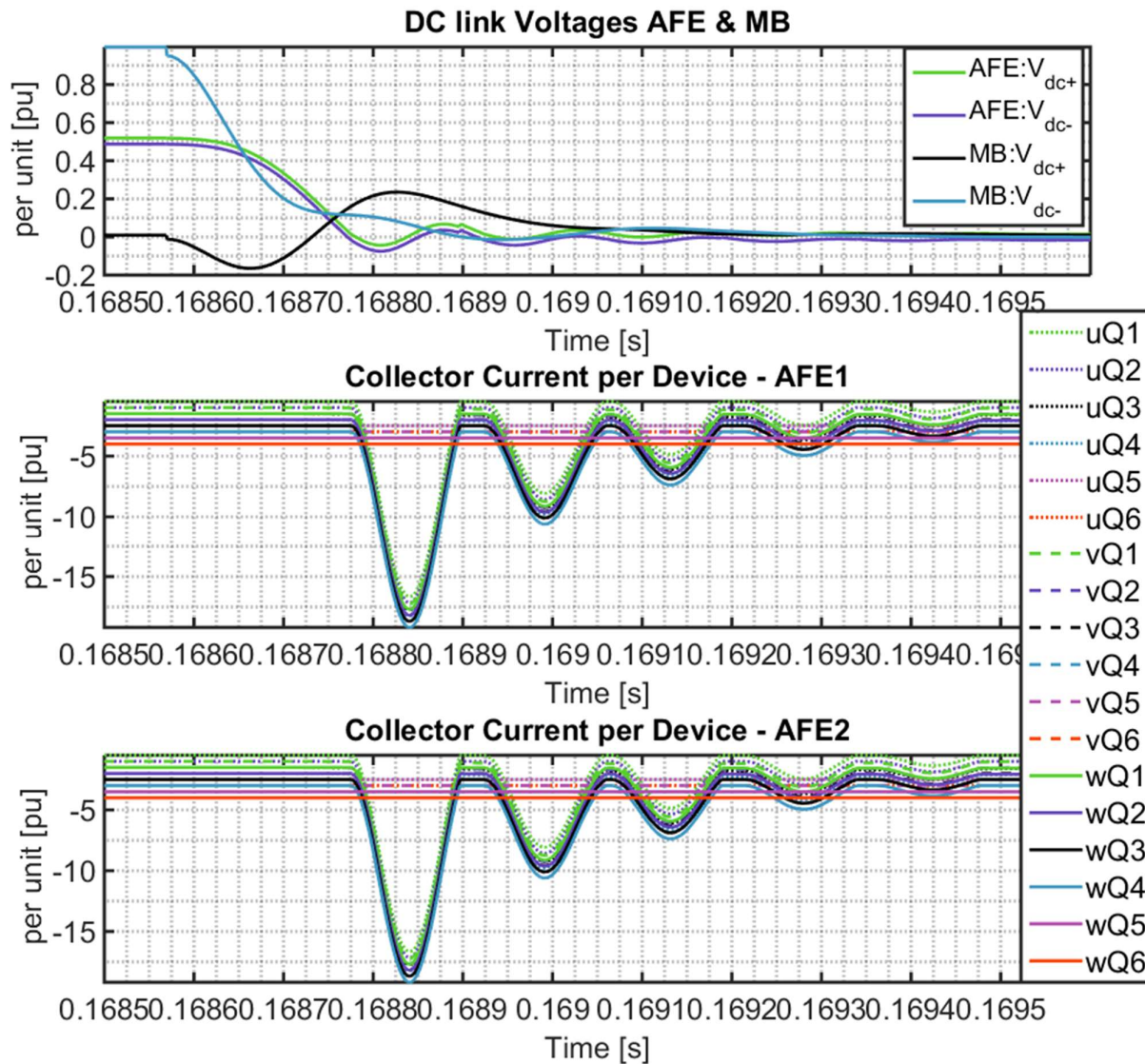


Figure 5.11: Collector Current per Devices in the AFE side and DC link Voltages during Full DC Link Short Circuit (Simulated)

Figure 5.12 shows the surge rating for the FWD of the MBN750H65E2 IGBT at 125 °C for half sinusoidal current pulses applied with duration shown in the x axis. The I^2t and the IFSM obtained before a failed condition was reached in the device are plotted. According to the IEC 60747-2 [61], the I^2t is the “integral of the surge forward current over the duration if the current surge” and the IFSM is the:

“forward current pulse of short time duration and specified waveshape, whose application causes or would cause the maximum rated junction temperature to be exceeded, but which is assumed to occur rarely and with limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions (for example a fault)” [61].

The results shown don't have any margin to the failure level, for the real application the manufacturer recommends 20 % margin in the values exhibited [62]. It is possible to notice that pulses shorter than 3 ms were not tested and therefore the devices characteristics are not guaranteed.

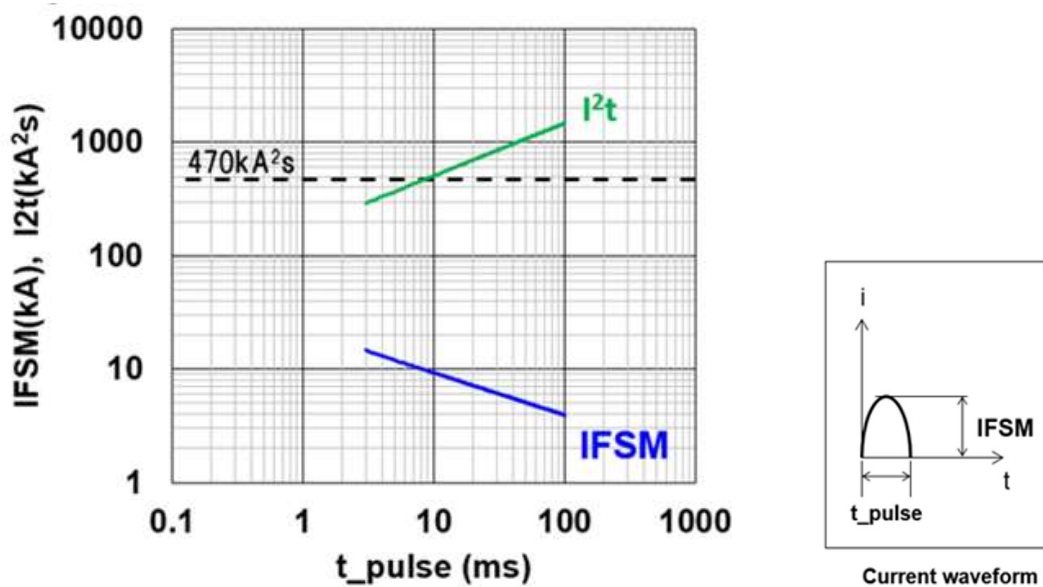


Figure 5.12: I^2t and IFSM before failed condition in the FWD [62]

5.3. Post Fault #2 Tests

The after-fault site tests described in Section 4.2 were once again performed at ambient temperature, yet this time the C-E 5 kVdc insulation tests was done for I_{CES} with the gate driver disconnected and keeping the Emitter and Gate short circuited, see Section 6.3.1. The Collector and Emitter busbars were kept, so all three devices inside the same flat-pack frame, see Figure 3.1, were tested at the same time. The test results are summarized in Table 5.1.

As previously stated, the insulation resistance of the flat-pack devices when measured alone is much higher than the one measured in the previous fault with the gate driver connected. The expected value for a brand new flat-pack unit of this model is around 2 GΩ. However, according to [63] and the plots presented in Section 7.4, the equivalent resistance of around 1 GΩ could still be normal, since the manufacturer mean value for the leakage current found was $3 * 1.65 \mu A$ for the full flat-pack power module and 5 kVdc of voltage applied.

Device Q4 of L2 in the AFE1 is the one that presented the most interesting result, since it was still able to sustain 5 kVdc voltage and had a high equivalent insulation resistance, but much lower than the value expected for new units. This result confirms that the C-E insulation measurement performed with the gate driver installed is only able spot devices with drastic internal damage. The real condition of degraded devices like Q4 of L2, could be masked by the 6.5 MΩ parallel resistance of the gate driver and would appear in good conditions and that it could be reused. That is likely what happened with device Q2 of phase module C, its reuse after Fault#1 led to this fault, as detailed in Figure 5.6.

Table 5.1: Insulation Test Results after Fault #2

Phase ↓	Test ^I ↓	Bridge→	AFE1	AFE2	MB1	MB2
		Module→	J2	E	G2	D
		Device ^{II} ↓	Result↓	Result↓	Result↓	Result↓ Vr ^{III} ↓
U	a	1	0.951GΩ	2.029GΩ	0.772GΩ	1.738GΩ
		2	0.974GΩ	1.543GΩ	1.245GΩ	2.074GΩ
		3	0.720GΩ	1.680GΩ	1.790GΩ	1.917GΩ
		4	0.811GΩ	1.791GΩ	2.014GΩ	1.577GΩ
		5	0.951GΩ	2.390GΩ	0.962GΩ	2.068GΩ
		6	0.741GΩ	2.502GΩ	0.987GΩ	2.267GΩ
	b	All to Hsk	>150GΩ	~200GΩ	~200GΩ	180GΩ
V	a	1	1.298GΩ	2.030GΩ	2.209GΩ	1.456GΩ
		2	1.384GΩ	2.155GΩ	2.670GΩ	1.267GΩ
		3	1.272GΩ	2.368GΩ	1.967GΩ	1.664GΩ
		4	0.831GΩ	2.142GΩ	1.876GΩ	1.452GΩ
		5	1.495GΩ	2.088GΩ	2.328GΩ	1.479GΩ
		6	1.367GΩ	2.205GΩ	1.930GΩ	1.433GΩ
	b	All to Hsk	~200GΩ	~270GΩ	250GΩ	350GΩ
W	a	1	1.478MΩ 2332V	1.837GΩ	Burst	231kΩ 372V
		2	2.080GΩ	1.865GΩ	Burst	2.255MΩ 3029V
		3	2.042GΩ	1.218GΩ	6.41GΩ 5089V	<10kΩ 8V
		4	72.3MΩ 5089V	1.755GΩ	Burst	454kΩ 735V
		5	2.040GΩ	1.748GΩ	<10kΩ 13.4V	1.682GΩ
		6	1.901GΩ	2.243GΩ	6.6kΩ 105V	2.651GΩ
	b	All to Hsk	>150GΩ	96.7GΩ	NA	NA

Legend

Burst
Considered Bad
Considered Good
Special condition

Again, the following notes apply:

- I. Test “a” is the C to E 5 kVdc Insulation Tester and test “b” is the HV circuit insulation to the heatsink.
- II. Device number as per Figure 3.4.
- III. Vr is the maximum voltage reached by the Insulation Tester when trying to perform the 5 kVdc test, i.e, the leakage current was higher than the Insulation Tester device capacity and the voltage stopped to rise.

- IV. Device Q3 of C2 values probably mean that at some point two of the internal three parallel semiconductors inside the frame opened because of the destruction process and only one device is being measured.

The 4 semiconductors chosen for further investigation in laboratory are also highlighted with a dashed purple line in Table 5.1, the results are shown in Chapter 7.

5.4. Converter Configuration to Resume Operation

Phase modules with measured values below 1 G Ω were the ones initially considered bad, yet the final decision on site was to replace all the devices of all phase modules. The converter was then put back in operation and there was no other record of faults for at least 2 years after the final commissioning.

It is important to note that the devices junction temperature estimation was reevaluated and temperature tests with strategic insertion of thermal stickers were performed, stressing each remaining module to its maximum operation conditions. No unexpected higher temperatures on the surfaces and heatsink were found.

5.5. Conclusion

The analysis of the second fault, or main fault, is performed in this chapter. The simulation developed gave very similar results when compared to the site measurements and is used to provide data for the analysis of internal variables not directly measured in the real application, like the device's voltages and currents. It was verified that although the fault initiates inside one single phase module, the effects of the Back EMF and the converter stray inductances can create alternative short circuit current paths through the FWDs that will spread the fault impact to other phase modules.

It is shown that it was very likely that the device Q2 of phase module C2 probably degraded by the first fault and reused in the converter, was the one that failed first after a few days of operation. Since this device is placed in series with another one in the vertical arm of the NPP topology, it most likely led to the failure of the second device of the arm, resulting in a half DC link short circuit which evolved to a full DC link short circuit.

More detailed results of the leakage current tests executed after this fault attested the fault spread to components in the other phase modules of the same bridge in the MB side, its parallel bridge and even on the AFE side. While some devices were not even able to sustain the test voltage, device Q4 of phase module L2 in the AFE side could sustain the voltage but showed a large deviation in the equivalent collector to emitter result when compared to healthy units. This device, a more evidently damaged one and two possibly healthy ones were selected as samples for further laboratory tests presented in Chapter 7.

Chapter 6. IGBT Internal Structure and Degradation Indicators

This chapter explores the possible degradations in the flat-pack IGBTs internal structure to support the analysis of the fault impact in the device characteristics and consequently in its remaining lifetime expectancy. The potential failure modes and mechanisms involved in the device deterioration are presented. Failure precursor parameters that can be used to identify the degradation are discussed. Finally, examples of damage to the IGBT structure are shown. The concepts explored in this chapter were used as a basis for comparison and helped determining the offline tests that could highlight parameter shifts and indicate the IGBT degradation, as presented in Chapter 7.

6.1. Flat-pack IGBTs Internal Structure

It is important to know the internal structure of the flat-pack IGBT modules to be able to compare with unhealthy units and understand the impacts that can be caused by the overstress generated by a fault in the converter. The typical internal structure of a flat-pack IGBT for a single or multi-chip module is shown in Figure 6.1. Besides the semiconductor devices, IGBT or FWD, the other main elements are [64] [65] [66]:

- a. *Die-attach*: contacts the die to the substrate mechanically, electrically, and thermally. The usual solder joint material is the Silver Sodium Lead alloy, PbSnAg.
- b. *Wire-bondings*: perform the electrical contact on the device top-side. The technic is usually done with aluminum and uses ultrasonic energy over time at ambient temperature to create the bonding. It can also use gold at 150 °C in a process called thermosonic bonding.
- c. *Substrate*: usually ceramic substrates with copper layers on top and backside. It provides an efficient, electrically insulated and thermally conductive, heat extraction path.

- d. *Encapsulant*: protects the assemblies from external mechanical and environmental conditions. Silicones have been widely used.
- e. *Base plate*: mechanical support and heat spreading towards the heatsink.
- f. *Case*: thermoplastic external housing structure.

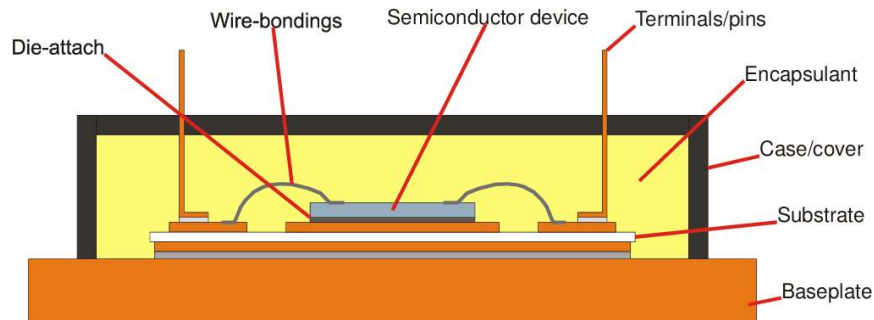


Figure 6.1 Typical Flat-pack Internal Structure [64]

As presented in Section 3.1.1, high power IGBTs are normally associated in parallel inside one flat-pack module. Figure 6.2 shows the placement of the dies and wire bonds for one module with three parallel IGBTs, A, B and C.

Due to its distribution, the junction temperature of the IGBT chips is never evenly shared among all dies, due to differences in the losses and heatsink surface temperatures. The converter design would frequently consider uniform junction temperature constrain for the module, although some of the chips can reach higher values. The extra thermal stress in those specific dies and wire bonds can reduce the device expected lifetime depending on the operation power cycles [67].

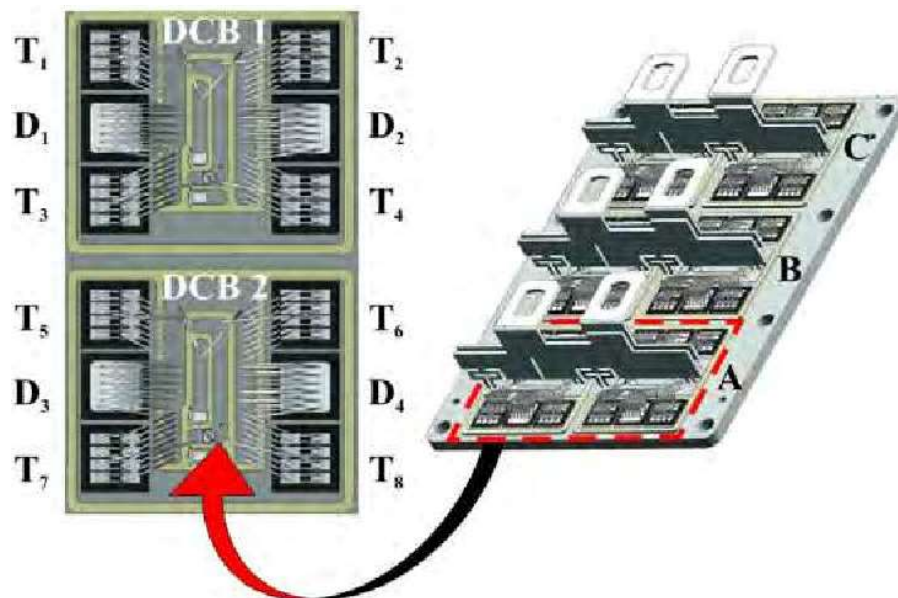


Figure 6.2 Multichip Flat-pack Module Internal View. [64]

6.2. FMMEA

The FMMEA (Failure Modes, Mechanisms, and Effects Analysis) gives the basis for the determination of the precursor parameters necessary for the post-fault evaluation of the IGBTs, as per proposed methodology shown in Figure 2.5. It helps to identify the critical failure mechanisms and its precursors, enabling the forecast of the device's remaining expected lifetime. [7]

Figure 6.3 brings the FMMEA of the IGBT with the main failure modes. Differently from the press pack IGBTs that can guarantee SCFM, failure modes in flat-pack devices can be of Short Circuit, Open Circuit or Parameter Drift type. [68]

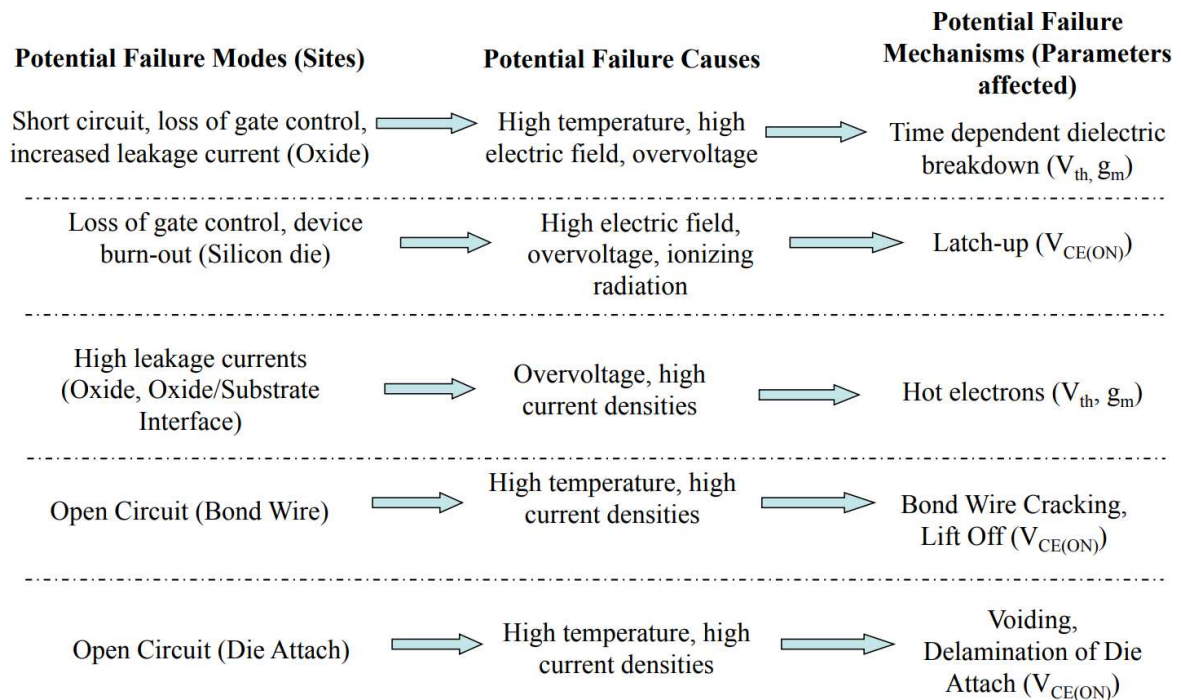


Figure 6.3 FMMEA of Flat-pack IGBTs [68]

The failure modes can also be divided into failures caused by overstress and wear-out failures. Overstress failure modes happen due to fast events of high energy such as gate or collector-emitter overvoltage, overcurrent, or burnout due to cosmic rays. These events may cause bond wire lift-off or rupture, latch-up, loss of blocking capability, rapid rise in junction temperature (thermal runaway) due to energy shocks (high-energy dissipation), and secondary breakdown in the inherent BJT structure. On the other hand, wear-out failures are usually associated to the deterioration of the

gate-oxide-layer characteristics. They show up as parameter drift and get worse over time until the complete loss of the device properties [69].

In the fault analysis performed in this work, some IGBTs presented evidence of overstress failure modes, like spread burnt areas and broken frames as result of energy expansion during the fault. However, the focus of the analysis is rather on the devices that experienced abnormal conditions subsequently to the initial fault. The overstress is not to the point in which the device would lose all its attributes, but rather a change on the original parameters as in an accelerated wear-out or degradation.

The failure modes keep accelerating one another until the complete deterioration of the package [69]. For instance, the influence in the heat extraction path caused by the delamination and voids can significantly increase the peak junction temperature of the IGBT or FWD and accelerate the evolution of other failure mechanisms like the bond wire lift off, metallization and crack of other solder layers [70]. Another example is the surge current during the abnormal conditions that can turn-on the parasitic transistor represented in Figure 3.2 causing a continuous excessive flow of current through the power supply line, causing the latch up phenomenon [71].

Some failures affect only the IGBT or only the FWD. For illustration, Figure 6.4 shows a damage that occurred only on a FWD die of a 750 A/6500 V flat-pack device from Infineon that happened due to a snappy recovery issue in which the FWD is submitted to high overvoltage and voltage oscillations when turning OFF at low currents.

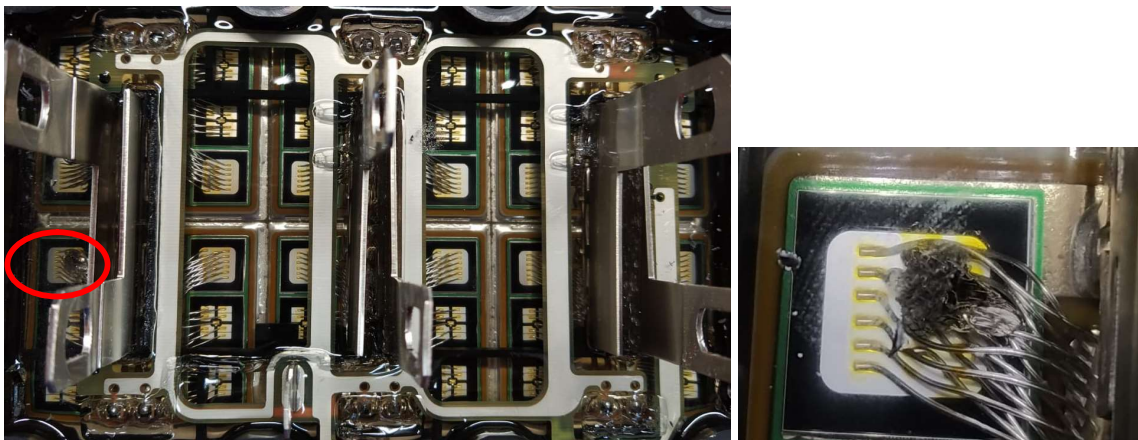


Figure 6.4 Example of damage FWD die inside a flat-pack structure

Figure 6.5 shows a failure affecting only the internal IGBT dies of a 1200 A/3300 V flat-pack device, also due to a turn OFF transitory. It is possible to notice the rupture of the bonding wires, characterizing an open circuit failure [5] [72].

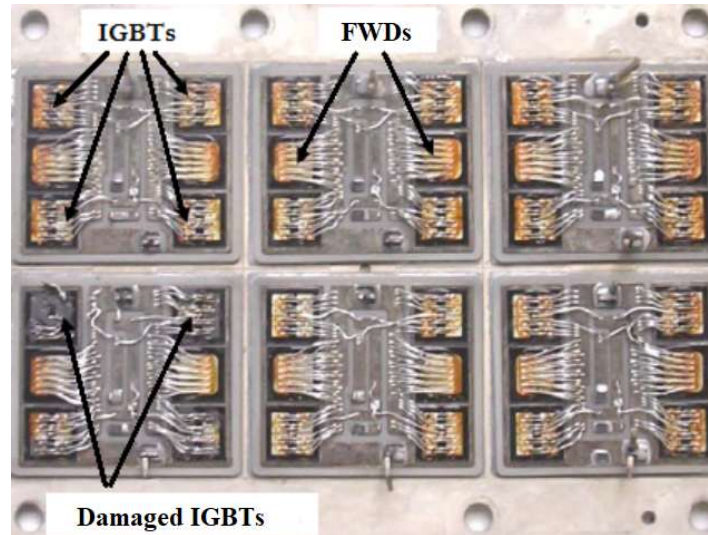


Figure 6.5 Example of damage IGBT die inside a flat-pack structure [5]

Figure 6.6 illustrates a more deeper and detailed images of the typical damage observed in the IGBT structure depending on the failure mode.

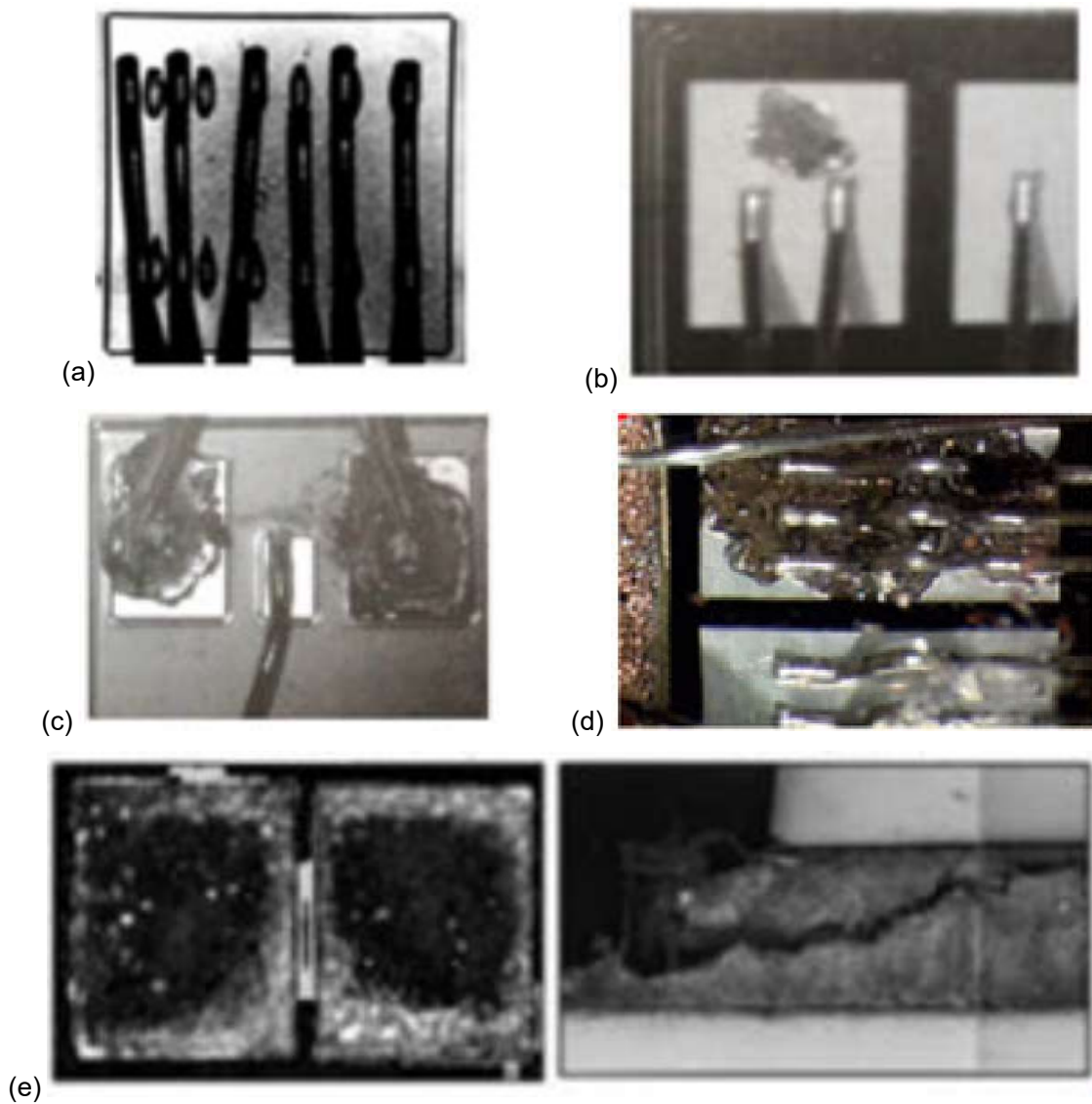


Figure 6.6 Internal Damage Patterns: (a) Bond Wire Lift-Off (Thermo-mechanical Fatigue), (b) Overvoltage, (c) Overcurrent, (d) Melting of metallization (Overtemperature), (e) Solder Delamination and Cracks [69]

6.3. Failure Precursor Parameters

A failure precursor is a change in a measurable variable or parameter that can be associated with an impending failure [6]. The main parameters that would be affected and can be correlated to the IGBT degradation are described in the next sections.

6.3.1. Leakage Current

As demonstrated by after fault tests results shown in the previous sections, the measurement of the leakage current or equivalent resistance between collector and emitter is also a parameter that can be used as a failure precursor. This current is also known as collector to emitter cut off current and is the current that still flows when the device is in OFF state. To avoid further damaging the devices while performing the test, the terminal Gate to Emitter should not be left open and the maximum OFF-state voltage defined by the RBSOA shall be respected at each tested temperature [53].

Figure 6.7 shows the measurement circuit for this test given by the IEC 60747-9 [54]. This is the standard followed by the IGBT manufactures to obtain the Electric Characteristics of the device datasheet. Three different configurations can be used in the gate and emitter terminals. When the terminals are short-circuited, the current is called, zero gate voltage collector current, or I_{CES} .

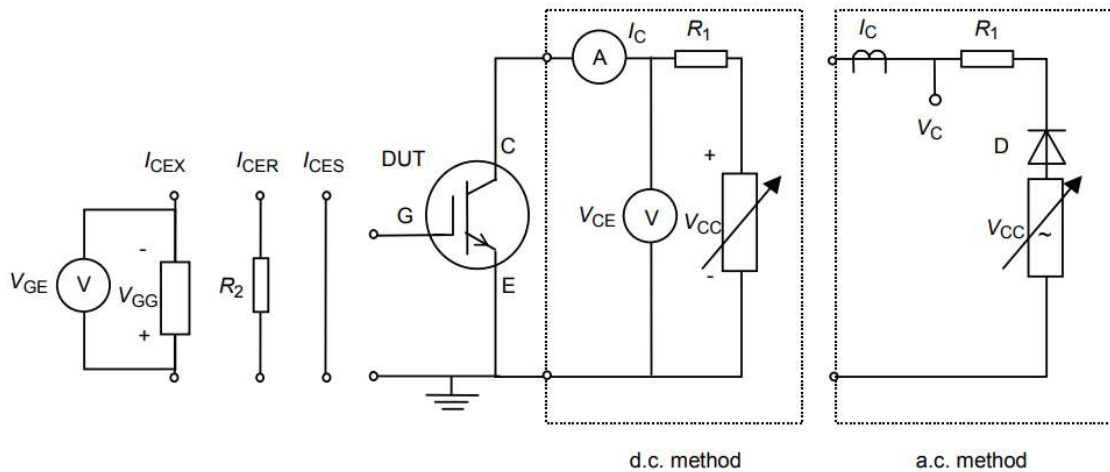


Figure 6.7 Circuit for measuring the collector cut-off current [54]

Where R_1 is a circuit protection resistor.

Figure 6.8 illustrate the expected differences between good and damaged samples and the device behavior in avalanche mode, when the leakage current increases fast [53]. This test should be conducted carefully since a degraded device can present deviations in the leakage current when compared to new units, but that are not a result of a complete short circuit as indicated by [25]. Due to the strong dependance of the leakage current on the applied voltage and junction temperature, the test is expected to be more sensitive for V_{CE} and T_j close to the maximum values.

At the same time, caution must be exercised to not surpass the device limits and further damage the component while executing the test.

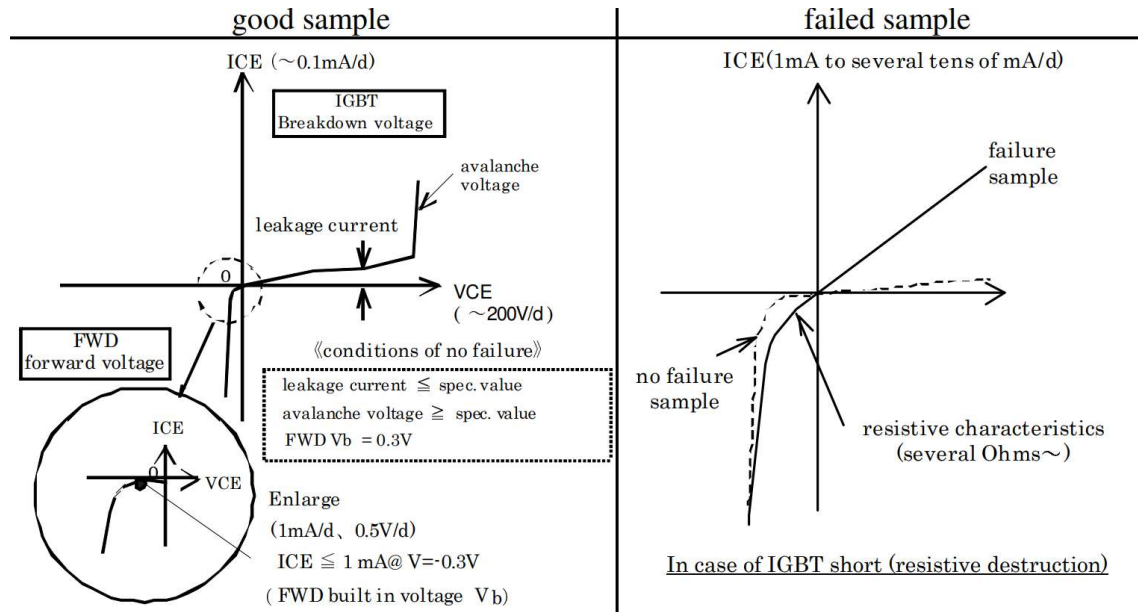


Figure 6.8 IGBT Electrical Characteristic Check (CE) [53]

As observed with the tests performed after Fault #1, if the gate driver is connected and resistance is in parallel with the Collector and Emitter, care should be taken with the interpretation of the results. Although a completely failed sample would still show higher leakage currents, if the value of the parallel resistance is much lower than the device equivalent Collector to Emitter resistance, degraded devices would show leakage current values close to the results of a healthy one. This can interfere in the conclusion about the IGBT condition.

Performing the test for I_{CES} with the gate driver disconnected and the Gate to Emitter terminals short circuited demonstrated to be a more sensitive and precise way to spot degradation, especially when compared to the reference values, as presented in Sections 5.3 and 7.4. Therefore, it is important to remove the gate driver from the IGBT while performing this measurement since the C-E parallel resistance of the gate driver can mask the real value of the leakage current.

The collector to emitter leakage current is a combination of two parts, one from the IGBT and one from the FWD [73]. Thus, it is not possible to know by the leakage current test alone if the parameter shift observed is due to a degradation in the IGBT or the FWD. In fact, the diode reverse current test circuit indicated in the IEC 60747-2 [61], is equivalent to the one in Figure 6.7. The circuit is shown in Figure 6.9. Again R_1 is a circuit protection resistor and D is the diode being measured.

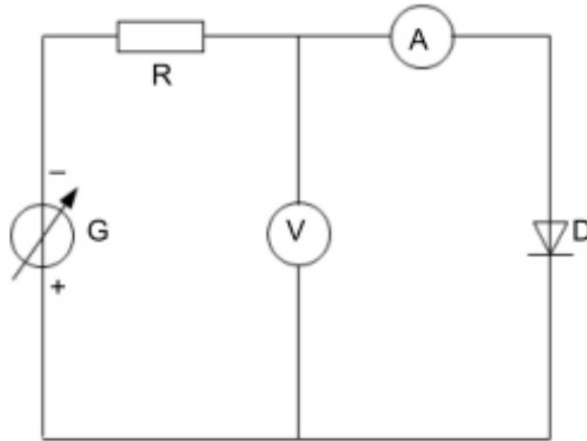


Figure 6.9 Circuit for measuring the diode reverse current [61]

The internal structure evaluation, as described in Section 6.2 can help to better distinguish the location of the damage.

6.3.2. Threshold Voltage

The threshold voltage (V_{th}) is the minimum gate to emitter voltage for the IGBT to start conducting. This parameter can be affected by the dielectric breakdown.

The IGBT is formed by a MOSFET at the input and a TBJ at the output, as shown in Figure 3.2. The gate electrode is built over an insulator layer of silicon dioxide, or simply “oxide”, MOS (Metal-Oxide Semiconductor) layer. An electric field applied to an oxide film causes the injection of holes into the oxide film to occur on the anode side, and it consequently creates traps in the oxide layer because of the electrical stress. There is a maximum electric field that makes the silicon dioxide lose its insulation properties. If the devices experience larger current, or mainly voltage, it will accelerate the degradation of the oxide. Higher temperatures were also proven empirically to lead to shorter time to breakdown.

As the number of traps increase, depending on the electric field strength and the time, the threshold voltage to start to conduct (V_{th}) decreases and an electric current via the traps called SILC (Stress Induced Leakage Current) is formed. If the number of traps continues to increase and the traps connect between the gate electrode and the Si substrate, the connection carries a high current that causes the gate oxide film to breakdown [71] [74].

Figure 6.10 shows the gate degradation process up to the point of a dielectric breakdown. The phases of the stress and its influence in the V_{th} are detailed below [74]:

- The gate current slowly changes.
- Charge is trapped inside the oxide layer causing V_{th} shift. This is also one of the reasons the gate current changes in time.
- Interface traps are created.
- SILC*: The leakage current increases especially in the low voltage regime. The gate I-V characteristic is exponential.
- Soft Breakdown*: the gate current experiences sudden jumps and becomes noisy. The gate I-V characteristic follows a power law.
- Hard Breakdown*: large increase of the leakage current with an almost ohmic conduction (the gate I-V characteristic is almost linear) due to the continuity of oxide traps creation. It is also indicated with "thermal" breakdown because is associated with an irreversible transformation of the oxide structure due to the discharge of the energy stored in the breakdown spot at the moment of the conductive path formation.

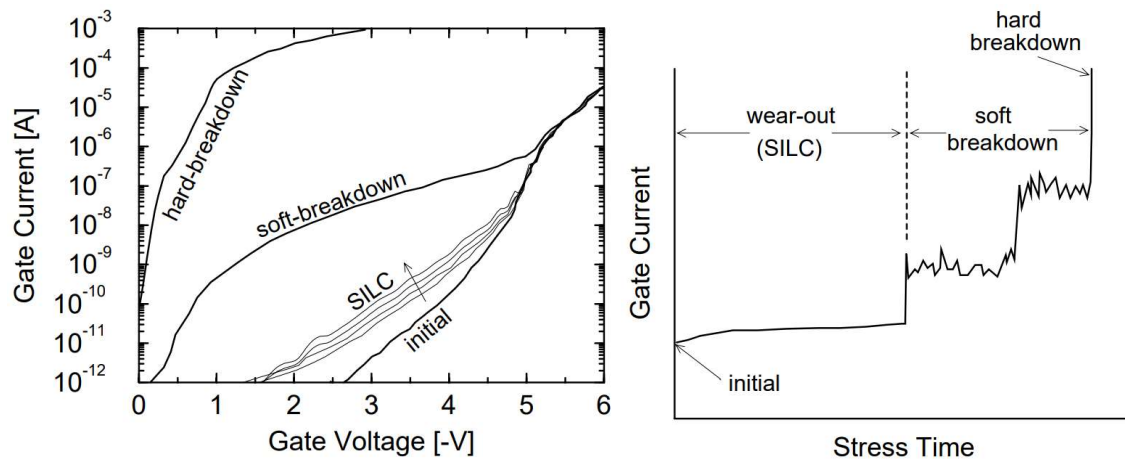


Figure 6.10 Gate behavior under dielectric stress (Left: I-V characteristics. Right: Gate Current Evolution) [74]

Even if the Hard Breakdown final stage is not achieved, the threshold voltage shift will most likely be permanent and can be used as a failure precursor when measured in the IGBTs not burst after a fault.

Figure 6.11 shows the difference on what to expect from the measurements of the Threshold Voltage, checking terminals G to E with C disconnected. In the ideal case the IGBT behavior stays inside the ellipse. There is some IGE current variation

close to the V_{th} but the current should be zero for the maximum VGE since no extra energy is necessary from the gate to turn the IGBT ON. When the Gate to Emitter is short circuited, the current keeps increasing strongly above V_{th} .

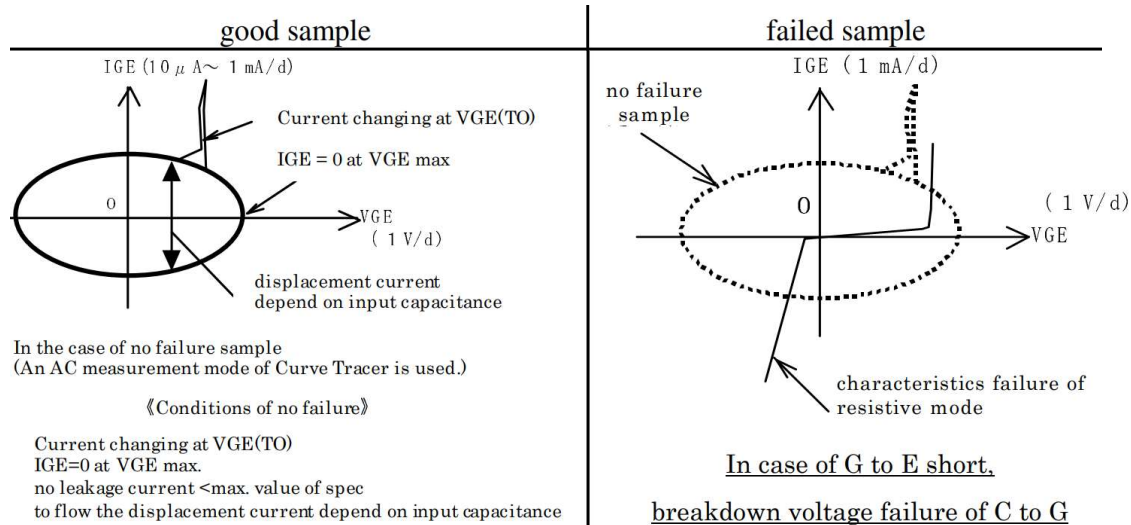
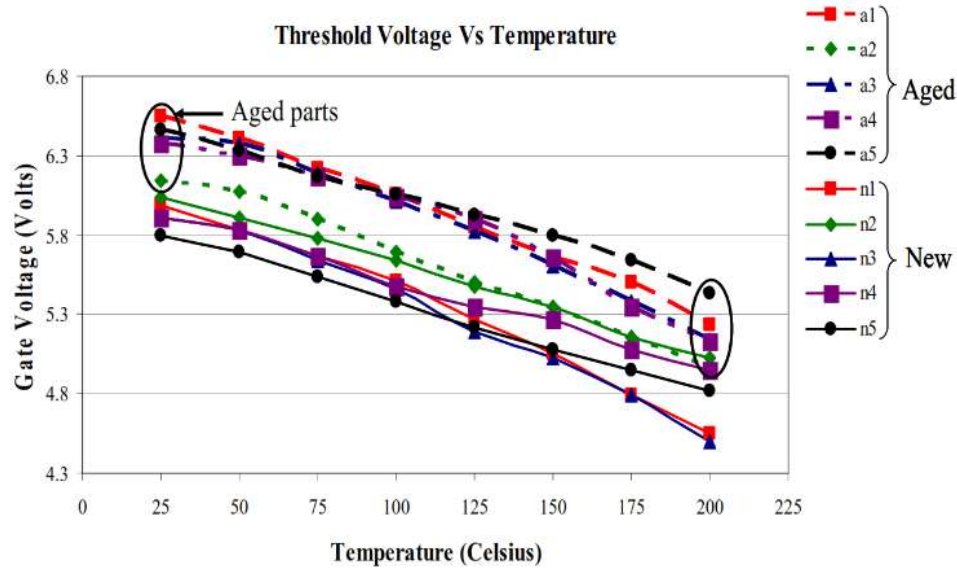


Figure 6.11 IGBT Electrical Characteristic Check (GE) [53]

The post fault effects on the devices are different from a power cycling aging process, as explained in Section 2.3, due to the characteristics of the fault as a high energy event over a very short period. Nevertheless, the results from the tests performed by [7] on the IGBT IRG4BC30KD submitted to accelerated aging process through power cycles are presented in this chapter for illustration.

The effect of the temperature in the threshold voltage for new and aged units are shown in Figure 6.12. Higher temperatures decrease the bandgap of the silicon and cause a reduction on V_{th} . Aged parts have a higher V_{th} than the new parts across all temperatures and the value diminishes with the temperature increase. The average threshold voltage difference between aged and new parts was around 10 % at both 25 °C and 200 °C.

Figure 6.12 V_{th} vs Temp. for degraded and new units [7]

6.3.3. Transconductance & ON-state Voltage

The transconductance is a gain factor that correlates the collector current dependence only on the gate voltage in the active region. It is a direct measurement of the MOS capacitance C_{ge} in Figure 3.3. The ON-state voltage is the voltage drop across collector to emitter when the IGBT is conducting current [75].

The transconductance has a negative temperature coefficient in the saturation region, i.e., when operating closer to the junction temperature the output current is smaller for the same input voltage. On the other hand, the ON-state Voltage, has a positive coefficient, due to increased equivalent resistance between C-E, the voltage drop is higher with an increase in temperature for the same current. The influence of the temperature on the transconductance and the ON-state voltage can be seen in the I_c vs V_{CE} curves of Figure 3.10.

While the oxide damage affects the threshold voltage, transconductance and collector-emitter ON-state voltage parameters shift can be related to die-attach degradation [7]. In fact, the p-n junction of the die has a negative temperature coefficient and an increase in the temperature at this junction will result in lowered resistance as observed.

The die-attach can suffer the separation in layers that come out of the surface, process called delamination, and the creation of empty spaces or voids inside the

structure. Those deformations can impact the thermal flow to the ceramic substrate, which is the most critical solder interface because they have the highest mismatch in the coefficient of thermal expansion of the materials used and the highest temperature swing. The ceramic substrate has also the largest lateral dimensions and the larger the lateral size of a layer, the bigger the thermo-mechanical stress. The heat flows around the voids, in a smaller area, creating local temperature gradients and diminishing the dissipation performance [64] [68] [70].

For a power cycling aging process, it is expected that the transconductance is higher for aged devices when compared with new ones, as it can be seen in Figure 6.13. This means that for the same gate voltage, aged devices would present a higher saturation current. Furthermore, the difference between aged and new parts was higher for the tests at ambient temperature.

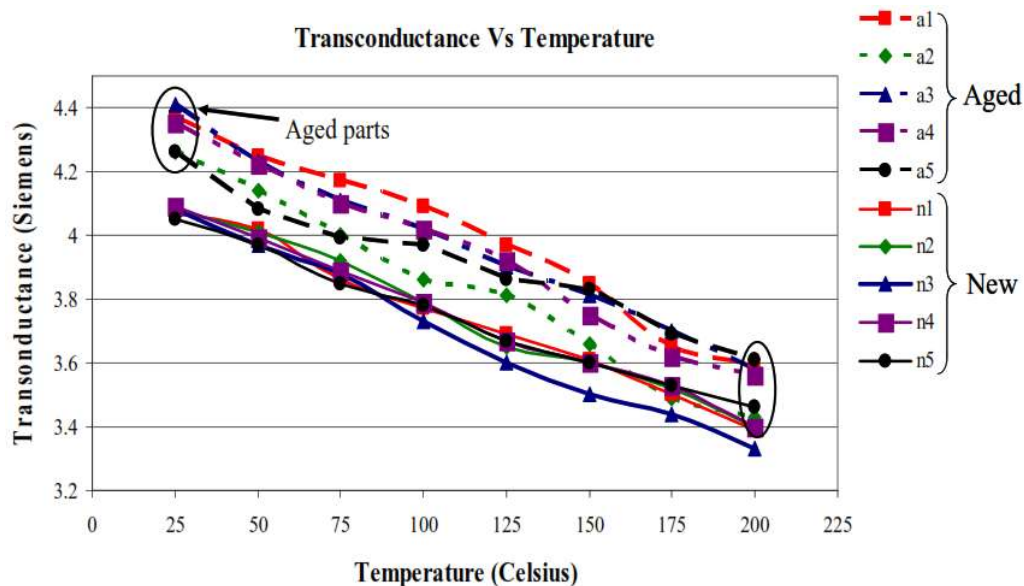


Figure 6.13 Expected Transconductance vs Temp. for degraded and new units [7]

At the same time, aged parts have lower resistances at high currents, having lower ON-state voltages in the linear region, Figure 6.14. The difference is bigger at higher temperatures, but from the experiment performed by [7], the voltage magnitude in the aged parts was still relevant at 25 °C, around 10 %.

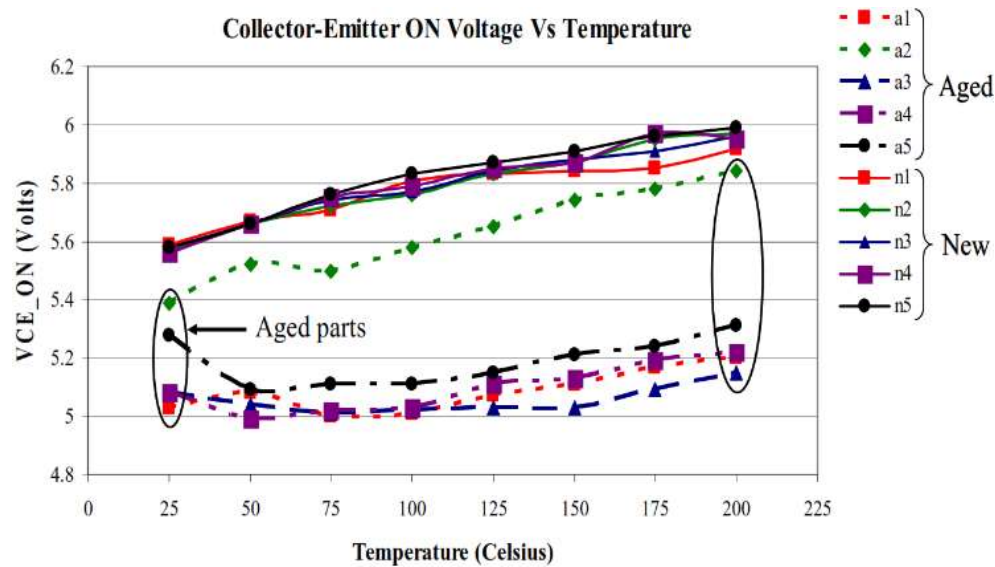


Figure 6.14 Expected Collector-emitter ON voltage variation with temperature [7]

6.3.3.1. I-V Curve

With the Transconductance and the ON-state voltage the IGBT I_c vs V_{CE} curve can be constructed for different gate voltages. Likewise, the FWD forward characteristics can also be plotted. Figure 6.15 shows the comparison of the curve for a good and failed sample, checking terminals C-E while applying different voltages to G-E. The values of I_c are higher for a lower V_{CE} in the failed sample. The test should be performed around the rated values since the impact of the degradation is not very evident for lower values of gate voltages and collector currents [7].

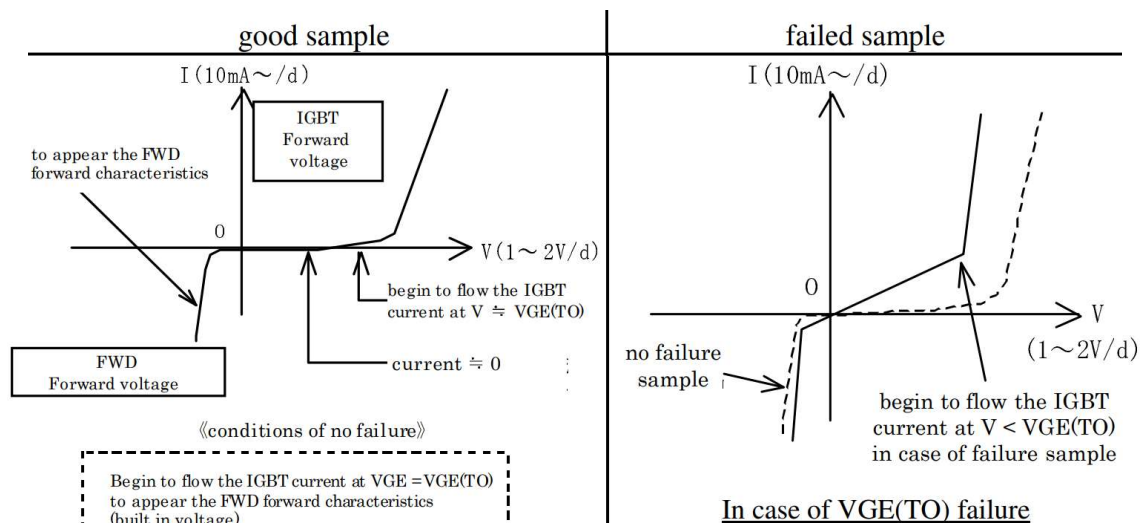


Figure 6.15 IGBT Electrical Characteristic Check (CGE) [53]

Aged IGBTs would also present lower pinch off voltages to enter the active region, as shown in Figure 6.16.

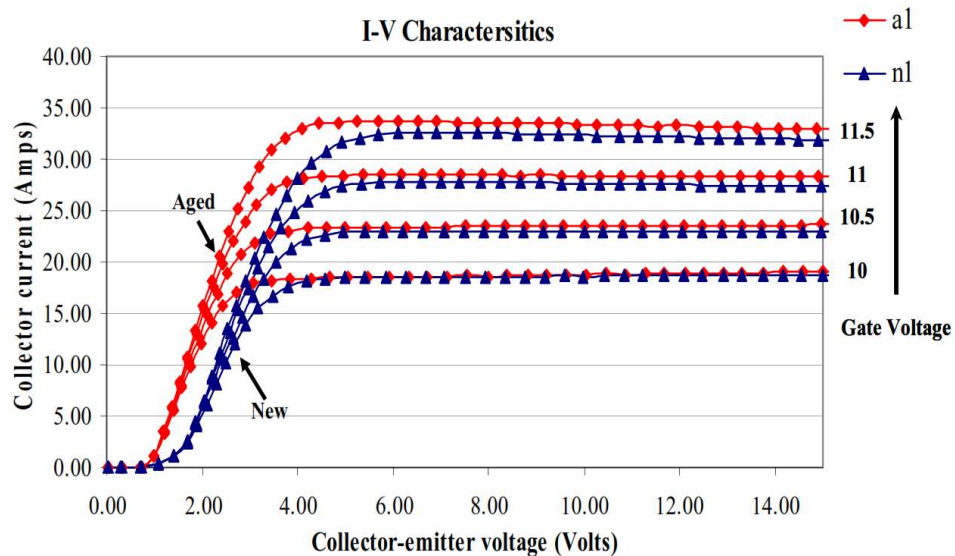


Figure 6.16 Expected I-V curves for aged and new IGBTs under high gate voltages [7]

The impact of the degradation in the die attach is not as significant at lower gate voltages and currents, as it can be seen in Figure 6.17. In this case, the degradation in the gate oxide film that also affects the threshold voltage has a more relevant impact. It causes an increase in the channel resistance, and thus a lower collector current when compared to new units [7].

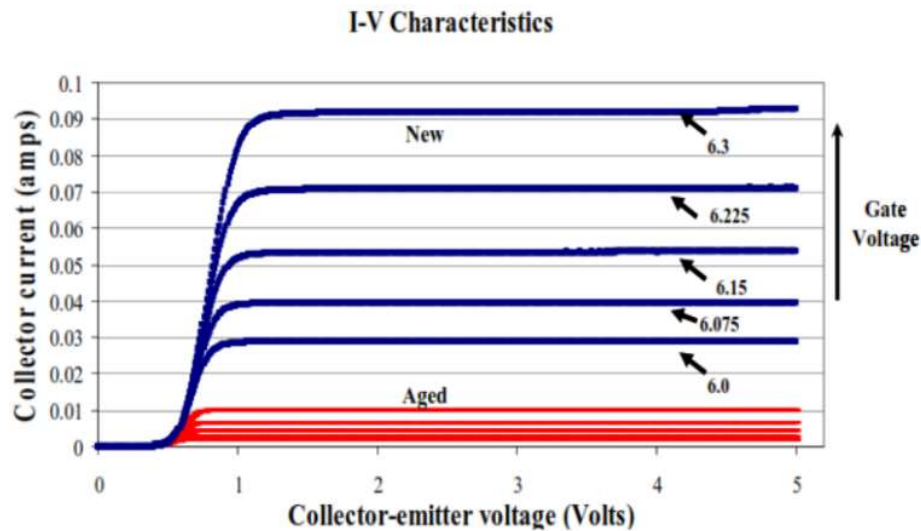


Figure 6.17 Expected I-V curves for aged and new IGBTs under low gate voltages [7]

6.4. Conclusions

In this chapter it was possible to verify the details of the internal structure of the flat-pack IGBTs under study. The components comprise three internal IGBTs and FWDs connected in parallel, each one is then a multichip group interconnected to the power terminals with wire bonds. The internal parts of the structure have a potential failure mode, with different possible causes that leads to different failure mechanisms. The device presents deviations in the precursor parameters because of the failure modes, most of the time the failure modes are combined and difficult to differentiate for completely failed devices, yet executing investigation and the correct test associated to each failure mode can help identify the characteristics of a degraded IGBT and complement the fault analysis. Although, as previously discussed, results from accelerated aging process are not directly comparable to post fault conditions due to the characteristics of the faults of having a high energy over a short time frame, the findings of [7] are presented for illustration of deviation in the precursor parameters and what to look for. It is explained for instance, that checking the transconductance can reveal degradation in the dye attach even at ambient temperature. The leakage current is another example, as already demonstrated by the tests explored in the previous chapters. It is highlighted here though, that the tests would be evaluating the IGBT and FWD ability to block high voltage at the same time. Determining what is the actual affected component can be only indirectly performed by looking at the other test results and the fault analysis or by opening the IGBT case and assessing the internal structure.

Chapter 7. Power Semiconductors Tests and Investigation

Results of offline / off-circuit tests that enable the identification of the parameters shift are shown in this chapter. The tests are applied to sample devices, affected by the main fault described in Chapter 5 and variations in the expected results that can be used as indicators of degradation and premature aging are analyzed.

The precursor parameters are verified in static operation of the device, either ON or OFF, as described in Chapter 6. The tests are performed at ambient temperature and close to the maximum junction temperature set with the aid of a hot plate and a closed loop temperature control circuit. The target temperature is calculated considering the maximum power loss during each test and the temperature increase from the junction to the hot plate.

Care is taken in the execution of the tests to not submit the devices to extreme conditions that would add a new layer of degradation to the devices and lead to a misinterpretation of the results. For that the maximum junction temperature and the limits of its SOA are always respected.

7.1. Device Samples Under Test

The four devices chosen for the laboratory tests were highlighted with a purple dashed line in Table 5.1. In this chapter, they will be referenced by the last 3 digits of their serial numbers for simplicity. The full serial number is hidden for confidentiality. Table 7.1 can be used to match the devices identification with the previous chapters.

Table 7.1: Identification Control for Sample Devices Under Test

Flat-Pack Case	Fault Analysis Control		C-E, Insulation Test		Comment
Serial Number	Device	Phase Module	Before Fault #2	After Fault #2	
xxxx04E	Q4	L2	2.26 G Ω – 5 kVdc	72.3 M Ω – 5 kVdc	Degraded
xxxx06E	Q1	L2	1.84 G Ω – 5 kVdc	1.48 M Ω – 2 kVdc	Damaged
xxxx06G	Q3	J2	New Unit	0.720 G Ω – 5 kVdc	Probably OK
xxxx17G	Q4	K2	New Unit	0.831 G Ω – 5 kVdc	Probably OK

As described in Section 4.3, unless for device Q2 of phase module C, the one that probably started Fault#2, all other devices were either brand new units or had its internal insulation individually checked, with gate driver disassembled, before restoring the converter after Fault #1. Therefore, the results of the equivalent insulation resistance before and after Fault #2 are also placed in Table 7.1 for comparison.

Device 04E was chosen due to its evident sign of degradation, with a deviation in the insulation resistance value, but still a high value in magnitude and still able to sustain 5 kVdc voltage. Device 06E serve as a reference of damaged unit once it was not able to sustain the test voltage. Devices 06G and 17G results will serve as references of good conditions or low degradation, since it stays under the manufacturer margins as shown in the next sections.

As previously stated, the 5 kVdc insulation tests were performed in all three internal semiconductors of each flat-pack case at the same time, connection busbars installed. On the other hand, the detailed investigation tests of this chapter were executed in each flat-pack internal IGBT and FWD at a time to identify the areas of highest degradation and match it with the images of the internal structure after the removal of the case. The device internal Circuit Diagram can be seen in Figure 3.3.

Figure 7.1 details how the internal semiconductors were numbered when looking at the flat-pack case.

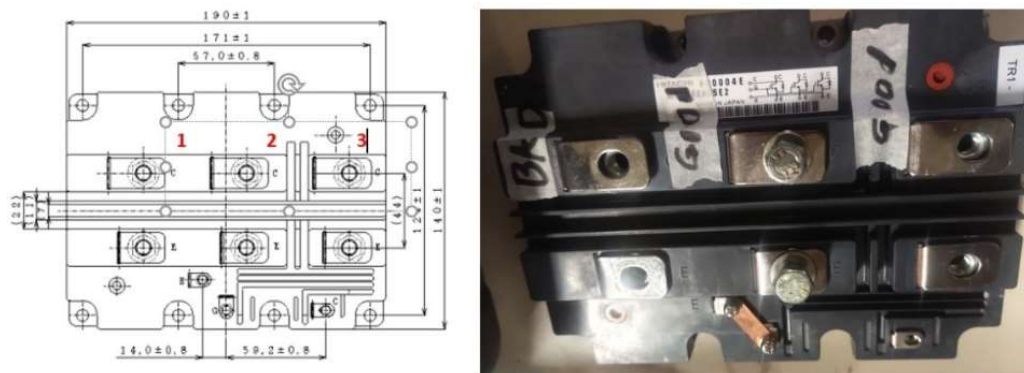


Figure 7.1 Pre damaged Flat-pack IGBT with the Indication of the Parallel IGBTs Position Inside the Frame.

7.2. Test Plan

Due to the results for the leakage current observed in the preliminary tests described in Chapter 4 and Chapter 5, the leakage current was the main device internal parameter to be investigated in detail in the laboratory tests. For that, the Insulation Tester MIC-10k1 from Sonel was used to apply the reverse voltage with the terminals gate and emitter short circuited. This instrument has high precision applying voltages in steps of 10 V or 25 V and extensive measurement capabilities, being able maintain test currents up to 6 mA.

Based on the failure modes and precursor parameters discussed in Chapter 6. Other tests with the IGBT and FWD in ON state were executed using a controlled current source model ESS-10-1000 from TDK. The tests were performed at ambient temperature and close to 125 °C, maximum junction temperature for the device model under study, [30]. Figure 7.2 shows the structure of the planned tests.

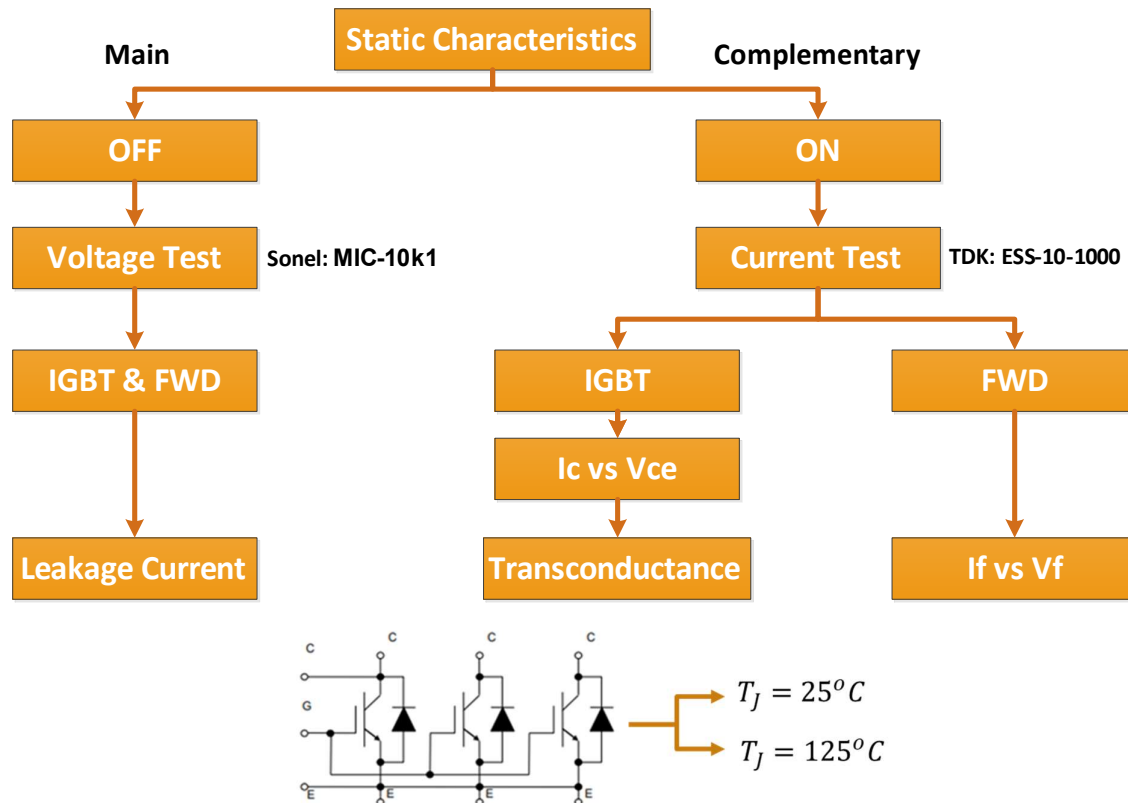


Figure 7.2: Post fault Test Plan

7.3. Temperature Control

The Hot Plate shown in Figure 7.3 was used to reach the desired temperature evenly at the DUT (Device Under Test) base plate. The plate is put in thermal equilibrium before each test.

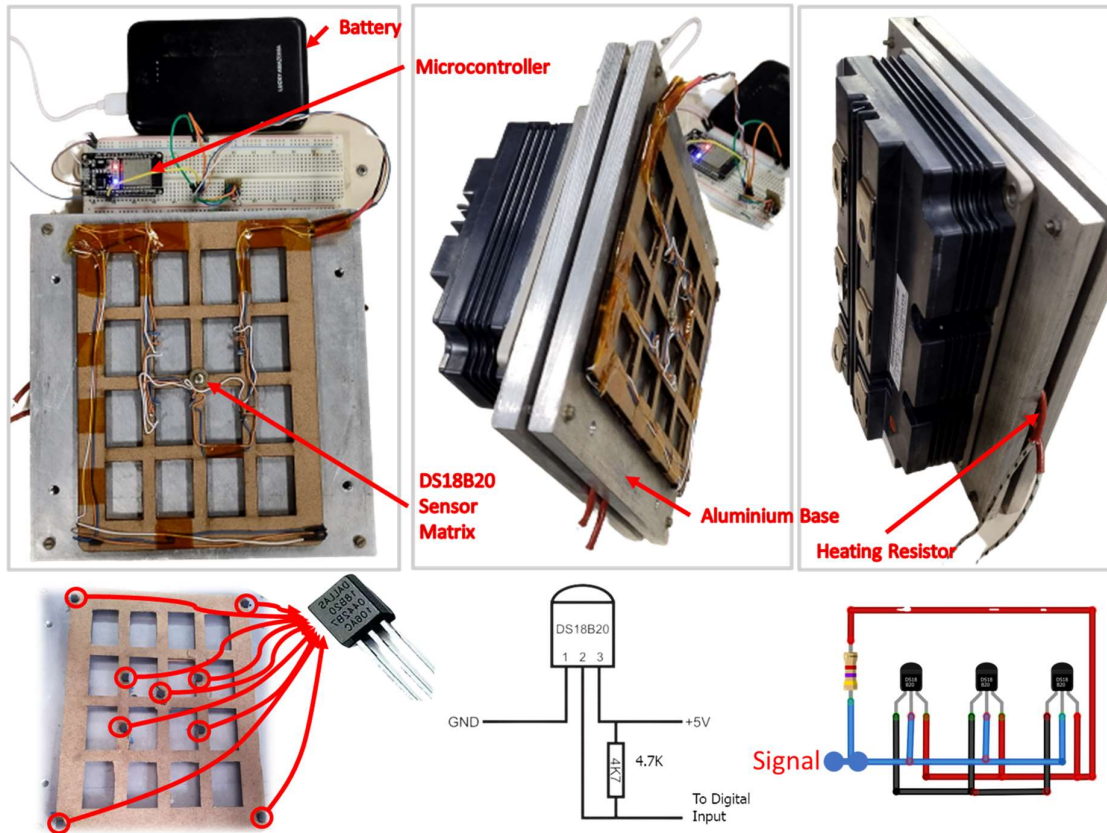


Figure 7.3 Hot Plate for Tests Close to the Maximum Junction Temperature (adapted from [76])

The hot plate comprises a set of heating resistors in between two aluminum plates, with a wooden matrix at the bottom on which the DS18B20 temperature sensors are placed. The matrix and the resistors cover the full area of the flat-pack base plate. A microcontroller is fed with the temperature sensors reading and controls the resistors current to keep the temperature at the desired value. The temperature setup and monitoring can be done through the hot plate software application. A thermal camera (InfraCAM SD, from FLIR) is also used as a safety precaution to confirm the device case and Hot Plate temperatures. Finally, a thermohygrometer measures the ambient temperature and humidity while the tests are performed. Figure 7.4 shows the test bench setup.

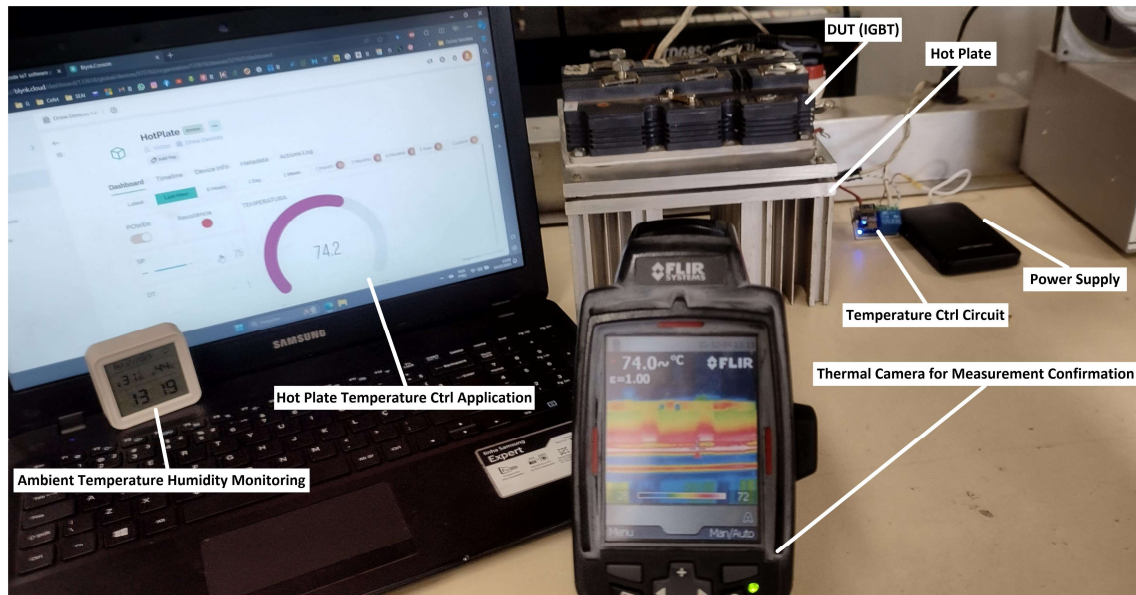


Figure 7.4 Hot Plate Test Setup and Software Application

A validation test was performed to obtain the time constant to achieve the thermal equilibrium of the hot plate. The thermal camera was used to validate the Hot Plate temperature evenly distributed throughout the area matching the device base plate in steady state. The results show that the temperature read by the sensors was similar to the ones read on the side in which the device is placed even during the heating process. The time to achieve 80 °C was 540 s starting at an ambient temperature of 25 °C, as demonstrated in Figure 7.5.

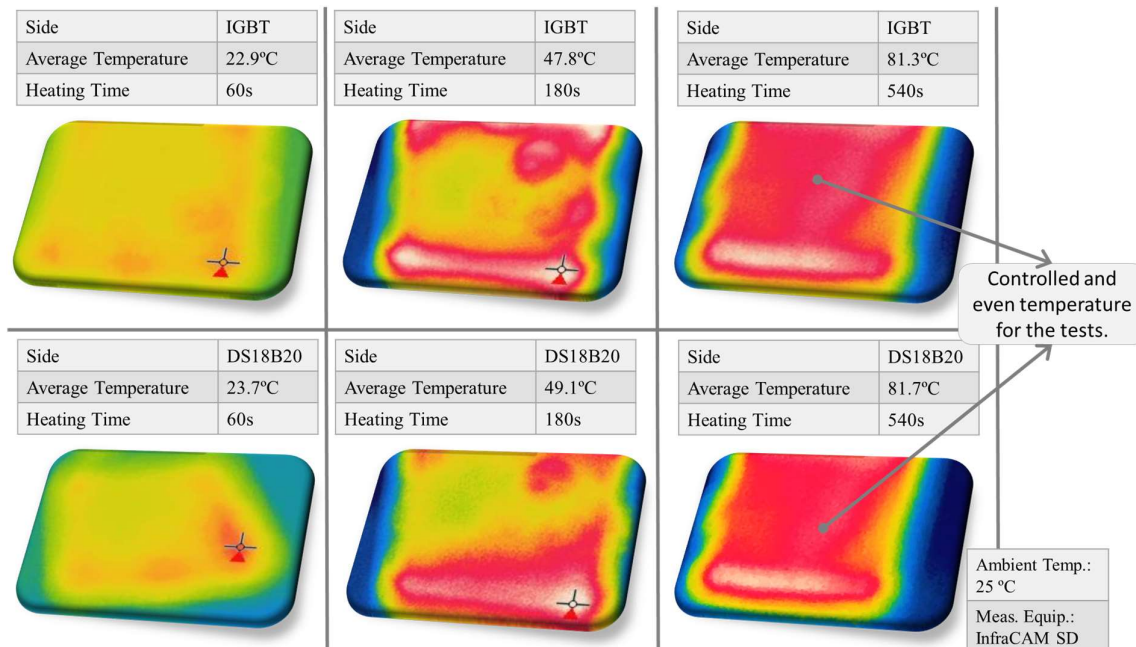


Figure 7.5 Hot Plate Temperature Control Validation Test [76]

The test temperature set for the hot plate was chosen for each test to have the junction temperature close to the maximum allowed so that its influence in the precursor parameters can be evaluated. At the same time, the temperature elevation due to the power losses estimated for each test is also considered to avoid the junction temperature to increase above the limit and cause damage to the DUT due to the test execution itself. For that, the thermal model of the elements involved in the heat transfer and the test duration were considered.

A common IGBT and FWD equivalent thermal circuit is shown in Figure 7.6, (a). Where the equivalent thermal impedance Z_T can be drawn as a RC network of different number of layers, as in Figure 7.6, (b), known as Foster model.

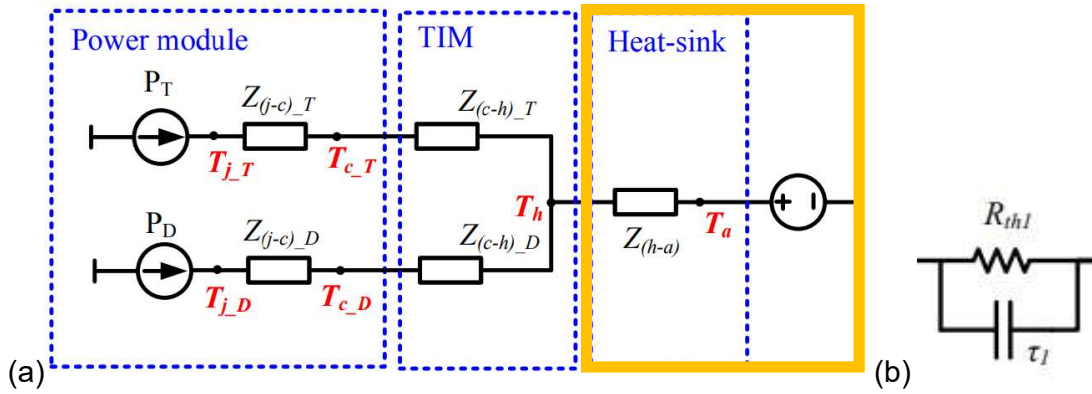


Figure 7.6 Equivalent Thermal Circuit (adapted from [77])

The tests described in the next sections are performed after the hot plate has reached the target temperature and since it is a closed loop-controlled circuit, T_h can be considered a fixed value, i.e., it won't be affected by the heat flow coming from the junction. The part highlighted in orange in Figure 7.6, (a), can be disregarded.

The Thermal Pad COH-1016LVC was used as TIM (Thermal Interface Material). Its thermal impedance can be considered as a thermal resistance calculated by Eq. (7.1) due to its fast time constant.

$$R_{th(c-f)} = \frac{\text{Interface Thickness}}{\text{Thermal Conductivity} * \text{Contact Area}} \quad (7.1)$$

Where:

- The thermal conductivity is given by the datasheet as $1.9 \frac{W}{m^{\circ}C}$
- The final thickness after tightening the device to the hot plate is 1.5 mm.
- The contact area is taken from the device base plate dimensions [30] as 0.0266 m^2 .

For fast dynamic events, the device manufacturer provides the transient thermal impedance curve, as shown in Figure 7.7, that estimates the temperature elevation from the case to the junction using the Foster thermal model. This model doesn't have a physical sense, it is rather a mathematical approximation obtained from fitting parameters of transient thermal tests [67]. For the device under analysis, after 0.4 s the influence of the thermal capacitance can be disregarded, remaining only the effect of the thermal resistances.

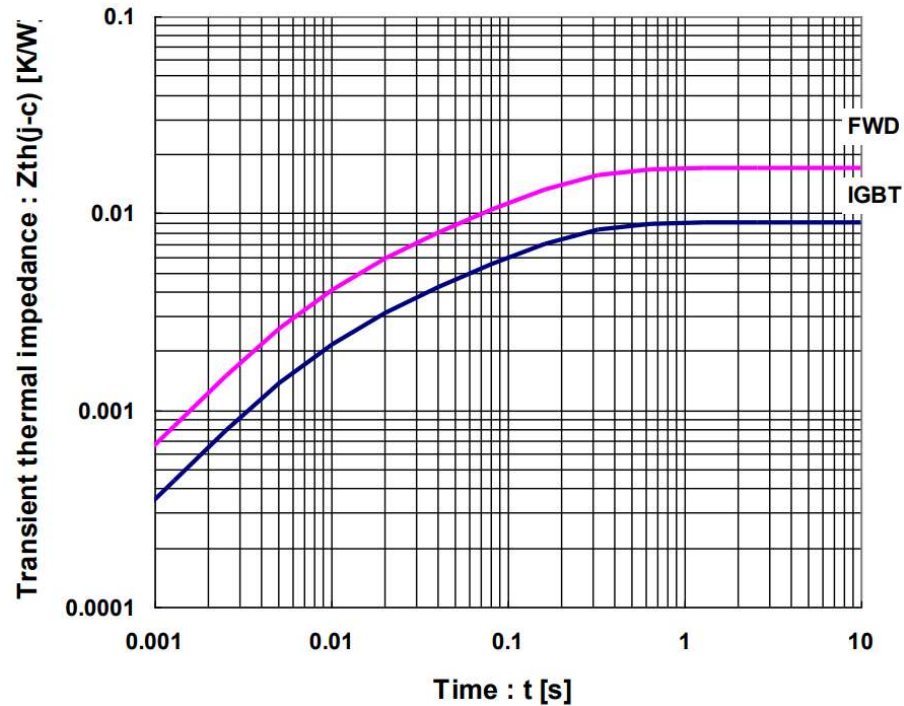


Figure 7.7 Hitachi, MBN750H65E2, Transient Thermal Impedance Curve [30]

Table 7.2 summarizes the thermal resistances. The values given for the junction to case thermal resistance are valid for the entire flatpack unit, while the value for each internal IGBT will be 3 times higher.

Table 7.2: Thermal Resistances Considered in the Tests at Maximum Junction Temperature

Device baseplate to Hot Plate	$R_{th(c-h)}$	0.0297 °C/W
IGBT junction to case	$R_{th(j-c)}$	0.009 °C/W, [30]
FWD junction to case	$R_{th(j-c)}$	0.017 °C/W, [30]

To understand if the device case, or more specifically the baseplate would have a considerable temperature increase that could influence the choice for the hot plate temperature during the tests, the behavior of the baseplate thermal capacitor needs to be analyzed for the average power and duration of each test.

The Foster model only calculates the temperature rise and is not good to estimate the actual baseplate temperature due its mass and material type, for that it is necessary to use Cauer model. This model is associated to the actual physical layers of the device structure. The equivalent thermal resistances and capacitances are calculated based on the geometry and property of the materials of each layer [78]. The Cauer-type thermal model at the die level is shown in Figure 7.8.

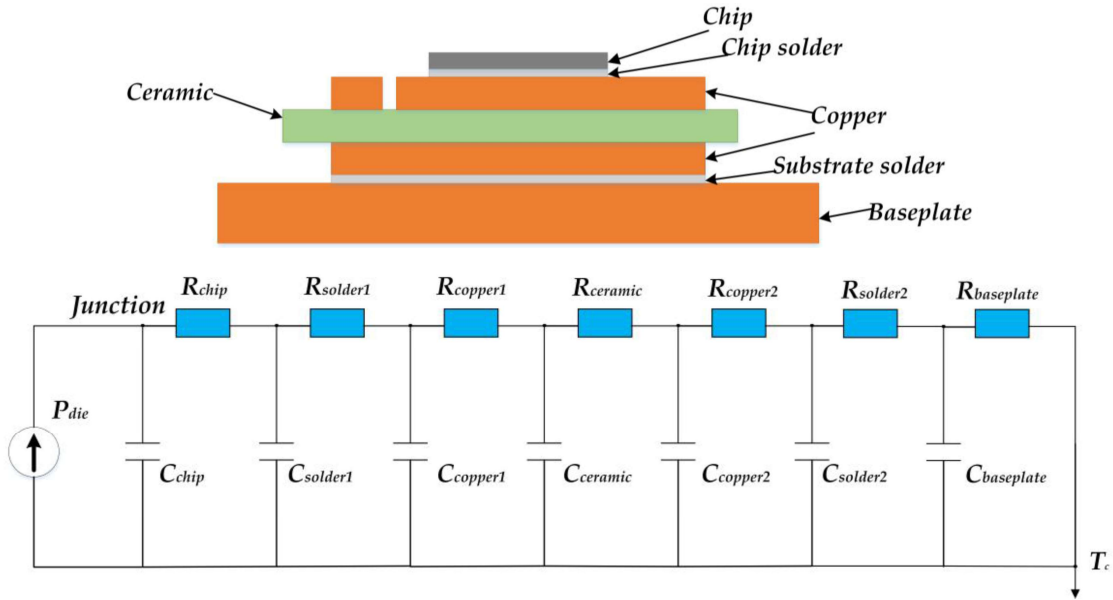


Figure 7.8 Cauer-type thermal model at die level, [78]

The base plate material, given by [30], is the AlSiC, which has a Specific Heat $c_{AlSiC} = 0.741 \text{ J/gK}$ and a density $\rho_{AlSiC} = 3.01 \text{ g/cm}^3$ [79]. The volume is also taken from [30] as $V_{baseplate} = 133 \text{ cm}^3$. The baseplate thermal capacitance is then calculated as:

$$C_{baseplate} = c_{AlSiC} \rho_{AlSiC} V_{baseplate} = 297 \text{ J/K} \quad (7.2)$$

To verify the temperature at the baseplate for that time a worst-case assumption can be used, considering that when the test starts the baseplate and the hot plate are at thermal equilibrium, but the whole power generated by the test will be transferred to the baseplate capacitor. The simplified circuit showing this test condition at the die level can be seen in Figure 7.9.

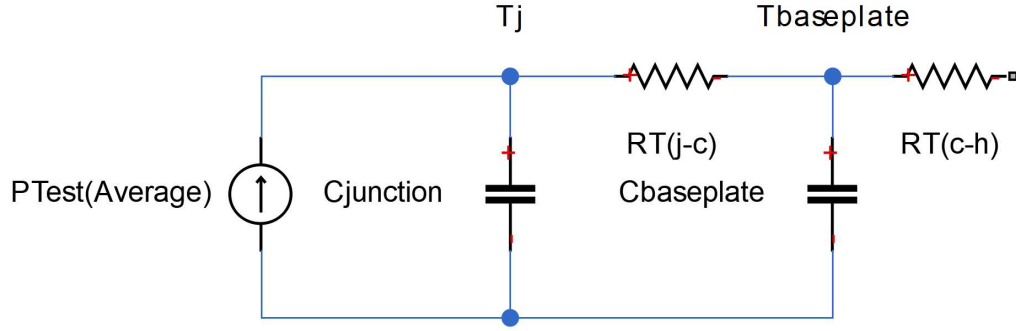


Figure 7.9 Simplified Thermal Equivalent Circuit For Baseplate Thermal Dynamics Evaluation

In reality, the baseplate time constant to rise the temperature is even slower since the heat coming from the junction power loss goes not only to the capacitor but also to the hot plate through the TIM until the capacitor is fully charged and then all the heat goes to the hot plate. At this point the temperature difference between the baseplate and the hot plate will be given by the test power times the thermal pad thermal resistance. However, as it will be seen in the next section this condition never occurs since the average power is more relevant at the tests that apply current with the IGBT in ON state, but the duration of this test is short, only 1 s. At the same time, the OFF-state tests in which the voltage is applied to DUT take longer to execute, up to 30 s, but the power generated is very low.

Thus, Eq. (7.3) can be used to decide on the hot plate temperature controlled value for each test:

$$T_{HotPlate} = T_{Jtarget} - P_{Testaverage} \left[R_{T(j-c)} + \frac{t_{test}}{C_{baseplate}} \right] \quad (7.3)$$

Where:

- T_{Jmax} : is the target temperature, to avoid damaging the IGBT, but still test it close to the thermal limits. A margin of 10 °C was given to account for errors in the parameters, i.e, $T_{Jtarget} \cong 115$ °C.
- $P_{Testaverage}$: is the estimated average power expected for the tests. This value is calculated based on the references for a healthy unit, since the possible misbehavior due to the degradation is unknown. The intermediate results were monitored along with the temperature measured with the thermal camera to avoid a unexpected condition that could lead to a much higher energy consumption and compromise the junction temperature.

$R_{T(j-c)}$: is the IGBT or the anti-parallel FWD thermal impedance, depending on the DUT. Since the minimal test duration is 1 s, the device thermal dynamics shown in Figure 7.7 is stabilized, and the value of the thermal impedance is reduced to the thermal resistances shown in Table 7.2. The value is multiplied by 3, since the tests are performed at each parallel internal component at a time.

- t_{test} : is the maximum test duration.
- $C_{baseplate}$: is defined by Eq. (7.2).

It is also important to highlight that another assumption usually considered in the thermal analysis is that the IGBT and the case temperature rise is uniform. As indicated in Section 6.1, the dies in the multichip structure shown in Figure 6.2 will present thermal deviations due to factors like thermal cross coupling (impact of the heat spreading of one die on its neighbors), current deviations, inhomogeneous cooling and uneven aging [67]. Figure 7.10 illustrates the thermal mismatches in a multichip device reaching up to 17 °C difference for a 1000 A simulated current.

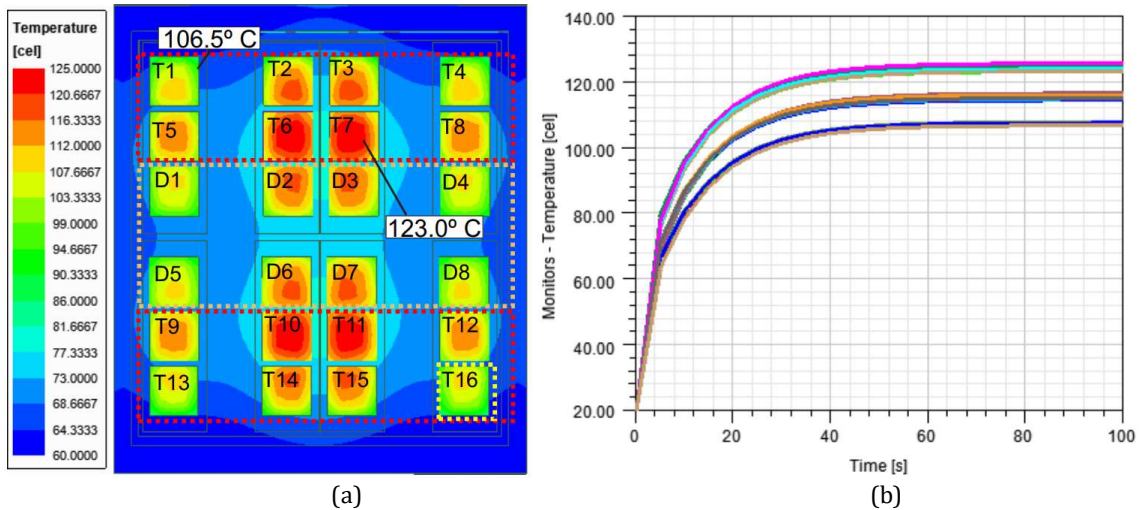


Figure 7.10 Simulation example of thermal deviation among 24 dies in a multichip device in (a) Steady-State and (b) Transient [67]

Specially for the tests performed in this work, since each parallel internal IGBT is tested at a time, only some internal dies will heat up at each test. Therefore, initially, only part of the baseplate is heating up and not the entire volume as considered in Eq. (7.2). The assumption is yet valid for simplicity because the thermal conductivity of the AlSiC is very high, 180 W/mK [79].

The concepts given in this section will be used next along with the estimation of each internal parallel IGBT or FWD of the flat-pack case expected power loss for

each test. Then based on this power, a highest thermal mismatch is estimated in the baseplate to prove that this discrepancy is not relevant in this analysis.

7.4. Test # 1 - Leakage Current

To perform this test, the reverse biased voltage was applied in steps up to the maximum value, V_{CES} , following the reference test instruction of [53]. At each step the voltage was held for 30 seconds. The test was done for the zero gate voltage collector current, I_{CES} , using the D.C. method, as per Figure 6.7. Care was taken to not surpass 6500 V, which is the maximum voltage limite of the SOA for the IGBT model under analysis. Figure 7.11 exemplifies the test setup.



Figure 7.11 Leakage Current Test, Insulation Tester Setup

7.4.1. I_{CES} at Ambient Temperature

Figure 7.12 shows a summary of the I_{CES} test results at ambient temperature for the 4 sample units. For device 04E, while the values of devices 2 and 3 were similar, indicating a consistent aging process, a clear deviation was found in IGBT1. This device could still sustain high voltage but presented much higher leakage current or lower insulation resistance between Collector and Emitter.

Reference curves obtained from interactions with the manufacturer [80], of one new device sample at 25 °C are also placed in Figure 7.12 for comparison. The curve is not of guaranteed values. The leakage current test is normally registered at maximum collector to emitter voltage, but the reference curve with intermediate values exemplifies the variation of the leakage current with the applied voltage.

Likewise, the mean and minimum values obtained from a distribution data of 9819 units of flat-pack devices tested at 25 °C and maximum V_{CE} voltage applied, 6500 V are marked in the plot [63]. Those results from the manufacturer were obtained for the full flat-pack devices with the three internal devices connected in parallel. Therefore, the results are divided by three as an approximation for direct comparison and the total units in the population can be considered 29457 embedded IGBTs and FWDs.

For the devices 06G and 17G the values of the separated IGBTs were similar indicating a consistent aging process. The values are also higher than the sample reference provided by the manufacturer and match the mean when extrapolated to the maximum voltage.

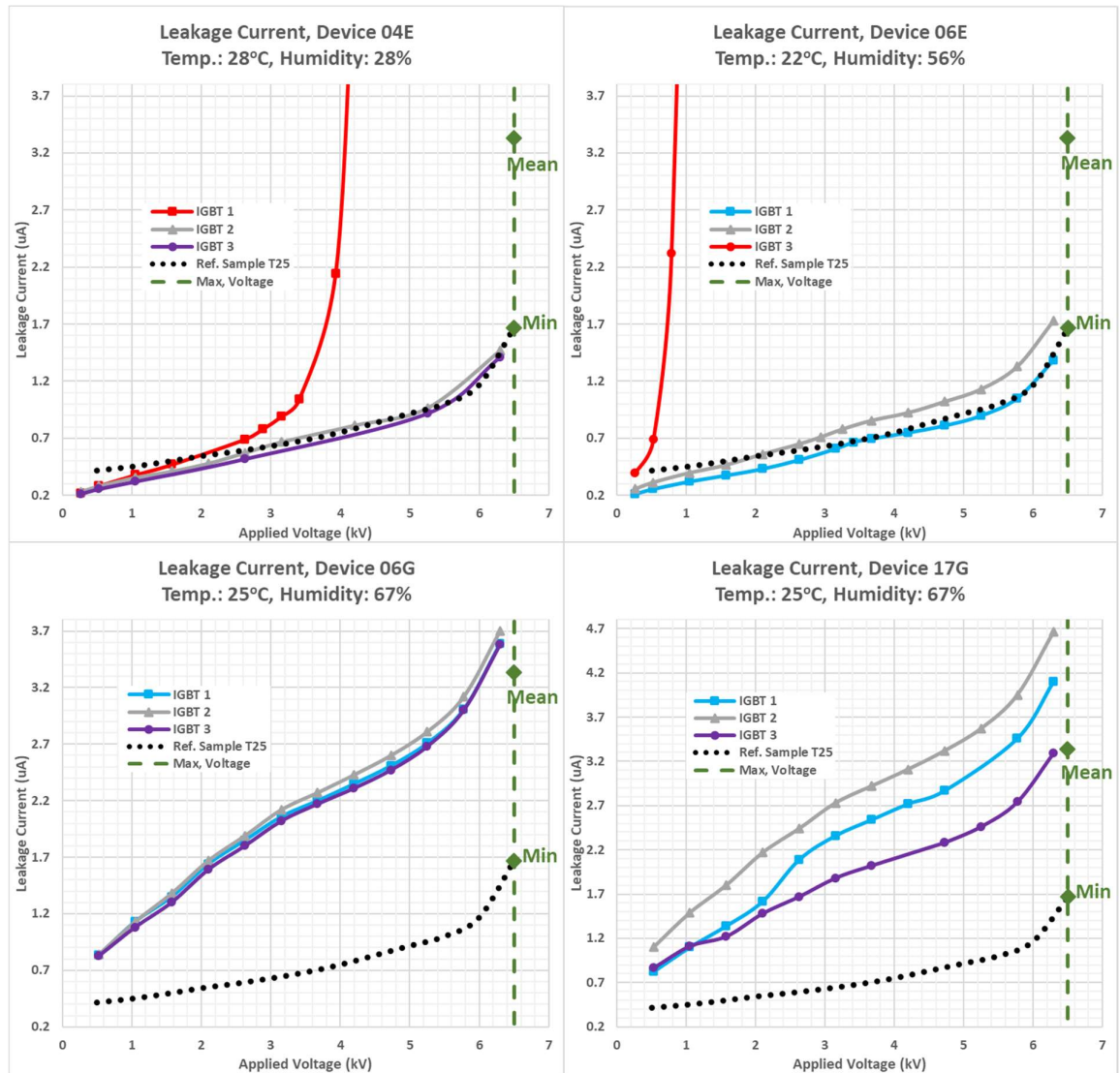


Figure 7.12 Collector Emitter Cut-Off Current Test Results at Ambient Temperature

Figure 7.13 shows a comparison of the degradation between devices 04E and 06E. The leakage current axis is now in mA for the visualization of the maximum values. It is possible to notice that the values reached are much higher than what was verified for the other devices and the references given by the manufacturer.

Device 06E has a low reverse breakdown voltage, around 1.5 kV, from which the leakage current starts increasing sharply. The plot is limited to 1.2 mA in the vertical axis to facilitate the comparison, but the test was extended to 2.7 kV and the leakage current reached 3.12 mA. On the other hand, in device 04E it was still possible to apply a reverse voltage close to the SOA limite, however the maximum leakage current was 1.16 mA, also very far from the other devices and from the

average value observed by the manufacturer when performing the test on a large population.

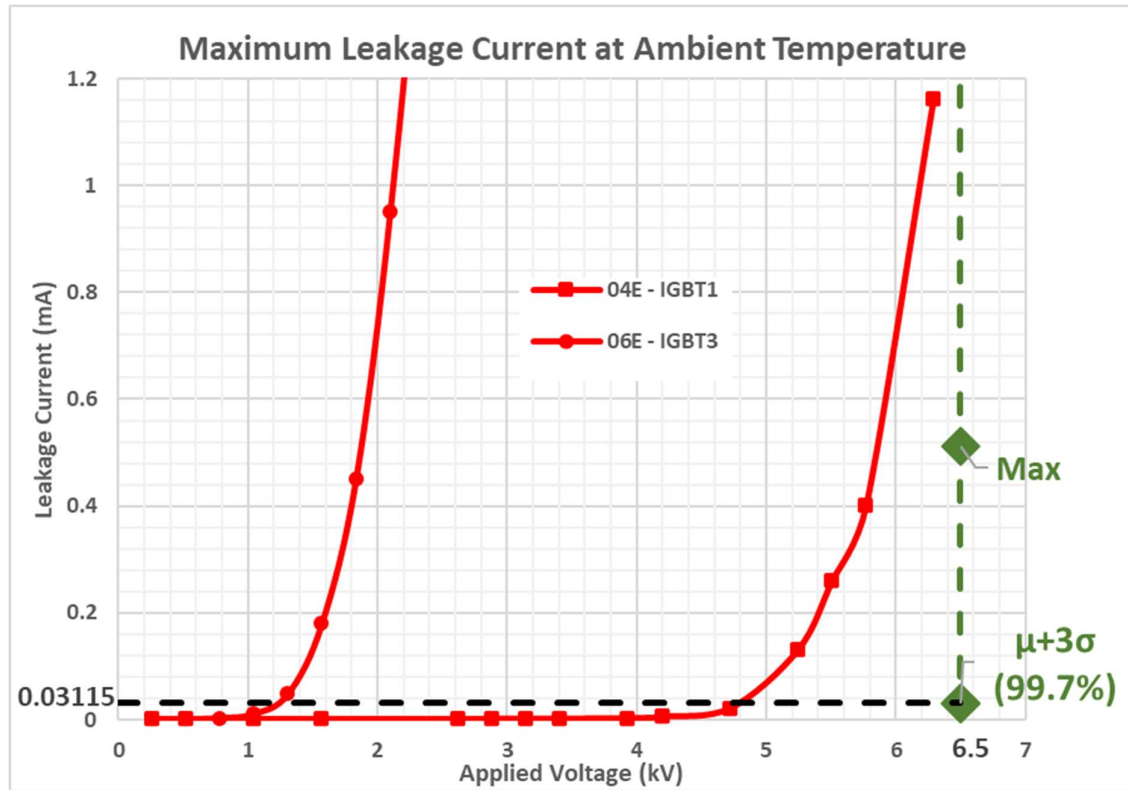


Figure 7.13 Degraded Samples I_{CES} at Ambient Temperature

Figure 7.13 also shows for reference, the maximum value obtained by the manufacturer among the 29457 device units and the value that covers 99.7 % of the population considering the standard deviation informed. The maximum leakage current obtained at 6.3 kV is about 2.3 times higher than the maximum value found among the population, which was by itself very far from the mean value, μ , shown in Figure 7.12 and 16 times the value of $\mu + 3\sigma$. This shows that the interpretation of the leakage current test results is complex and the device can appear to be under acceptable values if it is not tested carefully and under the correct range. In fact, the datasheet maximum value of I_{CES} at ambient temperature is much higher than the values found in [63], and it is not a good reference for a precise comparison when looking for signs of degradation. According to the manufacturer, this happens due to the high margins used for the datasheet characteristics since they are guaranteed values.

Not only the absolute values of I_{CES} for each voltage should be observed when analyzing devices 04E and 06E, but also the derivative of the leakage current

evolution with the applied voltage. Although the standard deviation among the manufacturer tested population was big, the characteristics of the variation of the leakage current with the voltage is given by the dotted black line in Figure 7.12. Furthermore, a stronger electric field generated by higher values of blocking voltage will increase the speed of the carriers in the space charge region, but not the number of carriers. Therefore, the leakage current does not increase strongly with the voltage applied unless the device experiences a breakdown, and the structure is damaged [81]. Testing the devices only at a specific voltage value doesn't give this notion to support the interpretation of the possible degradation.

7.4.2. I_{CES} at Maximum Junction Temperature

As it was observed if tested at high voltages, even the measurements taken at the ambient temperature can spot degradation if compared to the expected values for new units. This can facilitate the execution of those tests on site after a fault. However, while the electric field doesn't create new carriers, the temperature will and the I_{CES} varies considerably with the temperature, [73]. Figure 7.14 presents the leakage current test results using the Hot Plate. Again, a sample curve at 125 °C with intermediate values of applied V_{CE} voltages is plotted for reference [80]. The I_{CES} axis is now in mA to better scale the higher values at maximum junction temperature.

The leakage power loss during the test execution is estimated as the I_{CES} times the collector-emitter voltage [82]. The expected maximum current in the test was assumed to be the maximum value of the reference curve at maximum V_{CE} , i.e., 5 mA*6.5 kV=32.5 W. The temperature to be set in the control was calculated by Eq. (7.3) as 110 °C, considering:

- The FWD thermal resistance only for a worst condition in which all leakage current would be generated in the device of higher thermal resistance.
- Maximum test duration of 30 seconds.
- And again, assuming for worst case condition that all the heat generated during the test for 30 seconds goes to the thermal capacitance of the baseplate and nothing goes to the hot plate.

The temperature to be set in the hot plate and expected values for the device baseplate and junction, considering all current in the FWD, are summarized for the I_{CES} test in Table 7.3.

Table 7.3: I_{CES} Hot Plate Temperature Value and Temperature Estimation

Average Power (W)	$T_{HotPlate}(^{\circ}\text{C})$	$T_{baseplate}(^{\circ}\text{C})$	$\Delta T_{j-c}(^{\circ}\text{C})$
~32	~111	~113	~1

Although degraded and damaged devices will have high currents, the Insulation Tester has a maximum current capacity of 6mA. Besides they will be able to sustain less voltage, thus the power losses during the test are controlled such that the maximum junction temperature is not surpassed, to avoid causing extra damage to the DUT. For the device 06E in Figure 7.7 the maximum power loss under test is 18 W.

Similarly, to what is observed at ambient temperature, the damaged device, IGBT3, among the internal semiconductors of the flat-pack 06E, presented a much higher leakage current than the other devices for a much lower voltage. For higher junction temperature, the applied voltage is higher even in the damaged device, but with such a high leakage current that it reaches the instrument limit.

Device 04E however didn't present the same evident deviation in the leakage current as it was seen at ambient temperature, especially when compared to the other flat-pack devices or the sample unit given by the manufacturer as reference. This can be related to the fact that the leakage current can be modeled as comprising three separated individual components given by Eq. (7.4) [83] [84].

$$I_{leak} = I_{leak(D)} + I_{leak(SC)} + I_{leak(em)} \quad (7.4)$$

Where the last component $I_{leak(em)}$ is called emitter surface leakage current and is the one associated to the degradation. Its value is theoretically zero when the device is healthy and gradually increases with the Si material degradation levels. $I_{leak(em)}$ is directly proportional to the applied voltage, junction temperature, and degradation level.

The other components are the diffusion leakage current $I_{leak(D)}$, related to the parasitic thyristor formed in the PNPJ junction shown in Figure 3.2, and the space charge generation leakage $I_{leak(SC)}$, associated to the minority carriers passing through the depletion layer. These two components are also temperature dependent and increase exponentially with it [32] [73] [84].

Therefore, it is possible that the increase in the diffusion and space charge leakage currents surpassed the one due to the level of degradation that the IGBT1 of 04E reached. In fact, even at ambient temperature the degradation of the IGBT1 was subtle when the results are compared to the maximum value found by the manufacturer for many units tested. On the other hand, for the IGBT3 of unit 06E, the level of damage was so intense that the difference from this semiconductor to the other parallel internal was kept at higher absolute values of leakage current for higher temperatures.

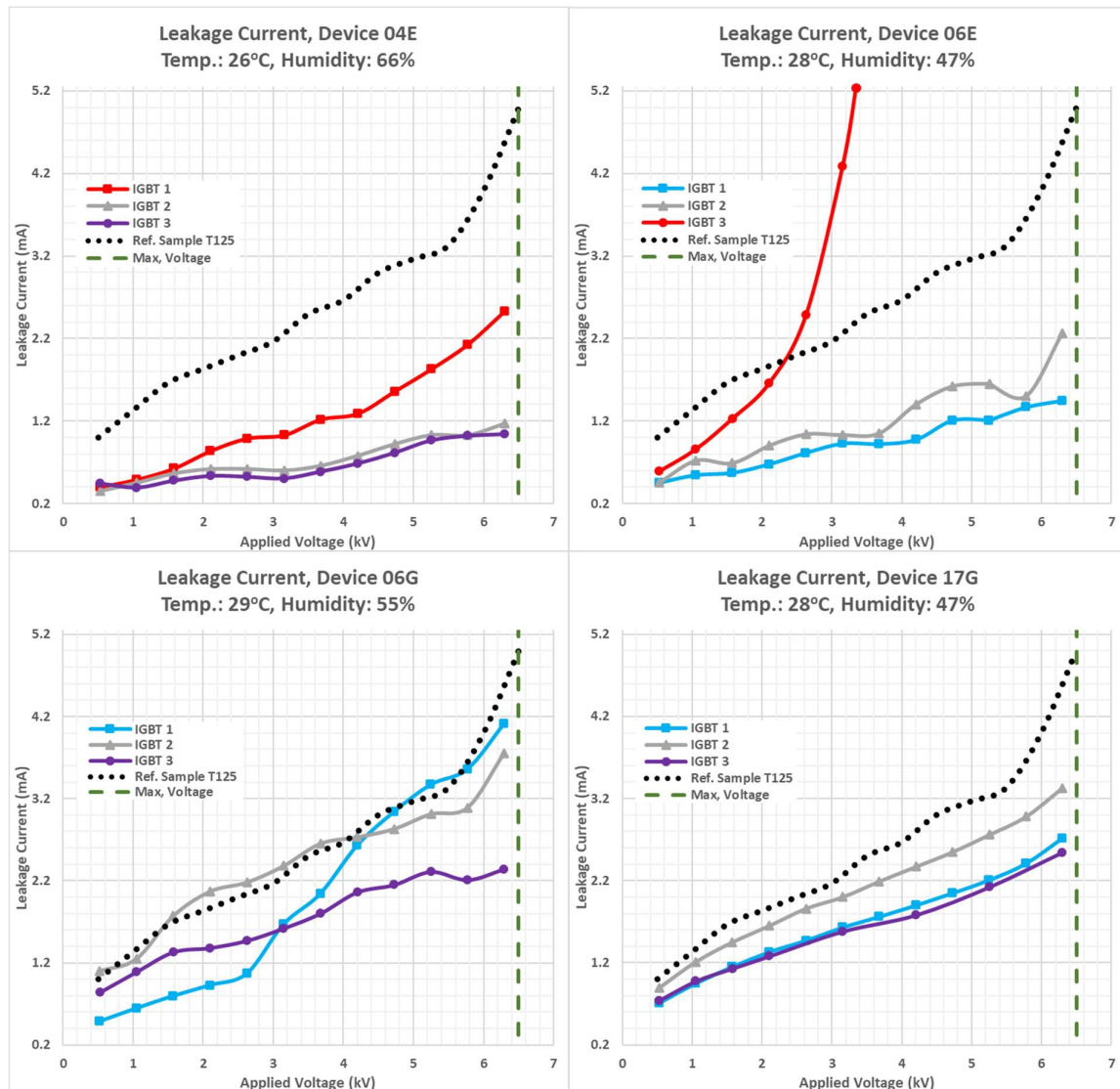


Figure 7.14 Collector Emitter Cut-Off Current Test Results at Maximum Junction Temperature

The tests at ambient temperature were repeated on IGBT1 of device 04E after the tests at high temperature for confirmation. The results are shown in Figure 7.15. Despite of a small difference that can maybe be explained by the higher humidity

when the second test was performed, the results at ambient temperature before and after the test close to maximum junction temperature were very similar.

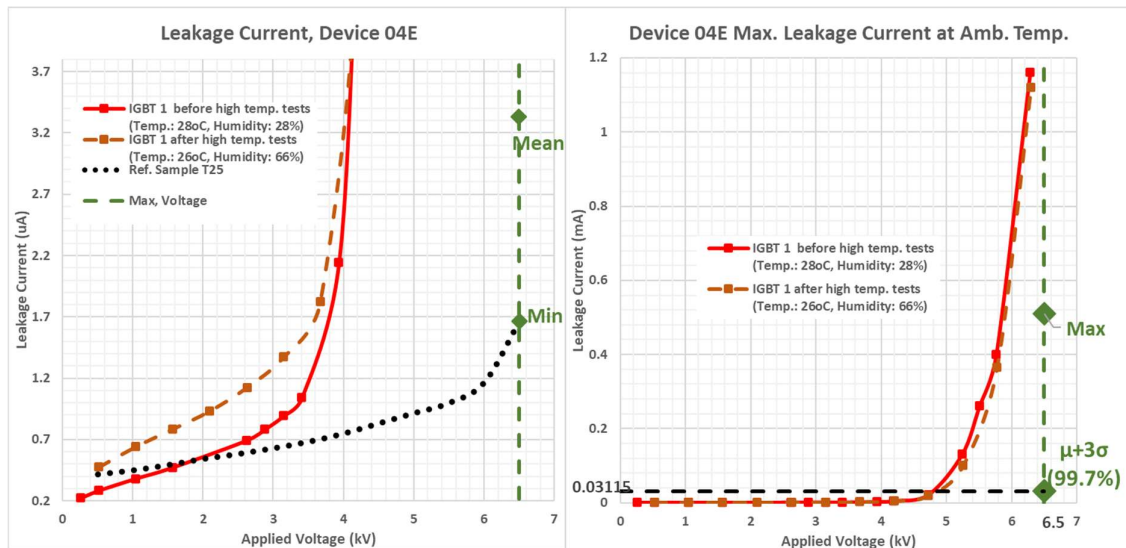


Figure 7.15 Collector Emitter Cut-Off Current Test Results at Ambient Temperature Confirmation for IGBT1 of Device 04E

7.5. Test # 2 – I_f vs V_f Curve

The test setup to obtain the I vs V curves for the FWD and the IGBT using the controlled current source is shown in Figure 7.16.

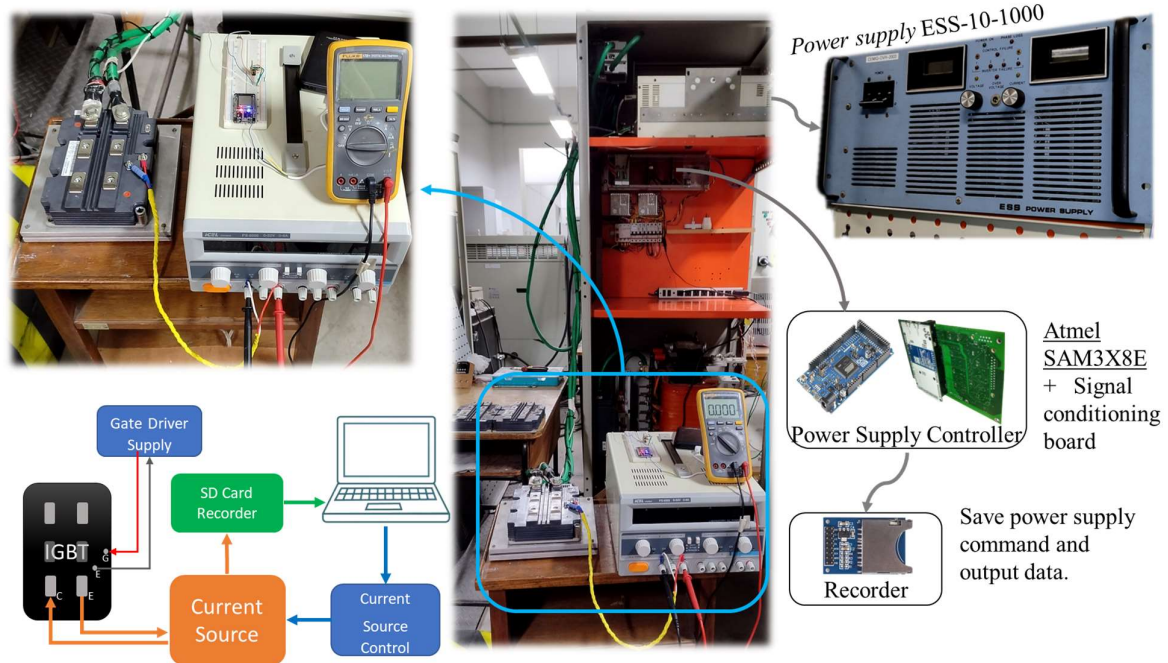


Figure 7.16 Current Power Supply Setup (adapted from [76])

A ramped reference is programmed in the Arduino controller ATSAM3X8E as exemplified in Figure 7.17. The commanded signal and the output data are saved in a recorder.

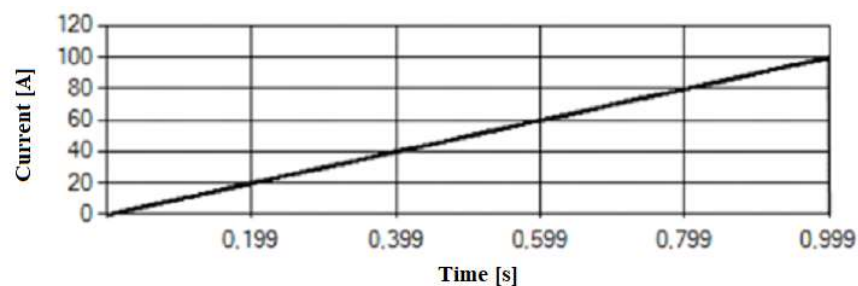
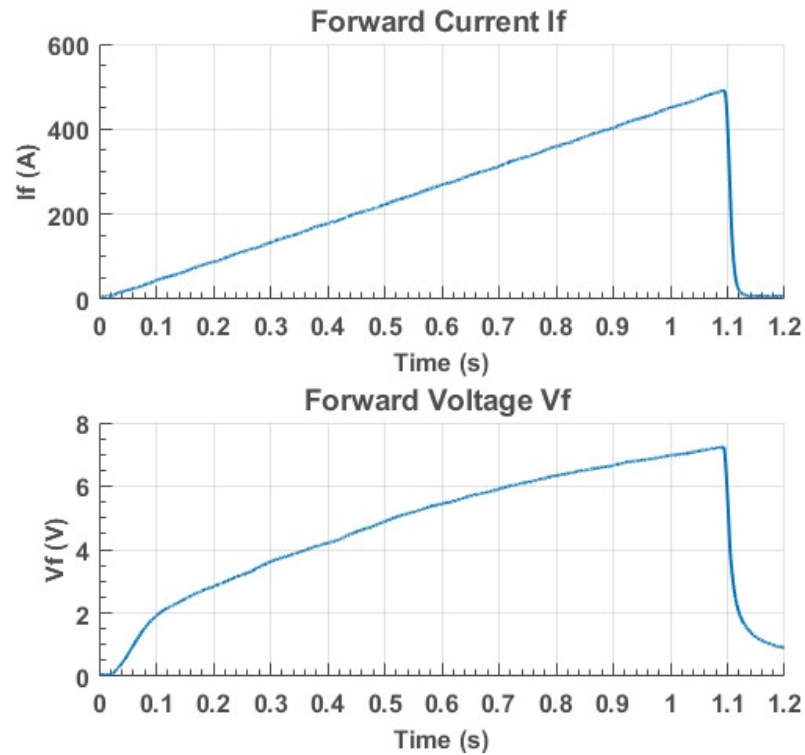
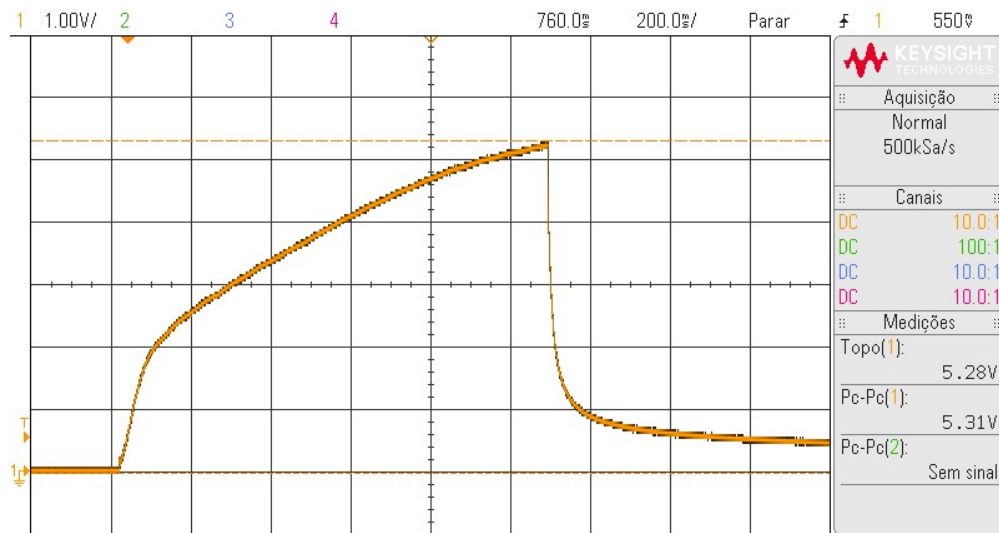


Figure 7.17 Example of commanded reference for the current source to achieve 100 A in 1 s

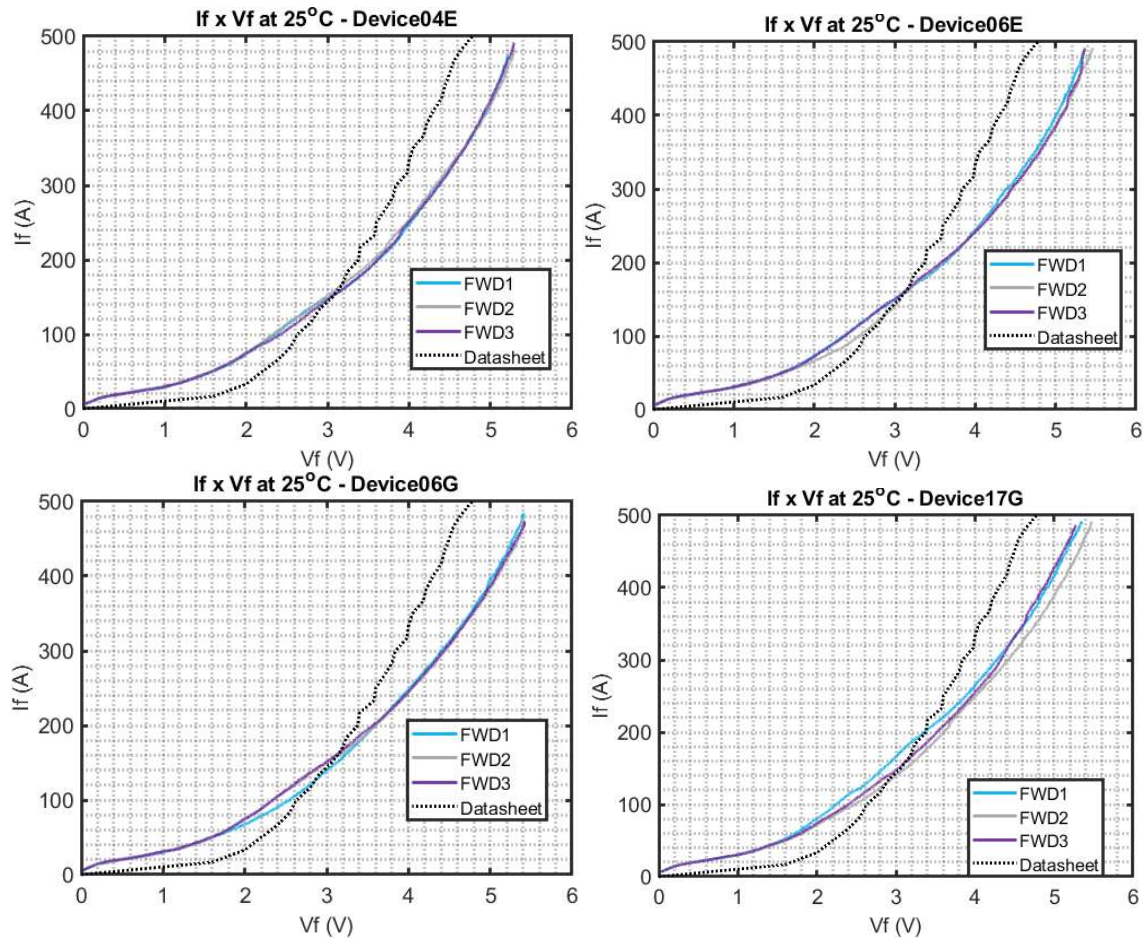
The anode current was imposed and ramped up from 0 to 500 A, limit of each internal parallel FWD in the flat-pack case, with the current and voltage measurements directly given by the current source recorder. Figure 7.18 illustrates the measurements in time given by the current source.

Figure 7.18 Current Source Recorded I_f and V_f

It was noticed that the forward voltage on the diode had an offset when compared to the direct oscilloscope measurement as shown in Figure 7.19.

Figure 7.19 V_f Voltage Recorded with an Oscilloscope

The final values of the forward voltage were adjusted to reflect the actual FWD voltage. Figure 7.20 shows the I_f vs V_f curve for the FWDs inside each flat-pack case compared to the datasheet reference shown by the dotted black line.

Figure 7.20 $I_f \times V_f$ per FWD Device at Ambient Temperature

The average power consumed for the time frame of the test was 1194 W. Using Eq. (7.3), the hot plate temperature would have to be controlled at 53 °C for the junction temperature to stay around 115 °C reserving 10 °C margin to the limit for safety.

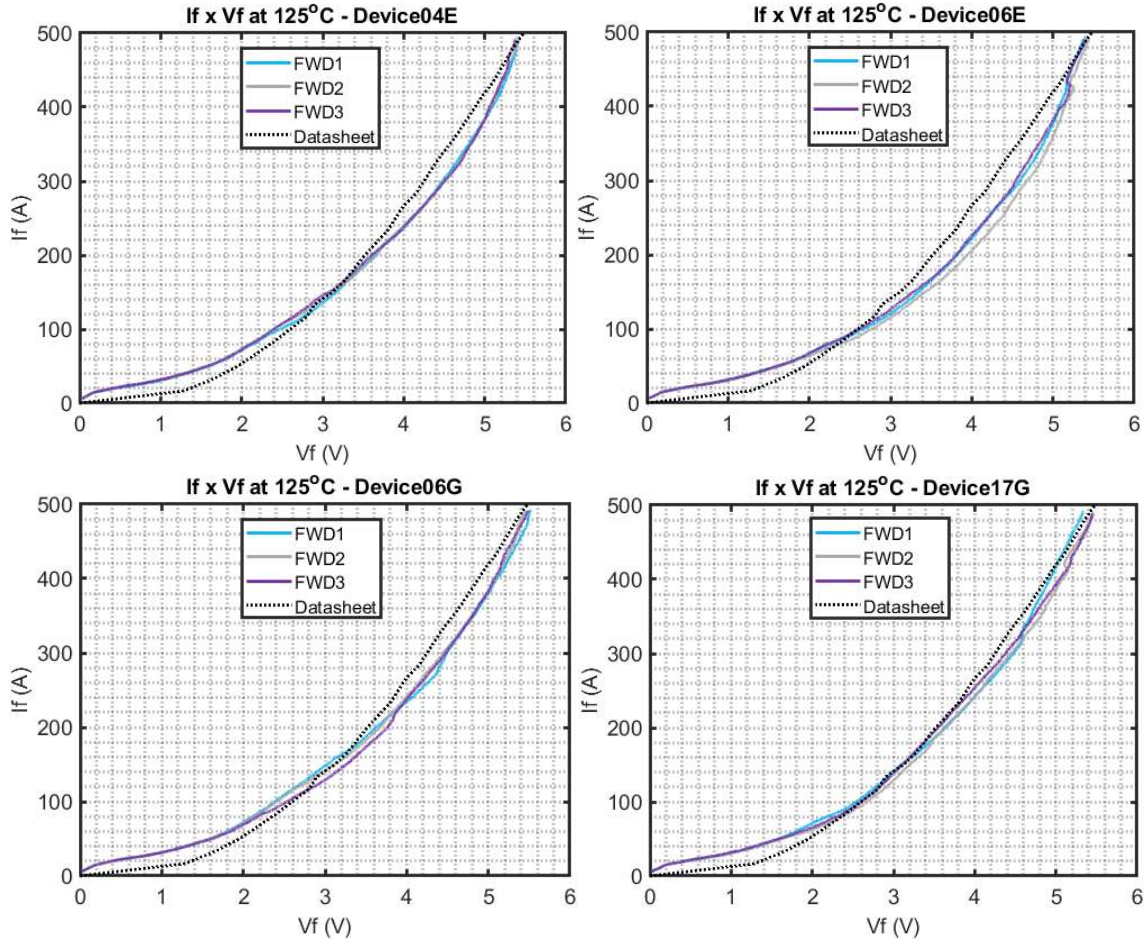
A step of the average power maintained for the test duration of 1.09 s gives the same outcome as the actual power ramp associated with the gradual increase on the forward current and voltages. This way it is easier to see that the Foster Thermal Impedance plot shown in Figure 7.7 is reduced to the FWD thermal resistance shown in Table 7.2. This thermal resistance, three times higher on each parallel internal FWD, gives a temperature difference of 61 °C.

The temperature to be set in the hot plate and expected values for the device baseplate and junction are summarized for the I_f vs V_f test in Table 7.4.

Table 7.4: I_f vs V_f Hot Plate Temperature Value and Temperature Estimation

Average Power (W)	$T_{HotPlate}(^{\circ}C)$	$T_{baseplate}(^{\circ}C)$	$\Delta T_{j-c}(^{\circ}C)$
~1194	~50	~54	~61

Figure 7.21 shows the I_f vs V_f curve for the FWDs inside each flat-pack case compared to the datasheet reference.

Figure 7.21 I_f X V_f per FWD Device Close to Maximum Junction Temperature

It is possible to observe that, despite the high current circulation observed in the FWDs described in Section 5.2.3, there is not much impact in the forward conductivity capability of the internal diodes of each device case. All units presented similar results demonstrating consistent aging process. The deviation from the reference curve is not as relevant as the ones observed in the leakage current at ambient temperature for the damaged device 06E or the degraded one 04E.

7.6. Test # 3 - I_C vs V_{CE} Curve and Transconductance

The I_C vs V_{CE} curve was obtained similarly to the procedure executed in test #2, with the same current source setup. For each internal parallel IGBT, the The curve was obtained with the IGBT turned ON for different gate voltages, always higher than its threshold voltage of 6.8 V for new units according to [30]. Figure 7.22 shows the current source measurements for the IGBT1 of device 17G, when 11 V is applied to the gate. The saturation seen at 0.86 s happens because the ESS-10-1000 power supply is a voltage controlled current source with an output voltage limit.

The saturation on the V_{CE} voltage helps to limit the losses during the test. When the IGBT goes in the active region, the collector current slope is very small and any small variation in the current could lead to a very high correspondent V_{CE} voltage.

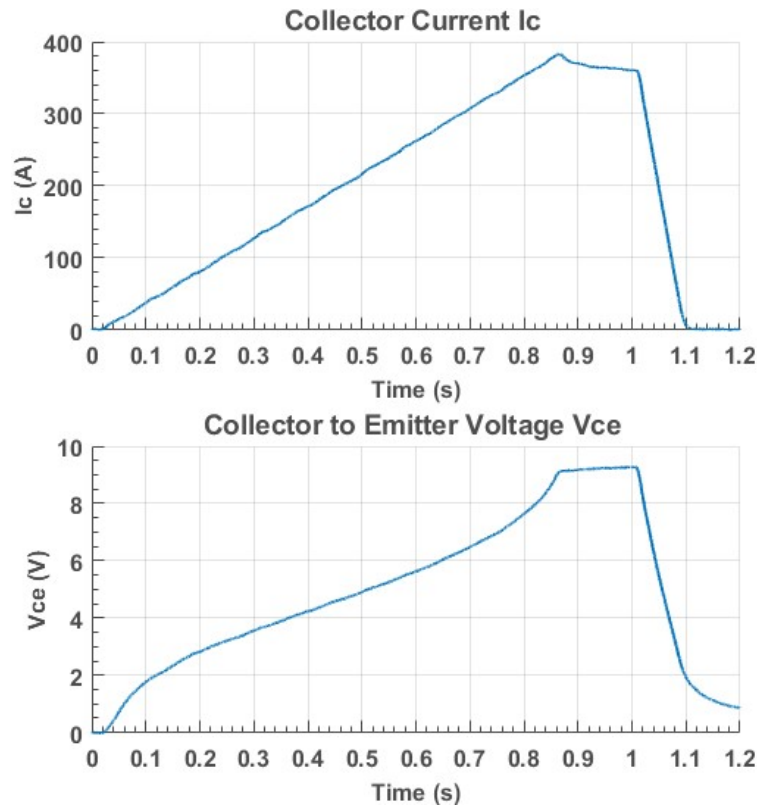


Figure 7.22 Current Source Recorded I_C and V_{CE} for $V_{GE}=11V$

The current source is controlled in closed loop to maintain the desired load current based on the control circuit voltage reference and measurement [85]. When the source reaches its saturation, V_{CE} will be limited and the current would be the maximum driven by the IGBT for the specific gate voltage.

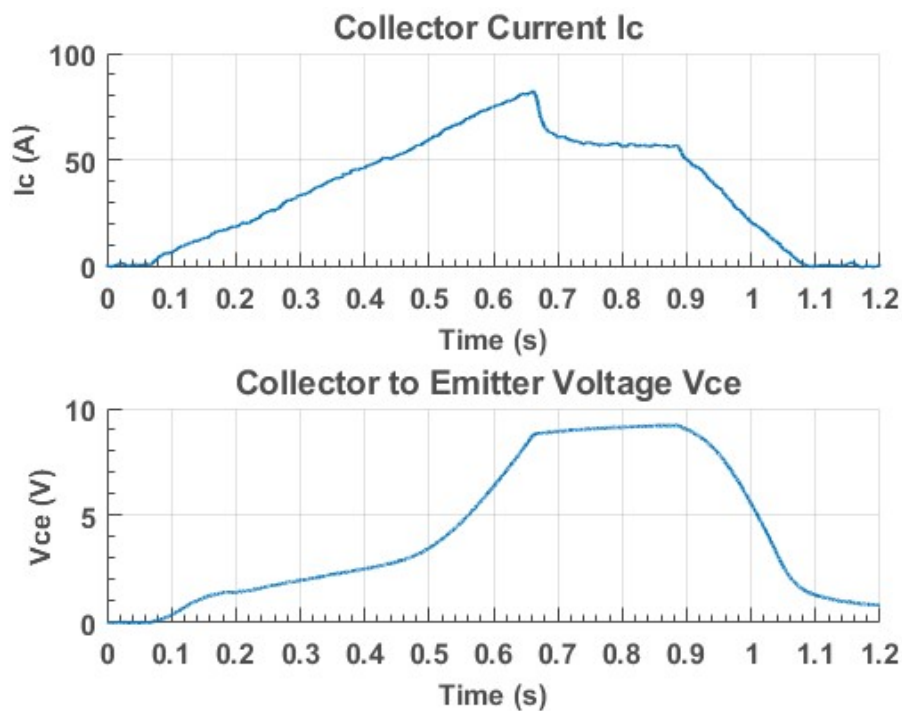
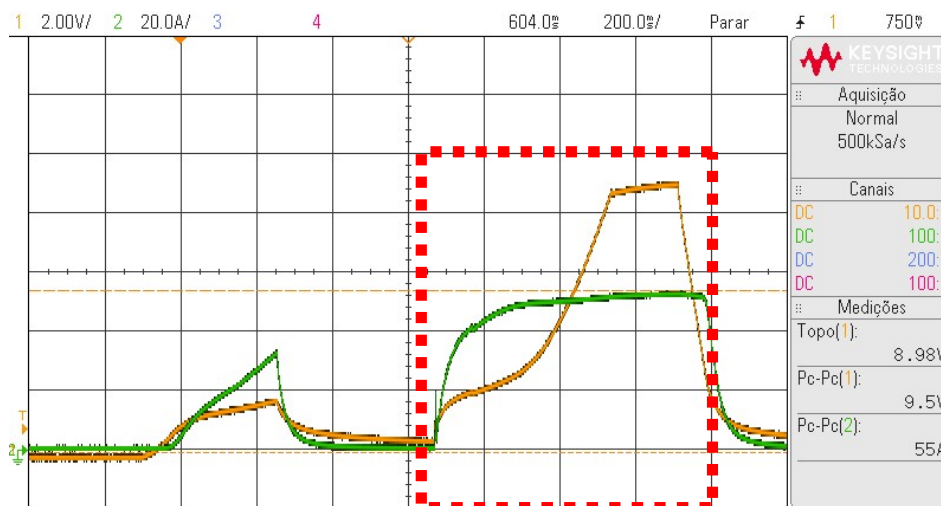
Figure 7.22 does not present the transition from the saturation region to the active region and the pinch-off voltage as it would be expected from Figure 3.10, instead, the current reaches a peak value and then drops to a lower value when the saturation is reached. It is important to highlight that this behavior is due to the power supply saturation and not the IGBT. As shown in Figure 3.10, the pinch-off voltage for $V_{GE}=11$ V is around 5.5 V.

Figure 7.22 shows the results taken directly from the current source recorder. For comparison, the measurements from the current source recorder and from an oscilloscope measuring directly the V_{CE} voltage and the collector current at $V_{GE} = 8$ V are shown in Figure 7.23 and Figure 7.24, respectively. The power supply applies an initial pulse shown in Figure 7.24 that is not relevant to the tests and can be disregarded. The second pulse highlighted in red is the one to be considered.

When directly measured by the oscilloscope in the IGBT the collector current has the expected waveform. The pinch-off happens around 2 V of V_{CE} and from that point on, any small increase in the collector current, makes the V_{CE} voltage increase fast in the active region, until the output voltage limit of the current source is reached.

The external current probe used for the oscilloscope current reading was limited to 100 A what prevented its use for the entire range of magnitudes that needed to be tested, thus the I_C vs V_{CE} final results with a new external conditioning signal recommended as a continuation of the work in Section 8.1. On the other hand, the current source recorded data was sufficient to extract the transconductance curve, since after reaching the limitation, the DUT will be in the active region and the pinch-off voltage is guaranteed, $V_{CE} > V_{GE} - V_{th}$, and the collector current depends only on the gate voltage and the transconductance gain.

The tests were not executed for 15 V of V_{GE} voltage since the manufacturer does not indicate the IGBT behavior in the active region for this value. As indicated in Section 3.3.3, this current is estimated as 2.3 times the current limit of the SOA, $I_{Cp} = 1500$ A, and configures the IGBT behavior under short-circuit. Not only the lab. current source model used wouldn't be able to reach this value, but it could also cause further damage to the IGBT.

Figure 7.23 Current Source Recorded I_c and V_{ce} for $V_{GE}=8$ VFigure 7.24 I_c (Green) and V_{ce} (Orange) Measurements with an Oscilloscope for $V_{GE}=8$ V

The transconductance curve at ambient temperature for each device and per internal IGBT inside the flat-pack case is shown in Figure 7.25. A reference datasheet curve, extracted from Figure 3.10, is also plotted.

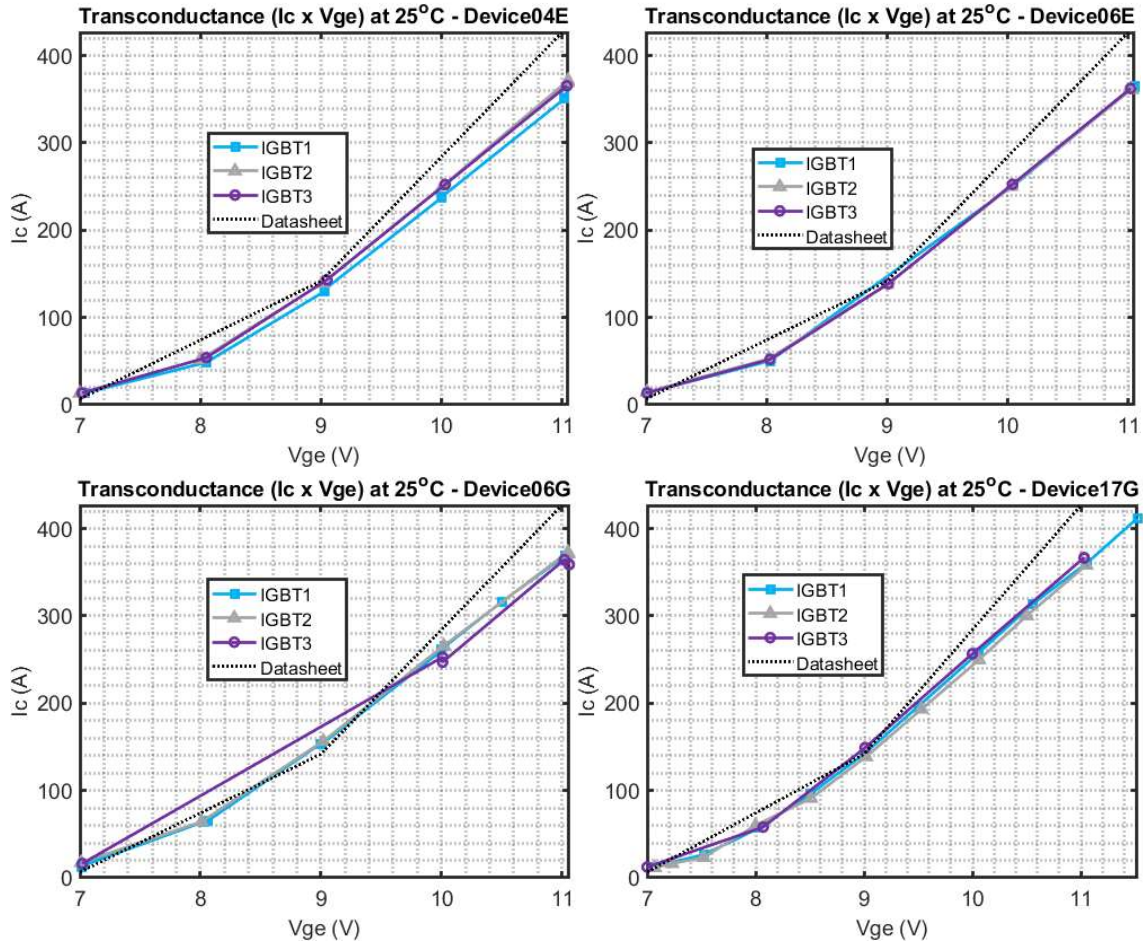
Figure 7.25 Transconductance Curves ($I_c \times V_{ge}$) per Device at Ambient Temperature

Table 7.5 presents the collector to emitter voltages reached on each device test. The mean and standard deviation values on each test are shown to demonstrate the proximity of the V_{CE} voltage among all test results, guaranteed by the current source in saturation.

Table 7.5: Arithmetic Mean and Standard Deviation in V_{CE}

Device	V_{CE} (V)	
	Mean	σ
04E	9.335	0.048
06E	9.342	0.009
06G	9.313	0.025
17G	9.275	0.044

The controlled temperature for the Hot Plate is calculated for each gate voltage. As an example, at 11 V the average power consumed for the time frame of the test was around 1265 W, taken from Figure 7.22. Each internal IGBT thermal

resistance gives a temperature difference of 34 °C from the junction to the case. The effect of 1s of the average power applied to the baseplate thermal capacitance would give a voltage difference of 4 °C to the hot plate. Again, the dynamic thermal impedance of the IGBT can be disregarded.

For a target junction temperature of ~115 °C, the temperature to be set in the hot plate using Eq. (7.3) and the estimated maximum temperature of the baseplate due to its thermal capacitor are summarized for the transconductance test in Table 7.6. Note that only the main gate voltages are listed, but the temperature set was interpolated for intermediate values of the gate voltages applied.

Table 7.6: Transconductance Test Hot Plate Temperature Value and Temperature Estimation

V_{GE}	Average Power (W)	$T_{HotPlate}(^{\circ}\text{C})$	$T_{baseplate}(^{\circ}\text{C})$	$\Delta T_{j-c}(^{\circ}\text{C})$
7	~92	~112	~112.5	~2.5
8	~216	~108	~109	~6
9	~461	~101	~103	~12
10	~922	~87	~90	~25
11	~1265	~77	~81	~34

Figure 7.26 shows the transconductance curve for the junction temperature close to its maximum. Again the datasheet curve, extracted from Figure 3.10, is plotted for reference.

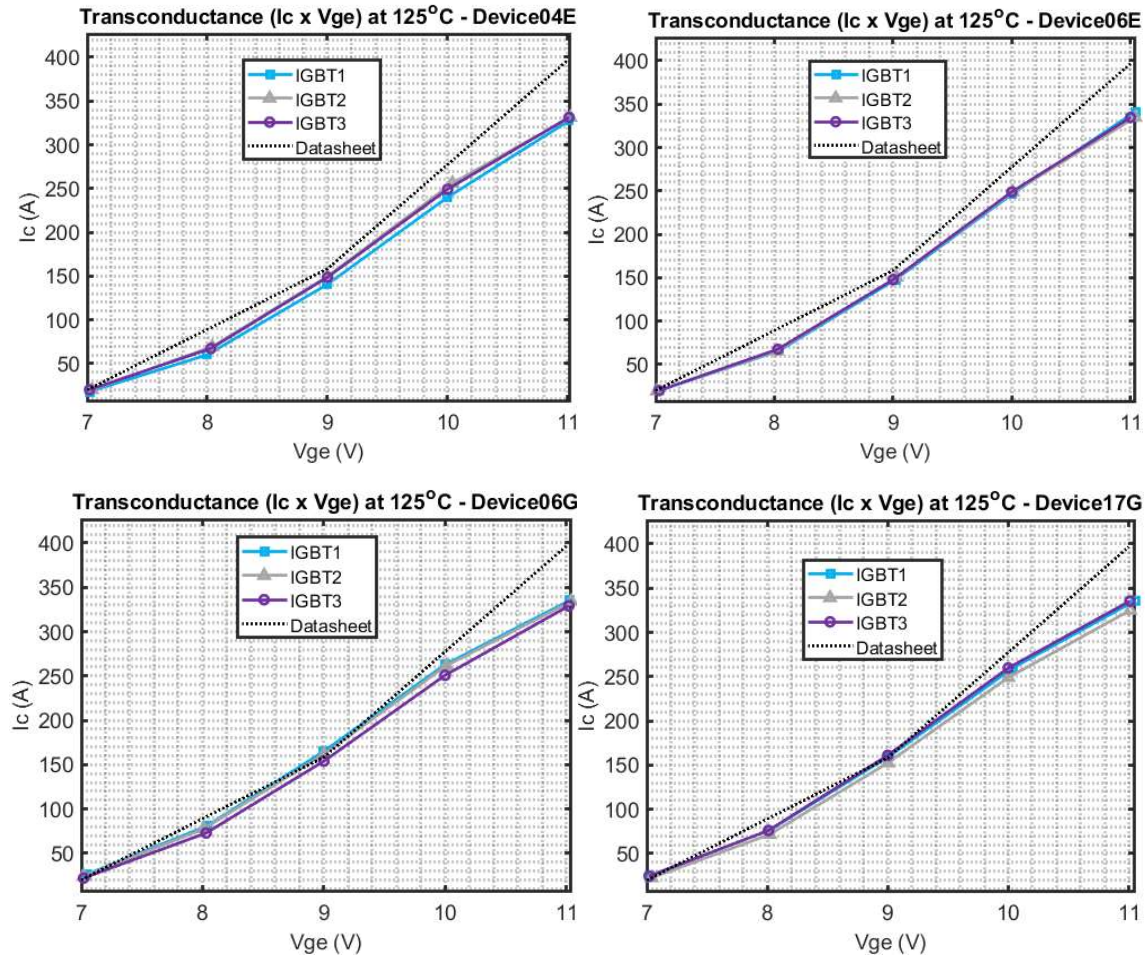


Figure 7.26 Transconductance Curves ($I_c \times V_{ge}$) per Device Close to Maximum Junction Temperature

In the saturation or linear region, the collector current is expected to be higher for aged devices as it can be seen in Figure 6.16. However, the results reveal that the transconductance wasn't strongly affected by the Fault #2. The curves were very close to the datasheet reference with a slightly lower slope.

7.7. Conclusions

This chapter presented the results of offline / off-circuit tests performed in 4 sample devices chosen after the analysis of the second fault in Chapter 5. The tests were performed in laboratory and indicated a damaged device and a degraded one, confirming the previous results. The tests were performed in each internal parallel semiconductor inside the flat-pack case for comparison. To apply high current, a controlled current source was used, while an Insulation Tester with higher than usual current capacity was chosen for the high voltage tests. Only the leakage current test was able to indicate the degradation while the transconductance and the I vs V curves were very similar for all units. It was interesting to observe that the parameter shift was similarly noticeable close to the maximum junction temperature and at ambient temperature, what characterizes the leakage current test as a worth doing tests on site or factory even without the hotplate structure crated in laboratory. Nevertheless, the test must be executed with the device disconnected from the circuit and with the gate driver disconnected. Besides, one should be careful in the interpretation of the results since the standard deviation found among units tested by the manufacturer and brought here as a reference is high. The deviation is more evident when voltages close to the maximum value are applied and when the derivative of the leakage current variation is considered, yet the person executing the test also needs to be careful to not pass the SOA limit and further damage the device while doing it.

Chapter 8. Conclusion

This work discussed the impact on the reliability of medium voltage converters after a fault event in a phase module, in which the faulty module is replaced but the others are only tested by simple in-circuit tests using a multimeter. It is demonstrated that the faults can have escalated consequences and affect the flat-pack IGBT components placed in other phase modules. The components may not completely fail, but rather present a degradation that is not evident leading the users to keep those modules and resume full operation. The component will be pushed out of the random failure period of its bathtub curve and the overall MTBF will be diminished by the lower MTBF on the degraded component. Therefore, although the modular design gives the advantage of diminishing the MTTR by allowing the fast replacement of the faulty module, the availability of the converter after the return to operation will be shorten, jeopardizing the plausibility of the common assumptions that the failures are independent and contained inside the module that give the main benefits of the modular design for segregation of parts in the converter panel and maintenance strategies.

The damage spread happens mainly because of the high energy event formed inside the phase module, i.e., the flat-pack devices failure leading to half or full DC link short circuit faults. The basic monitoring and protection internal to the phase module, the V_{CE} desaturation, is provided by the gate driver, which is reactive to the formation of the short circuit current. With the current already established, the interruption process tentative is sensitive and dangerous by itself since the turn-off process under high current generates high overvoltage due to the stray inductances between the IGBTs and the DC link, as detailed in Chapter 3.

Although in general the other phase modules would be checked after a fault, the offline in-circuit tests performed with a multimeter won't be able to detect the level of degradation observed in this study. The alternative proposed here is a methodology to estimate the overstress and degradation in power semiconductor devices after a fault that consists of two main paths: the fault analysis, modeling and simulating the system and using actual fault plots, and the evaluation tests that must be conducted in all IGBTs in the converter after a fault with the devices disconnected

from the circuit and from its gate driver. The procedure is applied to a case of study of two consecutive faults that happened in a real application of a MV NPP converter.

The first fault is explored in this work, mainly to give the history of the possible fault spread effects that were not completely addressed after the drive operation was restored. It is demonstrated that it is very likely that a degraded IGBT was reused and led to the second fault. More detailed tests are performed on IGBTs that were installed after the first fault and experienced only the second one. The results prove that the effects of the back emf and the oscillations due to the stray inductances can create alternate paths for the short circuit current and stress the components in other phase modules. In fact, these unideal conditions can degrade the components up to a point that it would still pass the normal test, but with large deviations in the expected values of the failure precursor parameters.

The application of the methodology to the second fault showed that the phenomena most likely to affect the other phase modules is the full DC link short circuit that creates a characteristic resonance between the dc capacitors and the stray inductances, explained in Section 5.2.3. The overcurrent is seen by the FWDs in the vertical arms of the NPP topology of all phases, they can lose their properties and increase much the expected leakage current. The characteristics of the fault as a singular event of high power emphasizes the benefits of the modeling and simulation developed as a tool to understand the degradation under the perspective of the PoF, since the regular rainflow counting algorithms are based on repetitive power cycles.

The proposed off-line / off-circuit tests complemented the analysis. They were able to spot a degraded device that was still able to sustain high voltages, but that presented a large deviation on its leakage current when turned OFF. The database created from the interactions with the manufacturer allowed the correct interpretation of the results when compared to new units, since the information in the datasheet was insufficient for a deeper analysis. It was found that although the leakage current has a large range of values considered acceptable for healthy units, devices Q4 of L2 in Table 5.1 had an evident parameter shift in the I_{CES} confirmed by detailed laboratory tests in Section 7.4. The deviation was masked when the test was executed with the device close to the junction temperature, but was remarkable at ambient temperature, what can be convenient for tests on site or shop floor.

Although the leakage current tests are not able to distinguish if the degraded device is the IGBT of the FWD, combining the findings of this test with the overstress

in the diodes estimated by the fault model and simulation can indicate that the actual deterioration is in the FWDs. There is no active protection strategy that can be used to control this reverse current and all modules connected in parallel with the DC link can be damaged. The magnitude of the current will depend only on the DC capacitance, the loop stray inductance and the resistances in the DC bus to phase modules circuit formed with the FWDs.

The methodology proposed here can be used as a tool to help in the after-fault decision making by providing a way of identifying the affected phase modules and avoiding reusing degraded devices. For instance, the magnitude and paths of the short circuit current obtained with the simulation provide the understanding on what devices were overstressed. However, the suggested tests are more complex than the ones that are normally performed with a multimeter to check the IGBTs states when conducting or blocking. Although the tests can spot deviations in the precursor parameters even at ambient temperature what facilitates its execution, they still require the disassembly of the IGBTs from the converter circuit and its gate drivers.

This methodology is also limited in fully understanding the impact of the degradation in the IGBT lifetime expectancy, which could support even further the decision to reuse the devices. The precursor parameters, the tests defined, the magnitude of the results found and the behavior of the short circuit current shown by the fault analysis and simulations can be used as a base in a future work to explore the online continuous monitoring of the IGBTs and estimating the remaining lifetime expectancy after a fault, as detailed in Section 8.1.

Finally, the findings of this thesis show that in case of short-circuits inside the phase module, mainly the ones involving a full DC link short circuit, special care should be taken with the devices of the other phase modules that are not apparently involved with the fault. It is demonstrated that the effects of a fault can extrapolate the phase module in which the short circuit was initially created and degrade devices in other phase modules on the AFE and MB sides. Only performing simple in-circuit tests after a fault can mislead into the interpretation that the devices can be reused, especially for insulation tests performed with the gate driver connected since it will lower the normal equivalent insulation resistance due to its own C-E lower resistance in parallel.

The modular design still offers many advantages for the product realization of a converter, like the standardization of the subassemblies that can simplify the

manufacturing process and costs. Furthermore, having enough spare modules can still be a way of resuming the converter's operation after a fault while the detailed after-fault evaluation proposed in this work is separately performed.

8.1. Future Work

Among the precursor parameters discussed in Chapter 6, it was possible to evaluate in this work the leakage current, the transconductance from the I_c vs V_{CE} curves and the I_f vs V_f curve of the FWD at ambient temperature and close to the maximum junction temperature.

Although a large deviation was only observed in the leakage current at ambient temperature for the degraded device, a sequence of complementary tests is planned as next steps to verify if the devices will continue to present minor change in the other precursor parameters. The further tests planned are listed next, they will be performed at ambient and at maximum junction temperature:

- I_c vs V_{CE} curve with a new external conditioning circuit for the current measurement, comprising a shunt resistor sensor and an amplifier board. The improvement will overcome the issue with the direct reading given by the power supply explained in Section 7.6.
- The test will be repeated for a small gate voltage being gradually increased until the devices start to conduct to evaluate the impacts on the threshold voltage.

Once all tests are performed, the intention is to open all flat-pack cases and analyze each device internal structure, removing the internal silicon according to the procedure given by [66]. After identifying the main points of interest, a defined area of the device will be selected for deeper inspection of the impacts in the structure with the aid of a metallographic microscope.

Furthermore, it is recognizable that understanding the converter conditions prior and after the fault can become more precise with the two main proposals that can be derived from this thesis and are described next.

8.1.1. IGBT Remaining Lifetime Expectancy

Typical lifetime models don't suit the type singular stress to which the power semiconductors are submitted because of the fault spread discussed in this study, because they are based on the stress generated by power cycles and mostly predict only two failure mechanisms, the bond wire failure, and the solder fatigue [86] [87]. Therefore, the findings of this work can contribute to extend the coverage of the lifetime models so that it can support the decision of what components will be exchanged and what could be kept in the converter.

There is an ongoing negotiation to send the other IGBTs listed in Table 5.1 as donation for R&D purposes in the TESLA laboratory. Many devices still show a high equivalent insulation resistance between Collector to Emitter and the simulation showed that some were not submitted to abnormal conditions, e.g., devices Q5 and Q6 in the horizontal arm of the AFE modules. Further investigation could be conducted on those extra power semiconductors to obtain a valid model for lifetime expectancy and expand the damage prognosis methodology proposed. A possible path could be the replication of the fault conditions trying to create a similar degradation to later submit the degraded components to power cycles under the rated conditions to verify the impact on the expected lifetime.

8.1.2. Online In-circuit Monitoring

Checking the precursor parameters online and without having to disassemble the devices from the converter, instead of performing the offline tests, can bring of great advantage for predicting a failure. Being continuously able to spot the deviations could be a way of automatically stopping the converter operation before the short circuit is formed or for the user to be advised of the probable time to fail, if combined to the lifetime expectancy models described in the previous section.

The real-time measurement of the condition of the component is known as CM (Conditioning Monitoring). Since the precursor parameters are small in magnitude when compared to the rated operation values and due to the noisy environment created by the IGBT switching, they are difficult to accurately extract during the converter operation [29] [88].

The behavior of the precursor parameters for the testes performed in this research and the points of overstress identified by the fault analysis can contribute to the challenges of developing an efficient smart gate driver for the online on-circuit monitoring. Since the collector cutoff current was the affected parameter by the faults analyzed in this work, the online chip-related aging monitoring method for IGBTs based on the leakage current proposed by [84] can be a starting point for further development of a similar strategy for medium voltage devices.

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Appendix A – IAS 2023 Paper [89]

Fault Modeling and Reliability Impact Analysis of Modular Design in Medium Voltage Converters

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Abstract - Modular design is largely applied to Medium Voltage Converters aiming to provide an easy way to replace a set of damaged devices after failure events, allowing a fast restorage of the operation. Arranging the semiconductors into converter phase modules for instance, allow the system to be taken out of operation only for the defective phase module replacement, which can be send to the supplier for repair. However, the indication of the failed semiconductors inside the phase module is usually only given by the gate driver and simple in-circuit tests performed with the aid of a multimeter during the downtime. In this paper, it is demonstrated that a failure occurring in one flatpack IGBT power semiconductor of any phase can cause escalated consequences and basic tests might not be enough to spot degraded devices in other phase modules. This is performed by the modeling, reproduction, and analysis of two consecutive faults in a real case application of a three-level medium voltage converter. Furthermore, additional post-fault offline tests are performed in flatpack IGBT samples that apparently survived the real case fault. The results reveal a relevant parameter shift that support questioning the benefits of the modular design. The deteriorated power devices might not fail immediately, but they will have a shorter lifetime expectancy impacting the overall reliability leading to a subsequent fault of likely greater consequences.

Keywords— *Fault Analysis, IGBTs, Post-fault Diagnosis, Degradation, Parameter Shift, Failure Prognosis, Reliability.*

I. INTRODUCTION

The use of Medium Voltage Converters is commonly associated with critical loads, i.e., those necessary to sustain production or to reach the main mission of an application [1]. The current vast use of MV converters in the steel industry is an example of its importance for the continuity of the production chain. The converters are present in all kinds of steel mills, run-out tables, coilers/uncoilers, and pinch roles. More specifically, since 1980, with the advancement of the semiconductors capability to sustain higher voltages and currents, the VSIs (Voltage Source Inverters) with self-commutated power semiconductor devices, like the IGBTs became the trend [2].

The converters allow the refined control of the production, reducing waste and improving the quality of the final product. Furthermore, they reduce the energy consumption, which is responsible for around 20% of the total cost of manufacturing steel. On the other hand, since steelmaking is a continuous

process, failures or unpredicted maintenance in the VSIs can lead to the shutdown of the entire plant. The cost of the downtime can reach hundreds of thousands of dollars per day depending on the production capacity. [3] [4]

Within this framework, the modular design is often adopted to reduce the MTTR (Mean Time to Repair) and help the fast retrieval of the operation. A part of the converter that is commonly built using the modularity concept is the converter phase module. It comprises the IGBTs, heatsink, snubber components and gate cards for each phase of the converter and are mechanically designed to be easy to remove and reconnect. They are referred as phase modules in this text to avoid confusion with the term power modules used for the flatpack semiconductors. One of the goals of the converter phase module design, is the ease of having spare modules that can replace the defective ones in case of a fault.

Nevertheless, this concept is based on reliability studies and prediction methods assuming that the failures are insulated and disregarding the failure interactions among components and with external factors [5]. Each possible phase module fault is usually treated as an independent event such that the overall reliability is the product of each individual success probability [6]. The determination of the phase module that needs to be replaced hinge on the fault indication coming from the gate driver, visual inspection and simple in-circuit tests that are performed with the help of a multimeter like applying individual pulses and checking the continuity/open circuit indication in the IGBT and the FWD (Freewheeling Diode).

The investigation developed in this work demonstrates that the post fault damage is not always contained inside the failed phase module as usually assumed. For that, a real case of two consecutive faults in the same three-level VSI converter is analyzed, Sections IV and V, under the PoF (Physics of the Failure) methodology presented in Section II, giving evidence that the second fault, here referenced as Main Fault, happened due to the reuse of phase modules with semiconductors that were degraded in the first fault.

The overstress in the semiconductors of different phase modules is evaluated by the study of the measured data and fault graphs complemented by the results of a simulation model in which the second fault is replicated. The subsequent fault current paths created by the interaction of the motor back emf, DC link capacitors and the converter stray inductances are explored, and the affected devices are tagged. Further

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offline tests are carried out in IGBT samples that experienced only the second fault. The results, presented in Section VI, show large deviations in the Collector to Emitter leakage current when compared to new units.

II. DAMAGE PROGNOSIS METHODOLOGY

Damage accumulation can be estimated through the number of power cycles under the operation conditions of each application. Statistic models and rain flow algorithms considering temperature, frequency, and current variations in the wire bonds can evaluate the expected remaining lifetime after a period of operation hours, [7]. However, since it is based on the repetition of the power cycles, this methodology is not able to compute the acceleration in the aging process due to a single and fast external unexpected event. In this case, the device experiences a high temperature variation over a short time caused by the short circuit current. The abnormal conditions and overstress accelerate the wear-out process. [8] [9]

The methodology proposed here is based on the PoF approach and derived from the hybrid Prognostic and Health Management (PHM) given by [10]. It explores the failure mechanisms and physical parameter variations that can lead to the fault. However, instead of accelerating the aging process in laboratory, the semiconductors submitted to the real fault are used. The process flow is shown in Fig. 1.

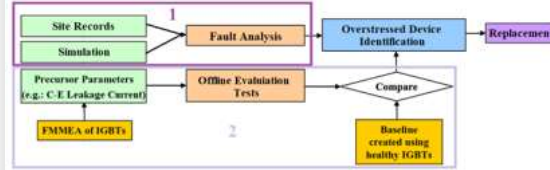


Fig. 1 - Damage Prognosis Methodology (adapted from [10])

In the fault analysis the focus is not on the most damaged phase module that initiated the fault and would be replaced, but rather in the fault spread and the estimation of the stress in the devices of the other phase modules. The investigation is complemented by the offline tests and comparison of the results with expected values in new units. The leakage Collector to Emitter current in OFF state is demonstrated here as an example of the parameter shift caused by the fault spread. The information obtained from interactions with the IGBT manufacturer and measurements of new IGBT units is used to create the baseline for comparison since the initial data available in the datasheet is not precise enough.

Online monitoring of the precursor parameters, as also included in [10], can provide a continuous estimation of the overall reliability during the converter operation. Nevertheless, it is left as a future work proposal since it requires very sensitive measurement strategies to spot variations in parameters of small amplitude under a high absolute value of voltages and currents in the MV converter, but, at the same time, sufficiently shielded to not be influenced by surrounding noisy environment due to switching, [11].

III. CONVERTER CIRCUIT AND PROTECTIONS

The case of study involves two subsequent faults that happened in a 6 MVA, 3-level, VSI assembled with flat-pack IGBTs. First there was a fault on the AFE (Active Front End) side verified to be due to an issue in the input filter assembly. Later, after the converter restoration, a second fault was

registered with evidence pointing to the failure of an IGBT that was deteriorated by the first fault. The impacts of this last fault are analyzed, and extra signs of degradations are recognized in brand new IGBT units that were submitted only to the second fault.

A. Phase Module Topology

The converter phase modules are arranged in NPP (Neutral Point Piloted) topology with 2 series IGBTs in the vertical arms, as presented by [12]. Fig. 2 shows the phase module circuit and an example of switching states to apply $V_{DC}/2$ with a positive current into the load. The representation of the switching states will be simplified by a 4 digits number taking advantage of the fact that IGBTs T1&T2 and IGBTs T3&T4 receive the same firing commands. The letter Q will be used to reference the whole flat-pack frame comprising the IGBT (T) and the FWD (D).

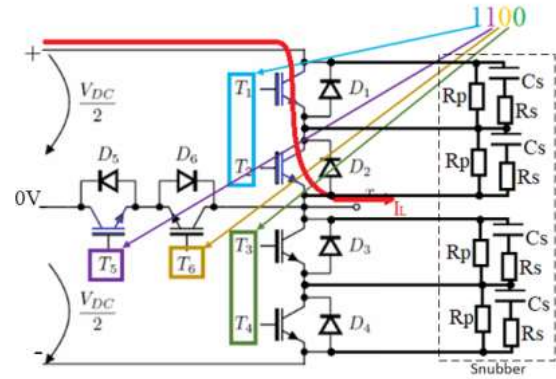


Fig. 2 – 3-level NPP topology and 4 Digits Representation for Switching States. Example of state 1100 with $i_L > 0$ (adapted from [13]).

TABLE I. summarizes the switching states and shows the devices that commute depending on the load current sign. To support the analysis in the next sections, it is important to remark that although the maximum switching voltage seen by the vertical IGBTs is half DC link divided by two or $V_{DC}/4$, the maximum blocking voltage is $V_{DC}/2$. For instance, when T3 and T4 are conducting, T1 and T2 receive the full DC link voltage. On the other hand, the horizontal IGBTs, T5 and T6, switch and block half DC link voltage.

TABLE I. ACTIVATED IGBTs VERSUS THE DESIRED OUTPUT VOLTAGE (ADAPTED FROM [13])

Output voltage level	$V_{DC}/2$	0	$-V_{DC}/2$
Switching signals sending on	T ₁ , T ₂ , T ₃	T ₃ , T ₆	T ₃ , T ₄ , T ₆
4 Digits Representation	1100	0110	0011
Current is leaded by	$i_L > 0$	T ₁ , T ₂	T ₃ , D ₆
	$i_L < 0$	D ₁ , D ₂	D ₃ , T ₆

The vertical switches Q1 to Q4 have also a parallel resistance of high value to equalize the steady state voltage distribution and an RC snubber to reduce the surge voltages during the turn-off. The applied IGBT is the MBN750H65E2 from Hitachi [14] and the gate driver is the Scale 1 from Concept [15]. The IGBTs and the snubber resistors are assembled with the thermal grease over one unique heatsink per phase, a PT100 is placed near the IGBT with the highest estimated temperature at full load, modulation, and speed. The

phase modules are designed to be identical and interchangeable.

B. Converter Circuit

The converter comprises 12 phase modules placed in two parallel bridges at the AFE (Active Front End) input and two at the MB (Machine Bridge) output. The AFE input has a LCL'L filter with a series reactor of high inductance, and a resonant branch. The output has a smaller series reactor and a dv/dt filter. Fig. 3 shows the converter single line diagram with the main components, measurement points and communication interfaces.

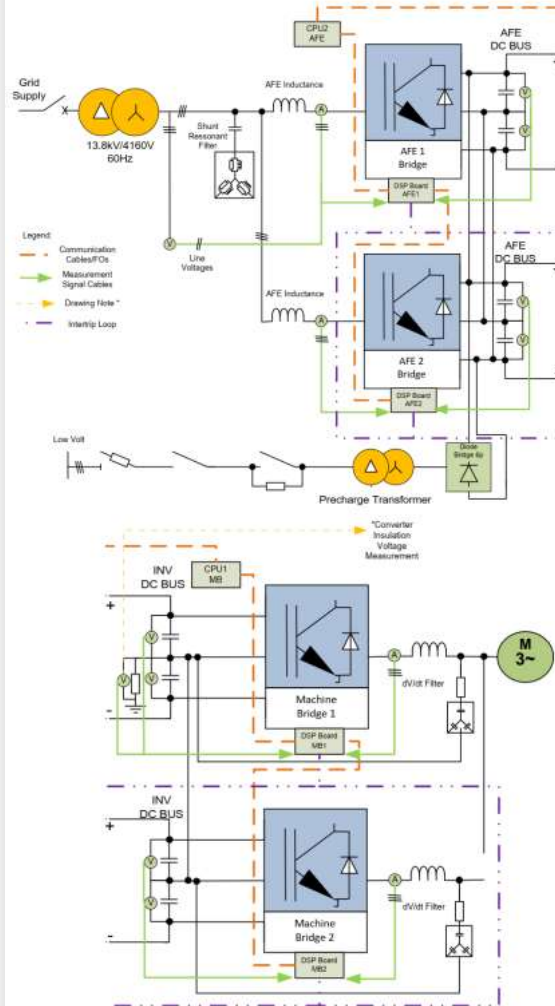


Fig. 3 - Schematics the converter under analysis (top: AFE, bottom: MB)

The DC link of the two AFEs are interconnected, as the DC link of the two inverter bridges. The AFE and the INV positive and negative DC link poles are also connected, but not the zero-volt (0 V) pole. A resistor is placed between the inverter bridge 0 V and the ground to monitor the system (transformer, converter, and motor) insulation.

The drive control architecture is formed by 2 CPUs, one for the AFE and one for the MB. Auxiliary faults and the overall control are processed in the CPUs. Each CPU is

connected to two dedicated DSP boards, one for each parallel bridge. These boards are responsible for the IGBTs firing and can monitor and fast actuate to suppress the commanded pulses in the case of critical faults.

The SHE-PWM (Selective Harmonic Elimination) [16], 5 angles, is the switching strategy of the AFE side, with a switching frequency of ten times the grid frequency, i.e., 600Hz. The MB side operates in H3-PWM at 660Hz. The sampling time is twice the MB output PWM frequency, i.e., $T_s = 1/2F_{\text{pwm}} = 757\mu\text{s}$.

The main measurements monitored by the converter control are shown in TABLE II.

TABLE II. MAIN MEASUREMENTS AND CONVENTIONS

	Main measurements	Convention	Read by Controller
1	3Ø currents at the of the PMs to the motor, before the dv/dt filter	1p.u. → rated value positive when going to the motor	MB
2	DC link Voltages referred to the 0V on the MB side	0.5p.u. → rated value*	MB
3	0V to ground insulation voltage	1p.u. → rated value*	MB
4	3Ø currents at the of the PMs to the grid, before the LCL'L filter	1p.u. → rated value positive when going to the converter	AFE
5	Input line voltages at the secondary side of the transformer, after the LCL'L filter	1p.u. → rated value*	AFE
6	DC link Voltages referred to the 0V on the AFE side	0.5p.u. → rated value*	AFE

*DC link and input voltage readings are not in the same base.

C. Converter Protection

The main protections inside the converter are obtained by the GD (Gate Driver) direct monitoring of the IGBT and the actuation of the DSP board based on the measurements and the status of feedback optical fiber. The GD has two protections, the undervoltage detection of its gate voltage and the short circuit protection based on the VCE desaturation monitoring. For the latter, the voltage is checked after the turn-on command, a short circuit fault is considered when the VCE voltage remains greater than 1.2 kV after the masking time, as illustrated in Fig. 4.

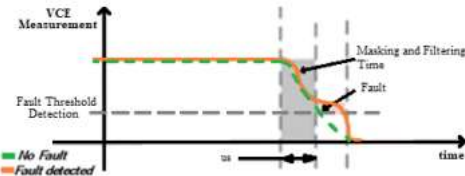


Fig. 4 – GD, VCE Desaturation Short Circuit Protection

The GD is configured not to turn-off immediately but rather send a failure status to the controller which will apply the hierarchical turn-off process. The IGBT is turned off only when the GD receives a light OFF signal in the firing command, as shown in Fig. 5. The maximum response time to detect the fault and turn the feedback light off is 10 μs , [17].

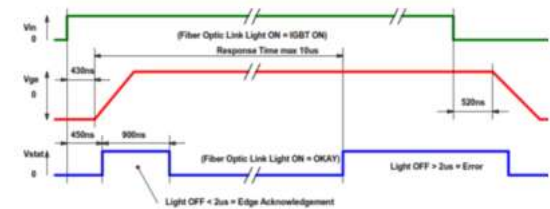


Fig. 5 – GD, VCE desaturation Short Circuit Protection (adapted from [17])

TABLE III. details the hierarchical turn-off sequence. The path after a trip and up to the off state is shown with red arrows. The normal possible switching states and intermediate states (dead time) are represented with blue arrows. If the trip is detected at the null state, the decision is taken based on the previous state sequence, e.g., if it's a null state coming from the positive state, then it takes the path $0110 \rightarrow 0100 \rightarrow 000$. The negative path is taken if the null state is coming from the negative state. The hierarchical turn-off process is decided by the DSP board FPGA and will respect the deadtime states before turning OFF all the IGBTs in the same phase. The deadtime for the case under analysis is 20 μ s. The DSP board processing time is much faster than the IGBT switching, around 33ns.

TABLE III. TRIP SEQUENCE FROM DSP AND FIRING STATES

Final State	Trip	Intermediate State (Dead Time)	Trip	Off State
Positive	1100	0100		
Null	0110			0000
Negative	0011	0010		
Legend:				
Trip Normal Sw States				

The DSP boards have a loop optical fiber protection, represented in purple in Fig. 5. When one of the boards identifies the fault, it sends to the others a light off signal that make them cut off the firing of the other bridges as well.

IV. FAULT #1 – INPUT FILTER INSULATION

This fault is of interest mainly to understand the converter conditions prior to the main fault explained in Section V. A complete RCA (Root Cause Analysis) developed for this fault concluded that there was a phase to 0 V short circuit at the converter input due to the loss of insulation between the terminals of the input resonant filter capacitors of phase V and its structure, referred to the 0 V.

Fig. 6 illustrates the filter assembly highlighting in orange the metallic frame connection of the capacitors to the zero volts reference. The connection was done to guarantee the limits of terminal to case voltage insulation as per capacitor's manufacturer datasheet. The FWDs and the arc flash bypassing the line inductor of phase V, shown in red, form a half wave dual polarity rectifier uncontrollably charging and discharging each half DC link set of capacitors. The current of this initial stage is here called Isc1 (short circuit current 1).

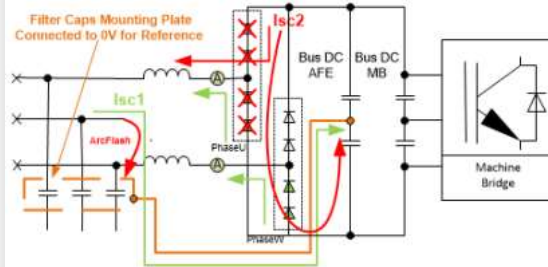


Fig. 6 – Filter Capacitor's frame reference connection and Short Circuit Current Path during Vvw Positive Semi Cycle

Fig. 7 shows the recorded fault graph with the dc link voltages on the AFE side, the six input currents per phase module (positive when going from the grid to the converter),

the line voltages at the secondary side of the transformer and boolean signals of the moment in which the DSP board stop sending the firing command (shifted in the y axis to facilitate visualization).

Even with the firing commands turned OFF, marked by the red vertical line in Fig. 7, Isc1 flows from phase U through the FWDs and charges the capacitors of the positive DC link while the voltage in phase U is bigger than phase V. At the same time, the negative capacitors discharge through the arc back to phase V. Similarly, during the rise of the line voltage VW, the negative capacitors are charged.

The DC link voltages and currents during this process are much higher than the nominal values of the converter operation, even reaching the DSP board end of scale (flat reading in the graph), and could be only interrupted by the opening of the main breaker. Although the command to open the breaker is sent at the trip detection, the opening process takes 60 to 80 ms.

The FWDs are weakened by this current flow, and fail to sustain the higher DC voltages, collapsing and generating the positive to negative short circuit with even higher currents. This moment is represented by Isc2 in Fig. 6 and the dashed red vertical line in Fig. 7.

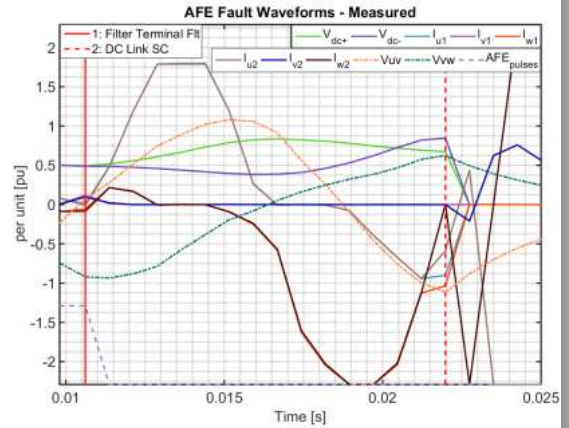


Fig. 7 – AFE Fault 1 Graph (Measured)

After the fault, a basic in-circuit pulse test using an external low voltage dc supply and the multimeter in voltage mode was conducted on site to evaluate the IGBTs and FWDs in blocking mode and the remaining ON state voltage when conducting a small current from the supply.

Those are often the only tests executed before replacing the damaged phase module and reinstating the converter operation. However, to support the fault investigation, the insulation between the HV circuit and heatsink was measured as well as the Collector to Emitter insulation when applying 5kVdc with a Megger. The cables were disconnected for the last test, but the GDs were kept on the IGBTs due to the difficulty to access it on site and to avoid leaving the Gate to Emitter terminals disconnected while applying High Voltage to the IGBTs.

TABLE IV. summarizes the results of the C to E insulation tests, each phase module is issued a letter representing the manufacturer serial number to facilitate the traceability in this text.

Phase modules C, G, I, J, K and L were sent back to the factory to be refurbished. They are given the number 2 from now on in this text to mark the change. All phase modules but C had all their IGBTs replaced by new units. For the phase module C only Q1 was changed.

TABLE IV. INSULATION TEST RESULTS AFTER FAULT #1

Phase	Test	Bridge	AFE1	AFE2	MB1	MB2
↓	↓	Module→	A	D	G ^{II}	J
↓	↓	Device ^{III} ↓	Result↓	Result↓	Result↓	Result↓ V _{tr} ^{IV} ↓
U	a	1	6.49MΩ	6.50MΩ	6.50MΩ	350KΩ 563V
		2	6.49MΩ	6.50MΩ	6.49MΩ	510KΩ 519V
		3	6.49MΩ	6.50MΩ	6.50MΩ	1.041MΩ 1854V
		4	6.49MΩ	6.50MΩ	6.49MΩ	312KΩ 301V
		5	6.50MΩ	6.49MΩ	6.50MΩ	6.51MΩ
		6	6.50MΩ	6.49MΩ	6.50MΩ	6.5MΩ
V	a	All to Hsk	112.7GΩ	104.0GΩ	166.6GΩ	175.3GΩ
		b	All to Hsk	112.7GΩ	104.0GΩ	166.6GΩ
		1	6.50MΩ	6.5MΩ	6.50MΩ	159KΩ 295V
		2	6.49MΩ	6.5MΩ	6.50MΩ	390KΩ 694V
		3	6.49MΩ	6.5MΩ	6.49MΩ	320KΩ 395V
		4	6.50MΩ	6.49MΩ	6.49MΩ	124KΩ 295V
W	a	5	6.50MΩ	6.50MΩ	6.50MΩ	6.51MΩ
		6	6.49MΩ	6.51MΩ	6.50MΩ	6.50MΩ
		All to Hsk	97.1GΩ	173.1GΩ	174.7GΩ	175.3GΩ
		b	All to Hsk	97.1GΩ	173.1GΩ	174.7GΩ
		1	Burst	< 10MΩ	< 10V	6.49MΩ Broken Frame
		2	Burst	6.50MΩ	6.50MΩ	6.50MΩ Broken Frame
W	a	3	Burst	6.49MΩ	6.50MΩ	6.50MΩ Broken Frame
		4	Burst	6.50MΩ	6.50MΩ	6.50MΩ Broken Frame
		5	Burst	6.50MΩ	6.49MΩ	6.49MΩ Broken Frame
		6	Burst	6.50MΩ	6.50MΩ	6.50MΩ Broken Frame
		All to Hsk	NA	135.6GΩ	106.1GΩ	NA
		b	All to Hsk	NA	135.6GΩ	106.1GΩ

- I. Test a is the C to E 5kVdc Megger and test b is the HV circuit insulation to the heatsink.
 II. Device number as per Fig. 2.
 III. V_{tr} is the maximum voltage reached by the Megger when trying to perform the 5kVdc test, i.e. the leakage current was higher than the Megger device capacity and the voltage stop to raise.
 IV. Phase module G was considered bad not because of the results from test a, but due to lower values of V_{tr} on the FWD when measuring with the multimeter.

The converter was restored but operated for only about a month before experiencing a new fault, which is explored in Section V.

According to the IGBT manufacturer data and similar C to E insulation tests performed in laboratory in new units of the MBN750H65E2, the expected equivalent resistance for one IGBT frame with three internal IGBTs in parallel is around 2GΩ. Notwithstanding, since the gate driver C to E resistance is a few MΩ we can conclude that the test was only able to spot highly damaged devices. Weakened devices still able to sustain the applied voltage but with deviation in the expected leakage current could have been hidden by the parallel smaller resistance of the GD.

V. FAULT #2: MAIN FAULT – REUSE OF WEAKENED IGBT

The study of this fault and the affected devices is developed from the site actual recordings and a simulation developed in PLECS with the circuit of Fig. 3, the parameters of the grid, transformer, converter and motor of this application and TABLE II. The simulated model replicates the fault and provides estimation on the internal variables that are not directly measured in the site records. The following assumptions apply:

- 1) The devices are considered as always in the saturation region. The IGBT ON state resistances is estimated from the slope in the static $I_c \times V_{ce}$ curve when conducting with a 15V V_{ge}, plus a forward offset voltage when the current is null. The same is applied to the FWD using the $I_f \times V_f$ curve.
- 2) The short circuit is simulated by a parallel switch in series with a SC resistance that bypasses the semiconductor.

- 3) The DC link capacitors are modeled with its Equivalent Series Resistance (ESR) of 10 mΩ and a series inductance of 90 nH.
- 4) Each phase module has a 1.2 μH stray inductance in the connection to the DC link and 0 V. Due to the converter construction, this connection is done with cables and not laminated busbars.
- 5) The AFE to MB DC link connection is also done by cables. This inductance is estimated as 3.6 μH.

The recorded graphs and the waveforms replicated in the simulation are shown Fig. 8 for the MB side. The graph shows the six output currents, the dc link voltages, the speed measurement from the encoder and the boolean signals to mark the firing commands OFF and when the main-circuit breaker (CB) opens. The recorded readings become flat whenever they reach the DSP board end of scale, those reading limits are marked in the simulated graph for reference.

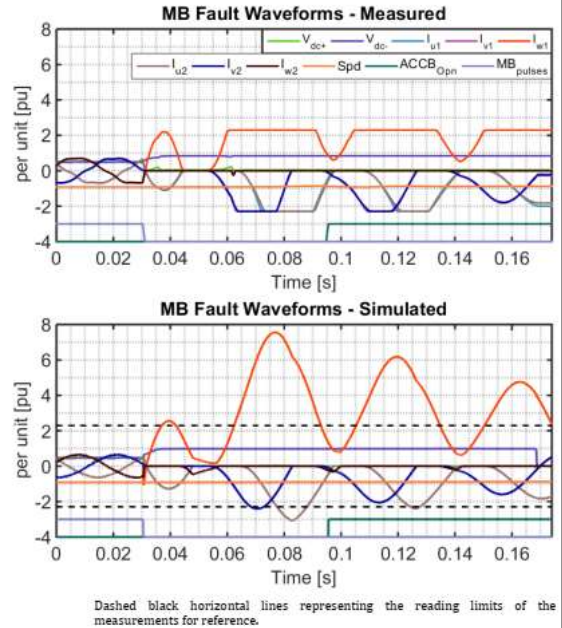


Fig. 8 – MB Fault Graph (Measured and Simulated Data).

Right before the fault, the motor was running at 0.92 p.u. speed to the negative direction. Phase W of MB1 had a negative current, which means that the current was flowing from the motor into the drive. The reference voltage was also negative since the motor power factor is 0.85 at full load. Therefore, the possible states or transitions of the phase W IGBTs at the trip detection are the ones shown in Fig. 9.

Phase module C2, now placed in phase W of MB1 was the most damaged one and probably where the fault started. It had IGBTs with broken frames and the device Q1 completely burst.

At the trip detection, the vertical positive IGBTs were not conducting or switching, but its blocking voltage can vary from V_{DC}/2 to full V_{DC}. Q1 was a new unit while Q2 was reused after the previous fault. Besides, the Collector to Emitter insulation of Q2 was tested only with the gate driver

This situation configures one of the risks associated with the use of IGBTs in series. The IGBTs are expected to have a very similar switching behavior, but if Q2 was weak, the deviations between the two IGBTs was affected, and the devices were overstressed. Furthermore, the gate driver protections as described wouldn't be able to detect Q2 in short circuit if Q1 would still switch the full voltage for a certain time. Q1 would accumulate all the losses expected for that vertical arm, besides sustaining the full DC link voltage when Q3 and Q4 are ON.

Note that Fig. 10 is only a representation of the states and transitions, the actual overvoltages and overcurrents associated to the stray inductances and the switching process of the semiconductor devices are not shown.

A. Back EMF effect

The oscillations of high current measured by the amperemeters positioned at the output of each phase module show that not only an inner loop is formed by the DC+ short circuit through Q1, Q2, Q6 and D5, but also an external current loop is generated providing a path for the current through the motor inductances and back EMFs. Fig. 11 shows the representation of this current path when the back EMF of the phase V is bigger than the phase W and the current circulates through phases U of the two MBs and through phase W of MB1.

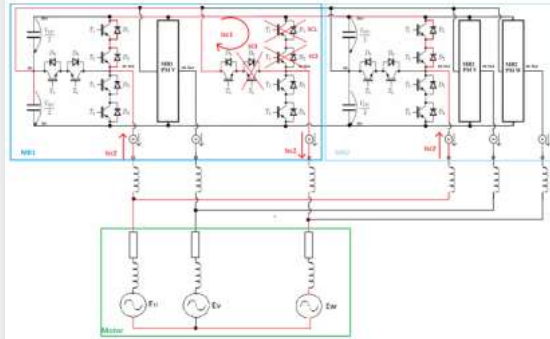


Fig. 11 – Back EMF effect and current circulation through motor ($E_v > E_w$)

I_{sc1} is the inner loop current due to the positive DC link short circuit and I_{sc2} is the outer loop that passes through the motor and depends on the back EMF. The current is positive in the MB1 PM W, passing through E_w in the motor and coming back through E_u , since E_v is bigger at this moment. This corresponds to the high current semi cycle seen in the trip graph, Fig. 8, right after the positive DC link short circuit.

There is no circulation path for the current in the MB2 PM W, because at this point T1 and T2 are healthy. In MB1 and MB2 PM U the current loop closes through the FWDs D1 and D2. This current loop stays on and oscillates between phase W and the other two phases U and V from MB1 and MB2 even after the main-circuit breaker is open, since it depends on the motor rotation due to the load inertia.

The voltage on the AC output will increase above the half DC link on the negative side according to the stray inductance to the 0 V and the slope of the short circuit current passing across it. Since the fault current di/dt is very high, it is likely that Q3 and Q4 fail in overvoltage. Besides, those IGBTs were probably already weakened by the high current conduction before the fault detection at stage 5 of Fig. 10.

Fig. 12 shows the values found on the simulation for the collector current right after the trip during the back EMF effect. The simulation confirms the overstressed in the FWDs D1 and D2 of MB1 and MB2.

Positive values mean current passing through the IGBTs and negative values are the current passing through the FWDs, unless for the Phase Module MB1 W in which the short circuit was simulated by a parallel switch. Note also that the plot was slightly offset in the vertical axes to allow the visualization of the waveforms even in the devices that have the exact same current values.

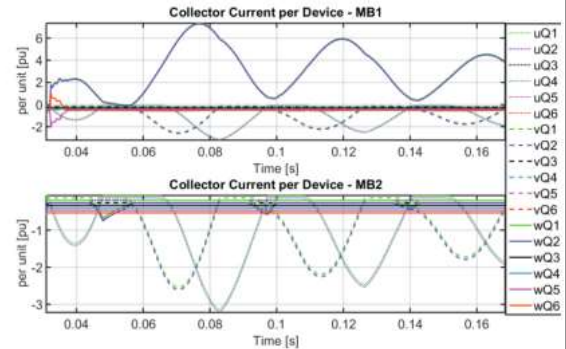


Fig. 12 – Collector Current per Device (Simulated)

B. Effect of the Stray Inductances

The stray inductances in the phase modules connection to the DC link and in the DC connection from the AFE to the MB will also create other alternative short circuit currents passing through the FWDs. Those currents are generated when the DC link capacitors are short circuited, and the energy is discharged fast in the stray inductances leading to LC oscillation of short duration.

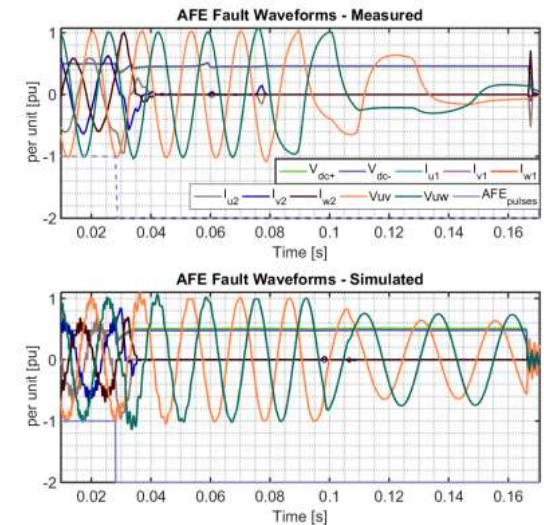


Fig. 13 – AFE Fault Graph (Measured and Simulated Data)

The FWDs will normally block the current, but the LC oscillation can make the voltage in the capacitors to invert polarity and force the current circulation through the diodes. For the half DC link short circuit, the devices C+ and C- block

the short circuit current flow in the other phase modules since they are in anti-series connection. However, the phenomenon is expressive after a full DC link short circuit with the current flowing through the vertical FWDs and affecting even the devices in the AFE side.

In the real case fault, the DC+ to 0 V short circuit evolves to a DC+ to DC- short circuit when the devices Q3 and Q4 fail from sustaining the full DC link voltage for a long time. Due to a damage in the DSP controller board, the readings on the MB side froze at around 0.165 s, yet the DC link short circuit can be confirmed by the graph on the AFE side, though. Fig. 13 brings the records of the AFE side and the reproduced simulated results.

The firing pulses are turned off on the AFE side right after the MB DSP board detects the fault due to the intertrip fault loop mentioned in the Converter Circuit section. The voltage measurement dies out about 60 ms later, after the opening of the main-circuit breaker. The full DC link short circuit is registered at the end of the graph.

Fig. 14 presents a closer look in the simulated DC link voltages and the collector currents the devices on the AFE side. Although diodes have a substantial surge rating, all the vertical FWDs are overstressed with a high overcurrent that cannot be interrupted by a protection action and last for around 400 μ s.

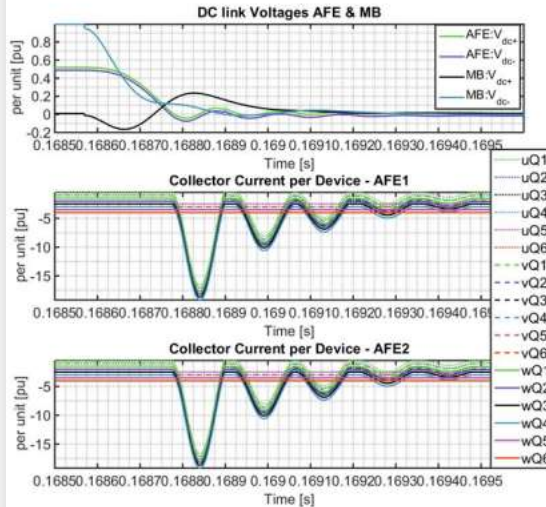


Fig. 14 – Collector Current per Devices in the AFE side and DC link Voltages during Full DC Link Short Circuit (Simulated)

VI. POST FAULT TESTS

The after-fault site tests were once again performed, yet this time the C-E 5kVdc insulation tests was done with the gate driver disconnected and keeping the Emitter and Gate short circuited. The test results are summarized in TABLE V.

As expected, the insulation resistance of the IGBTs when measured alone is much higher than the one measured in the previous fault with the gate driver connected.

Although only the IGBTs with equivalent resistance under 1G Ω were initially considered the bad ones, the final decision was to replace all phase modules. The converter operation was then reestablished and there was no other record of faults.

IGBT Q4 from L2 in the AFE1 is the one that presented the most interesting result, since it was still able to sustain 5kVdc voltage and had a high equivalent insulation resistance, but much lower than the value expected for new units. This result also confirms that the measurement performed with the gate driver installed is only able spot IGBTs with drastic internal damages.

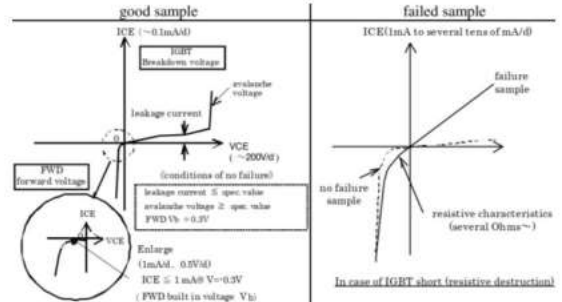
TABLE V. TEST RESULTS AFTER THE MAIN FAULT

Phase	Test	Bridge	AFE1	AFE2	MB1	MB2
		Module	Result	Result	Result	Result
U	a	Device	Result	Result	Result	Result
		1	0.951G Ω	2.029G Ω	0.775G Ω	1.736G Ω
		2	0.974G Ω	1.543G Ω	1.245G Ω	2.074G Ω
		3	0.720G Ω	1.680G Ω	1.790G Ω	1.917G Ω
		4	0.811G Ω	1.791G Ω	2.014G Ω	1.577G Ω
		5	0.951G Ω	2.390G Ω	0.962G Ω	2.068G Ω
		6	0.741G Ω	2.500G Ω	0.987G Ω	2.267G Ω
	b	All to Hsk	>150G Ω	>200G Ω	>200G Ω	180G Ω
	b	Module	Result	Result	Result	Result
		1	1.298G Ω	2.030G Ω	2.309G Ω	1.456G Ω
		2	1.384G Ω	2.155G Ω	2.670G Ω	1.267G Ω
		3	1.272G Ω	2.368G Ω	1.967G Ω	1.664G Ω
		4	0.831G Ω	2.148G Ω	1.876G Ω	1.453G Ω
		5	1.495G Ω	2.086G Ω	2.328G Ω	1.479G Ω
V	a	Device	Result	Result	Result	Result
		1	1.367G Ω	2.205G Ω	1.930G Ω	1.433G Ω
		2	1.367G Ω	2.205G Ω	1.930G Ω	1.433G Ω
		3	1.367G Ω	2.205G Ω	1.930G Ω	1.433G Ω
		4	1.367G Ω	2.205G Ω	1.930G Ω	1.433G Ω
		5	1.367G Ω	2.205G Ω	1.930G Ω	1.433G Ω
	b	All to Hsk	>200G Ω	>200G Ω	250G Ω	350G Ω
	b	Module	Result	Result	Result	Result
		1	1.478G Ω	1.837G Ω	Burst	233k Ω 372V
		2	2.080G Ω	1.865G Ω	Burst	2.25M Ω 502V
		3	2.042G Ω	1.718G Ω	6.41G Ω 20.0V	<10k Ω 8V
		4	72.3M Ω 208V	1.755G Ω	Burst	454k Ω 73V
		5	2.040G Ω	1.748G Ω	<10k Ω 13.4V	1.682G Ω
W	a	Device	Result	Result	Result	Result
		1	1.901G Ω	2.243G Ω	6.6k Ω 102V	2.653G Ω
		2	1.901G Ω	2.243G Ω	6.6k Ω 102V	2.653G Ω
		3	1.901G Ω	2.243G Ω	6.6k Ω 102V	2.653G Ω
		4	1.901G Ω	2.243G Ω	6.6k Ω 102V	2.653G Ω
		5	1.901G Ω	2.243G Ω	6.6k Ω 102V	2.653G Ω
	b	All to Hsk	>150G Ω	96.7G Ω	NA	NA
	b	Module	Result	Result	Result	Result
		1	1.478G Ω	1.837G Ω	Burst	233k Ω 372V
		2	2.080G Ω	1.865G Ω	Burst	2.25M Ω 502V
		3	2.042G Ω	1.718G Ω	6.41G Ω 20.0V	<10k Ω 8V
		4	72.3M Ω 208V	1.755G Ω	Burst	454k Ω 73V
		5	2.040G Ω	1.748G Ω	<10k Ω 13.4V	1.682G Ω

Device Q3 of C2 values probably mean that at some point two of the internal three parallel IGBTs inside the frame opened because of the destruction process and only one device is being measured.

A more detailed OFF-state Collector to Emitter insulation test was executed in laboratory in the IGBTs Q4 of L2 and Q1 of G2. The reverse biased voltage was applied in steps up to the maximum value, VCES, following the reference test instruction of [18]. The leakage current that still flows in OFF-state or the collector to emitter cut off current, I_{ces} , was measured. The reference curves shown in TABLE VI. indicate the expected differences between good and damaged samples and illustrate the device behavior in avalanche mode, when the voltage is above the limit of the IGBT Reverse Safe Operation Area (SOA) and the leakage current increases fast.

TABLE VI. IGBT ELECTRICAL CHARACTERISTIC CHECK (CE) [18]



* Checking terminals C to E. G-E must be short circuited.

Fig. 15 shows the I_{ces} test results at ambient temperature for the Q4 of L2 flat-pack unit. The test was performed on each one of the three parallel IGBTs inside the frame separately. While the values of two separated parallel devices were similar indicating a consistent aging process, a clear deviation was found in one of the parallel IGBTs. In this case, the avalanche region was affected and starts sooner than expected for IGBT 1. It could still sustain high voltage, but