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ROBUSTNESS ANALYSIS AND ENHANCEMENT STRATEGIES FOR QUANTUM-DOT CELLULAR AUTOMATA STRUCTURES

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Dissertação de Mestrado submetida à Banca Examinadora designada pelo Colegiado do Programa de Pós-Graduação em Engenharia Elétrica da Escola de Engenharia da Universidade Federal de Minas Gerais, como requisito para obtenção do Título de Mestre em Engenharia Elétrica.

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Robustness Analysis and Enhancement Strategies for Quantum-dot Cellular Automata Structures

Brazil

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To Thiago Fernandes Leão and Nicolas Reis Cotrim,
I hope somehow to inspire you, as your smiles inspire me to try my best every day.

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Resumo

A nanotecnologia QCA (*Quantum-dot Cellular Automata*) tem sido apontada como possível sucessora para o CMOS (*Complementary Metal-Oxide Semiconductor*). A transmissão e o processamento de informação em circuitos QCA ocorrem sem o fluxo de elétrons, resultando em um baixo consumo de energia. Além disso, altas frequências de relógio são esperadas para os circuitos QCA futuros, além de uma menor área em relação ao seus análogos em CMOS. Não obstante as várias vantagens em comparação ao CMOS, a nanotecnologia QCA precisa superar vários desafios, a maioria deles relacionados à fabricação e à robustez. Por isso, a criação de estruturas QCA robustas e metodologias para análise de erros para QCA são passos obrigatórios para sua consolidação.

Este trabalho introduz um Simulador de Defeitos para QCA que emprega uma nova metodologia para análise de erros em estruturas. Tais erros podem ser causados por defeitos nas células ou desvios de fase inesperados nos sinais de relógio. O simulador oferece uma medida quantitativa do nível de robustez de uma estrutura, denominada taxa de simulações sem erro. Além disso, ele produz um mapa de calor através do qual é possível identificar os pontos de polarização mais fracos de uma estrutura sob determinadas circunstâncias de teste.

Depois da identificação dos pontos fracos das estruturas por meio dos mapas de calor, mudanças estruturais estratégicas são realizadas a fim de criar estruturas modificadas de robustez aumentada. Então, o desempenho dessas estruturas modificadas é comparado ao desempenho das estruturas regulares através de uma nova rodada de simulações. Testes realizados demonstraram a robustez superior dos componentes fundamentais modificados, na presença de defeitos de classes combinadas. Além disso, um leve aumento da robustez foi observado quando esses componentes foram usados para substituir componentes regulares dentro de circuitos e sistemas QCA mais complexos.

Em relação aos sinais de relógio QCA submetidos a desvios de fase, a estratégia de relógio assíncrono é proposta como alternativa ao tradicional esquema de relógio síncrono para diminuir a ocorrência de erros. O Simulador de Defeitos QCA foi usado para gerar desvios aleatórios, possibilitando a comparação entre os esquemas de clock síncrono e assíncrono. Os resultados para os testes realizados com os componentes fundamentais mostraram um aumento na taxa de simulações sem erro para desvios na faixa de 0 a $\pi/4$ radianos.

Palavras-chave: QCA. Robustez. Análise de erros. Estruturas robustas.

Abstract

QCA (Quantum-dot Cellular Automata) has been pointed out as a candidate for CMOS (Complementary Metal-Oxide Semiconductor) succession. The transmission and processing of information in QCA circuits occurs without flow of electrons, resulting in tremendously low power consumption. Furthermore, the design of QCA circuits generally requires less area than its CMOS counterpart and high clock frequencies are supposed to be achieved. Despite its many advantages in comparison to CMOS, QCA has to overcome several challenges, most of them related to its physical implementation and robustness. Thus, the creation of robust QCA structures as well as methodologies for error analysis for QCA are mandatory steps to the consolidation of this emerging nanotechnology.

This work introduces a QCA Defects Simulator that employs a novel methodology for errors analysis in QCA structures. Such errors may occur at output signals due to either structural defects into the cells or unexpected shifts in the clock signals. The tool provides a quantitative measure of the robustness level of the structure, named error-free simulations rate. Moreover, it produces a heat map by which it is possible to identify the weakest polarization points when the structure is submitted to structural defects testing under certain classes of defects.

After the weak polarization points in structures are identified by means of the heat maps, they undergo an addition of cells and strategical structural changes in order to create modified robustness enhanced structures. Then, the performance of the modified structures are compared to their regular counterparts. Results of the tests performed demonstrated the superior robustness of the modified fundamental components under combined classes of defects. Moreover, a slightly robustness enhancement was achieved when the modified fundamental components were used to replace their regular counterparts within more complex QCA circuits and systems.

Regarding to the robustness enhancement of phase-shifted QCA clock signals, an asynchronous clock strategy is proposed as an alternative to the traditional synchronous clock. The clock shifts testing at QCA Defects simulator was used to generate random shifts in the clock signals, allowing the comparison of the error-free rates for both synchronous and asynchronous clock signals strategies. The results for tests performed with fundamental components showed an increasing in the error-free simulations rate for shifts within the range of 0 to $\pi/4$ radians.

Keywords: QCA. Robustness. Error analysis. Robust structures.

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CMOS	Complementary Metal-Oxide Semiconductor
QCA	Quantum-Dot Cellular Automata
MQCA	Molecular Quantum-Dot Cellular Automata
NML	Nanomagnet Logic
SOI	Silicon-on-insulator
RCA	Ripple Carry Adder
ALU	Arithmetic Logic Unit

Contents

1 Introduction

1.1 Motivation

Complementary Metal-Oxide Semiconductor (CMOS) technology has been widely used for the realization of integrated circuits since the late sixties (HOEFFLINGER, 2012). The vast knowledge of its manufacturing process as well as the application of the scaling theory allowed a remarkable increment in the devices integration density (BROWN et al., 2004). Practical observations of the amount of transistors in a single chip has endorsed the predictions of Moore (1965). However, despite the advantages, scaling has resulted in some severe problems such as power consumption and reliability concerns (ITRS, 2004). As the feature-size decreases, quantum effects and current leakage becomes more significant thereby promoting the increment of the static power consumption (FRANK, 2002). The large-scale integration of the devices causes a huge demand for thermal dissipation that are not always possible to meet, resulting in reliability losses. The alarming situation may lead to the discontinuity of the scaling process in a short-medium term, which encourages the rising of new nanotechnologies that enable the continuity of the feature size reduction (KAUR et al., 2015). The Beyond Moore terminology is associated to the new nanotechnology devices that will emerge as possible CMOS successors (HUTCHBY et al., 2002).

Quantum-Dot Cellular Automata (QCA) is among the promising emerging nanotechnologies that aim to solve the challenges faced by CMOS. The QCA operation principle takes advantage of the quantum mechanical phenomena to transport the information and perform logic operations without electric current flow, which implies in a low power consumption (LENT et al., 1993). A very high packing density may be achieved, since each cell is in the range of a few nanometers. However, QCA has to overcome several challenges before its consolidation (SAHNI, 2008). Undoubtedly, the most worrisome one is the extremely difficult physical implementation. High-resolution lithography techniques has been developed in order to eventually enable the fabrication of molecular QCA (HU et al., 2005). Prototypes of Metal-Island QCA and NML (Nanomagnetic Logic) devices have been successfully implemented as reported in (TóTH; LENT, 1999) and in (ALAM, 2010). However, none of the QCA realizations surpassed the performance of their CMOS counterparts so far.

Moreover, defects in the QCA cells or in the external clocking circuit —which provides the clock signals that are responsible for the information sequencing —may imply in concerns on robustness, since they are often closely related to the occurrence of errors (DAI; WANG; LOMBARDI, 2010). Such defects may be attributed to temperature issues

or to the pronounced effect of the manufacturing process variability, more likely to occur in nanoscale (HARON; HAMDIOUI, 2008). The creation of methodologies for error analysis as well as the proposal of robustness enhancing techniques for structures and information sequencing are mandatory steps towards the consolidation of the QCA nanotechnology (DYSART, 2009).

1.2 Contributions

This thesis introduces a QCA Defects simulator, implemented according to the precepts of a novel methodology for error analysis. The tool allows the robustness analysis of QCA structures under several classes of defects inserted into the cells or in the clock signals. The effect of defective elements to a structure expected behavior is evaluated and the results are presented by means of tables and heat maps. This graphical tool uses a color range in order to highlight the defective cells that are more likely to cause errors to the outputs.

Furthermore, the work describes robustness enhancing strategies for both the arrangements of cells that might contain defective elements and the clocking circuits, which comprise the timing synchronization mechanisms regarding QCA.

The polarization strengthen techniques comprises changes in the positioning, along with the addition of cells to specific regions of the structure. The additional cells strength the Coulomb interactions and increase the resilience to defects, as reported by Dysart, Lohmer and Kogge (2008). Two distinct scenarios are analyzed for the robustness enhancement. In the first one, thick wires (DYSART, 2003) are used to surround all the structure with extra devices, thereby promoting the robustness enhancement through redundancy. The impact on the robustness is evaluated, as well as the possible creation of secondary effects as the increment in the number of cells and response time. A similar procedure is employed to analyze the results of the tests in the second scenario, where QCA Defects simulator is previously used in order to identify the weakest regions of the same structure. Once the weaknesses are identified, the strengthen technique is applied only to those regions.

Since QCA nanotechnology is highly dependent on the information flow sequencing, phase shifts in the clock signals may be harmful to the performance of a structure. According to (OTTAVI et al., 2007), since one or more clock signals are affected by undesirable phase shifts, synchronization errors are likely to occur, which in turn may challenge the operation of the entire system. An asynchronous clock strategy is proposed as an alternative to the traditional synchronous clock, in order to enhance the robustness of the clock signals. The QCA Defects simulator is used to generate random shifts in the clock signals, in order to allow the comparison of the error-free simulation rates for both synchronous and asynchronous clock signals strategies.

Finally, the robustness-enhanced structures obtained with the aim of the QCA Defects Simulator are employed in order to design four circuits of gradual levels of complexity, *i.e.* an inverter (TOUGAW; LENT, 1994), a three-input majority gate adapted from (TOUGAW; LENT, 1994), a full adder and a ripple carry adder adapted from (BRUSCHI et al., 2011). The use of the strengthen technique creates redundant mechanisms for information propagation with a reduced increment in the number of cells in a structure, compared to the indiscriminate use of thick wires.

1.3 The thesis roadmap

This master thesis is organized into seven chapters, including this Introduction. The remaining chapters are outlined below.

Chapter 2 is entitled Background and divided into two main sections. The first section of Chapter 2 introduces the concepts of the QCA nanotechnology, while its second section presents the general aspects of robustness, later focusing on the QCA context.

Chapter 3, Related Works, is a summary of the methodologies for error analysis in the nanotechnology QCA that has been previously reported in the literature.

Chapter 4 is entitled QCA Defects Simulator. Its first section discusses a novel methodology for error analysis in defective circuits. Its second section presents the implementation of such methodology as an extension to an existing simulation tool. Finally, its third section discusses the resources used for presenting the simulation results. The use of heat maps and tables make the results easier to be interpreted.

Chapter 5 defines, in its first section, strategies for robustness enhancement for both cell-defective and clock-defective circuits. The robust structures designed by means of such strategies are presented in the second and third sections.

Chapter 6 presents the designs and simulation results of four logic circuits where the techniques for robustness enhancement are applied, *i.e.* an inverter (TOUGAW; LENT, 1994), a three-input majority gate adapted from (TOUGAW; LENT, 1994), a full adder and a ripple carry adder adapted from (BRUSCHI et al., 2011).

Chapter 7 concludes the work and presents suggestions for future works.

1.4 Definitions

This section defines some key terms often used along the thesis.

- **Device:** The fundamental building block of an electronic system. For instance, transistors are the devices for CMOS, as cells are for QCA.

- **Structure:** Any arrangement of devices. Comprises all the categories defined below: Fundamental and logic components, circuits and systems.

- **Fundamental Component:** An arrangement of devices designed under the purpose of transporting and distributing information within a logic component/circuit or interconnect different circuits into a system, *i.e.* wires and fan outs.

- **Logic Component:** An arrangement of devices designed to implement an elemental logic function, *i.e.* the logic gates.

- **Circuit:** A collection of components combined together in order to perform a complex logic function, *i.e.* full adders, multiplexers and memory cells.

- **System:** A set of circuits interconnected in order to process a higher level function, *i.e.* Ripple Carry Adders (RCAs), processors, routers, memory architectures and ALUs (Arithmetic Logic Units).

- **Defect:** In the context of this work, defects are flaws of the cells of a structure, generally caused by manufacturing process variations.

- **Errors:** Errors, in this work, are unexpected deviations in the behavior of the system. In the circuit's context, an error occurs when, given a known input vector, the state of the outputs is unexpected.

- **Robustness:** Robustness, in the context of this work, may be defined as the system capability to get along with defects and operate under unusual conditions.

- **Defect-Tolerance:** The terms robustness and defect-tolerance here are interchangeable. That is, a defect-tolerant system possess good resilience to defects.

- **Characterization Round:** The term is applied to denote one complete execution of all procedures inherent to the novel methodology for defects simulation in QCA proposed in this work.

2 Background

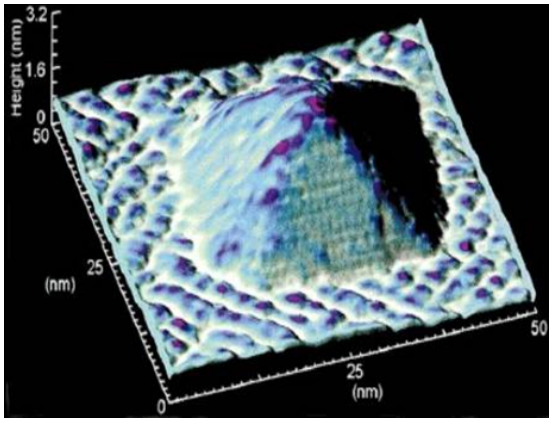
This chapter introduces the essential concepts to the better understanding of this work. Its contents are divided into two major sections. The first one, entitled Quantum-Dot Cellular Automata, elucidates the basics regarding QCA. The second major section focuses on the concepts of robustness and defect tolerance, in both general and particular contexts.

2.1 Quantum-dot Cellular Automata

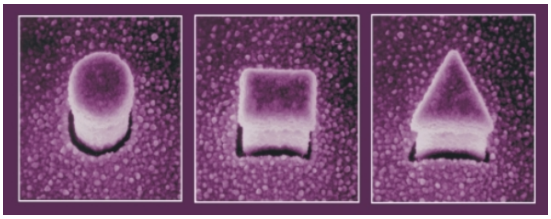
Quantum-Dot Cellular Automata (QCA) is a new computation paradigm described by Lent et al. (1993) in which the information transport and processing occur by means of Coulomb interactions rather than electric current flow, enabling a low power consumption. QCA devices have dimensions of few nanometers and are expected to operate at speeds within the range of Terahertz (KIM; WU; KARRI, 2006). QCA is considered one of the promising emerging nanotechnologies candidate for CMOS succession (ITRS, 2004).

2.1.1 QCA Cells

A QCA cell is the most fundamental device of the nanotechnology QCA. It comprises four or five nanometer-sized quantum dots, in which electrons may be confined. Due to their unique electronic and optical properties, quantum dots have a range of applications besides the construction of the QCA cells. For instance, they can be used to implement single-electron transistors, tunable lasers, solar cells and photo detectors (ALFEROV, 2001). Some atomic force microscopy images of quantum dots are depicted in Figure 1.



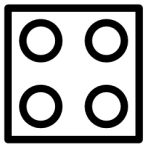
(a) An InAs quantum dot structure grown on GaAs substrate (NSTC, 1999).



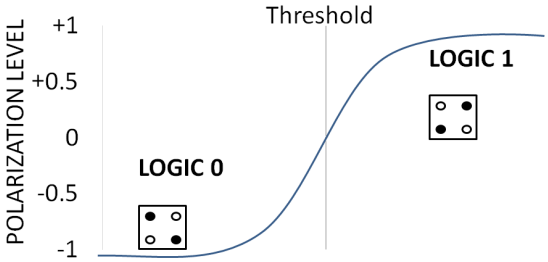
(b) The quantum dot shape may vary depending on the process and application requirements (LIANG; XIE, 2015).

Figure 1 – Quantum dot examples

The four-dot QCA cell model is depicted by Figure 2a. As introduced by (LENT; TOUGAW, 1997), it comprises four circles, which represent the quantum dots, strategically positioned at the internal corners of a square-shaped substrate. Two electrons are hold trapped into those structures due to the very high inter-dot potential barriers. According to the Coulomb repulsion effect, the electrons must be as far apart as possible. Consequently, there are two possible logic states (opposite diagonals), which permits a binary logic. By convention, the maximum polarization states, which correspond respectively to logic 0 and logic 1, are called -1 and +1. A cell can continuously assume any polarization level within those limits. Figure 2b depicts the two possible interpretations for the cell logic state, which depends on the comparison between the threshold and the polarization level.



(a) The representation of a four-dot QCA cell.



(b) The QCA cell logic state interpretation depends on the threshold of the polarization level. In the figure, a fulffiled circle represents a trapped electron.

Figure 2 – A QCA cell and its two possible logic states

2.1.2 Principle

As exposed in Section 2.1.1, a cell carries its individual information, which comprises its logic state along with the corresponding polarization level. It is possible to propagate such information along a path to an output through a cells arrangement. The same quantum mechanical phenomena, that explains the positioning of the two trapped electrons at the opposite diagonals of a cell, is responsible for the two-way electrostatic interactions between two or more cells within a common radius of influence (LENT; TOUGAW, 1997).

Whereas initially the cells on the path are at their ground states, a cost of energy, defined as Kink Energy (E_k), is required in order to provoke changes in their individual polarization levels so that the information is propagated to the outputs (TOUGAW; LENT, 1996). As shown in (DYSART, 2009), E_k is computed as the difference between the two-way electrostatic interactions of two adjacent cells (i and j) whereas they have either the opposite ${E^{diff}}_{i,j}$ or the same ${E^{same}}_{i,j}$ polarization levels (2.1).

$$E_{ki,j} = {E^{diff}}_{i,j} - {E^{same}}_{i,j} \tag{2.1}$$

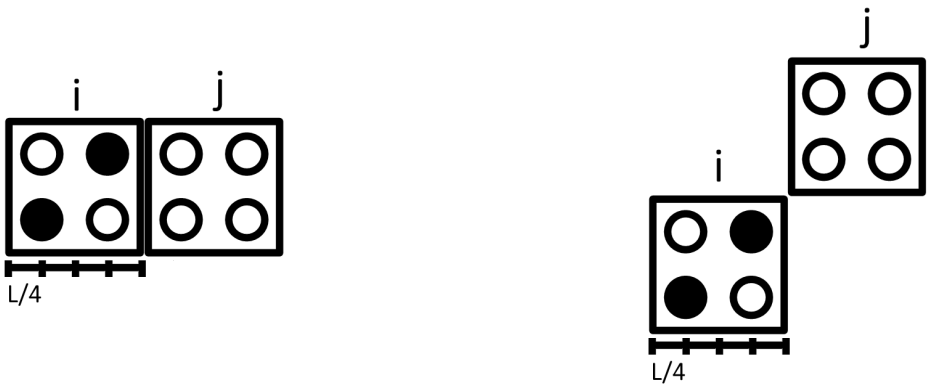
In order to find the terms of the difference of the equation (2.1), the two-way electrostatic interaction between the dots of both cells —whose width and length, in nanometers, are expressed in terms of the letter L —are calculated and summed over all i and j according to (2.2).

$$E_{i,j} = \sum_{n_i=0}^{3} \sum_{n_j=0}^{3} \frac{1}{4\pi\epsilon_0\epsilon_r} \frac{q_{n_i} q_{n_j}}{|r_{n_i} - r_{n_j}|} \tag{2.2}$$

Where:

$E_{i,j}$	: Amount of energy for the cells i and j having any polarization levels
n_i	: Index of the dots in cell i
n_j	: Index of the dots in cell j
ϵ_0	: The permittivity of the free space (For the vacuum it is 8.8545 x 10^{12} F/m)
ϵ_r	: The relative permittivity of the material system (For a GaAs/AlGaAs cell it is roughly 12.9)
q_{n_i}	: The electronic charge located on dot n_i (The elementary charge is 1.6022 x 10^{-19} C)
q_{n_j}	: The electronic charge located on dot n_j (The elementary charge is 1.6022 x 10^{-19} C)
$\|r_{n_i} - r_{n_j}\|$	: The distance between the dots n_i and n_j

By replacing the appropriate values for the constants along with the interdots distances, it is possible to calculate the energies E^{diff} and E^{same} whether the cells i and j are placed in line or in diagonal as depicted in the Figure 3.



(a) Cells i and j positioned in line.

(b) Cells i and j positioned in diagonal.

Figure 3 – Two different arrangements for the cells i and j. A fulfilled dot represent a trapped eletron. The polarization of the cell i is arbitrarily established as +1.

For the cells i and j placed in line as depicted in Figure 3a, the energies E^{same} and E^{diff} are calculated as follows:

$$E^{same} = \sum_{n_i=0}^{3}\sum_{n_j=0}^{3}\frac{1}{4\pi\epsilon_0\epsilon_r}\frac{q_{n_i}q_{n_j}}{|r_{n_i}-r_{n_j}|} = \frac{1.6022\times10^{-19}C^2}{4\times\pi\times8.8545\times\epsilon_r\times10^{12}F/m}\times \left(\frac{1}{1.0000}+\frac{1}{0.7071}+\frac{1}{1.0000}+\frac{1}{1.5811}\times\right)\times\frac{1}{10^{-9}m\times L}$$

$$E^{same} = 2.3019\times10^{-52}\frac{1}{\epsilon_r}\frac{C^2m}{V}\times\left(\frac{4.0467\times10^{9}m^{-1}}{L}\right)$$

$$E^{same} = 9.3151\times10^{-43}\frac{1}{\epsilon_r\times L}J$$

$$E^{diff} = \sum_{n_i=0}^{3}\sum_{n_j=0}^{3}\frac{1}{4\pi\epsilon_0\epsilon_r}\frac{q_{n_i}q_{n_j}}{|r_{n_i}-r_{n_j}|} = \frac{1.6022\times10^{-19}C^2}{4\times\pi\times8.8545\times\epsilon_r\times10^{12}F/m}\times \left(\frac{1}{0.5000}+\frac{1}{0.9014}+\frac{1}{0.9014}+\frac{1}{1.5000}\right)\times\frac{1}{10^{-9}m\times L}$$

$$E^{diff} = 2.3019\times10^{-52}\frac{1}{\epsilon_r}\frac{C^2m}{V}\times\left(\frac{4.8855\times10^{9}m^{-1}}{L}\right)$$

$$E^{diff} = 1.1246\times10^{-42}\frac{1}{\epsilon_r\times L}J$$

Likewise, for the cells i and j placed in diagonal as depicted in Figure 3b, the energies E^{same} and E^{diff} may be calculated as follows:

$$E^{same} = \sum_{n_i=0}^{3}\sum_{n_j=0}^{3}\frac{1}{4\pi\epsilon_0\epsilon_r}\frac{q_{n_i}q_{n_j}}{|r_{n_i}-r_{n_j}|} = \frac{1.6022\times10^{-19}C^2}{4\times\pi\times8.8545\times\epsilon_r\times10^{12}F/m}\times \left(\frac{1}{1.4142}+\frac{1}{0.7071}+\frac{1}{1.4142}+\frac{1}{2.1213}\right)\times\frac{1}{10^{-9}m\times L}$$

$$E^{same} = 2.3019\times10^{-52}\frac{1}{\epsilon_r}\frac{C^2m}{V}\times\left(\frac{3.2998\times10^{9}m^{-1}}{L}\right)$$

$$E^{same} = 7.5958\times10^{-43}\frac{1}{\epsilon_r\times L}J$$

$$E^{diff} = \sum_{n_i=0}^{3}\sum_{n_j=0}^{3}\frac{1}{4\pi\epsilon_0\epsilon_r}\frac{q_{n_i}q_{n_j}}{|r_{n_i}-r_{n_j}|} = \frac{1.6022\times10^{-19}C^2}{4\times\pi\times8.8545\times\epsilon_r\times10^{12}F/m}\times \left(\frac{1}{1.1180}+\frac{1}{1.8022}+\frac{1}{1.1180}+\frac{1}{1.8022}\right)\times\frac{1}{10^{-9}m\times L}$$

$$E^{diff} = 2.3019\times10^{-52}\frac{1}{\epsilon_r}\frac{C^2m}{V}\times\left(\frac{2.8983\times10^{9}m^{-1}}{L}\right)$$

$$E^{diff} = 6.6716\times10^{-43}\frac{1}{\epsilon_r\times L}J$$

For the in line arrangement of cells i and j, depicted in Figure 3a, the amount of energy required for the devices having different polarization, E^{diff}, is calculated according

to the equation 2.2 as $1.1246 \times 10^{-42} \frac{1}{\epsilon_r \times L} J$. Such value is substantially higher than the energy of $9.3151 \times 10^{-43} \frac{1}{\epsilon_r \times L} J$ required for the cells having the same polarization (E^{same}), computed similarly to E^{diff} by means of the equation 2.2. Since any electrostatic system tend to the ground, which is the state of less energy, aligned cells are likely to have same polarization. Thus, QCA arrays of aligned cells usually perform the function to propagate information forward in a structure (TOUGAW; LENT, 1996).

On the other hand, for the diagonal arrangement of the cells i and j depicted in Figure 3b, the value obtained for E^{diff}, $E^{k}_{i,j} = 6.6716 \times 10^{-43} \frac{1}{\epsilon_r \times L} J$, is slightly lower than the amount of energy E^{same}, computed as $7.5958 \times 10^{-43} \frac{1}{\epsilon_r \times L} J$. Therefore, for the same reasons aforementioned in the previous paragraph, diagonally positioned cells are likely to have opposite polarization. Thus, QCA cells placed in diagonals usually play the role to successive invert the logic state through a QCA array (TOUGAW; LENT, 1996).

Therefore, the transmission and processing of information in QCA are based on the principle of the Kink Energy, which is a consequence of the electrostatic interaction guided by the Coulomb's Law. Two or more cells positioned in a row are able to transmit a logic state from an input to an output. Moreover, cells positioned in diagonal successive invert the logic state through a QCA arrangement.

2.1.3 Structures

Due to the principle previously explained in the section 2.1.2, QCA cells may be arranged to transmit information and perform computation. In this work, any arrangement of cells, regardless of its primary purpose, is generally called as a structure. QCA structures, in turn, may be categorized into fundamental/logical components, circuits or systems, according to the definitions of the Section 1.4.

Some of the first QCA structures are reported in the literature by Tougaw and Lent (1994). They are illustrated in Figure 4. There, the terms input and output refer, respectively, to the starting and to the endpoint of a arrangement of common QCA cells from the left to the right of the observer.

There are two possibilities by which the information could be initially driven to an input cell. The first one regards to an interface between the cells and external signals, which would be applied by means of contacts placed in a specific layer just underneath the QCA layer. The second possibility is that an input is driven by means of the two-way electrostatic interactions among the cell and its antecedent. Such situation is more likely to happen in internal QCA wires, *i.e.* wires built-in within another larger structure in order to perform a low level information interchange. Once the information is successfully propagated through the wire to its destination point, which is the output, it can serve as input to any interconnected structure thereafter. It can also be externally transported by

means of specific interface contacts placed in a layer underneath the QCA layer.

The QCA wire, depicted in the Figure 4a is responsible for sequentially propagating a logic state from one cell to the next cell, from the starting (input) to the endpoint (output). The inverter, in turn, takes advantage of a diagonally positioned cell to invert the logic state of the signal applied to the input. The inversion principle is explained in Section2.1.2. Once inverted, the signal is transmitted forward to the output. The three-input majority gate (Figure 4c) has a core cell, also known as device cell, positioned in the middle of the component, which is surrounded by other four cells in a cross-shaped disposition —three inputs and one output. The referred core cell is responsible for performing the computation, once it is likely to assume the same logic state present at the majority of its inputs and propagate it to the output. The majority gate is considered, along with the inverter, the most basic logical components in QCA, since any logic can be created from them (TOUGAW; LENT, 1994). For instance, two circuits which perform more complex logic functions, the XOR gate and the full adder depicted in the Figures 4d and 4e, have many of wires, inverters, majority gates and further components built-in within their structures.

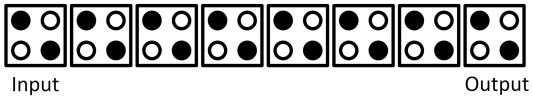
The researchers are always looking forward to create innovative QCA designs. Thus, more than two decades later from the initial proposal, different approaches have been emerging in order to improve the architecture of the QCA components and circuits. For instance, some robust components and circuits have been being proposed, as thick wires ((DYSART, 2003) (DYSART; LOHMER; KOGGE, 2008)), thick co-planar crossings ((BHANJA et al., 2007)), inverters (BEARD, 2006), majority gates (FARAZKISH; SAYEDSALEHI; NAVI, 2012) (ROOHI et al., 2014) and full adders (SAFAVI; MOSLEH, 2013) (FARAZKISH, 2015) (ROOHI; DEMARA; KHOSHAVI, 2015). Furthermore, the emerging of new QCA systems, able to perform more complex tasks have been reported in the literature, as memories (SARDINHA et al., 2015) (ANGIZI et al., 2015) , processors (WALUS et al., 2005) (FAZZION et al., 2014) and a router (SILVA et al., 2015).

2.1.4 QCA Clocking

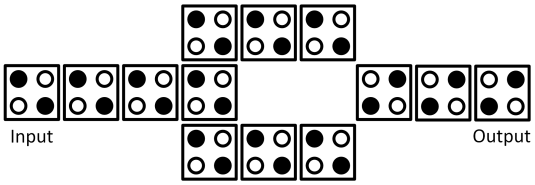
The operation of the QCA structures is highly dependent on a synchronous information flow (OTTAVI et al., 2007). Therefore, the designer must ensure that all the inputs of the logical components or circuits are driven at the same time by the fundamental components. Otherwise, a wrong logic processing is likely to happen. Such event may lead the structure to produce erroneous logic states, which implies in severe concerns on its robustness.

The key for ensuring the straight information flow within the QCA structures is to control the polarization changes of the devices, as demonstrated in the proposal of the adiabatic switching paradigm (LENT; TOUGAW, 1997). The two electrons confined into

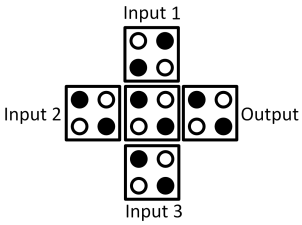
the quantum dots of a cell may switch their configuration to the opposite diagonal by tunneling. The transition leads the cell to a change between the two logic states thus its polarization. Such process shall occur in an adiabatic manner, by gradually adjusting the level of the inter-dot potential barriers in order to allow or deny the electron tunneling. Suddenly changes in the polarization level should be avoided, as they can lead the system to reach a metastable state that may cause undesirable delays or wrong logic processing (LANDAUER, 1994).



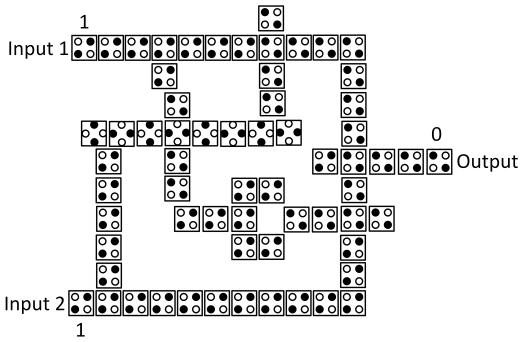
(a) A wire.



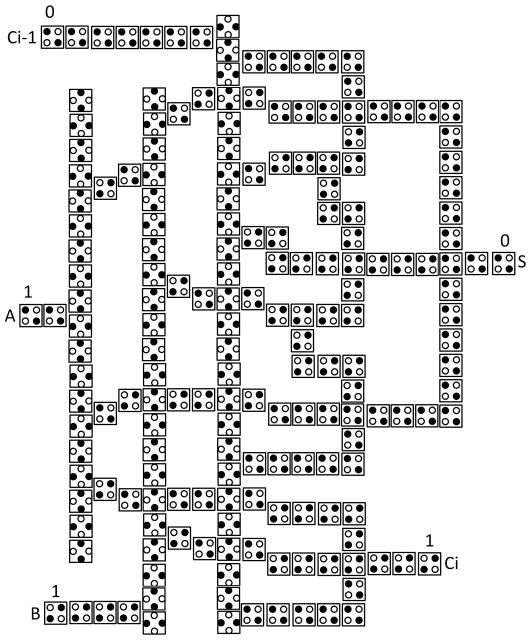
(b) An inverter.



(c) A three-input majority gate.



(d) A XOR.



(e) A full adder.

Figure 4 – The four components and one circuit reported in (TOUGAW; LENT, 1994).

External signals should control the devices adiabatic switching in each clock zone. Those signals are called clock signals, which are provided by an external clock circuit. Interconnects of such external circuit should be positioned underneath the QCA layer, being able to deliver the clock signal to every cell in the system. The inter-dot potential barrier control occurs by means of the interactions between the cells electrical field and its counterpart created by the flow of the clock signals through the interconnects. A possible placement of the clock circuit within a QCA system is illustrated in Figure 5. Metallic clock wires should be placed according to a specific clocking scheme, which is a predefined pattern that aims to address the clock signals to the respective clock zones. Some examples of clocking schemes may be found in (VANKAMAMIDI; OTTAVI; LOMBARDI, 2008) and (CAMPOS et al., 2015).

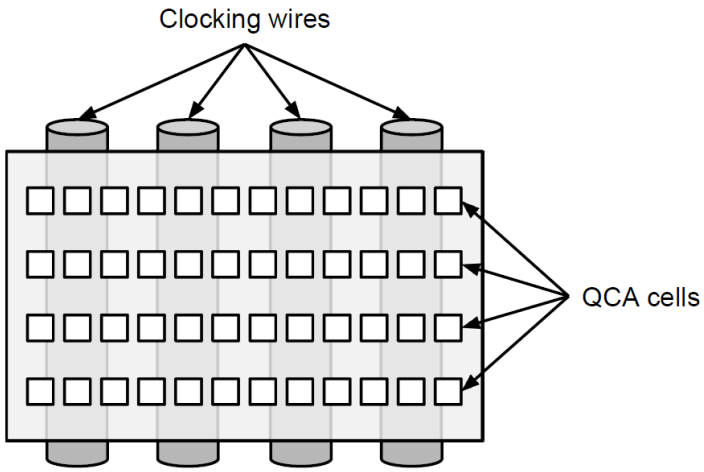


Figure 5 – Interconnects from the external clock circuit, i.e. clocking wires, underneath the QCA layer (CAMPOS, 2015).

A clock signal has four sequential phases: Switch, hold, release and relax (LENT; TOUGAW, 1997). The inter-dot barriers of a cell are differently managed in each phase in order to allow or deny the electron tunneling thus changes in the polarization level. The conventional approach for the clocking design is to provide synchronous clock signals, i.e. each phase have an individual time of $\pi/4$ radians, which corresponds to a quarter of the clock signal period.

Figure 6 depicts the general behavior of the inter-dot potential barriers level associated to the clock phases.

In the switch phase, the inter-dot potential barriers are linearly raised from the lowest to the highest level possible. At this time, the cell is susceptible to external influences and are able to change its polarization level according to the electrostatic interactions with its neighbors.

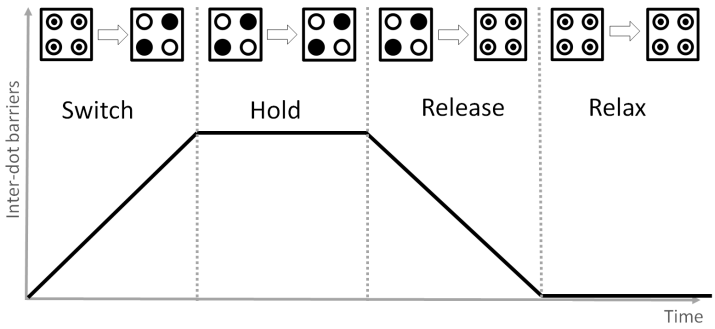


Figure 6 – The cell inter-dot potential barrier behavior at the four distinct clock phases.

In the hold phase, the inter-dot potential barriers are kept at the highest level achieved in the previous (switch) phase, so the cell is insusceptible to external influences despite the electrostatic interactions between itself and its neighbors.

In the release phase, the inter-dot potential barriers are linearly lowered from the highest to the lowest level possible. At this time the cell is able to depolarize. After the end of the depolarizing process, a cell shall not carry remainder polarization.

At last, in the hold phase, the inter-dot potential barriers are kept at the lowest level achieved in the previous (release) phase, so the cell remains depolarized until a new cycle restarts at the switch phase.

The cells of a QCA system are usually grouped into sequential sub sections, most known as zones. A single clock signal is applied in order to synchronize the polarization change process of all the cells within a zone. In the traditional clocking distribution model, the clock signal of a zone is naturally phase-shifted in relation to its counterpart of the adjacent zone, as depicted in Figure 7. The phase shift P for the clock signals in the traditional model is given by the relation: $P = (\pi/2) \times i$, where i is a sequential zone identifier: $0 \leq i \leq 3$. The identification scheme for clocking zones is cyclic, that is, the clocking zone 2 is succeeded by the clocking zone 3, which in turn precedes the clocking zone 0 that starts a new cycle. The zones arrangement in QCA circuits enables the information transport and processing in a pipeline fashion.

2.1.5 QCADesigner Simulation Tool

QCADesigner is a simulation tool launched in the early 2000s through a joint effort of some researchers from the ATIPS laboratory at the University of Calgary, Canada (WALUS et al., 2004). The simulator is widely applied within the molecular and semiconductor QCA structures simulation field, since it is considered as the most complete tool available to date designed for such purpose (LIU; O'NEILL; SWARTZLANDER, 2013). QCADesigner is open source, thus it allows the integration of new features to the current state-of-art tool. For instance, (REIS et al., 2016) introduces a standard cells library implemented

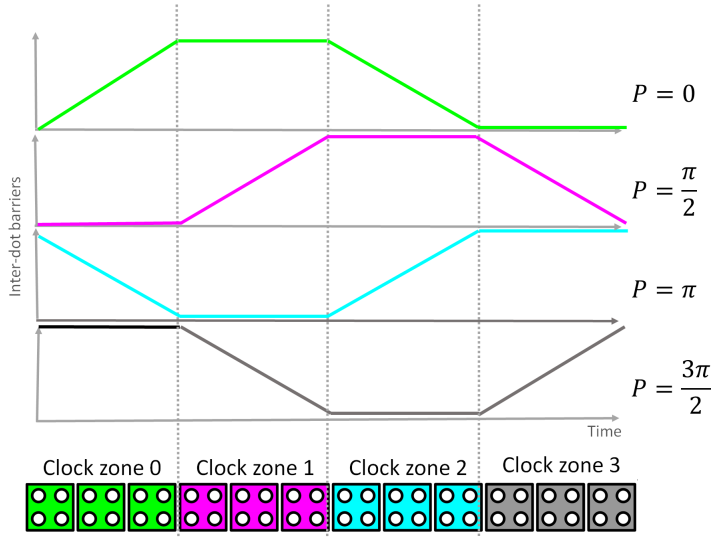


Figure 7 – A QCA wire divided into four zones and their respective clock signals (depicted in the same colors). The phase shifts are indicated next to the graphs.

into that simulation tool, which was devised according to the precepts of USE, a novel QCA clocking scheme (CAMPOS, 2015). The most recent official release of QCADesigner, the version 2.0.3, was launched in 2009.

One of the most important aspects of the QCADesigner is that such tool allows an user to quickly layout a QCA design and determine its functionality by means of two efficient simulation approaches —The Bistable and the Coherence Vector engines —which are introduced on the following subsections.

2.1.5.1 Bistable Engine

In the Bistable engine, each cell is modeled as a simple two-state system, described by the Hamiltonian Matrix 2.3.

$$H_i = \begin{bmatrix} -\frac{1}{2}P_j {E^k}_{i,j} & -\gamma \\ -\gamma & \frac{1}{2}P_j {E^k}_{i,j} \end{bmatrix} \tag{2.3}$$

Where:

P_j : Polarization of the cell j
${E^k}_{i,j}$: Kink energy between cells i and j
γ : Tunneling energy between the eletrons in the cell, which is controlled by the clock signal

The Bistable engine approach consists of solving a quantum mechanic system that comprises the electrostatic interactions between each cell in the structure and its neighbors. The Intercellular Hartree Approximation (ICHA), method by which such quantum mechanic system is solved, consider the sum of the Hamiltonian over all cells

within an radius of effect i. Within the QCADesigner tool, the neighborhood, i.e. the radius of effect of one cell to another, is defined by a specific parameter for both Bistable and Coherence Vector engines. The polarization of each cell is computed until the whole circuit converges to the ground state, which is defined by means of a preset of tolerance.

The Bistable engine is efective to simulate large circuits in a short amount of time. Thus, it has been serving as the foundation for the majority of the QCA works that has been done so far (LIU; O'NEILL; SWARTZLANDER, 2013). However, this method does not consider the most complete version of the Hamiltonian, since it ignores the quantum correlations within and between cells. Thus, the price of this relatively quick computation is inaccuracy regarding the QCA dynamics, as the bistable engine undermines the intercellular entanglement, which sometimes causes incorrect logic states at the outputs of the circuits.

A more accurate time-dependent engine —The Coherence Vector —is also available within the QCADesigner. Such engine is described in the next subsection.

2.1.5.2 The Coherence Vector Engine

The Coherence Vector engine, which principle is based on deculping the two-way cells interactions by using the density matrix approach, is adopted to describe the two-way interactions between devices within and among QCA structures. Such engine is considered as the most accurate among the two options included in the tool QCADesigner version 2.0.3, since it allows a time-dependent analysis, also taking into account power dissipation effects (LIU; O'NEILL; SWARTZLANDER, 2013). The Coherence Vector concept and formalism are briefly described in the following.

Much as to that described for the Bistable engine, in the devices model devised for the Coherence Vector each cell is considered as a simple two-state system which can be also described by the Hamiltonian matrix (2.3). Background positive elementary charges $(+\frac{1}{2}e)$ are included within the dots, so that they are taken into account for the cost of energy ${E^k}_{i,j}$ calculation, helping at the establishment of the electronic balance of the QCA devices. Thus, the Hamiltonian matrix depends both on the Kink Energy as on the distance between two neighbor cells, represented by the variable Ω_i. The model also consider the radius of effect i and the variable γ_i, which is the vector form of the density matrix of one cell, *i.e.* the coherence vector $\overrightarrow{\lambda}$, whose representation in motion can be described as follows (2.4).

$$\frac{\delta \overrightarrow{\lambda}}{\delta t} = \overrightarrow{\Gamma} \times \overrightarrow{\lambda} - \frac{1}{\tau}\left(\overrightarrow{\lambda} - \overrightarrow{\lambda_{ss}}\right) \tag{2.4}$$

The parameter $\overrightarrow{\Gamma}$ in (2.4) represents the energy environment of the cell, while τ regards to the relaxation time, *i.e.* the lasting of the depolarization process for a cell.

Its value depends strongly on the environment, i.e. the QCA physical realization type. Alongside, the variable $\overrightarrow{\lambda_{ss}}$ refers to the steady state coherence vector. The whole formalism behind the development of $\overrightarrow{\Gamma}$ and $\overrightarrow{\lambda_{ss}}$, as well as a more detailed description of all elements in the equations may be found in (LIU; O'NEILL; SWARTZLANDER, 2013).

The coherence vector for each cell is calculated through a time-marching algorithm. The $\overrightarrow{\Gamma}$ and $\overrightarrow{\lambda_{ss}}$ values are evaluated and stepped forward in time. Despite the high complexity of the quantum mechanical equations involved makes the engine computationally costly, the Coherence Vector is considered as the most accurate approach for estimating the polarization levels of the cells in a QCA system among the two simulation engines available in the tool QCADesigner version 2.0.3. Thus, it is used for all simulations presented in this work.

2.1.6 QCA Types

This section describes the four classes proposed for QCA physical realization, highlighting their advantages and disadvantages.

2.1.6.1 Metal-island

A metal-island device was implemented in (ORLOV et al., 1997) as the first physical realization of a functional QCA cell. Aluminum islands and aluminum-oxide tunneling junctions were used in order to perform the quantum dots on an oxidized silicon substrate. Two double-dots, also known as half-cells, were used to reproduce the electrostatic interactions within a device. Such model was consisted of two pairs of vertically aligned dots, D1/D2 and D3/D4, positioned alongside each other. Four electrodes, VA/VB and VC/VD, were placed just before and after pair of dots, serving as input and output interfaces between the device and the external equipment from the experimental setup. When a push-pull voltage drop $\delta V_A = -\delta V_B$ was applied to the input probes VA/VB, a consequent direct polarization appeared in D1/D2, which in turn induced a reverse polarization in D3/D4. Such induced polarization was sensed by means of the output electrodes VC/VD. The reported behavior represented a milestone for the QCA paradigm, since it has confirmed the theoretical predictions regarding the operation of the device.

The results obtained from the aforementioned experiment have motivated the emerging of a scheme that enabled the adiabatic switching paradigm in metallic QCA devices (TóTH; LENT, 1999). The inter-dot potential barriers were controlled by means of a variable differential voltage applied to three terminals of a QCA half-cell, i.e. a cell without the output double-dots. The model suitability was proved by means of computational simulations. However, less than year later from the initial scheme proposal, its identical physical realization was reported in (ORLOV et al., 2000).

Although the implementation of metallic devices was important to proof the concept behind the QCA paradigm, the metal-island type does not seem to be a reasonable choice for the future systems, due to some key issues. For instance, extremely low temperatures, in the range of milikelvin, are required in order to enable the devices operation. Moreover, the metal-island are relatively large (about 1 micrometer in dimension) (LIU; O'NEILL; SWARTZLANDER, 2013).

2.1.6.2 Semiconductor

Standard semiconductor materials are employed in order to manufacture the most of the QCA prototypes (LIU; O'NEILL; SWARTZLANDER, 2013). Some works report successful physical implementations of QCA devices by means of the electron-beam lithography process. For instance, Perez-Martinez et al. (2007) used four metallic AlGaAs gates in order to simultaneously perform the quantum dots and the surface contacts for noninvasive voltage probing. The dots were placed on a GaAs substrate. In (MACUCCI et al., 2003), QCA cells were fabricated in the silicon-on-insulator (SOI) material system. The interaction between the input and the output double-dots was predicted by means of a simulation code. Thereafter, experimental measurements confirmed the expected behavior of the device. Finally, the interactions between neighbor devices has been investigated in (SMITH et al., 2003). The materials and manufacturing process employed to fabricate the cell, as well as its physical structure, were similar to those reported in (PEREZ-MARTINEZ et al., 2007). Even though each dot contained more than a hundred electrons, the movement of a single charge from one dot to its neighbor resulted in a field that was large enough to induce polarization changes for both the dots within the same cell and for the dots in the neighbor cells.

The lithography process has been increasingly improved over the last years due to the challenges imposed by the continuous scaling of the CMOS transistors (NEISSER; WURM, 2015). Despite the QCA semiconductor type takes some advantage on such technological improvements, the extremely reduced sizes of the cells - in the range of a few namometers - makes the state-of-art lithography unsuitable for the mass production of the QCA devices due to the extremely critic conditions of variability required for the process. Furthermore, all prototypes that have been already realized are not able to work at room temperature (LIU; O'NEILL; SWARTZLANDER, 2013). Instead, Perez-Martinez et al. (2007), Macucci et al. (2003) and Smith et al. (2003) reported their physically implemented devices working in the range of milikelvin.

The challenges imposed by the lithography process and operation temperature do not necessarily impede the realization of the semiconductor prototypes, since they are manufactured only for proof of concept purposes. Nevertheless, they make the type an unlikely choice for the mass production of the QCA devices.

2.1.6.3 Molecular

The molecular type represents the reunion of several desirable characteristics for a QCA device: The achievement of speeds in the Terahertz range, operation at room-temperatures, cell sizes of 2nm or smaller and mass production fabrication enabled by means of the self-assembly process (LIU; O'NEILL; SWARTZLANDER, 2013).

A molecular QCA device consists in a single molecule, in which charge may tunnel between specific sites. For the benefits mentioned above, the type has attracted considerable interest from some research groups around the world. The molecule $\{(\eta_5 - C_5H_5)Fe(\eta_5 - C_5H_4)\}_4(\eta_4 - C_4)Co(\eta_5 - C_5H_5)^{2+}$, synthesized and characterized by Jiao et al. (2003), has four ferrocene groups strategically located at the corners of a square-shaped structure. It is introduced on the theoretical chemistry study by Lu and Lent (2004) as a candidate for the molecular QCA device. The work results support that $\{(\eta_5 - C_5H_5)Fe(\eta_5 - C_5H_4)\}_4(\eta_4 - C_4)Co(\eta_5 - C_5H_5)^{2+}$ is able to encode binary logic states due to its bistable electronic feature. Furthermore, the study also indicates that the molecule can switch its logic state due to electrostatic interactions among its neighbors.

Besides $\{(\eta_5 - C_5H_5)Fe(\eta_5 - C_5H_4)\}_4(\eta_4 - C_4)Co(\eta_5 - C_5H_5)^{2+}$, other molecules have been indicated as possible molecular QCA devices in (LENT; ISAKSEN; LIEBERMAN, 2003) and (LENT; ISAKSEN, 2003). However, as pointed out by Pulimeno et al. (2013), none of them may be considered as suitable candidates for real systems, since the works have analyzed the molecules in vacuum, thus comprising ideal systems.

Moreover, there are no reports of experimental results in whose such molecules perform the function of a QCA cell. Indeed, a very reduced number of experimental attempts have been carried out in order to find a suitable molecule for the real QCA paradigm. The first part of a work performed by Li, Beatty and Fehlner (2003) introduces a novel unsymmetrical heterobinuclear, two-dot, $Fe - Ru$ candidate molecule. The charge transfer to a film of $Fe - Ru$ molecules was measured and reported in the further work (LI; FEHLNER, 2003).

However, even though the aforementioned works represent a progress to the molecular QCA type, further work still need to be done in order to enable the devices manufacturing. To date, there are no reports of molecular QCA prototypes already physically realized. Finally, since the dimensions involved in QCA fabrication are quite small, a high precision manufacturing process is required in order to assemble operational molecular cells. The lack of control on the technological process represents another critical challenge imposed to the Molecular Quantum-Dot Cellular Automata (MQCA) paradigm besides the choose of an appropriate molecule (LIU; O'NEILL; SWARTZLANDER, 2013).

2.1.6.4 Magnetic

The Magnetic Quantum-Dot Cellular Automata has emerged as a QCA type in which the devices operate through magnetic interaction between nanoparticles rather than electrostatic interaction between trapped charges, as reported for all the other classes previously described (subsections 2.1.6.1, 2.1.6.2 and 2.1.6.3). The magnetic QCA type has been commonly referred in the literature as Nanomagnet Logic (NML). The information is encoded to a NML device due to its single domain magnetic dipole. Despite some particularities, such as the interaction class by which information is transmitted and the clocking organization, both electrostatic and magnetic cells have analogous polarization vectors. Thus, NML possess some of the most remarkably characteristics of other QCA types, as the ultra low power consumption and operation at room temperature (molecular QCA).

Several NML logical and fundamental components have been already physically realized (IMRE et al., 2006), (ORLOV et al., 2008), (VARGA et al., 2010), (PULECIO; BHANJA, 2010), (NAKATANI; NOMURA; ENDO, 2009), (NIEMIER et al., 2010). For instance, (IMRE et al., 2006) reports the first physically implemented NML logical component - a three-input majority gate, in which five 135x70x30 nm^3 rectangular devices were implemented by means of nanomagnets. The devices were placed in a cross-shape arrangement, in such a way that the central nanomagnet was surrounded by the four others. Three of the four surrounding devices represent the inputs, while the remaining nanomagnet plays the output device rule. All the possible logic states combinations were tested at the inputs of such majority gate, which yield 25 % of correct results at the output. Although it might seem a non-expressive percentage, the authors highlight that the probability of all eight nanomagnets assuming the correct orientation is less than 0.4 %, thus the correct results cannot be attributed to random events. More reports of physically implemented logical components may be found in (NAKATANI; NOMURA; ENDO, 2009) and (NIEMIER et al., 2010). They comprise the gates NAND/NOR and AND/OR. Both were implemented through rectangular devices of 200x100x10 nm^3 and 150x60x40 nm^3 dimensions, respectively.

Some works focus on predicting the performance of magnetic QCA, which is an essential step toward the consolidation of future NML systems. According to Csaba et al. (2002), the switching speed of magnetic devices may be calculated as a few hundred MHz, assuming that the magnets ordering is performed through adiabatic clocking. Such expected speed is far behind from that observed for the state-of-art CMOS devices, which is the range of Gigahertz. However, besides such fact counts negatively to NML, magnetic devices may be considered as options for systems which not require much speed but an extremely low power consumption. As highlighted by Crocker, Hu and Niemier (2010), the estimated power dissipation in NML is lower than in the sub-90nm CMOS technology.

Csaba et al. (2004) predict a power dissipation value of 10 kT at $10^{-7}s$ for a NML device of 120x60x20 nm^3 dimensions.

NML has been pointed out as a promising choice for the physical realization of QCA systems, since the challenges regarding to its manufacturing process seem to be less critical in comparison to those found in the other classes. Nevertheless, there are difficulties to be overcame in order to consolidate the magnetic QCA. The most of these challenges are related to the hybrid integration between the nanomagnets and the current technology, i.e. the control of the inputs, outputs and clocking.

2.2 Robustness

Regardless of the future QCA systems shall be implemented using self assembly or lithography, defect rates tend to rise substantially due to the high susceptibility of the devices to the variability of the manufacturing processes (HUANG, 2010). Hence, the design of robust QCA structures is a mandatory step towards the consolidation of such emerging nanotechnology.

This section is dedicated to elucidate the key concepts regarding the robustness of the future QCA systems. As defined in (EL-MALEH; AL-HASHIMI; MELOUKI, 2008), the robustness, i.e. defect tolerance, of a structure or system refers to its capability of absorbing a number of defects and unusual conditions and still be able to perform its functions.

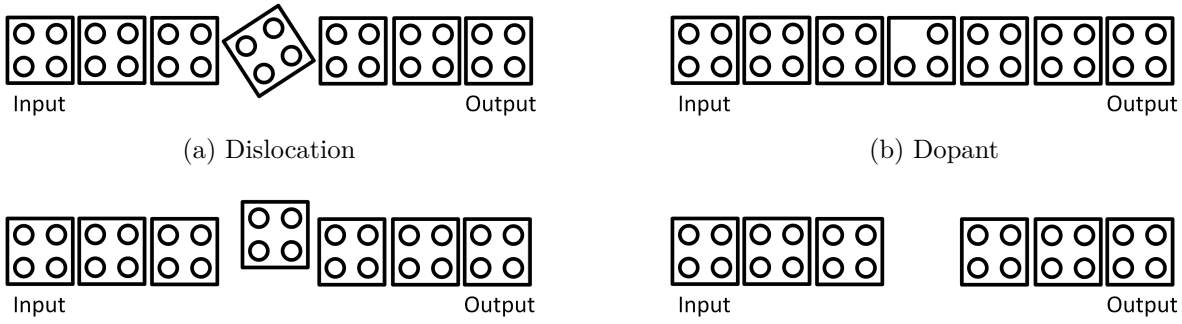
2.2.1 QCA Defects Modeling

As already stated in the Section 1.4, in the context of this work, defects are flaws of the cells of a circuit, generally caused by manufacturing process variations. Defects are subject of several researches for different technologies, such as CMOS (BLYZNIUK et al., 2001), Carbon nanotubes (CHARLIER, 2002) and QCA (DAI; WANG; LOMBARDI, 2010). Defective cells might lead to errors, i.e. unexpected deviations in the behavior of the system. In the circuit's context, an error occurs when, given a known input vector, the state of the outputs is unexpected. However, defects not necessarily imply in the erroneous behavior of the circuit. As long as the function of a defective circuit is properly performed, it cannot be considered as erroneous.

The researchers are always looking forward to create methods for enhancing the systems robustness, i.e. increasing the system capability to get along with defects and operate under unusual conditions. Therefore, since the consequences of the defects may vary from one system to another, the emerging of efficient new strategies for robustness enhancement depends strongly on an efficient defect characterization, i.e. defects modeling.

According to Dai, Wang and Lombardi (2010), the defects more likely to occur in the QCA technology may be categorized between two distinct phases of the manufacturing process: The synthesis phase (where the individual cells are manufactured) and the deposition phase (where the cells are attached to a surface). Synthesis defects may result in a cell with extra or missing dots, while deposition defects are related to the misplacement at placing individual cells in specific locations. The defects modeling adopted in this work is depicted in Figure 8. It comprises four defect classes, from both phases of the manufacturing process, which were named accordingly to the classes reported in (ARMSTRONG; HUMPHREYS; FIJANY, 2003). Dopant defects are likely to occur in the synthesis phase of the manufacturing process, while dislocation, interstitial and vacancy defects are related to the deposition phase.

The dislocation defects are caused by cells that are moved around its axis (rotated), as depicted in Figure 8a, while the dopant defect occurs when a QCA cell has one or more extra or missing dots. Such situation is exemplified in Figure 8b. Furthermore, a misaligned (in relation to the horizontal, vertical or both axes) device (Figure 8c) is called a interstitial-defective cell, while the absence of the entire device is referred as the vacancy defect (Figure 8d).



(a) Dislocation (b) Dopant

(c) Interstitial (d) Vacancy

Figure 8 – The four defect classes (dislocation, dopant, interstitial and vacancy) used in this work. They are exemplified through a wire in which the fourth (middle) cell is always defective.

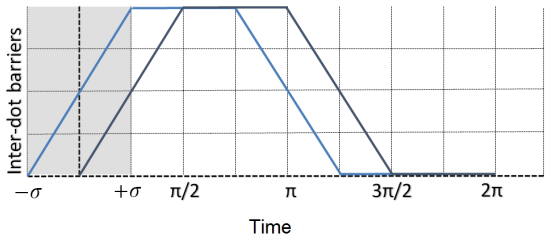
The consequences of a defect vary from one defect class to the others, which results in distinct levels of concerns on robustness. The effects of a dopant-defective cell to the behavior of a QCA circuit are almost always fatal. Besides the missing/extra dot makes the switch between the distinct logic states more difficult, it can also introduces wrong information to be propagated forward. On the other hand, a misplacement-related defect offers less damage to the circuit operation, since only significant positioning deviations are likely to induce the erroneous behavior of the circuit (HUANG et al., 2004).

2.2.2 QCA Clocking Phases Shifts Modeling

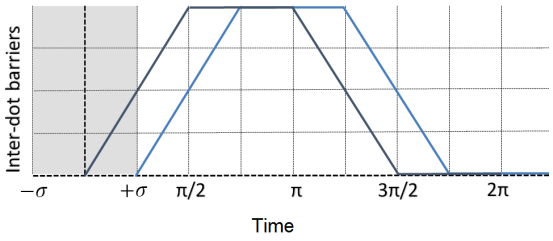
Besides the defective cells, the behavior of a QCA system may be substantially affected due to shifts in the phases of the clock signals (OTTAVI et al., 2007), (KARIM et al., 2009). As previously explained in the Section 2.1.4, the clock signals are provided by an external circuit, which is also subjected to defects and unusual operation conditions, such as temperature effects. A defective clocking circuit may result in the addition of a standard deviation σ to the natural phase shift P of the clock signals. Since the QCA is highly dependent on a synchronous information flow, such unusual condition may lead the outputs of the QCA circuit to an erroneous state.

The phase shift P for deviated clock signals may be modeled as: $P = (\pi/2) \times i \pm \sigma$, where i is the sequential clocking zone identifier, such as $0 \leq i \leq 3$, and σ is the standard deviation introduced by the external clocking circuit defective condition. According to (OTTAVI et al., 2007), σ values higher than $\pi/4rad$ would increase the probability of having two clocking zones whose phases are inverted, a condition that is unlikely in reality. Thus, a reasonable interval for the clocking phase shift standard deviation is $0 \leq \sigma \leq \pi/4rad$.

The regions shaded in gray on both graphs depicted in Figure 9 represent the $\pi/4rad$ boundaries for the standard deviation σ in the clock signal phase. According to the model adopted in this work, the clock signal is allowed to assume any phase shift between such boundaries.



(a) A clock signal, depicted in blue, whose phase is advanced by $\pi/4rad$ relative to the reference signal, shown in black.



(b) A clock signal, depicted in blue, whose phase is delayed by $\pi/4rad$ relative to the reference signal, shown in black.

Figure 9 – The boundaries for the standard deviation in the clock signal phase.

The deviations in the clock signals phases are likely to cause errors in the output signals of the QCA circuits, since they potentially affect the correct information sequencing. Such errors may manifest themselves in one of two possible ways, which are unwanted delays or logic states inversions (KARIM et al., 2009). The unwanted delay error occurs because the clocking zone attributed to the output cell latches out of sequence, so the information is propagated forward either sooner or later than expected. Finally, inversions are likely to occur whether an out of sync latching takes place in a diagonal arrangement of QCA cells.

3 Related Works

This chapter introduces some of the most relevant related works regarding the robustness of QCA structures. Its contents are divided into four subsections. The development of defect-tolerant structures is discussed in the first sub section, while the devising of methodologies for error analysis in defective structures is the subject for the second subsection. Thereafter, in the third part of the chapter, the state-of-art of the development of strategies for enhancing the robustness of clocking circuits is introduced. Finally, a description of the methodology already reported in the literature for the analysis of errors due to phase-deviated clocking signals in QCA structures is reported in the last subsection.

3.1 QCA Defect-Tolerant Structures

Several works report the application of robustness enhancing techniques in the QCA paradigm. Researchers have proposed robust QCA structures able to perform tasks of distinct complexity levels, such as components and circuits. For all works, simulations were performed with 18x18 nm^2 cell technology.

Beard (2006) introduces a defect-tolerant NOT gate, whose operation principle is based on a redundant blocks structure. The input signal is split among two paths and synthesized together after the polarization state inversion, that is enabled by two cells positioned in diagonal. Tests for such robust NOT gate were performed using the simulator QCADesigner, version 2.0.3 (WALUS et al., 2004). Misalignment defects were manually inserted into QCA cells. The maximum displacement tolerated by each cell in the design was determined by independently moving them and measuring its resulting polarization level. Polarization values below 40 % of the theoretical limits (+1 and -1) were considered insufficient to drive the adjacent cells and transport the information, leading the output to an unexpected logic state. The results indicated that the input cell tolerates the highest displacement values (44 nm to the left) while the cell after the diagonal arrangement, responsible for receiving the signal immediately after the polarization inversion, may be moved by only 6 nm without inducing an unexpected logic state at the output.

Fijany and Toomarian (2001) introduce the defect-tolerant three-input Block Majority Gate, which consists in a regular array of precisely placed QCA cells that performs the majority boolean function. Similarly to the standard majority gate introduced by Tougaw and Lent (1994), each one of the three inputs and the output are positioned at the four sides of the structure. All results presented in (FIJANY; TOOMARIAN, 2001) were obtained with blocks of 11x8 cells, despite the authors observed that a minimum block size of 5x4 cells is enough to preserve the robustness characteristics of the structure.

Considered defects were displacement and vacancy, and the analysis of the functional and non-functional devices was performed through simulation by using the tool AQUINAS Lent (1997). The paper does not report quantitative results, *i.e.* the error-free simulations rate for the Block Majority Gate. However, good observations regarding the resilience of the structure for misaligned and missing defective cells were highlighted in the final conclusion.

Another defect-tolerant three-input majority gate is introduced in (FARAZKISH; SAYEDSALEHI; NAVI, 2012). It consists of nine core cells in a square-shaped disposal, thus a configuration of 3x3 devices. The core of the majority gate is surrounded by another four cells placed at the middle of each of its four sides, *i.e.* the inputs and the output. The redundancy provided by the cells added to the core of the structure are responsible for the defect-tolerance enhancement. The defects modeling comprises three defect classes (misaligned, missing and rotated cells). In order to evaluate the robustness of the devised majority gate, Farazkish, Sayedsalehi and Navi (2012) computed the resulting system kink energy in the presence of a defective middle cell. Moreover, simulations were performed by means of the tool QCADesigner version 2.0.3 with the purpose of ensuring the results of such physical proof. The paper does not report the details of the defects insertion procedure, *i.e.* the number of simulations performed, error-free percent and the range of displacements/rotation angle for defective cells. However, it is stated in the conclusion that the presented structure demonstrates significant improvements in terms of area, complexity, and robustness in comparison to previous designs.

Additionally to the three-input robust defect-tolerant gates presented in (FIJANY; TOOMARIAN, 2001) and (FARAZKISH; SAYEDSALEHI; NAVI, 2012), in a more recent work, Roohi et al. (2014) report the design of a robust five-input robust majority gate. The proposed structure is symmetrical, which enables a redundant mechanism similar to that reported in (BEARD, 2006) for robustness enhancing. The design presented is also flexible and expansible, and the paper exemplifies its use to design a set-reset latch and a full adder. Finally, the expectations about the robustness of the five-input majority gate proposed were confirmed by means of simulations using the tool QCADesigner version 2.0.3. Misalignment defects were manually inserted into the cells of the majority gate, while the logical state at the output is evaluated. The results indicated that the robustness may vary among different positions within the structure. Tolerated displacement values are between 6 nm to 14 nm.

Many papers report the design of defect-tolerant circuits besides the components aforementioned. Undoubtedly, the majority of the works found in the literature focus on the design of QCA full adders, since they are essential blocks to design more sophisticated systems as the ALUs of the processors. Farazkish (2015) introduces a robust version of the original first full adder reported in the literature by Tougaw and Lent (1994). The

defect-tolerance in such circuit is achieved by replacing the five regular three-input majority gates (TOUGAW; LENT, 1994) by majority blocks of 3x3 cells size. Furthermore, some QCA wires within the circuit were duplicated in order to create redundancy. The defects modeling mentioned along the paper comprises four defect classes which are likely to happen at synthesis phase: Misalignment, omission and rotation of the cells. Unlike the most of the works regarding QCA defect-tolerance, the analysis does not proceed by means of simulations. Instead, the full adder robustness enhancing is evaluated through physical proof, *i.e.* the interaction among all cells within the design is computed by means of the kink energy. The paper reports an error-free rate of 66.66 %, obtained from nine specific situations, in which one cell at a majority gate is missing at a time.

One defect-tolerant full adder, one 4-bit RCA and one 8-bit RCA are presented by Sen, Rajoria and Sikdar (2013). The full adder has a dense structure, which comprises thirty-one cells distributed on five layers. The multi-layer approach for QCA circuits design is used in order to minimize the area occupied by a circuit. The full adder total area is $0.01\mu m^2$. A five-input structure is used to compute the sum. Three of five inputs are within the main layer, while the remaining two others are placed on different layers above and beneath and connected to the majority gate by means of the two via layers. The carry out bit is computed from the result of a co-planar three-input majority gate at the main layer. The defects modeling considered in this work comprises misalignment, displacement, omission and addition. The paper reports results regarding the defect-tolerance analysis for each cell in the full adder, except for the vias. The results —obtained through the simulation tool QCADesigner —show a highly sensitive device (core) cell for the five-input majority gate, since it can tolerate only the displacements or misalignments within the range of 1.9 - 2.0 nm. As for the omission and addition defects, regardless of the layer on which a cell is missing or added, at least one output yield unexpected results.

To date, the most compact defect-tolerant full adder and a four-bit RCA are introduced in (ROOHI; DEMARA; KHOSHAVI, 2015). The RCA is designed from the interconnection of four full adder blocks. The full adder has only twenty-three cells distributed on three layers. Two three-input modified majority gates were used in order to compute the sum and carry out outputs. The first one was designed from diagonally placed wires, while the second, most known as rotated the majority gate, has the four cells surrounding its device (core) cell clockwise rotated by ninety degrees. The defects modeling considered in this work comprises misaligned, displaced, missing and extra cells. The paper presents the results of the defect-tolerance analysis for the full adder. Although the paper reports a simulation waveform for the defect-free RCA, such circuit is not tested against defects. Considering the cells on all layers, the most critical value for misalignment and displacement is 4 nm. Such value refers to a cell in the middle layer, which serves as the via between the two majority gates in the design. Regarding to the tests for extra cells, the results presented shown that about eight to fourteen cells can be added to the full

adder circuit at any layer without causing errors at the outputs. On the other hand, the circuit is more sensitive to omission defect, since at least one cell removed from the first or second layers yield erroneous outputs. In the third layer, three cells may be removed without cause errors. All the simulations in this work were performed by means of the tool QCADesigner version 2.0.3.

According to the definitions introduced in the beginning of this work (Section 1.4), QCA systems may be designed by interconnecting circuits in order to perform a more specific task. Therefore, a robust RCA may be considered a system at first glance. To the best of the author's knowledge, there is no reports of systems tested against defects beyond the RCAs. Even though some works present a sort of architectures for N-bit robust RCA, the robustness analysis usually is shown only for the individual full adder blocks. The absence of reports for defect-tolerance behavior in larger structures, *i.e.* systems, may be attributed to the lack of methodologies which allow a comprehensive error analysis for defective structures in an automatic manner. The next subsection focuses on a literature review of the existing methodologies for error analysis in QCA.

3.2 Methodologies for Error Analysis in QCA Structures

According to (DYSART, 2009), the development of mechanisms for investigating the consequences of defective devices in the structures operation is an essential step toward the consolidation of the emerging nanotechnologies. This section is an overview of some of the most representative approaches for error analysis in QCA available in the literature to date. Most works are simulation-based approaches, which means that the cell behavior is modeled through quantum mechanical equations that are computationally solved in order to obtain accurate results on the cells polarization. Except for (ARMSTRONG; HUMPHREYS; FIJANY, 2003), which adopt the tool AQUINAS, the works usually are developed with the aim of the open-source simulator QCADesigner version 2.0.3.

Armstrong, Humphreys and Fijany (2003) report an automatic flow for errors analysis in QCA structures. Such errors are likely to occur due to the presence of one or more defective cells. The methodology applies an extensive defect model that comprises four distinct defect classes: Dopant, dislocation, interstitial and vacancy. The defects are applied to the cells in a structure through Monte-Carlo techniques, then the modified design is passed on to the simulator. Once the simulation is completed, the resulting outputs are compared to a reference, *i.e.* an user-defined threshold, so the eventual errors may be registered. Once a set of simulations are performed, the registered results are accessed in order to generate reports that outcome the mean, variance, and 95 % confidence levels of the specific structure topology for the defect classes applied. Although the methodology is quite good described in the paper, there are no results reported.

Tahoori et al. (2004) introduce an approach for error analysis in QCA structures. Unlike (ARMSTRONG; HUMPHREYS; FIJANY, 2003), it requires a higher level of manual intervention in order to set the test conditions and analyze the results. For each simulation performed, the insertion of defects proceeds according to a pattern pre-defined by the user. The possible defect classes in such approach are omission, displacement and misalignment of the cells. The user must inform the number of defects to be inserted, the index of the defective devices and a parameter d, which represents the shift value for the displaced and misaligned cells. Results are presented for a three-input majority gate, a double wire and an inverter chain. The nature of the errors detected is presented as a correlation between the value of the d parameter and the position of the defective cell. All results of this work are shown by means of several tables, which is not always convenient, especially when numerous simulations are performed. Moreover, there are flexibility constraints for the error analysis methodology described in such work, since the defect insertion patterns must be manually set by the user.

Schulhof, Walus and Jullien (2007) investigate the effect of random displacements in the cells of some basic QCA components, such as the regular wire, the NOT gate, the three-input majority gate and the coplanar/multilayer crossovers. Two hundred unique simulations were performed for every component, in which the cells are randomly displaced within a circular area whose diameter is within $0 \leq R \leq r_{max}$. The parameter r_{max} was chosen among 0 to 50 % of the cell size. The percentage of error-free simulations is recorded so that the tolerance of such components against displacement defects could be determined. The effect of scaling is also investigated in this work, since simulations for 1 nm, 5 nm, 10 nm, and 20 nm cell sizes were performed. The results indicated that different components have different tolerances to displacement defects. The coplanar crossover and inverter perform the weakest, while the wire is the most robust. The displacement tolerances found are functions of circuit layout and geometry rather than cell size.

Dai, Wang and Lombardi (2010) introduce an information-theoretic approach to evaluate quantitatively the uncertainties in the operation of both regular and defective QCA components. Since the approach is based on non-deterministic models, each structure has an information transfer capacity level that may vary between 0 (the worst) and 1 (the best) values. The device operation is substantially affected by defects, as for the cells size and temperature. Hence, those are the factors included in the statistical modeling of the cells behavior. Regarding the defect classes, displaced and misaligned cells were considered. Along with the statistical models developed, the QCADesigner simulation engine is used to accurately predict the polarization level of all the cells within the component. The described approach is employed to prove that redundant mechanisms are suitable for enhance the robustness of the structures. Although an exact number is not informed, the results reported were obtained from several simulations. They confirm the direct correspondence between the robustness of a defective QCA component and the

use of spatial redundancy, e.g. thick wires and block-shaped structures. The information transfer capacity for the three and five cells-width components are within 10 % to 15 % better, compared to the structures in which redundant mechanisms were not employed. Nevertheless, the potential for information propagation degrades as quick as the values of displacements and misalignments become larger.

The tolerance to rotation defects in QCA components, as the wire, the bend wire, the fanout, the inverter and the majority gate is investigated in (YANG et al., 2012). The work comprises a manual simulation-based approach for defect insertion in QCA structures. For each simulation performed, a rotation angle between 0 and 2π rad, with a $\pi/5$ step, must to be chosen. Then, the cell is rotated clockwise and counterclockwise by the angle selected with several different stimuli applied to the input(s), according to the test vector {1,1,-1,-1,1,-1,-1,1}. The integrity of the signal(s) at the output(s) is evaluated for an 50 % threshold for the logic level expected, then, the results are registered for both error-free and erroneous simulation rounds. By analyzing the results, it is possible to notice different rotation angle tolerances for different QCA devices. Likewise in Schulhof, Walus and Jullien (2007), the inverter is the less robust structure among all tested, while the regular wire performs the best robustness.

The method introduced in (KHATUN et al., 2006) consists in a Monte-Carlo generator for misplacement and missing dots defects within or for QCA cells. A statistical model is developed to simulate the interactions among defective devices in QCA structures and evaluate the influence of the defects to the structure output(s) response under a range of temperatures. Parameters such as success rate (SR) and breakdown displacement factor (BDF) were defined and calculated numerically through the method. The first one refers to the error-free simulations percent, while the latter represents the maximum displacement value that a cell can take without inducing an error to be propagated to the output(s) signal(s). The paper reports the results for a regular wire that were tested against displacement, misaligned and missing/extra defects by means of such numerical method. As expected, the component is more tolerant to all sort of defects at lower temperatures. For the cases presented, the BDF value found was about 3.4 K, which suggests a threshold temperature from which the wire functionality are sharply decreasing. Moreover, the more dots are missing from a cell, the bigger is the impact on the operation of the structure, *i.e.* the SR is likely to decrease by 10 % for each dot taken out of a cell in the wire.

3.3 QCA Robust Clocking Circuits

To the best of the author's knowledge, there is no reports of implemented strategies for robustness enhancement of the QCA phase-deviated clocking signals besides the asynchronous clocking proposed in this work (Section 5).

However, Karim et al. (2009) emphasizes that the maximum polarization level kept at a slightly lower value might help to avoid errors caused by phase-deviated clocking signals. The strategy is based on the creation of a weak on-state, where the cells in the relaxed zone retain some residual polarization. Nevertheless, the mechanisms involved in such strategy are not fully understood, thus further work needs to be done in order to explore its potential.

3.4 Methodology for Error Analysis in Phase-shifted Clock Signals

Besides defective cells, defective clocking circuits may lead to unusual conditions in the clocking signals which are likely to cause errors at the output(s) of a QCA structure. To date, only one method was proposed to explore the consequences of defective clocking circuits for the operation of QCA structures.

The works (OTTAVI et al., 2007) and (KARIM et al., 2009) describe a simulation-based approach for estimating the impact of random phase-shifted clocking signals to the operation of QCA components. The method was implemented in the simulator QCADesigner version 2.0.3. For each structure, a set of 1,000 simulations is performed according to the following steps. First, a defect-free simulation determines the behavior of the component under ideal clocking conditions. Second, a variable $X = i \times \pi \pm \tau$, which characterizes a Gaussian probability distribution, must be set in order to determine the shifts values. The index i represents the clock zone attributed to the cell, while the parameter τ refers to the phase deviations, which are randomly chosen within a 0.04 rad width range. During the third step, the reference results obtained from the first step allow the automatic comparison against simulations with phase-shifted clock signals in order to determine if the circuits continue to operate properly. Finally, after all simulations, the success rate is calculated as the percentage of circuits whose output(s) pattern behavior is not substantially affected due to the presence of phase-shifted clocking signals.

According to the results reported in the aforementioned work, the regular wire is the QCA structure less susceptible to errors due to phase-deviated clock signals. On the other hand, the fanout of 2 and the fanout of 3 performed the worst in the presence of shifted clocks. For all the structures tested, a decreasing success rate was observed as a linear function of increasing shifts values.

4 QCA Defects Simulator

This chapter introduces the QCA Defects Simulator developed in this work, which is based on a novel methodology for analysis of errors related to defective cells or phase-shifted clock signals. The tool QCADesigner version 2.0.3 is extended by a defects simulation module in order to provide support to an automatic process for evaluation of the structures, which provides the error-free simulations rate and the design heat map as the output data.

The remaining contents of the chapter is divided into three main subsections. The first one refers to the introduction of the novel methodology for defects insertion and error analysis for QCA. The intermediate subsection describes the defects simulation module that is implemented as an extension for the tool QCADesigner. At last, the third part of this chapter introduces the means by which the output data is presented.

4.1 Methodology

The majority of the error analysis methods already reported in the literature for the QCA paradigm proceed to the manual defect insertion, such as in (TAHOORI et al., 2004) (DAI; WANG; LOMBARDI, 2010) and (YANG et al., 2012). Nevertheless, there are some approaches that enable the defect insertion and results analysis through automatic process, as described in (ARMSTRONG; HUMPHREYS; FIJANY, 2003), Schulhof, Walus and Jullien (2007), (KHATUN et al., 2006) and (KARIM et al., 2009). However, almost all automatic methods reported are not enough flexible to allow the insertion of multiple defect classes into the cells in a same structure at the same time. Moreover, the error analysis approaches usually use fixed parameters for the defects value, as the displacement/misalignment shifts, rotation angles and the number of extra/missing dots in a cell (TAHOORI et al., 2004), (DAI; WANG; LOMBARDI, 2010) and (YANG et al., 2012). A most complete approach for error analysis for QCA structures is reported in (ARMSTRONG; HUMPHREYS; FIJANY, 2003). It allows a flexible defects insertion by means of probability values and further settings. The more detailed description of the method may be found in the Section 3.2. However, the paper does not report any results.

This work introduces a novel simulation-based methodology for error analysis for QCA, which provides support for two frameworks of defect insertion: to the clocking circuit and into the cells of a structure. The latter framework, which has already been published in the Proceeding of the 28th Symposium on Integrated Circuits and Systems Design (REIS; TORRES, 2015), allows that four defect classes can be freely combined and iteratively inserted into the devices within a design according to the settings of one of three possible probability models. The behavior of the structures in the case of defective

clocking circuits may be verified through the addition of random shifts to the phases of the clock signals. No matter if the consequences of a defective clocking circuit or of defective cells are being analyzed, the error detection occurs by means of comparisons between simulations results of a reference structure, *i.e.* without the presence of unusual conditions, and of the very same structure subjected to defects. Occasional error events are registered for each simulation performed. The number of iterations necessary for the completion of a full characterization round, also called the round stop criteria, should be verified by means of an algorithm that constantly monitors the error-free simulations rate along all the process. Such algorithm should determine the achievement of the round stop criteria by detecting variations within a range of tolerance along a fixed number of iterations.

A flow chart, which comprises all the methodology steps grouped into three primary categories, is illustrated in Figure 10. The first category, named Initial Procedures, comprises the parameters setting step. Such initial configuration should precede to the insertion and simulation of defects into the cells of the QCA structure or to the addition of shifts to the phases of the clock signals. Once the parameters are properly set, the flow continues to the Intermediate Procedures. Such step comprises the insertion of defects and iterative analysis of the behavior of the outputs. The round stop criteria is checked in each iteration, so that when its condition is achieved, the methodology is read to continue to the Final Procedures, which comprise basically the analysis and the generation of output data regarding the final results.

The methodology flow chart is briefly explained in the following subsections (4.1.1 to 4.1.3). Since the QCA Defects Simulator introduced in this work is devised to allow a flexible insertion of defects and to provide an efficient mean for visualizing and interpreting the results, all the defect classes, probabilities, round stop criteria elements and further details concerning the novel approach are defined by means of user-set parameters. The next subsection describes the methodology initial procedures, which consists primarily in the parameters setting procedures. All the parameters nomenclature may be found at the methodology flow chart previously depicted in Figure 10.

4.1.1 Initial procedures

The initial procedures of the methodology require user interaction. They comprise the structure selection, the parameters setting and the start of the iterative process for error simulation. First of all, a design to be analyzed must be selected. It should be implemented in a tool like QCADesigner. Once the design is selected, error simulation parameters must be set. The predicted parameters are briefly described in the items 1 to 6.

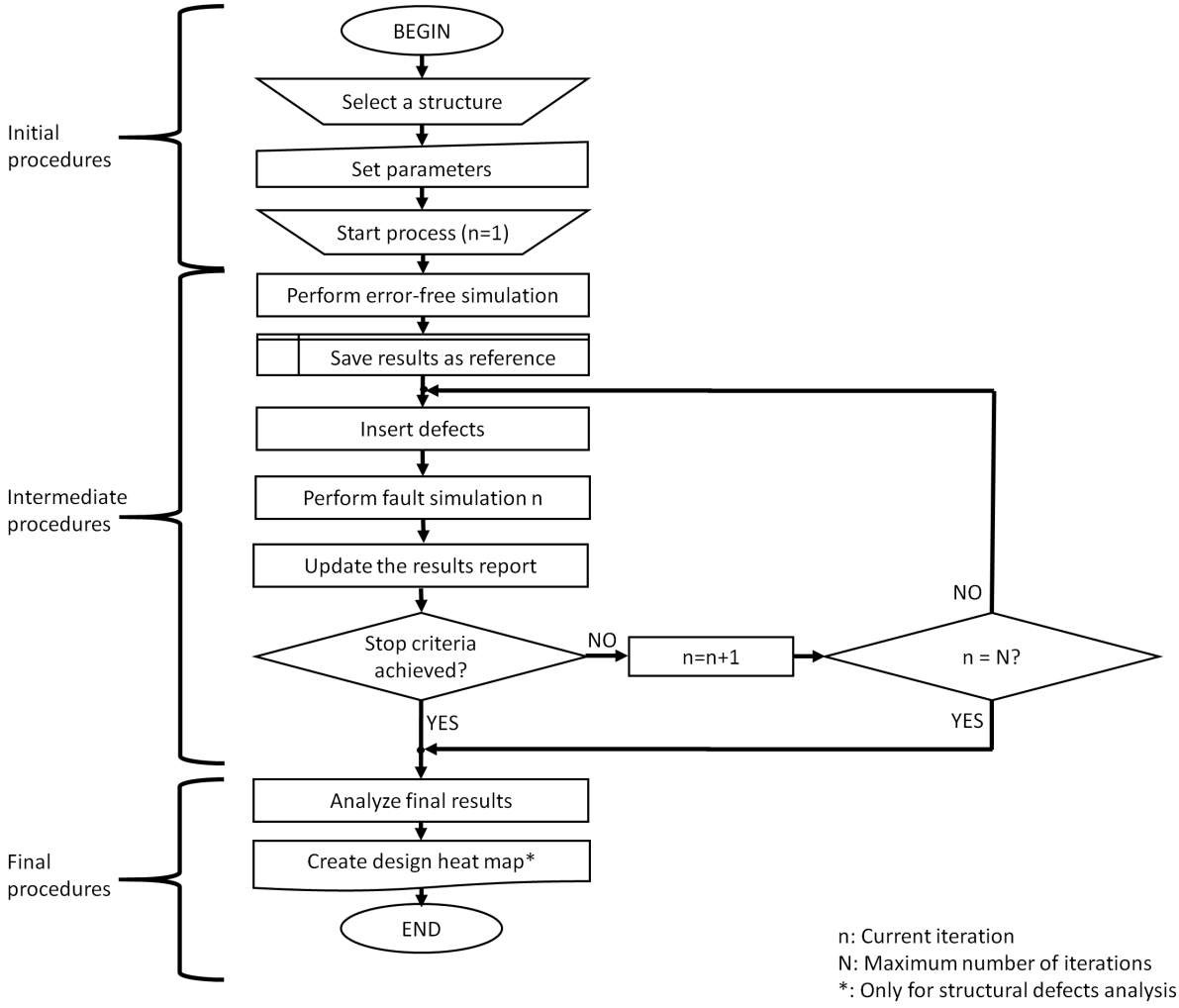


Figure 10 – Methodology flow chart.

1. Sample interval
   The 'Sample Interval' parameter defines the frequency with which the output signals of a QCA structure should be read. The parameter value is a percentage of the frequency of the clock signals, e.g. a value of 50 % means that the sample frequency is half of the frequency of the clock signals.

2. HIGH threshold (%)
   The 'HIGH threshold' parameter determines the percentage of the value of polarization (+1) from which the logic state is interpreted as logic 1.

3. LOW threshold (%)
   The 'LOW logic level' parameter determines the percentage of the value of polarization (-1) from which the logic state is interpreted as logic 0.

4. Round configuration
   The round configuration comprises a subgroup of parameters related to the round stop criteria, which is assessed by a specific algorithm that determines the completion

of the methodology 'Intermediate Procedures'. Such parameters are briefly described in the following.

a) Error-free rate tolerance (%): Establishes a reasonable basis for the error-free simulations rate variation, *i.e.* the maximum ordinary variation allowed for the error-free simulations rate.

b) Stable iterations (units): This parameter determines a number of iterations for such the error-free rate tolerance (%) must be met. Once the variation of the error-free simulations rate is within the limits established by the 'Error-free rate tolerance' parameter for the number of iterations determined by the value set in the parameter 'Stable iterations', the round stop criteria is complete. A specific algorithm, thus, should identify the achievement of such condition in order to determine the beginning of the Final Procedures. For instance, if the tolerance is set to 10 % and the number of stable iterations required is 100, the round stop criteria to be accomplished is that the error-free rate variation remains within those 10 % variation limits for at least 100 successive characterization rounds.

c) Maximum number of iterations (units): Determines the maximum number of times the whole process (defect insertion, simulation and error analysis) is performed. In case of the probability model 'Sequential', this value indicates the maximum number of iterations executed for each cell of the structure. Such parameter aims to avoid that the stop algorithm remains stuck at an unstable condition for ever.

5. Defects type
This parameter regards to the choice of the defects type option for error analysis proceedures. Two options are allowed for the setting of such parameter at this point, as described in the following.

a) Structural defects: When this option is checked, at each defects simulation, defects from four possible distinct classes (item 6a) are inserted into the cells in a QCA structure according to selected probability models (item 6b).

b) Clock phase shifts: When this option is checked, values for the shifts are randomly chosen within a pre-selected range for each one of the four clock signals in the circuit.

The next settings (item 6) are only necessary in the case of the structural defects analysis is selected, otherwise no more parameters need to be set. Therefore, those settings are grouped into the 'Structural Defects Configuration' set of parameters.

6. Structural Defects Configuration

The Equation 4.1 introduces all the conditions to be observed while inserting defects into the cells of a QCA structure. Further information regarding the parameters may be found in the next items 6a and 6b.

$$DIC_{n,i} = S_n \times DC_i \times P \tag{4.1}$$

Where:

DIC : The matrix of defects inserted into the cells of a structure
n : The cell index (n $\in \mathbb{N} | 1 \leq n \leq N$. N is the total of cells of the structure.)
i : The defect classes indexes (0: dislocation, 1: dopant, 2: interstitial, 3: vacancy)
S : The selector for a cell n (0: defects are not inserted, 1: defects are inserted)
DC : The selector for the defect classes (0: class not selected , 1: class selected)
P : Probability value, which depends on the probability model selected

a) Defect classes

This parameter defines one or more classes of defects that can be inserted into the cells of the QCA structure during analysis. The possibilities contemplated in the QCA Defects Simulator are detailed in Section 2.2.1. They comprise four classes —Dislocation, Dopant, Interstitial, Vacancy —that may be freely combined by the user while setting the parameters at the methodology 'Initial Procedures' step. The selector DC_i, introduced in the equation 4.1, is set to one if the defect class is selected by the user. Otherwise, DC is set to zero during the whole characterization round.

Besides the defect classes selection, the actual insertion of a defect into each cell depends on the probability value assigned to every selected defect class. This assignment may vary according to the probability model chosen. Probability models are explained in the next item.

b) Probability model

Probability model defines the strategy of defect insertion into each cell of a design. There are three possible options for this parameter.

i. Sequential: Defects are compulsory inserted into every cell in a design in a sequential manner. That means, a defect class is randomly selected among all the defect classes chosen by the user and inserted into a single cell per simulation. For each iteration, the two processes (defect insertion and simulation) must run for all cells of the design. Thus, for the 'Sequential' probability model, the value of P in equation 4.1 is always one for the

defect class randomly selected among the defined ones and zero for the remaining.

ii. Assignable: One or more defects out of the defined defect classes might be inserted into the cells of a design. The probability of a defect insertion into each cell, the value of P in equation 4.1, is manually assigned to every defined defect class. Defect insertion process must run repeatedly for every n index, that is, from the first to the last cell in the design. Afterwards, a simulation is performed.

iii. Uniform: The defect insertion process for 'Uniform' probability model is analogous to 'Assignable' probability model. However, the probability value for defect insertion into each cell is now fixed. Its value is given by the inverse of the amount of cells in the design. Hence, it is expected to have an average of one failure per simulation.

Probability model selection as well as value assignment for probabilities should consider the device manufacturing process in question. That attribution may not be trivial, especially for emerging nanotechnologies such as QCA, since their manufacturing process is not yet established. Thus, the parameter setting may be based on other mature technologies, whose manufacturing processes are already well consolidated.

After the design has been selected and all parameters have been successful set, the error simulation process is ready to be started. From this moment on, the methodology does not require any further user interaction and the intermediate procedures are ready to be started.

4.1.2 Intermediate procedures

The intermediate procedures of the methodology comprise the defect insertion, simulation and error detection procedures. Each one of the steps are thoroughly described in this subsection. First of all, a defect-free simulation is performed. The result of this simulation, *i.e.* the signal logic states and the polarization level values at the output(s), are saved as reference for determining error events in next simulations.

After, defects are inserted either to the clocking circuit of the QCA system or into some cells of the design, according to the probability model set. Defect levels, e.g. absolute values of dislocation, interstitial and dopant (dot chosen to be removed) from each cell, as well as the clock phase shifts values are randomly defined. In the case in which the structural defects option is set in the 'Defect Type' parameter, the interstitial displacement and misalignment limits correspond to fractions of the defective cell size (width/length), within the 0 to 100 % range. Thus, quantum dots may exceed the limits of a cell, entering

the subsequent cell, depending on the interstitial defect values defined. The boundaries for the displacement/misalignment of a QCA cell are illustrated in Figure 11.

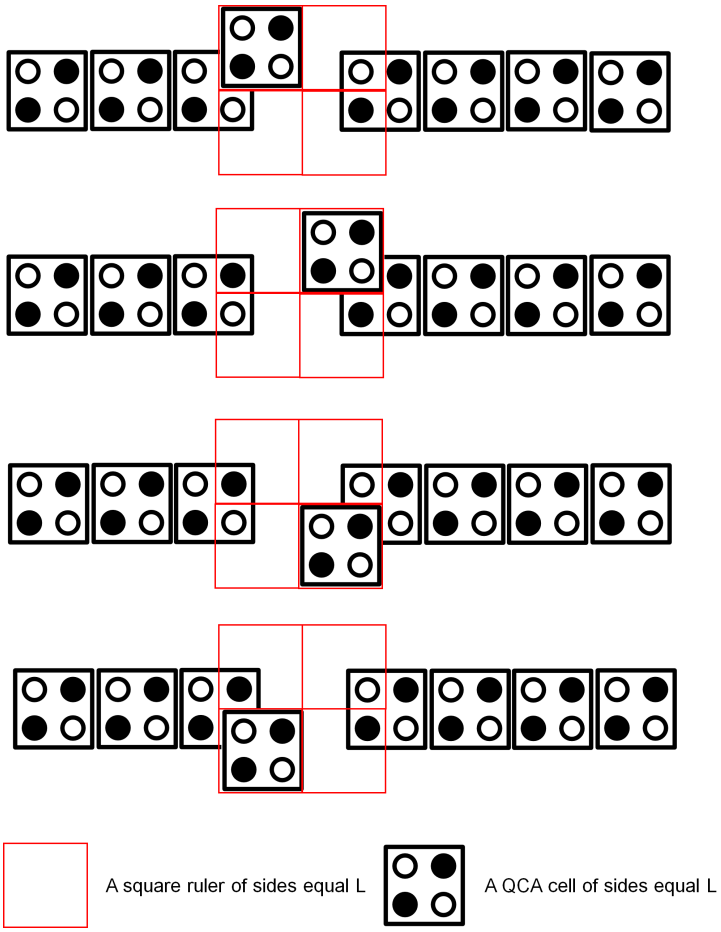


Figure 11 – The boundaries for displacement/misalignment of a cell in the QCA Defects Simulator. The cell is allowed to occupy any position within the limits of the square ruler. Four extreme placements for a defective cell are shown through the QCA wire example.

Bigger values of the 'Maximum Number of iterations' parameter might lead to more possibilities for error analysis, except when the round stop criteria is achieved at an early stage or the parameters 'probability model' and 'defect class' are set simultaneously to 'Sequential' and 'Vacancy'. At this specific situation, the concept of defect level may not be applied and the defective cell in each simulation is pre-defined.

Thereafter, the simulation is performed for the QCA structure in which either the cells or the clocking circuit responsible for delivering the clock signals are defective. At this point, the iterative analysis process is ready to start. The output signal(s) obtained from the defective simulation are compared to those from the reference. The errors eventually detected, as well as the identification of either the defective cells in the structure or the clock phase shifts values are registered. Moreover, the error-free simulations rate is iteratively updated and continuosly saved. The defect insertion and simulation processes,

as well as the iterative analysis, are repeated until the round stop criteria defined by the 'Round Configuration' group of parameters is achieved.

From this moment on, the flow continues to the methodology 'Final Procedures', where the design heat map is created.

4.1.3 Final procedures

The final procedures of the methodology regard to the final results analysis that lead to the design heat map creation. For each cell in a structure, a color from a pre-defined range of colors is used in order to indicate how often defects inserted into this cell led to an error. Thus, the heat map creation is not valid for the analysis of clock phase shifts framework.

Based on the information registered from all simulations performed until the round stop criteria achievement, a cross-reference between error events and defective cells may be established as explained in the following. First, a cells ranking is created. Initially, the weights attributed to individual cells are equal to zero. Then, for each simulation performed, the error-free simulations percent is evaluated in order to determine whether an error event occurred at each one of the outputs in the structure. In the positive case, the weight of the defective cells in such simulation is incremented by one, regardless of the class to which the defect is attributed to.

In the end of the ranking process, a list of the cells sorted from the highest to the lowest weight values allows the creation of a graphical representation of the cross-reference between error events and defective cells, *i.e.* the heat map. More details concerning the heat maps may be found in Section 4.3.

4.2 Implementation

This subsection describes the error analysis module developed in this work, which reproduces exactly the steps of the methodology flow presented in Figure 10. Such module is implemented as an extension to the QCADesigner version 2.0.3.

4.2.1 Error analysis module interfaces

Two distinct interfaces were designed regarding the error analysis extension module introduced on this work. Both of them may be accessed through the corresponding shortcuts added to the same 'Simulation' division at the QCADesigner main menu. Such accesses are named 'Error exploration settings' and 'Error exploration start', as illustrated in Figure 12.

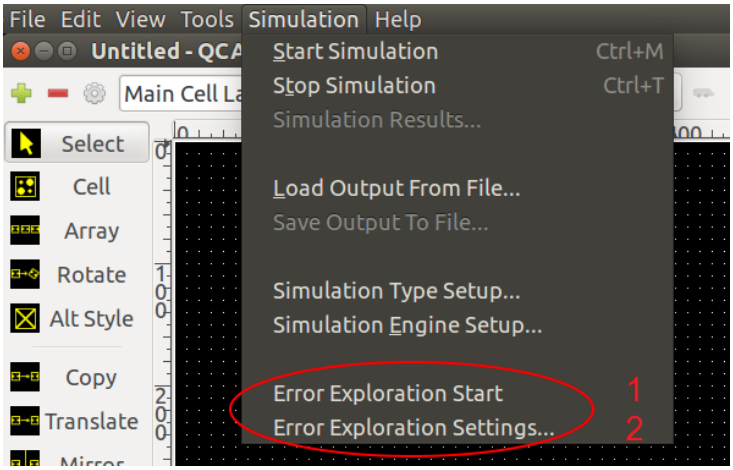
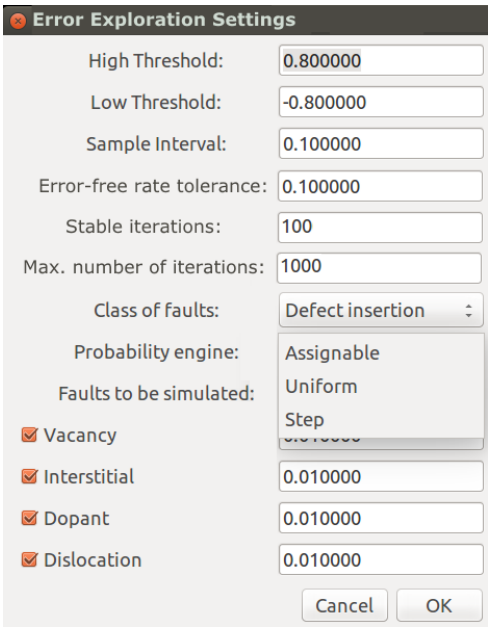
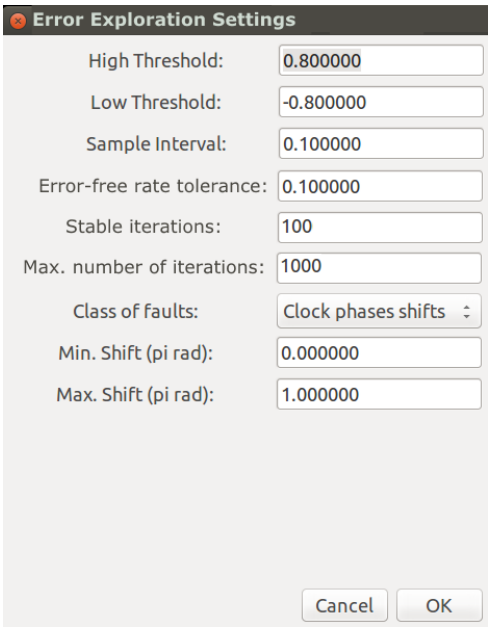


Figure 12 – The two error analysis module interfaces may be accessed through the shortcuts highlighted in red, which were integrated in the QCADesigner main menu.

Before starting a new characterization round, all the methodology parameters, defined in the Initial Procedures (section 4.1.2), must be set through the 'Error Exploration Settings' window, which may be opened by clicking on the 'Error exploration settings' shortcut, labeled as '2' in the Figure 12. Two distinct perspectives for such window are depicted in Figure 13a and Figure 13b. Both illustrations refer to the same object, which is able to change its configuration according to the value set to the parameter 'Simulation Type'.



(a) The parameter setting window opened under the insertion of 'Structural Defects' perspective.



(b) The parameter setting window opened under the 'Clock Phase Shifts' perspective.

Figure 13 – The two distinct perspectives for the 'Error Exploration Settings' window.

By filling in the settings window, the user must keep in mind that the high and low limits for every parameter must to be respected. A summary of parameters range may be found in the Table 1.

Table 1 – List of the available Error Analysis Module parameters that should be set through the specific window, along with its corresponding ranges and units

Index	**Description**	**Options**	**Defects Type**	**Low Limit**	**High Limit**	**Unit**
1	Sample Interval	N/A	Structural/ Clock Phase Shifts	0	100	%
2	HIGH/LOW Thresholds	N/A	Structural/ Clock Phase Shifts	0	100	%
3	Error-Free Simulations Rate Tolerance	N/A	Structural/ Clock Phase Shifts	0	10	%
4	Stable Iterations	N/A	Structural/ Clock Phase Shifts	0	Max. Number of Iterations	iter
5	Max. Number of Iterations	N/A	Structural/ Clock Phase Shifts	0	up to 1,000,000	iter
6	Defects Type	Structural/ Clock Phase Shifts	N/A	N/A	N/A	N/A
7	Defects Classes	Dislocation/ Dopant/ Interstitial/ Vacancy	Structural	N/A	N/A	N/A
8	Probability Model	Assignable/ Uniform/ Sequential	Structural	N/A	N/A	N/A
9	Min. Phase Shift	N/A	Clock Phase Shifts	0	1	π rad
10	Max. Phase Shift	N/A	Clock Phase Shifts	0	1	π rad

Once all the parameters depicted in Table 1 are correctly set, the user should proceed to the methodology 'Intermediate Procedures' steps by clicking on the 'Error Exploration Start' button. When pressed, such button opens a pop up window by which is possible to indicate an output path for the files generated and updated along all the process. Since a valid path and a base filename are correctly chosen, the QCA Defects Simulator starts at its first iteration, requiring no further user intervention. Figure 14 depicts the

window by which an output path, as well as the base name for all files automatically created during the Defects Simulator execution, are indicated.

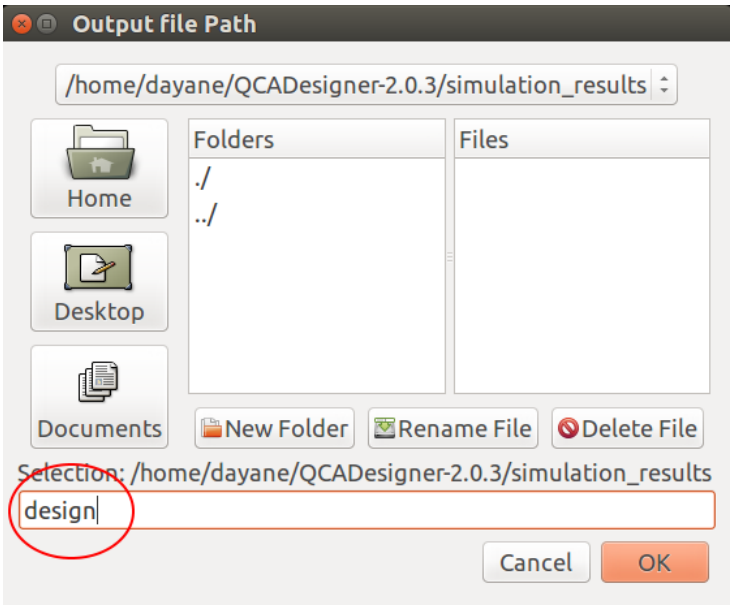


Figure 14 – The error analysis module interface for output files setting and characterization round starting. The basis name field is highlighted by a red circle. Here, the name 'design' was used as an example.

While processing, the QCA Defects Simulator might provide some output messages at the QCADesigner status bar. For instance, when a simulation is performed by means of the Coherence Vector Engine, the following message is shown: 'Coherence Vector Simulation... X %', where X represents the current percent status of the simulation. Moreover, while reading, updating or writing the results files, a message at the status bar indicates the current iteration, the filename and the pendant operation to be executed at that time.

Once the characterization round is done, no more messages are shown at the QCADesigner status bar. The final result files may be found in the path indicated through the window depicted in the Figure 14. Their contents are automatically updated to the most recent version available at the end of the characterization round execution. Moreover, the heat map of the design is created. It consists of a design file similar to the original but with modified colors which represent the distinct levels of weaknesses of the cells throughout the QCA structure. More details about the result files, as well as a description of the heat map concept may be found in the next section.

4.3 Presenting the Results

This section introduces the two possible frameworks by which the output data is presented within the QCA Defects Simulator developed in this work. The first one consists

of an iteratively updated result file, while the latter regards to the creation of the design heat map at the end of one characterization round. The next subsections (4.3.1 and 4.3.2) are dedicated to explore the details of both frameworks.

4.3.1 The Result File

The result file format varies according to the defects type chosen by means of parameter setting. For structural defects testing, the file head includes information about the defect classes considered in the test, as well as the probability model by which the defects are inserted into the cells in a design. After the preliminary head information, the events summary for each simulation file is exhibited, having the indication of the outputs status alongside the eventual erroneous sample indexes. Moreover, the summary carries the indication of the defective cells indexes. The bottom of the results file has the register of the iteratively updated error-free simulations rate, as well as the evolution history of such error-free simulations indice along all iterations of the characterization round.

For clock phase shifts testing, instead of information regarding defect classes and probability models, the file head includes only information about the high and low limits for the shifts values. Similarly to that described for structural defects testing, after the preliminary head information, the events summary for each simulation file is exhibited, having the indication of the outputs status alongside the eventual erroneous sample indexes. Moreover, the summary carries the shifts applied to the four original phases of the clock signals. The updated error-free simulations rate are registered at the bottom of the results file for both structural defects and clock phase shifts testings.

The result files templates for both structural defects and clock phase shifts tests are depicted in Figure 15.

```
1  [CONFIGURATION]
2  DOPANT=                                  % 0/1
3  DISLOCATION=                             % 0/1
4  INTERSTITIAL=                            % 0/1
5  VACANCY=                                 % 0/1
6  PROBABILITY_MODEL=                       % ASSIGNABLE/ SEQUENTIAL/
                                            % UNIFORM
7  REFERENCE_DESIGN=                        % original design path
8  ITERATIONS_COUNT=                        % iteratively incremented from 0 to N
9  NUMBER_OF_CELLS=                         % cells in the design
10 NUMBER_OF_INPUTS=                        % number of input cells
11 NUMBER_OF_OUTPUTS=                       % number of output cells
12 [#CONFIGURATION]
13 [SIMULATION FILE 1]
14 OUTPUT1 =
15 OUTPUT2 =                                    NO ERRORS/ ERRONEOUS
16 OUTPUTN =                                     SAMPLES REGISTER
17 [DEFECTIVE CELLS]
18 DISLOCATION = CELL1, CELL2, CELLN ...
19 DOPANT = CELL1, CELL2, CELLN ...         % index of defective cells
20 INTERSTITIAL = CELL1, CELL2, CELLN ...
21 VACANCY = CELL1, CELL2, CELLN ...
22 [#DEFECTIVE CELLS]
23 [#SIMULATION FILE 1]
24 [ERROR-FREE SIMULATIONS RATE]
25 X %                                      % iteratively updated error-free rate
26 [#ERROR-FREE SIMULATIONS RATE]
27 [HISTORICAL VALUES]
                                            % error-free simulations rate
28 O1, O2, ..., ON                         % along all iterations until
                                            % the stop criteria achievement
29 [#HISTORICAL VALUES]
```

(a) Structural defects result file.

```
1  [CONFIGURATION]
2  MIN. SHIFT=                              % INFERIOR LIMIT
3  MAX. SHIFT=                              % SUPERIOR LIMIT
7  REFERENCE_DESIGN=                        % original design path
8  ITERATIONS_COUNT=                        % iteratively incremented from 0 to N
9  NUMBER_OF_CELLS=                         % cells in the design
10 NUMBER_OF_INPUTS=                        % number of input cells
11 NUMBER_OF_OUTPUTS=                       % number of output cells
12 [#CONFIGURATION]
13 [SIMULATION FILE 1]
14 OUTPUT1 =
15 OUTPUT2 =                                    % NO ERRORS/ ERRONEOUS
16 OUTPUTN =                                     % SAMPLES REGISTER
17 [CLOCK PHASES SHIFTS VALUES]
18 CLOCK 0 =
19 CLOCK 1 =                                % shifts deviations values
20 CLOCK 2 =
21 CLOCK 3 =
22 [#CLOCK PHASES SHIFTS VALUES]
23 [#SIMULATION FILE 1]
24 [ERROR-FREE SIMULATIONS RATE]
25 X %                                      % iteratively updated error-free rate
26 [#ERROR-FREE SIMULATIONS RATE]
27 [HISTORICAL VALUES]
                                            % error-free simulations rate
28 O1, O2, ..., ON                         % along all iterations until
                                            % the stop criteria achievement
29 [#HISTORICAL VALUES]
```

(b) Clock phase shifts result file.

Figure 15 – File results templates.

4.3.2 The Heat Maps

A heat map is a graphical representation of the cross-reference between error events and defective cells, which is obtained from the final ranking of the weaknesses of the cells in a QCA structure, as previously explained in subsection 4.1.3. The heat map is created at the end of a characterization round where structural defects were inserted into the devices in a QCA structure. For each cell, a color from a pre-defined range of colors is used in order to indicate how often defects inserted into that cell led to an error. Figure 16 shows the range of colors applied here and the respective error rates associated to each color.

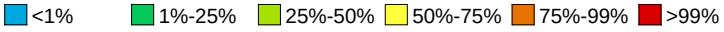


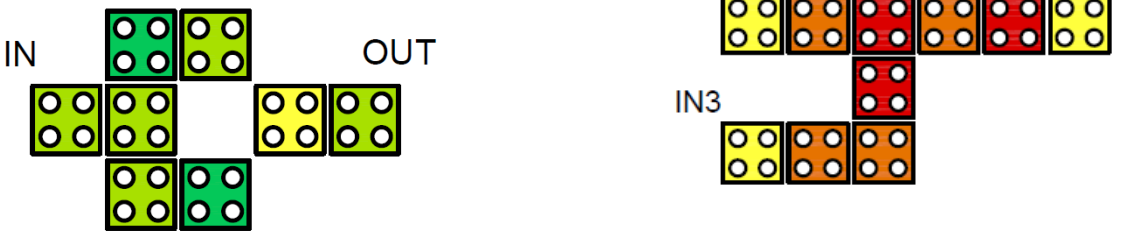
Figure 16 – The range of colors used in the creation of a heat map. Defects inserted into the blue cells led to error events in a circuit in less than 1 % of the simulations, *i.e.*, for every 100 defects inserted into the cell, no more than one of them resulted in an error event. Analogous reasoning may be applied to the remaining colors.

According to the range of colors presented in the Figure 16, structural defects inserted into dark blue cells led to errors at the output signal(s) of a QCA structure in less than 1 % of the simulations, *i.e.*, for every 100 defects inserted into the cell, no more than one of them resulted in an error event at the outputs of the structure. Defects inserted into green colored cells led to errors in 1-25 % of all simulations. Analogous reasoning may be applied to light green, yellow and orange colored cells complying with their respective percentage ranges indicated in the illustration. Defects inserted into red colored cells led to errors in more than 99 % of all simulations in which the cells suffered under a defect.

It is important to highlight that the number of iterations, the probability model and the subgroup of parameters 'Round Configuration' should be carefully set in order to ensure that the colors depicted in a heat map correspond to a realistic representation regarding to the correspondence between defective devices and error events. If the number of iterations is insufficient, wrong conclusions may be draw by analyzing the output heat map. For instance, suppose that a 28-cell structure undergoes defects simulation through sequential probability model, with all the four defect classes defined. Considering that, each cell should be made defective at least four times, so that defects from all the four classes may be inserted into each cell. Thus, a reasonable number of minimum iterations in a characterization round for that situation is four. For each iteration, 28 simulations are performed —since one cell is defective per simulation in the 'Sequential' probability model —yielding a total of 72 simulations, which corresponds to a rate of 4 simulations/cell.

The Figures 17a and 17b depict some examples of real heat maps in order to better illustrate their meaning. The first figure refers to a NOT gate, while the second represents a

majority gate. Since this section does not intend to analyze any results obtained from Error Analysis Module, the heat maps are depicted but not interpreted. Further information about results analysis may be found in the Sections 5 and 6.



(a) A heatmap for a NOT gate tested against all structural defect classes with an uniform probability.

(b) A heatmap for a majority gate tested against dopant structural defects with an uniform probability.

Figure 17 – Examples of heat maps.

The heat maps are important visual resources that assist in the development of strategies for robustness enhancement for the QCA paradigm, since they allow in the identification of weak polarized regions within the structures. Since a weak region is identified, additional cells placement may be a good choice to ensure an extra polarization strength hence decreasing the likelihood of such cells to cause errors to the signal(s) at the output(s). In the next chapter, 5, there are further information about the heat map-based techniques applied in this work, by which the robustness of the QCA structures could be enhanced.

5 Strategies for Robustness Enhancement

This chapter presents the strategies for robustness enhancement of QCA structures explored in this work. They consist of the use of redundant devices, as well as structural modifications aiming at strengthen the regions of weak polarization within the structures. Furthermore, the chapter describes the use of the QCA Defects Simulator proposed in this work (Chapter 4) in order to identify the weak polarization regions within the structures and to verify how effective are the strengthen strategies when applied to those specific regions in order to enhance the structures' robustness. Such analysis is carried out for four basic structures —a regular wire (WIR1), a bend wire (BWI1), a fanout of 2 (FO21) and a fanout of 3 (FO31).

The aforementioned analysis lead to the proposal of new robustness enhanced QCA structures, though, the modified wire (WIR2), bend wire (BWI2), fanout of 2 (FO22) and fanout of 3 (FO32), which may be used to implement more complex components, circuits and systems (Chapter 6).

Furthermore, the last part of the chapter introduces the use of asynchronous clock signals as a solution to enhance the robustness of clocking circuits against clock phase shifts. Some results obtained from tests using the proposed QCA Defects Simulator are also presented. They certify the efficiency of the solution proposed for the basic structures WIR1, BWI1, FO21 and FO31.

5.1 QCA Fundamental Components under Structural Defects

This section describes the tests performed with some QCA fundamental components under structural defects testing framework. The aim of such tests was to devise new strategies for robustness enhancement of the components. The testing procedure, as well as the results analysis and solutions proposed are explained in the following sub sections (5.1.1 to 5.1.5).

5.1.1 Components Selection

QCA circuits and systems are often implemented through some basic logical components, such as logic gates, interconnected by fundamental components such as regular and bent wires, fanouts and wire crossings. According to Wang, Stroud and Touba (2010), it is predicted that interconnects will consume the bulk of chip area in future nanotechnologies such as QCA. Furthermore, even the most basic QCA logical components may host interconnect elements embedded within their structures. The NOT

gate introduced in (LENT et al., 1993) is a typical example of such referred feature. It has an fanout of 2 built-in immediately after its input cell, which serves as the polarization strengthen element before the logical state inversion that occurs by means of a diagonal-positioned cell. For the reasons presented, it is very important to test the QCA fundamental components against structural defects.

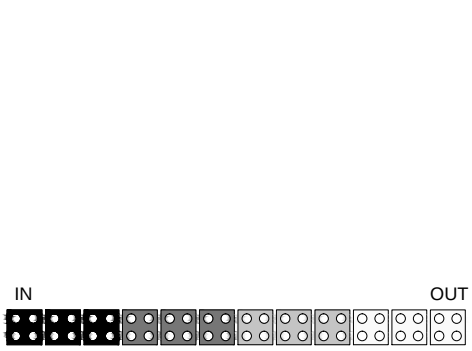
Four fundamental components were selected to be submitted to the QCA Defects Simulator developed in this work, as depicted in Figure 18. The choice of such fundamental components was based on the fact that they are used in almost every QCA structure implemented, as stated in some previous works that also investigated the effect of structural defects to their expected behaviors (YANG et al., 2012) and (KARIM et al., 2009). Both types of wires chosen, *i.e.* the regular and the bend ones (Figs. 18a and 18b), are used to transmit information within QCA structures. While the regular wire performs information transport between aligned structures, the bend wire is usually used to construct the turning when not aligned components need to be interconnected within the structure. Moreover, the fanouts are responsible for the signal distribution task, by ensuring the logic state propagation through different aisles. The fanout of 2 (Fig. 18c) distributes a single signal into other two directions, while the fanout of 3 (Fig. 18d) propagates it into three distinct paths within the structure.

5.1.2 Testing Settings

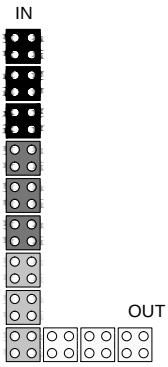
After the choice of the four fundamental components to undergo structural defects testing, the QCA Defects Simulator parameters must be set according to the desired testing conditions. The goal here is to design a robustness enhanced structure that is able to perform reliable under all sort of defect classes comprised in the proposed methodology. In order to do so, for each component, four rounds of tests are performed, each one of them considering a single class of defects at a time. Thus, at the end of the whole testing process, it is possible to have four distinct heat maps that, when analyzed together, allow the identification of critical regions in the structures.

After the defect class selection, the probability model parameter was set. In order to ensure that all the cells of the component would equally host defective cells, the sequential model was used. As previous exposed in Section 4, such model considers one defective cell per simulation. Once all devices of a structure were made defective, one characterization round is complete.

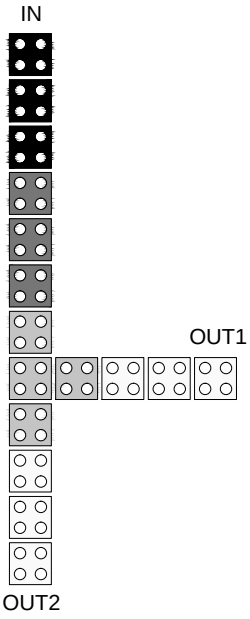
In the first set of tests for each component, the parameter 'Number of Iterations' was adjusted either to 4 (in the tests when the dislocation, dopant and interstitial defect classes are defined) or to 1 (when the vacancy defect class is defined). Thus, for tests with dislocation, dopant and interstitial defects, it was possible to ensure that each cell hosted four variations of the same defect class along one characterization round.



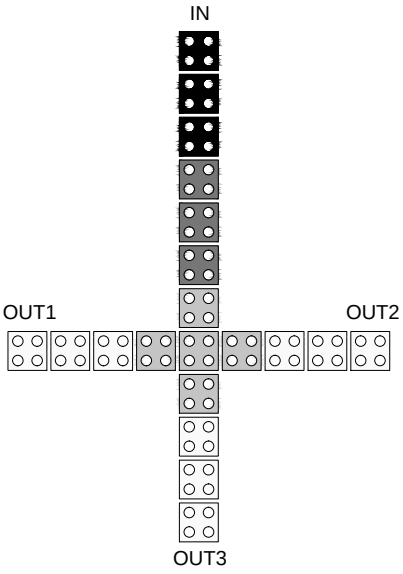
(a) A regular wire.



(b) A regular bent wire.



(c) A regular fanout of 2.



(d) A regular fanout of 3.

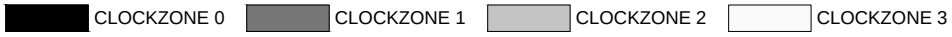


Figure 18 – The four fundamental components selected for undergo defects testing.

In the second set of tests for each component, the parameter 'Number of Iterations' was adjusted to 16, since all the defect classes were defined at the same time. Thus, each cell was likely to host sixteen variations of four combined defect classes along one characterization round.

The parameters 'Stable iterations' and 'Maximum Number of Iterations' were equally set. For the first set of tests, their configured values were the number of cells of each component times 4. Similarly, for the second set of tests, their configured values were the number of cells of each component times 16. The multipliers 4 and 16 aim to determine how many variations among the defined defect classes each cell is likely to host

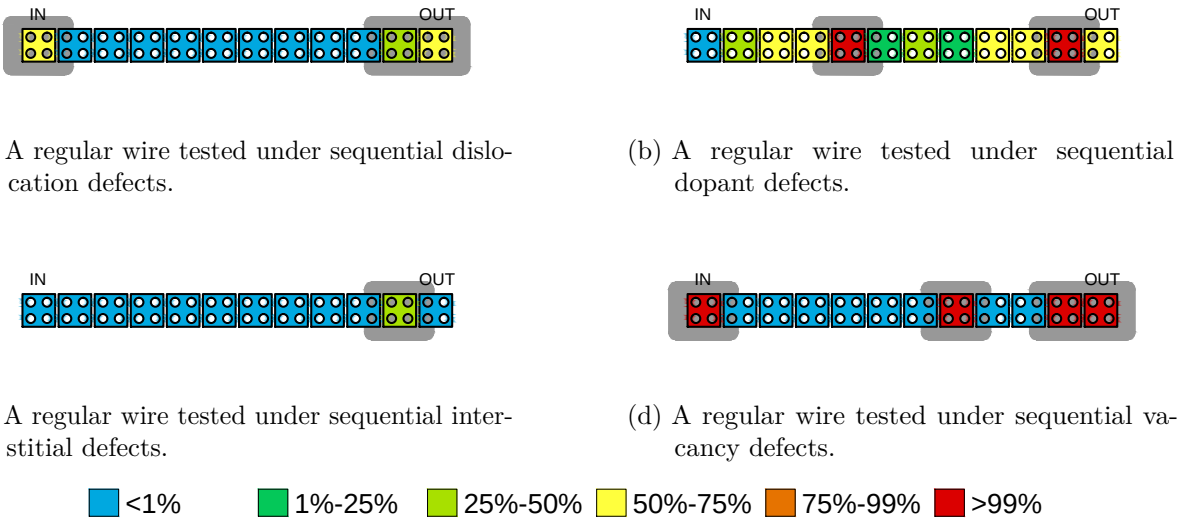
along one characterization round.

Finally, the sampling interval is set to 10 % and the threshold for which a signal is interpreted as logic zero or one is 80 % of the standard polarization level limits (-1 and +1).

Once the aforementioned conditions were adjusted, the heat maps created in the end of each testing round were submitted to a qualitative analysis in order to identify possible critical regions of cells that, when defective, might induce the structure to propagate erroneous signals to the outputs. The method by which such analysis was carried out is described in the next subsection (5.1.3).

5.1.3 Qualitative Analysis of Heat maps

The heat maps created in the previous step of the methodology are now analyzed in order to identify possible critical areas that, when defective, might lead the structure to an erroneous polarization behavior. The heat maps for each component tested were put together in order to identify possible pitfall points in common to every defect class. Such process is named as qualitative analysis. Figure 19 depicts the heat maps of the regular wire, when possible critical points were identified and highlighted by means of gray shadows.



(a) A regular wire tested under sequential dislocation defects.

(b) A regular wire tested under sequential dopant defects.

(c) A regular wire tested under sequential interstitial defects.

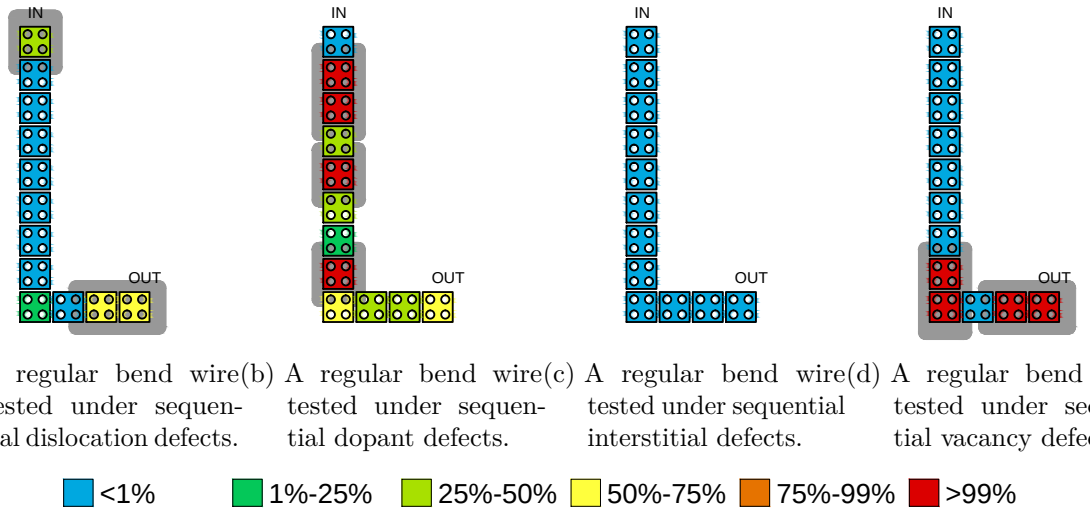
(d) A regular wire tested under sequential vacancy defects.

Figure 19 – The heat maps for the regular wire submitted to every four classes of defects in the sequential structural defects testing. The gray shadows highlight the weakest polarization regions of the structure.

As may be noticed through the analysis of the colors distribution in the heat maps, defective cells at the input and output of a regular wire often lead to the erroneous behavior of the system. In terms of quantities, a defective cell at the input resulted in errors in

more than 50 % of the simulations for the dislocation and vacancy defect classes. Likewise, a defective cell at the output region, which comprises the final two consecutive cells before the OUT label in Fig. 19, resulted in errors in more than 50 % of the simulations for 3 out of 4 defect classes. Thus, the regions to be strengthen in the regular wire, in order to enhance its robustness, should comprise mostly the inputs and outputs.

The same analysis reasoning was applied to the heat maps of the bend wire, as illustrated in Figure 20.



(a) A regular bend wire tested under sequential dislocation defects.

(b) A regular bend wire tested under sequential dopant defects.

(c) A regular bend wire tested under sequential interstitial defects.

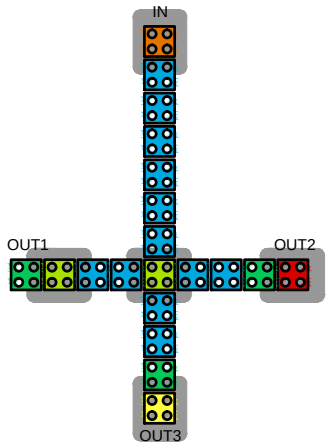
(d) A regular bend wire tested under sequential vacancy defects.

Figure 20 – The heat maps for the bend wire submitted to every four classes of defects in the sequential structural defects testing. The gray shadows highlight the weakest polarization regions of the structure.

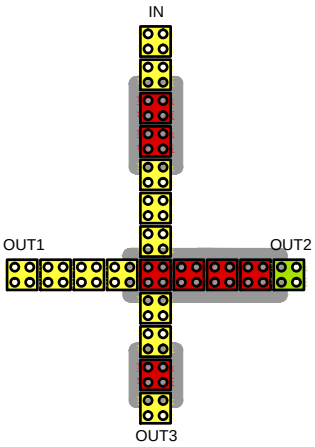
The analysis of the colors distribution in the heat maps indicate that defective cells at the output and the turning proximities of a bend wire often lead to the erroneous behavior of the system. In terms of quantities, a defective cell at the output resulted in errors in more than 50 % of the simulations for 3 out of 4 defect classes (dislocation, dopant and vacancy). Likewise, a defective cell at the turning region, which comprises three consecutive cells disposed in 'L' shape at the bend corner, resulted in errors in more than 50 % of the simulations for 2 out of 4 defect classes (dopant and vacancy). Thus, the regions to be strengthen in the bend wire, in order to enhance its robustness, should comprise mostly the outputs and turnings.

Finally, the fanouts (fanout of 2 and fanout of 3) were also tested against structural defects in order to identify their weakest polarization points. As the results found are similar for both structures, only the fanout of 3 heat maps are depicted in this subsection (Figure 21). The heat maps of the fanout of 2, created from the structural defects testing, may be found in the Appendix B.

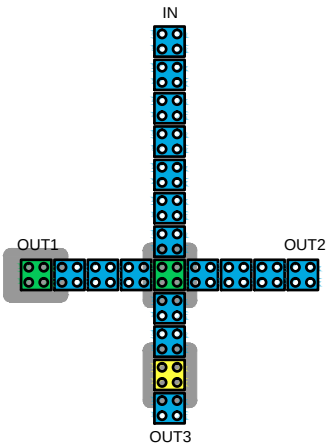
Through the analysis of the heat maps presented, which might be conducted



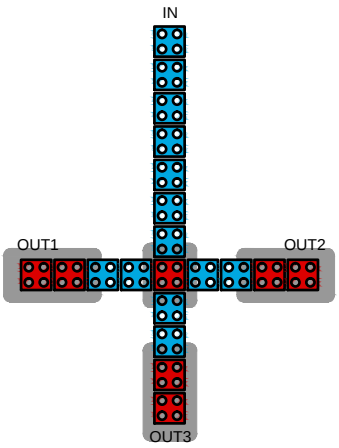
(a) A regular fanout of 3 tested under sequential dislocation defects.



(b) A regular fanout of 3 tested under sequential dopant defects.



(c) A regular fanout of 3 tested under sequential interstitial defects.



(d) A regular fanout of 3 tested under sequential vacancy defects.

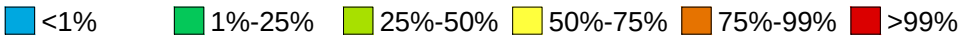


Figure 21 – The heat maps for the fanout of 3 submitted to every four classes of defects in the sequential structural defects testing. The gray shadows highlight the weakest polarization regions of the structure.

analogously for those created from the fanout of 2 defects testing, it is possible to conclude that defective cells at the input, outputs and the turning proximities of a bend wire often lead to the erroneous behavior of the system. In terms of quantities, a defective cell at the input and nearby resulted in errors in more than 50 % of the simulations for 2 out of 4 defect classes (dislocation and dopant). Likewise, a defective cell at 2 out of 3 outputs and nearby resulted in errors in more than 50 % of the simulations for the dislocation, dopant and vacancy defect classes. Finally, a defective cell at the turning region, which comprises

the five adjacent cells arranged in a cross-shaped disposition in the structures' middle, resulted in errors in more than 99 % of the simulations for 2 out of 4 defect classes (dopant and vacancy). Thus, the regions to be strengthen in the fanouts, in order to enhance their robustness, should comprise mostly the input, outputs and turnings.

In summary, for all the fundamental components analyzed, the inputs, outputs and turnings became as the critical points of the QCA structures to be strengthen. However, some of the heat maps obtained from the structural defects testing, such as those depicted in Figures 19b, 19d and 20b, revealed a lack of uniformity in the results. The presence of defects in some cells that, at first, may be considered as non-critical due to their positioning —nor at the inputs, outputs and turnings —have been pointed out as strongly related to the occurrence of errors. Furthermore, some components that are built as structures with a high level of organization among its devices, as fanout of 2 and fanout of 3, has not demonstrated a regular distribution of critical cells between the symmetrical parts (Figures 21b and 21c).

The aforementioned unexpected results may be attributed to both the low number of simulations performed and to the infinite possibilities for the defect values (displacement, misalignment and rotation), which are randomly chosen among a continuous range. More details about the choose of the defect values at the QCA Defects Simulator introduced in this work may be found in Section 4.1.2. A high variability of the defect values may be seen as a positive characteristic of the simulator, since it enables the investigation of the components' behavior under a wide range of defects in a broad spectrum of values, likewise the situation that is supposed to happen in a real manufacturing process of QCA structures. On the other hand, the wider the range of the defect values, the higher the number of simulations required in order to obtain accurate results, otherwise is not possible to ensure a similar distribution for the defect values in each cell. Consequently, some results may be inaccurate.

In order to avoid different distributions for the defect values into the cells in a same structure, thus, the unexpected results —as those shown in the Figures 19b, 19d, 20b, 21b and 21c —a possible solution may be adopt four or five fixed discrete values within a pre-established range. Although this solution is suggested, it requires a deep investigation in a further work. Another option to ensure a better distribution of the defect values is to perform a significant higher number of simulations, in the order of thousands, for each cell in the structure. The exact number of simulations may be defined according to both the structure size and the precision desired in the tests. However, as highlighted by Liu, O'Neill and Swartzlander (2013), the high computational cost of a simulation through the Coherence Vector model available in the QCADesigner makes the performance of a high number of simulations impracticable by conventional computational resources. The use of distributed systems may be seen as an option in this case, since they allow the execution

of multiple tasks, thus, the conclusion of all necessary characterization rounds as proposed in this work in a timely manner. Such option proposed needs computational resources not available for the research group at the time of this work. Hence, the option is presented here as an opportunity for further research.

The strategies for strengthening the polarization level at the critical regions of the QCA structures are presented in the next subsection 5.1.4.

5.1.4 Strengthen Strategies

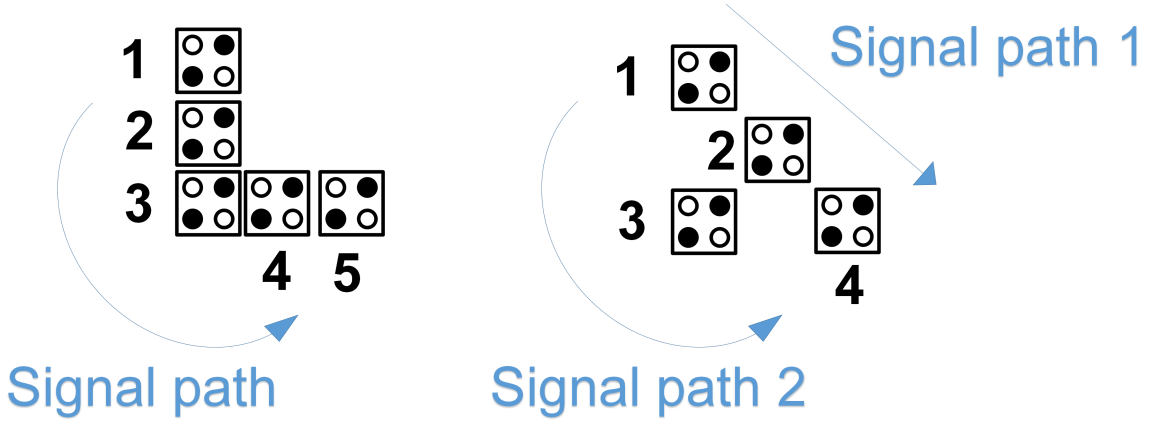
The most common techniques used to enable polarization strengthening within a QCA structure are related to the creation of redundant paths in order to ensure the signal routing within the QCA structure even in the presence of defective devices. Different levels of redundancy may be used in order to enhance the robustness of a QCA structure. For instance, it is possible to design a highly robust component by surrounding all its extremities by numerous redundant devices, *i.e.* an approach similar to that described by Dysart (2009) for creating n-wide thick wires. The cells addition strategy creates redundant mechanisms that are responsible not only for intensifying the polarization levels to be transmitted ahead within the structure, but for providing alternative paths to the signal propagation in case of structural defects. The more cells added within a component, the more safe it becomes regarding to error events caused by defects (DYSART, 2009).

Despite the use of the redundancy techniques enables the creation of highly robust structures, a high level of redundancy often results in oversized structures, that require greater efforts in area and high simulation times due to the large number of devices within the structure. Thus, in this work, polarization strengthening strategies based on redundancy and structural modifications were applied only to the critical regions of the selected components, which were identified by means of the qualitative analysis process described in the subsection 5.1.3.

On the other hand, oversized QCA structures are undesirable since they require more area. Besides, a high increment in the computational cost is likely to occur for circuit simulation in state-of-art simulators like QCADesigner. Thus, this work does not intend to apply oversized blocks in order to devise redundancy strategies. Instead, the goal here is to determine a good trade-off between efforts in area and enhancement of robustness.

In order of create efficient redundant mechanisms for the critical areas, the input and output cells of the fundamental components analyzed was surrounded by three new cells —one at the horizontal and the other two at the vertical axes. Moreover, a structural modification in the turnings of the bend wires and fanouts has been carried out. Such modification comprises the use of successive inversions of the polarization level, a technique based on already reported experiences with inverter chains (GUPTA; JHA; LINGAPPAN,

2007), (PADGETT, 2010). This strategy has been applied to the turning regions since it allows the creation of new robust structures that use one cell less than the original components. The decreasing in the number of cells occurs since whether one cell is added to the upright of the corner of the critical point, another two devices at the horizontal and vertical adjacencies are removed. Fig. 22 illustrates the concept of the structural modifications in a 'L' shaped turning region.



(a) A regular 5-cell 'L-shaped' turning. The arrow in blue represents the only one possible path for signal routing within the structure.

(b) A modified 4-cell 'L-shaped' turning. The two arrows in blue represent the redundant paths for signal routing within the structure. Note that the path 1 is based on successive inversions of the logic state promoted by three diagonally-positioned cells placed in row.

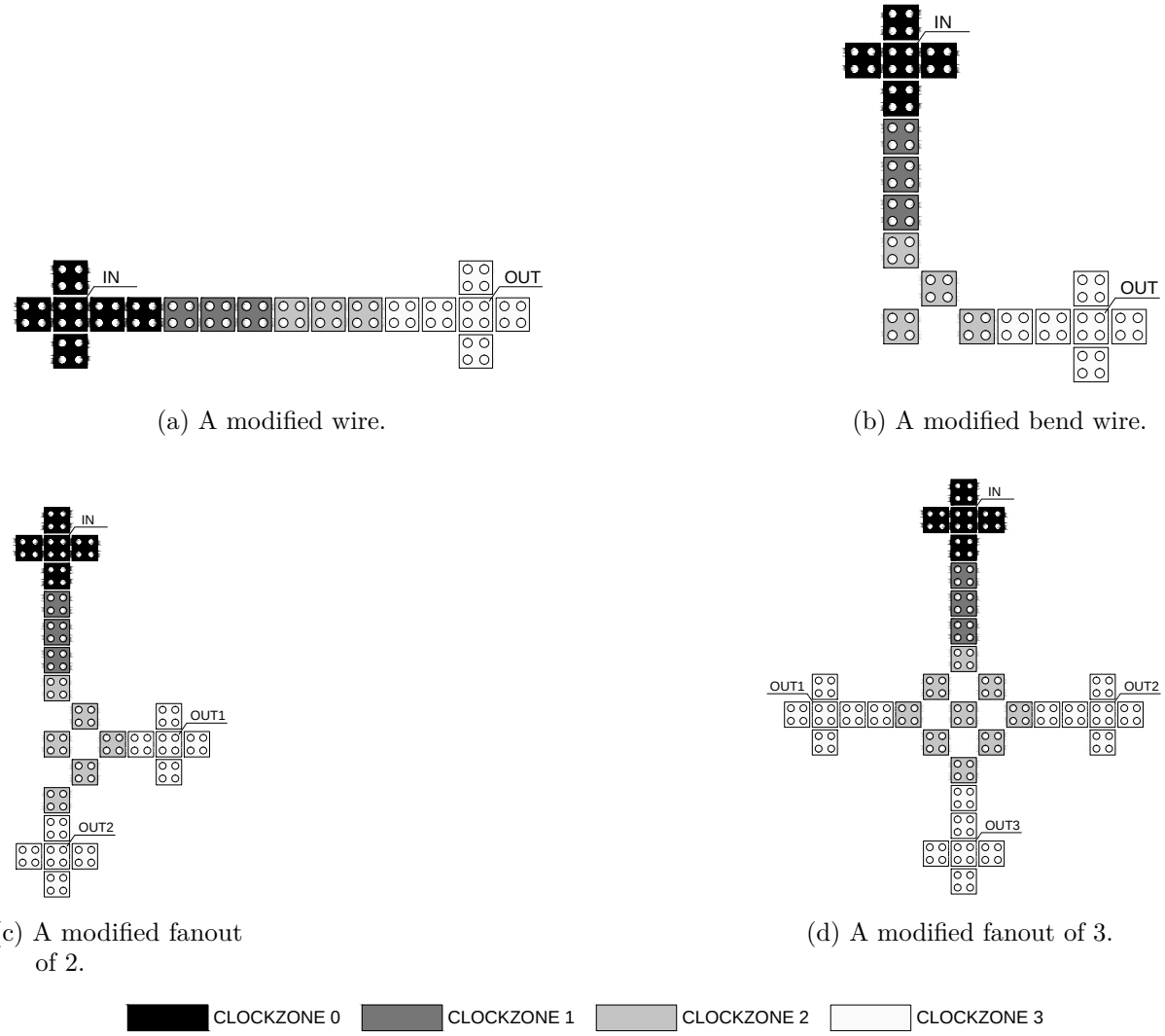
Figure 22 – The structural modifications in a 'L' shaped turning region.

The strengthened inputs and outputs, alongside the modified turnings demonstrate excellent potential to propagate the correct signal even in the presence of defects of combined defect classes, as demonstrated in the simulation results presented in the next subsection 5.1.5.

Figure 23 depicts the modified QCA fundamental components designed from the use of the aforementioned robustness enhancement strategies.

5.1.5 Regular × Modified Components

Once the modified components were designed, they were also submitted to structural defects testing through the QCA Defects Simulator, under the very same conditions as the original structures, as mentioned in subsection 5.1.2. Table 2 depicts the error-free simulations rate for both types of fundamental components (original/modified). The heat maps for all tests performed, either for original or modified structures, may be found in the Appendix (section B).



(a) A modified wire.

(b) A modified bend wire.

(c) A modified fanout of 2.

(d) A modified fanout of 3.

Figure 23 – The four modified fundamental components.

Table 2 – Comparison between error-free simulations rate for regular and modified fundamental components.

	Error-free simulations rate (%)		
	Regular Component	**Modified Component**	**Rate Variation**
Wire	72.40 %	86.46 %	+14.06 %
Bend Wire	70.83 %	87.85 %	+17.02 %
Fanout of 2	72.27 %	85.16 %	+12.89 %
Fanout of 3	64.38 %	88.75 %	+24.37 %

From the data presented in Table 2, it is possible to note that the error-free simulations rate of all modified structures had a sharp increment. Such observation may be attributed to the robustness enhancing strategies applied for the implementation of the proposed components. The modified fanout of 3 performed the best —the structure has reached an error-free simulations rate of 88.75 % against the 64.38 % of its regular

counterpart, under the very same test conditions. It represents an increase of 24.37 % in the referred error-free simulations rate.

Such positive result reported for all fundamental components testify the efficiency of the robustness enhancing strategies applied in this work. The superior performance of the modified fundamental components, which was demonstrated by the results summarized in Table 2, leads to a further step of this work, described in Chapter 6. This step comprises the use of the modified structures to implement more complex circuits, *i.e.* logical components, circuits and systems. The modified circuits are expected to be more robust than their regular counterparts.

5.2 QCA Fundamental Components under Phase-Shifted Clock Signals

This section describes the tests performed with the same QCA fundamental components presented in the sub section 5.1.1 under phase-deviated clock signals testing framework. The aim of such tests was to devise a new strategy for robustness enhancement of such components under the referred unusual conditions. The testing settings and procedure, as well as the results analysis and the solution proposed are explained in the following sub sections (5.2.1 to 5.2.2).

5.2.1 Testing Settings

Similar to the reported for structural defects testing, phase-deviated clock testing requires that the QCA Defects Simulator parameters is set according to the testing conditions desired. The goal here is to propose a clocking scheme that is able to perform reliable under phase deviations within the range of 0 to 45 °, which is the shifts interval already studied in the previous works (OTTAVI et al., 2007) and (KARIM et al., 2009). However, since the solution proposed is new, a wider range for the phase shifts is selected, *i.e.* 0 to 90 °, in order to measure its impact when the system is submitted to greater clock phase shifts.

For each component, twenty-four rounds of tests are performed, each one of them considering an equal division of the entire ninety degrees range. Thus, the testing procedure considers a step of 3.75 ° between successive sub ranges. Deviations are randomly added to the shifts of each one of the four clock signals for each range sub division, by an uniform probability. The testing stop criteria requires that the error-free rate variation does not surpass the value of 1 % along at least 100 iterations. Whether this criteria is not achieved within 1000 iterations, the testing process is interrupted. Such condition is not desirable, since it potentially indicates a divergent result. Finally, the sampling interval is set to

10 % and the threshold for which a signal is interpreted as logic zero or one is 80 % of the standard polarization level limits (-1 and +1).

Once the aforementioned conditions were adjusted, the error-free rates obtained allow the identification of possible critical sub ranges and conditions that are likely to lead the system to behave as unusual or erroneous. The method by which such analysis was carried out is described in the next sub section (5.2.2).

5.2.2 Qualitative Analysis of Waveforms

The simulation results, *i.e.* waveform graphs, obtained from the previous step are now analyzed in order to identify patterns for the synchronization problems that are likely to lead a structure to propagate forward an erroneous signal. Hence, it is important to highlight that the purpose of the qualitative analysis described in this subsection is strictly related to the identification of such patterns. Therefore, at this moment, the analysis of how often a phase-shifted clock signal lead to errors due synchronization problems is not take into account. Such analysis is carried on in the subsection 5.2.4.

Figure 24 depicts one random example of waveform graphs where is possible to identify defective patterns that are likely to lead the wire to propagate a wrong logic level to the output. In Figure **??**, the phases of the clock signals corresponding to the clock signals of the zones 0 and 1 are phase-shifted in $-42°$ and $+45°$, respectively. The red square in the graph is used to highlight a lack of synchronization defective pattern which occurred between the clock signals 0 and 1. The clock signal that controls the inter-dot barriers in the zone 1 was at its switch phase, at the same time that the zone 0 was early depolarizing, with its respective clock signal at the release phase. Such defective pattern caused by the phase shifts in both clock signals is likely to cause that the signal value previously stored during the hold clock phase of zone 0 is not propagated to the next zone, resulting in error.

From the analysis of the phase-shifted clock waveforms, as well as from previous researches regarding the same problem (OTTAVI et al., 2007) and (KARIM et al., 2009), it is possible to conclude that the phase-shifted clock signals negatively interfere to the proper operation of the components analyzed.

As already discussed in section 2.1.4, the emerging nanotechnology QCA is highly sensitive to the phase sequencing along the four clock zones. Thus, it is essential that the information propagated to the zone on the switch phase does not fade away while such zone is on hold phase. The information stored on hold phase is transmitted to the next zone, which at this moment is already in switch phase. A phase shift deviation may cause a premature depolarization of the cell if the release clock phase occurs at the time it is supposed that such clock zone is still in hold phase. Such unusual condition might cause

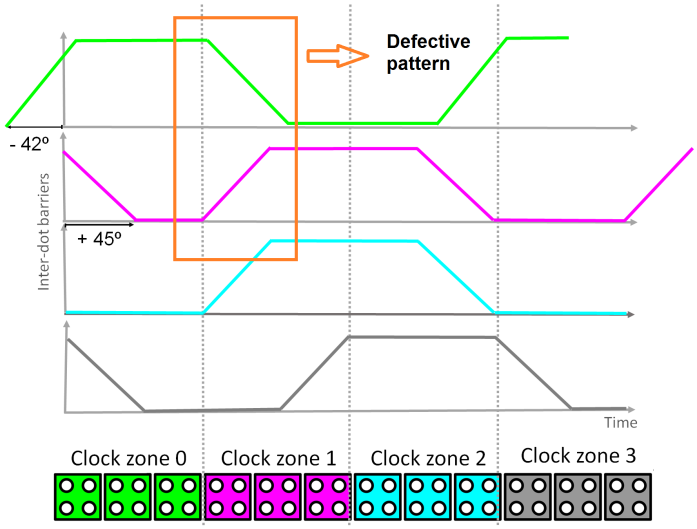


Figure 24 – A wire where 2 out of 4 clock signals phases were shifted. The shifts were within the range of 41.25 to 45.0 °.

severe problems in the transmission of information in a QCA structure, leading the system to operate with errors.

As explained, several errors due to lack of synchronization in QCA structures are likely to occur in case of the information is not stored into the cell for the whole hold clock phase duration. Thus, the solution proposed in this work consists of a new QCA clocking scheme that uses different times for the four clock phases —Switch, hold, release, relax. The new approach proposed has been named asynchronous clocking scheme. The solution is described in the next subsection (5.2.3).

5.2.3 Asynchronous Clocking Scheme

The asynchronous clocking scheme, introduced for the first time in the 2^{nd} Nanocomputing Workshop (REIS; TORRES, 2015), is presented in this work as an alternative method for robustness enhancing of QCA structures in the presence of phase-shifted clock signals. In such approach, the period (T) and the duration of the switch and release phases of the clock signals remain unaltered. Nevertheless, the time of the hold and relax phases (T_{hold} and T_{relax}) are changed according to the equations 5.1 and 5.2.

$$T_{hold} = (1 + \alpha) \cdot 90° \tag{5.1}$$

$$T_{relax} = (1 - \alpha) \cdot 90° \tag{5.2}$$

Where:

α : Asynchrony parameter $(0 \leq \alpha < 1)$

The asynchrony parameter (α) is used to determine a percentage of increase/decrease to the duration of the hold/relax clock phases in the asynchronous clocking scheme. According to the equations 5.1 and 5.2, this parameter is added to/subtracted from the value 1, which represents the rate of 100 %, in order to create a multiplier for the standard duration of the hold/relax clock phases. For instance, if an α of 0.2, which corresponds to 20 %, is applied to the hold/relax clock phases that last 1 ns in the synchronous clocking scheme (standard approach), the durations of the phases in the asynchronous clocking scheme may be calculated using the equations 5.1 and 5.2 as 1.2 ns and 0.8 ns, respectively.

Since the duration of T_{hold} is increased, it is expected that the information propagated to the clock zone in the switch phase remains stored for a longer instant of time before the depolarization process begins, in release phase. This way, the next clock zone is more likely to propagate such remaining information even in the presence of phase-shifted clock signals.

The last clock phase, relax, will only ensure that the cells are free of eventual undesirable residual polarization. Thus, decreasing T_{relax} should not imply in additional impediments to the properly operation of the component, as long as a minimum time for polarization relax is guaranteed.

The definition of values for the asynchrony parameter occurs by means of a 'trial and error' approach, once the behavior of different structures in the presence of different α values may not considered as a pattern. For the tests performed in this work, four asynchrony values were selected: 10 %, 20 %, 30 % and 40 %. A $\alpha = 0$ % means that the traditional clocking scheme (synchronous) is being used. An asynchrony of 10 %, in turn, indicates that the hold phase is increased by 10 %. On the other hand, the relax time is decreased to 90 % of its original duration.

The next sub section (5.2.4) presents the results of the four selected fundamental components (wire, bent wire, fanout of 2 and fanout of 3) submitted to clock phase shifts deviations where both synchronous and asynchronous clocking schemes were used.

5.2.4 Synchronous × Asynchronous Clocking Schemes

The four fundamental components depicted in Figure 18 (wire, bent wire, fanout of 2 and fanout of 3) were submitted to clock phase shifts deviations for both synchronous and asynchronous clocking schemes. Four values were used for α, in order to determine its impact on the feasibility of the proposed. Table 3 summarizes the results found for all α values. The data regarding the individual tests for shift-deviated clock signals separated per distinct value of α may be found in the Appendix (section C).

Table 3 – Average error-free simulations rate for QCA fundamental components under synchronous and asynchronous clocking schemes

	Shifts Range (Synchronous Clock)			**Shifts Range (Asynchronous Clock)**		
Component	**0 to 45°**	**45 to 90°**	**0 to 90 °**	**0 to 45 °**	**45 to 90 °**	**0 to 90 °**
WIR1	92.4 %	72.3 %	84.4%	99.9 %	71.7 %	85.8 %
BWI1	96.8 %	50.2 %	73.5 %	99.9 %	44.76 %	72.34 %
FO21	96.1 %	50.0 %	73.0%	94.9 %	48.7 %	72.0 %
FO31	95.6 %	50.5 %	73.1 %	93.9 %	50.6 %	72.2 %

The data presented in the Table 3 allow to conclude that the regular and the bend wires yield higher error-free simulation rates for asynchronous clocking strategy, within clock phase shifts within the range of 0 to 45 °, regardless of the value of the asynchrony parameter adopted. The error-free simulation rate increase is 7.5 % for WIR1 and 3.1 % for BWI1. Nonetheless, the results for FO21 and FO31 indicate an error-free simulation rate decreasing of 1.2 % and 1.7 % respectively. Further analysis need to be done in order to determine the reason for such decreasing. However, from the analysis of the expanded data found in the Appendix C) is possible to verify that high values of the asynchrony parameter ($\alpha = 30\%$ and $\alpha = 40\%$) lead the FO21 and FO31 to perform poorly in the presence of clock phase shifts. Thus, such resulting low values for the error-free simulations rate contribute to the decreasing of the average value for all values of α, which is depicted in Table 3.

As already explained in the section 2.2.2, clock phase shifts higher than 45 ° are unlikely in reality. Thus, the values of the error-free simulations rates for the comprehensive range (0 to 90 °), as well as the latter subrange (45 to 90 °) are not analyzed here, since such tests were performed only for demonstrate that the asynchronous clocking scheme does not lead the system to an undefined behavior in the presence of higher clock phases shifts. Once the two analyzed clocking schemes (asynchronous and synchronous) performed similar in those clock phase shift ranges, no more commentaries are necessary.

Finally, it is possible to conclude that the asynchronous clocking scheme demonstrated good potential as enhancing robustness strategy for phase-shifted clock signals in the tests with the structures WIR1 and BWI1. However, the influence of α —the asynchrony parameter —in the efficiency of the robustness enhancing strategy needs to be further investigated. Once the high sensitivity of the asynchronous clocking scheme to the value of α is proved, other further work regards to the creation of an efficient solution for the setting of such parameter.

6 Robust QCA Circuits and Systems

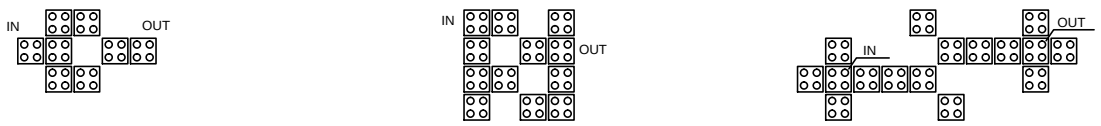
The strengthen techniques presented in the subsection 5.1.4 were used to replace the regular built-in fundamental components in more complex structures, with the purpose of enhancing their robustness. The referred structures are the classical NOT and 3-input majority logic gates from (TOUGAW; LENT, 1994), as well as a full adder and a RCA adapted from (BRUSCHI et al., 2011).

Then, the modified structures were submitted to the error analysis methodology developed in this work, by means of the QCA Defects Simulator. Some results of the simulations with the original, modified and robust circuits already reported in the literature are shown and analyzed in the subsequent sections of this chapter.

6.1 Inverter

Three NOT gates were submitted to the QCA Defects Simulator under the four classes of structural defects, selected at the same time in a combined way. The defects were inserted into the devices by means of the sequential probability model.

For simplification purposes, the structures are called here as INV1 (the original inverter from (TOUGAW; LENT, 1994)), INV2 (the robust inverter proposed by Beard (2006)) and INV3 (the inverter proposed in this work). The latter is based on the Tougaw and Lent (1994) inverter with modifications in the input, turnings and in the output according to the strengthen techniques reported in the subsection 5.1.4. The three inverters are depicted in Figure 25.



(a) INV1 (b) INV2 (c) INV3

Figure 25 – The three inverters submitted to structural defects testing.

The remaining parameters of the QCA Defects Simulator were set as follows. To ensure that the number of simulations performed is likely to cover one defect from each of the four classes for all the cells of the component, the parameters ‘Stable iterations’ and ‘Maximum Number of Iterations’ were equally set. Their configured values corresponded to the number of cells of each component times four, which was the number of defect classes defined. Thus, the parameters ‘Stable iterations’ and ‘Maximum Number of Iterations’

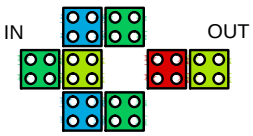
were set for INV1, INV2 and INV3 as 32, 48 and 64 respectively. Finally, the sampling interval parameter was set to 10 % and the threshold for which a signal was interpreted as logic zero or one was defined to 80 % of the standard polarization level limits (-1 and +1).

Table 4 summarizes the results obtained when the aforementioned NOT gates were submitted to random structural defects from all of the four defined defect classes with sequential probability.

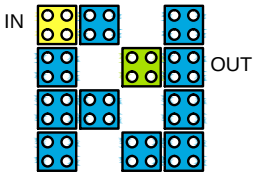
Table 4 – The results of one characterization round for three types of NOT gates under random defects from the four defect classes combined.

Probability Model	**Structure Type**	**Structure Name**	**Error-Free Simulations (%)**	**Simulations Counter**
Sequential	Inverter	INV1	65.63	32
		INV2	89.58	48
		INV3	90.63	64

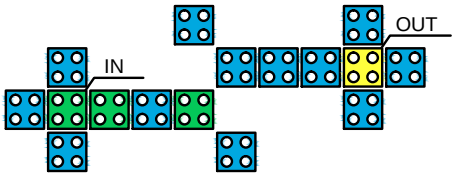
The comparison between the quantitative values of the error-free simulations rates indicates that the modified inverter (INV3) surpasses the performance of both the original (INV1) and that proposed by Beard (2006) (INV2) in 25 % and 1.05 % respectively. Such results endorse the efficiency of the strengthen strategies utilized. Besides the numerical data, the heat maps created at the end of the tests are depicted in the Figure 26.



(a) INV1 under combined defects.



(b) INV2 under combined defects.



(c) INV3 under combined defects.

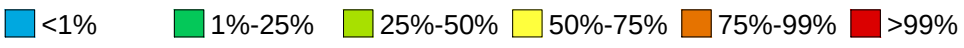


Figure 26 – The heat maps of the three inverters under structural combined defects and sequential probability model.

In Figure 26a it is possible to note that the cell positioned in diagonal, which is responsible for the logic level inversion, led to error in more than 99 % of the simulations when defective. Such fact may attributed to the lack of redundancy of the referred device, *i.e.* when the device is defective, thus, not able to perform properly the logic level inversion,

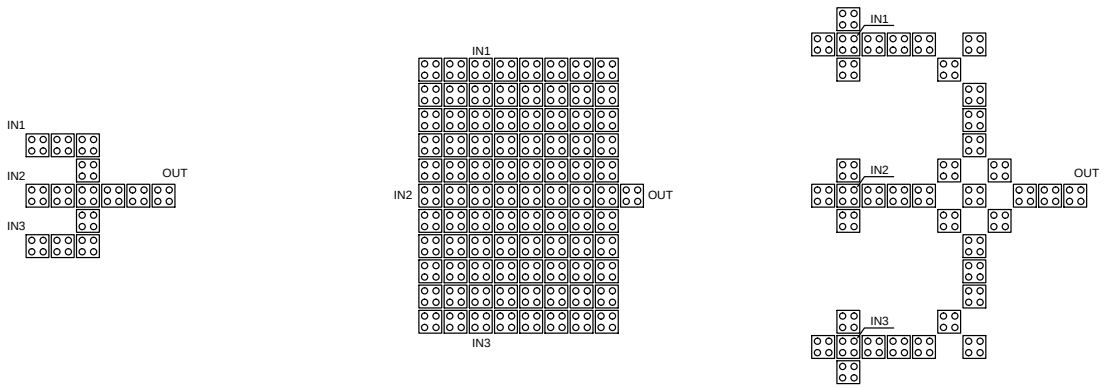
there is no spare devices able to perform such function. Therefore, the correct operation of the logical component is compromised.

Both the inverters INV2 and INV3 have redundant devices responsible for performing the inversion of the logical level at their inputs. Consequently, the cells tend to have a much lower level of criticality, *i.e.* when such devices are defective, they rarely lead to error events. In the INV2, the most critical cell that perform the logic level inversion lead to error when defective in 1-25 % of the times. In the INV3, in turn, the counterpart device cause an error in the presence of defects in 25-50 % of the times.

6.2 3-input Majority

Three 3-input majotity gates were submitted to the QCA Defects Simulator under the four classes of structural defects, selected at the same time in a combined way. The defects were inserted into the devices by means of the sequential probability model.

For simplification purposes, the structures are called here as MAJ1 (a variation of the first QCA majority gate proposed in (TOUGAW; LENT, 1994)), MAJ2 (the 3-input majority block proposed by Fijany and Toomarian (2001)) and MAJ3 (the 3-input majority gate proposed in this work). The latter is based on the Tougaw and Lent (1994) 3-input majority gate with modifications in the inputs, turnings and in the output according to the strengthen techniques reported in the subsection 5.1.4. The three majority gates are depicted in Figure 27.



(a) MAJ1 (b) MAJ2 (c) MAJ3

Figure 27 – The three majority gates submitted to structural defects testing.

The parameters of the QCA Defects Simulator were set in a similar way to those reported for the inverters in subsection 6.1. Thus, the 'Stable iterations' and 'Maximum Number of Iterations' values were set for MAJ1, MAJ2 and MAJ3 as 56, 356 and 156 respectively. The remaining parameters —the Sampling Interval and the HIGH/LOW

Thresholds —were also set to 10 % and 80 % respectively, alike to that reported for the inverters.

Table 5 summarizes the results obtained when the aforementioned 3-input majority gates were submitted to random structural defects from all of the four defined defect classes with sequential probability.

Table 5 – The results of one characterization round for three types of 3-input majority gates under random defects from the four defect classes combined.

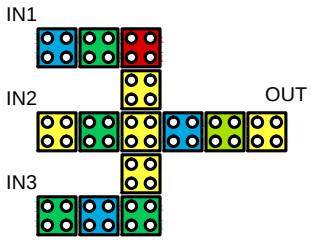
Probability Model	**Structure Type**	**Structure Name**	**Error-Free Simulations (%)**	**Simulations Counter**
Sequential	3-input Majority Gate	MAJ1	55.36	56
		MAJ2	92.98	356
		MAJ3	74.36	156

The comparison between the quantitative values of the error-free simulations rates indicates that the modified 3-input majority (MAJ3) surpasses the performance of the original gate (MAJ1) in an expressive percentage of 19 %. Nevertheless, MAJ3 performance is below the percentage obtained for MAJ2 by 18.26 %. Such difference result was already expected, since the MAJ2 has 50 cells more than the proposed MAJ3. Thus, the MAJ2 is a structure that utilizes a great number of redundant devices disposed in a form of a block. The massive redundancy mechanism is very efficient to avoid errors propagation. On the other hand, the computational cost for simulation for the MAJ2 is quite elevated, as well as the area required for the implementation of such gate.

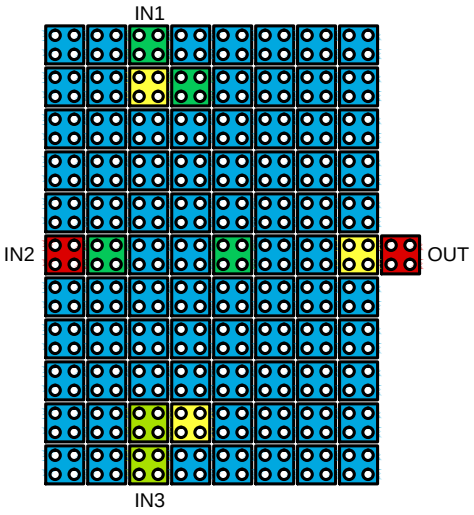
The Coherence Vector simulations of MAJ3 are performed by means of the tool QCADesigner version 2.0.3, in a quad-core machine (Intel Core i7-860, 2.80 GHz, 8 GB RAM) running Linux Ubuntu version 14. One simulation for MAJ2, which comprises 89 cells, took 85 seconds. For comparison purposes, the simulation of a modified majority gate, MAJ3, which comprises 39 cells, may be completed in 40 seconds under the same mentioned test conditions

Besides the numerical data, the heat maps created at the end of the tests are depicted in the Figure 28.

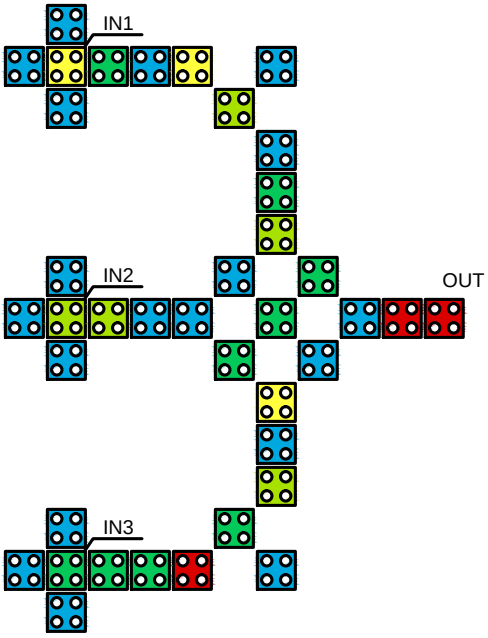
In Figure 28a it is possible to note that three devices vertically positioned in the middle of the structure, as well as the input 2 and output cells, led to error in 50-75 % of the simulations when defective. Such devices consist of high critical points of the structure, along with the cell of the superior turning, which is associated with error events while defective in more than 99 % of the times. Such fact may attributed to the highly compact nature of MAJ1. Furthermore, the device has no redundant structures, similarly to the fact reported for the regular inverter in the Section 6.1. Therefore, the correct operation of the logical component is easily compromised in the presence of defects.



(a) MAJ1 under combined defects.



(b) MAJ2 under combined defects.



(c) MAJ3 under combined defects.

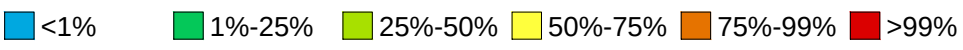


Figure 28 – The heat maps of the three majority gates under structural combined defects and sequential probability model.

Both the majority gates MAJ2 and MAJ3 have redundant devices responsible for performing the inversion of the logical level at their inputs. Consequently, their cells tend to have a much lower level of criticality, *i.e.* when such devices are defective, they rarely lead to error events. In the MAJ3, the most critical cell that belongs to the component's

core, *i.e.* the region of the structure responsible for performing the majority logic function, led to error when defective in 1-25 % of the times.

Moreover, it is also noticeable the presence of some red cells in all majority gates. The color red indicates high level of critically since those cells, when defective, are likely to cause error events in more than 99 % of the situations. In the regular MAJ1, a red cell is placed at the top turning region, while in the robust MAJ2 red devices may be found at the input and output. Furthermore, in the proposed MAJ3 red cells are positioned at the bottom turning region and at the output.

The presence of such red cells in the aforementioned tests may be primarily attributed to two combined reasons —the multiple selection of defect classes and a low number of iterations. Since the purpose of the test was submit the structures to varied defects, all the four defect classes were simultaneously defined and the number of iterations was set to four. Therefore, for each iteration, every defined defect class had an equal probability of 1/4 to be selected for taking part into the defect insertion process for a given cell. In the end of one characterization round —which comprised four iterations —each defect class had its overall probability of occurrence in the cell multiplied by four ($4 \times 1/4$).

Nevertheless, in some cases the random selection of defect classes yielded unexpected results. In both MAJ1 and MAJ3, along all iterations of the defects testing, three vacancy and one dopant defects were inserted into the cells in the turnings. The defects lead to error events in all the four situations. Once a higher number of iterations were defined, the effect of the defect class repetition tended to be minimized. However, despite such unexpected result, the error-free simulations rate confirm that the proposed majority gate MAJ3 has a 19 % increased performance in comparison to the regular majority gate (MAJ1).

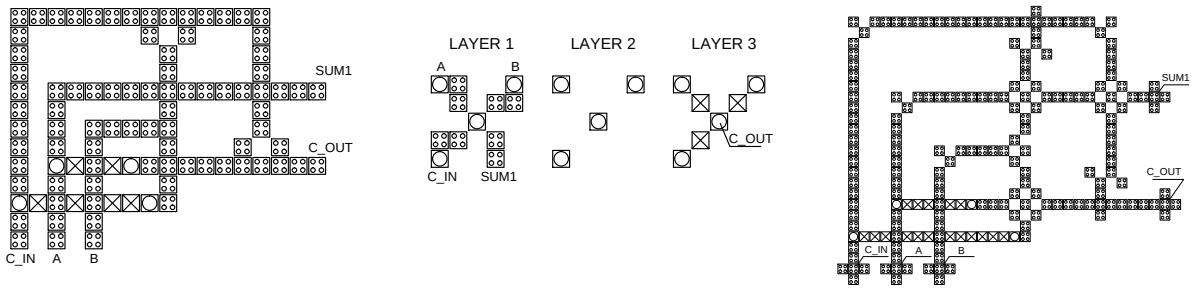
Regarding to MAJ2, very few critical points may be observed within its structure. The absolute majority of its cells has few or no impact in the components operation while defective. However, the input 2 and the output demonstrated highly potential to determine the proper operation of the device, since when such cells turn into defective, error events occur in more than 99 % of the times.

6.3 Full Adder

Three full adders were submitted to the QCA Defects Simulator under the four classes of structural defects, selected at the same time in a combined way. The defects were inserted into the devices by means of the sequential probability model.

For simplification purposes, the structures are called here as as ADD1 (a variation of the full adder proposed in (BRUSCHI et al., 2011)), ADD2 (the ultra-compact robust full

adder from (ROOHI; DEMARA; KHOSHAVI, 2015)) and ADD3 (the full adder proposed in this work). The latter is based on the Bruschi et al. (2011) full adder with modifications in the inputs, turnings and in the output according to the strengthen techniques reported in the subsection 5.1.4. The three full adders are depicted in Figure 29. ADD1 and ADD3 utilize the multilayer crossover technique, in which a cell is a distinct layer is depicted by a X circumscribed into the square-shaped QCA cell. ADD2, in turn, is an ultra-compact structure that uses the multilayer approach beyond wire crossings. Therefore, its layers are depicted separately.



(a) ADD1 (b) ADD2 (c) ADD3

Figure 29 – The three full adders submitted to structural defects testing.

The parameters of the QCA Defects Simulator were set in a similar way to those reported for the inverters and majority gates in subsections 6.1 and 6.2. Thus, the 'Stable iterations' and 'Maximum Number of Iterations' values were set for ADD1, ADD2 and ADD3 as 432, 92 and 820 respectively. The remaining parameters —the 'Sampling Interval' and the 'HIGH/LOW Thresholds' —were also set to 10 % and 80 % respectively, alike to that reported for the inverters and majority gates.

Table 6 summarizes the results obtained when the aforementioned full adders were submitted to random structural defects from all of the four defined defect classes with sequential probability.

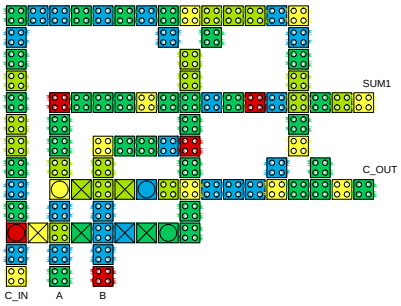
Table 6 – The results of one characterization round for three types of full adders under random defects from the four defect classes combined.

Probability Model	**Structure Type**	**Structure Name**	**Error-Free Simulations Rate**	**Simulations Counter**
Sequential	Full Adder	ADD1	66.20 %	432
		ADD2	46.74 %	96
		ADD3	68.34 %	820

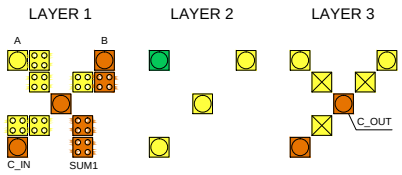
The comparison between the quantitative values of the error-free simulations rates indicates that the modified full adder (ADD3) surpasses the performance of both the

original (ADD1) and that ultra-compact proposed by Roohi, DeMara and Khoshavi (2015) (ADD2) in 2.14 % and 21.6 % respectively. Such results endorse the efficiency of the strengthen strategies proposed. It is also interesting to highlight that the great difference between the error-free simulation rates of ADD2 and ADD3 —both originally considered as robust circuits —is not unexpected at all. When the ultra-compact robust ADD2 was proposed, it was tested only against single misalignment defects as reported in (ROOHI; DEMARA; KHOSHAVI, 2015). It seems that its ultra-compact feature represents a big concern when more than one defect classes are considered in a single analysis, like in the tests performed through the methodology proposed.

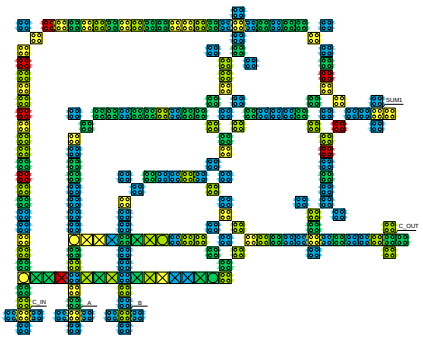
Besides the error-free simulations rate presented in Table 6, the heat maps created at the end of the testing process are depicted in the Figure 30.



(a) ADD1 under combined defects.



(b) ADD2 under combined defects.



(c) ADD3 adder under combined defects.

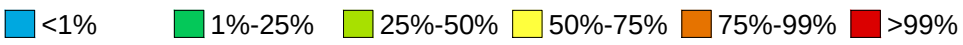


Figure 30 – The heat maps of the three full adders under structural combined defects and sequential probability model.

The full adders heat maps visual analysis is a tough task, due to the high number of built-in fundamental components within the ADD1 and ADD3 structures. However, the analysis shall consider the proportion of high critical cells in the circuit, *i.e.* the cells

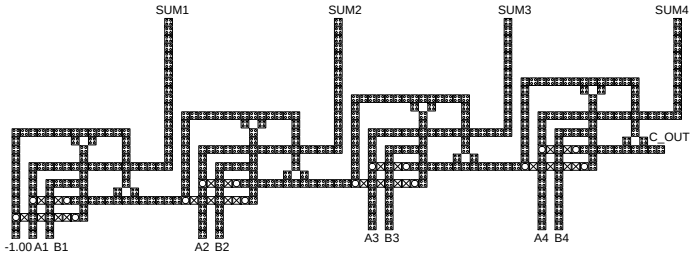
that causes errors when defective in more than 99 % of the times. ADD1 has a number of cells within such category of 5 out of 108 total cells of the structure, which is 4.6 %. Furthermore, ADD3 has 8 highly critical cells out of the 405 cells in the design, which is 3.9 %. Finally, the ultra-compact ADD2 has 4 highly critical cells among the 24 cells of the structure, which represents 16.7 %.

Thus, the proposed adder ADD3 has the lower proportion of highly critical cells among the three full adders submitted to structural defects testing. Regarding to ADD2, it is not possible to clearly distinct between critical/non-critical regions since it is a very compact structure. Therefore, many cells of the structure has shown a worrisome critically level under the defects testing methodology presented. It seems like it is a tradeoff between compactness and robustness in this case. The structure ADD2, as well as another compact QCA structures reported in (SEN; RAJORIA; SIKDAR, 2013) and (SEN et al., 2015), makes use of the multilayer approach, *i.e.* overlapped QCA layers, in order to accommodate a great number of cells within a reduced area. The multilayer strategy for designing more compact QCA circuits is valid, however, in the most of the reports regarding the use of such strategy, its use is limited to wire crossing. Since the multilayer QCA is a controversy and still not realizable approach for wire crossing in QCA (LIU; O'NEILL; SWARTZLANDER, 2013), there is no studies enough to ensure that such strategy is robust enough to implement logical devices such as majority gates and inverters built-in a more complex QCA circuit.

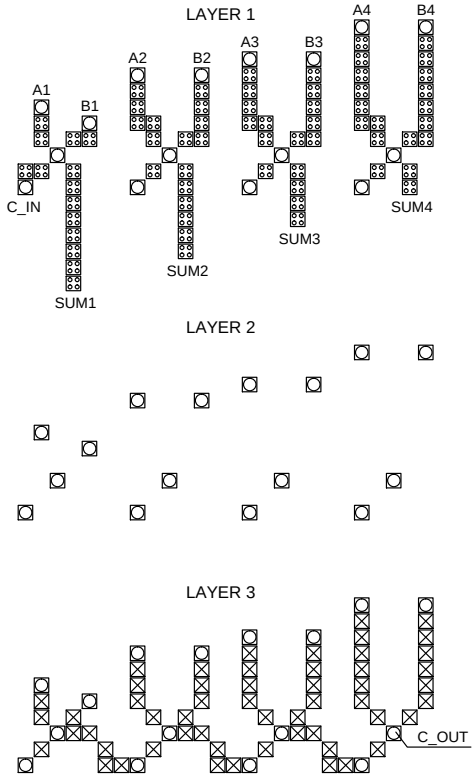
6.4 4-bit Ripple-carry Adders

Three types of 4-bit ripple-carry adders were submitted to the QCA Defects Simulator under the four classes of structural defects, selected combined together. The defects were inserted into the devices by means of the uniform probability model. Regarding to the setting of the parameters, the 'Error-free rate tolerance', 'Stable iterations' and 'Maximum Number of Iterations' values were set for all the RCAs as 1 %, 200 and 2000 respectively. The remaining parameters —the 'Sampling Interval' and the 'HIGH/LOW Thresholds' —were also set to 10 % and 80 % respectively, alike to that reported for the inverters, majority gates and full adders.

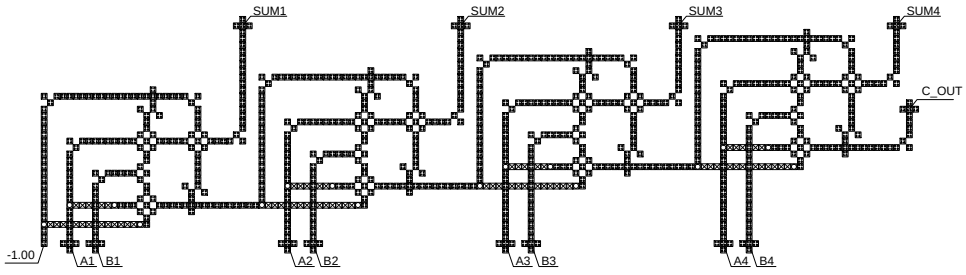
For simplification purposes, the structures are called here as as RCA1 (a variation of the RCA proposed in (BRUSCHI et al., 2011)), RCA2 (the ultra-compact robust RCA from (ROOHI; DEMARA; KHOSHAVI, 2015)) and RCA3 (the RCA proposed in this work). The latter is based on the Bruschi et al. (2011) RCA with modifications in the inputs, turnings and in the output according to the strengthen techniques reported in the subsection 5.1.4. The three RCAs are depicted in Figure 31.



(a) RCA1



(b) RCA2



(c) RCA3

Figure 31 – The three RCAs submitted to structural defects testing.

Table 7 summarizes the results obtained when the aforementioned RCAs were submitted to random structural defects from all of the four defined defect classes with uniform probability.

Table 7 – The results of one characterization round for three types of RCAs under random defects from the four defect classes combined.

Probability Model	Structure Type	Structure Name	Error-Free Simulations Rate	Simulations Counter
Uniform	Ripple-carry Adder	RCA1	72.27 %	299
		RCA2	64.93 %	230
		RCA3	80.53 %	223

The analysis of the 4-bit RCAs proceeds a quite similar to that one reported in Section 6.3), since they were implemented as systems derived from the union of four basic full adder blocks. However, the tests performed for such structure underwent a different probability model —the uniform probability model was used at this time.

Likewise already concluded for the full adders ADD2 and ADD3, the great difference between the error-free simulation rates of RCA2 and RCA3 - both designed to be robust - is not unexpected at all, for the same reasons mentioned in the Section 6.3.

Besides the error-free simulations rate presented by means of the Table 7, the heat maps created at the end of the testing process are depicted in the Figure 32.

Highlighting the contribution of every component to the overall robustness of the system through a heat map becomes a non-trivial task for large structures as the 4-bit RCAs presented. For such reason, the analysis proceeds in more general terms. Despite some cells next to the key points remain into (highly critical), it is possible to observe a general trend of slighting of the color in almost all regions of the structure. For instance, through visual analysis, it is noticeable that many red cells (highly critical) have turned into light blue (non-critical).

Finally, it is not possible to clearly distinct between critical/non-critical regions in RCA3, likewise to its corresponding full adder block whose testing results were already presented in the Section 6.3. Therefore, all the regions of the structure has shown a worrisome number of critical cells under the defects testing methodology presented. It seems like the tradeoff between compactness and robustness comes up again.

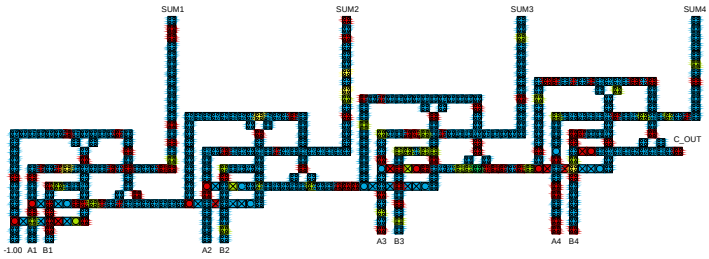
6.5 Discussion

This chapter presents the application of the robustness-enhanced fundamental structures introduced in the Chapter 5 to modify more complex circuits and systems, thereby implementing novel robust structures. It is possible to note that, besides the

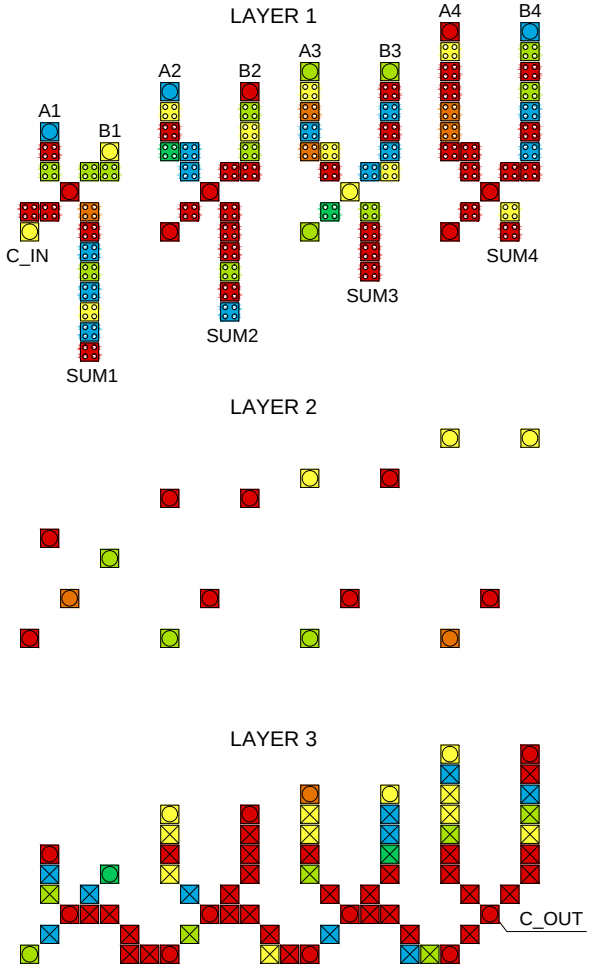
implemented circuits are functional, they also perform better under structural defects testing in the most of the times —the only exception here is for the MAJ3, which performs below the MAJ2 under combined defects and sequential probability.

As already mentioned in Chapter 4, although the heat map is a very efficient graphical resource which allows the mapping of critical points within a QCA structure, a minimum number of simulations should be performed in order to preserve the quality of the results, thus the heat map reliability. Another point to be improved in heat maps consists of their analysis procedures. The larger the circuit, the greater the number of built-in components present in the design. Hence, drawing a conclusion about the critical points to be enhanced while proposing a robust design may be turn into a very tough task.

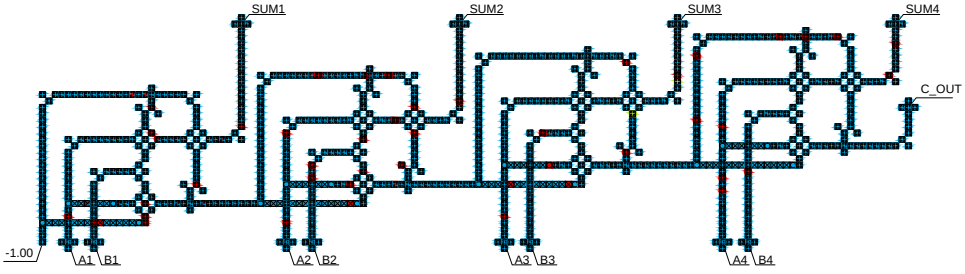
Considering that, the general approach for robustness enhancement proposed in this work, *i.e.* the strengthen of all inputs, outputs and turnings, while simple and straightforward, may represent a good standardized solution for robustness enhancement of QCA structures.



(a) RCA1 under combined defects.



(b) RCA2 under combined defects.



(c) RCA3 under combined defects.

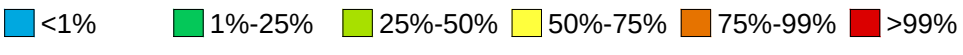


Figure 32 – The heat maps of the three RCAs under structural combined defects and uniform probability model.

7 Conclusions

The CMOS supremacy in the framework of ASIC design has been threatened by challenges mainly related to the alarming pace of the increase of power consumption, as consequence of the scaling process. The size reduction of transistors shall not continue to occur uninterruptedly, due to physical limits and technology issues. Considering that, researchers worldwide are looking forward to find viable solutions that could slow down the reaching of CMOS miniaturization limits or even replace the current state-of-art technology.

Among other nanotechnologies pointed out by ITRS (2004), QCA is a promising candidate for CMOS succession. Its fundamental units are called cells, which can be arranged in order to enable the transmission and processing of information. It is important to highlight that QCA structures are able to perform computation and transport information without flow of electrons (electric current), demanding less power than in the traditional CMOS circuits. Furthermore, the size of cells are typically about few nanometers and the design of QCA circuits generally require less area than CMOS circuits. High clock speeds are supposed to be achieved in the QCA paradigm (KIM; WU; KARRI, 2006). The development of robust structures is one important step, though, to enhance the probability that QCA might be applied for future applications. Although there are some researches in the field of defects and error simulation for QCA circuits, there are not many tools available for turn the design of these structures into a less tough task.

The main contribution of this work is to introduce a QCA Defects Simulator that employs a novel methodology for errors exploration in QCA structures. Such errors may occur at output signals due to either structural defects into the cells or deviations in the standard shifts of clock signals. The tool provides a quantitative measure of the robustness level of the structure, named error-free simulations rate. Moreover, it produces heat maps by which it is possible to identify its weakest polarization points.

By using such presented tool, it was possible to test four fundamental components (a regular wire, a bend wire, a fanout of 2 and a fanout of 3) under several structural defect classes, as reported in the Section 5. Eventual pitfall points within the structures were identified. In order to promote the polarization reinforcement for purpose of avoiding that error events may occur due to the identified points, structural modifications to the structures were proposed. The modified structures were tested by means of the novel QCA Defects Simulator, which demonstrates their superiority in terms of robustness for all the cases. In a further stage of the work, the modified fundamental components were used to replace the traditional ones in some selected more elaborated structures, as majority

and NOT logic gates, a full-adder and a 4-bit RCA. Once again, the results obtained for such structures demonstrated improvement of robustness level compared to traditional structures already reported in the literature. The results are discussed in more details in Chapter 6 and fully presented in the Appendix B.

Furthermore, the QCA Defects Simulator employs the flow presented in (OTTAVI et al., 2007) in order to test the structures against deviations in the shifts of clock signals. Since the error events caused by shifts deviations may be attributed to the lack of synchronization problems, asynchronous clock signals were proposed to diminish the problem and decrease the error rates. The same four fundamental components (a regular wire, a bend wire, a fanout of 2 and a fanout of 3) were submitted to the testing process using two models of clocking: The synchronous (traditional) and the asynchronous proposed here. Results shown a general small improvement of the error rate performance within the deviations range of 0 to $\pi/4$ rad. According to Ottavi et al. (2007), shifts higher than $\pi/4$ rad are very unlikely to occur since they led to the signal phase inversion. However, in order to ensure the viability of the new asynchronous clock solution for phase shifts greater than $\pi/4$ rad, tests were performed for an additional range (within $\pi/4$ rad to $\pi/2$ rad). The results show that the solution proposed is safe but no efficient for great deviations, since the error rate for such case was very similar to that reported for traditionally clocked circuits.

For future works, it might be suggested the addition of new features to the QCA Defects Simulator, such as more probability models and defect classes to be considered. Another important contribution to the viability of such created tool is the development of more fast and accurate simulation engines besides Coherence Vector that may be incorporated to the QCADesigner. Although the engine currently used is quite accurate, it takes too long to process a characterization round, especially whether the structure has count many cells. The issue of the high computational cost of the simulation process through the Coherence Vector may be also addressed by the use of distributed systems. Moreover, also with the purpose of diminishing the time of one characterization round whereas the computational resources may not be improved, the author suggest as a future work to set discrete defect values within a pre-defined range. Both suggestions are explained in more details in Section 5.1.3.

The methodology could be also applied to develop a library of robust QCA structures employing robustness enhancing techniques presented in this work.

Finally, tests similar to those reported in this work may be performed for different temperature values besides the 1 K used as default by the QCADesigner tool. Such analysis will enable the investigation of the effects of the temperature increment in the robustness of the structures presented in this work, for both structural defects and phase-shifted clock signals frameworks.

Undoubtely, the QCA Defects Simulator itself plus the results obtained from its application (REIS; TORRES, 2015), (REIS; TORRES, 2015) are important contributions to the QCA design paradigm.

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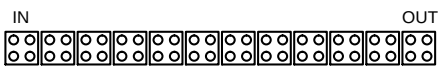
Appendix

APPENDIX A – Analyzed QCA Structures

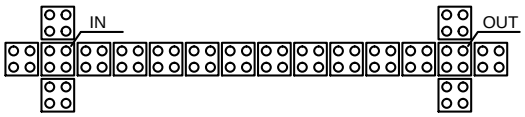
A.1 Wire

WIR1 - Regular



Number of cells: 12
Latency: 1

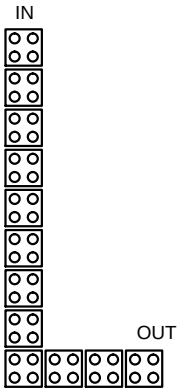
WIR2 - Modified



Number of cells: 18
Latency: 1

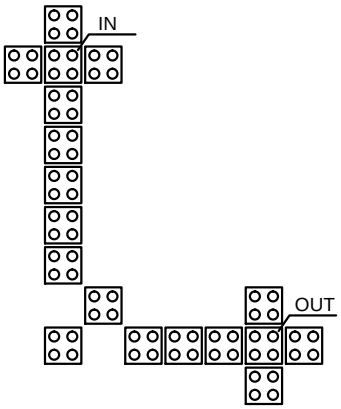
A.2 Bend Wire

BWI1 - Regular



Number of cells: 12
Latency: 1

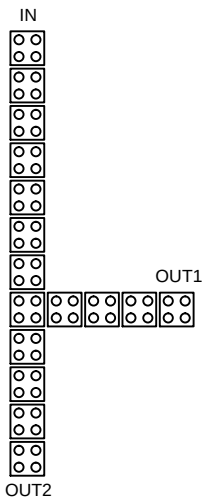
BWI2 - Modified



Number of cells: 18
Latency: 1

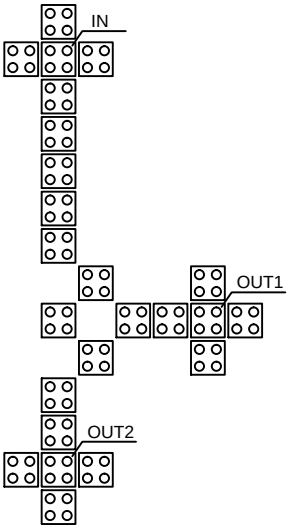
A.3 Fanout of 2

FO21 - Regular



Number of cells: 16
Latency: 1

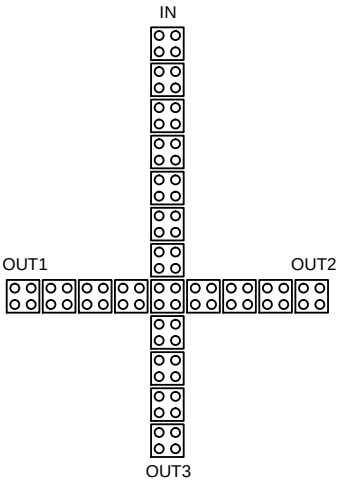
FO22 - Modified



Number of cells: 24
Latency: 1

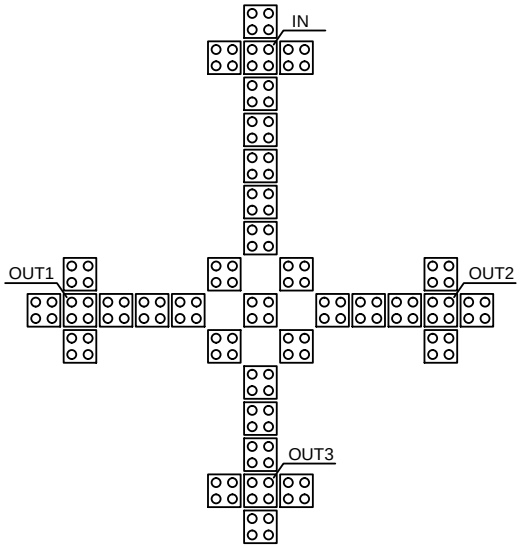
A.4 Fanout of 3

FO31 - Regular



Number of cells: 20
Latency: 1

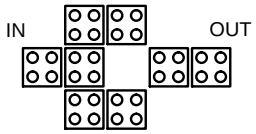
FO32 - Modified



Number of cells: 35
Latency: 1

A.5 Inverter

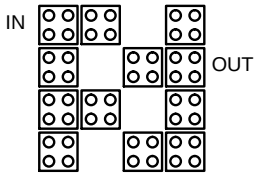
INV1 - Regular



Number of cells: 8

Latency: 0

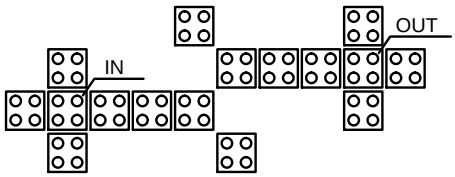
INV2 - Beard



Number of cells: 12

Latency: 0

INV3 - Modified

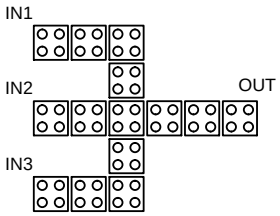


Number of cells: 16

Latency: 0

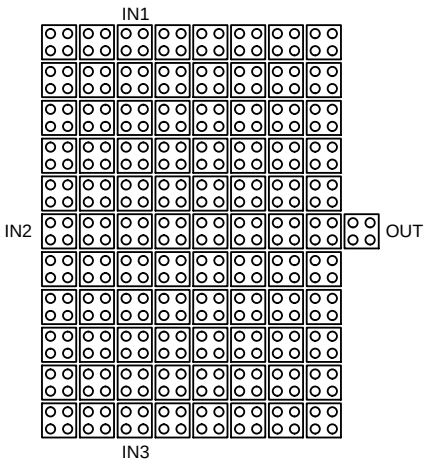
A.6 3-input Majority gate

MAJ1 - Regular



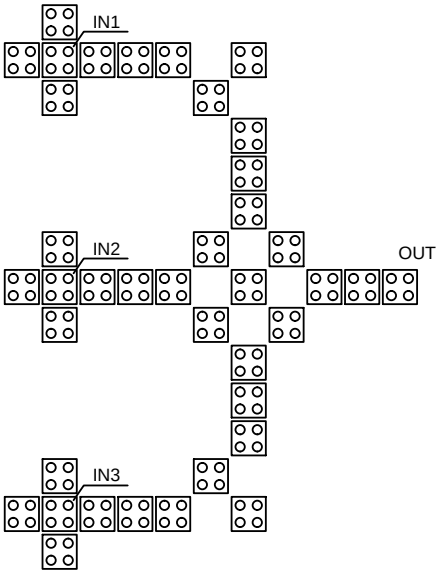
Number of cells: 14
Latency: 0

MAJ2 - Fijany et al



Number of cells: 89
Latency: 0

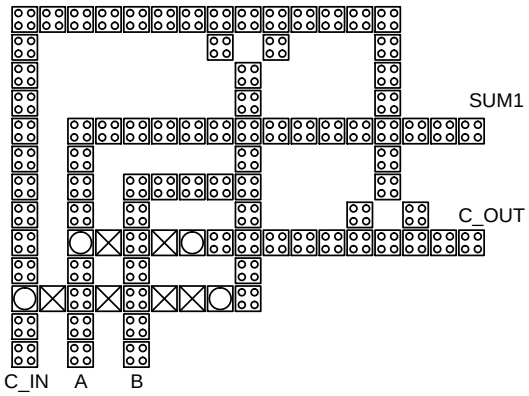
MAJ3 - Modified



Number of cells: 39
Latency: 0

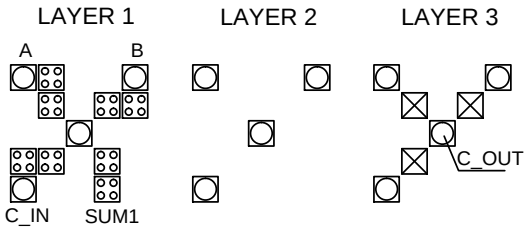
A.7 Full Adder

ADD1 - Regular



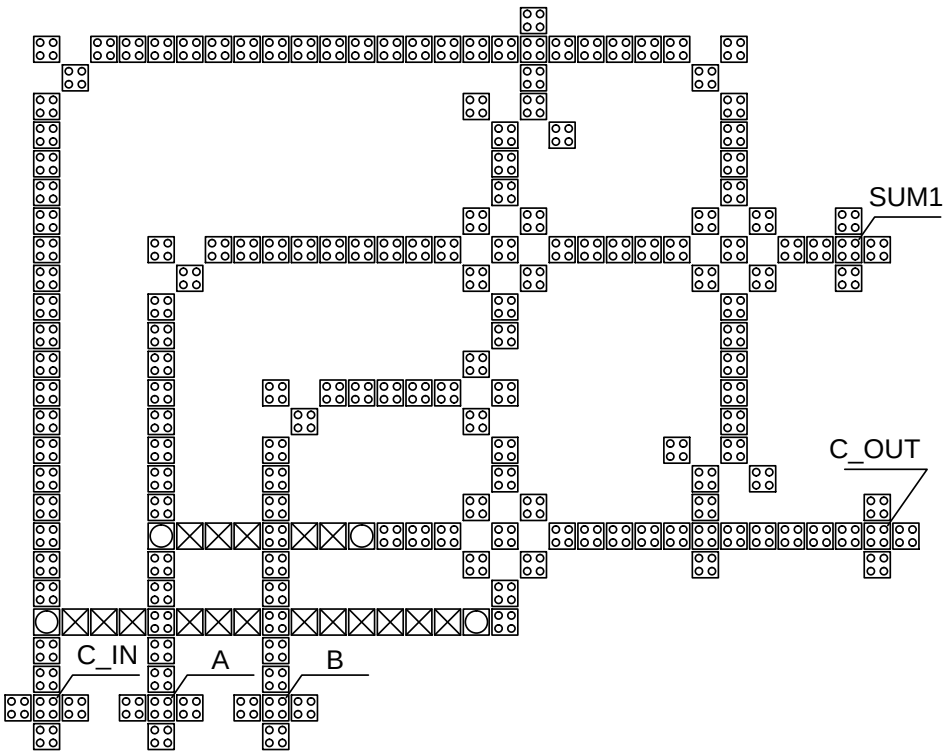
Number of cells: 108
Latency: 2

ADD2 - Roohi et al



Number of cells: 23
Latency: 0

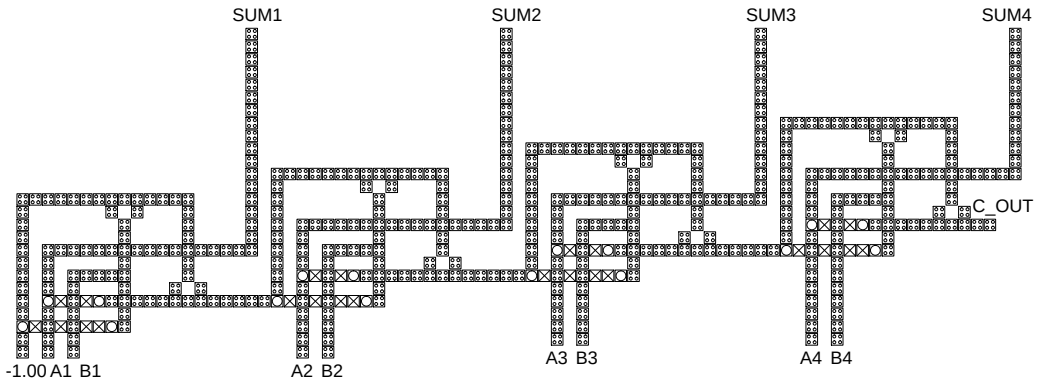
ADD3 - Modified



Number of cells: 205
Latency: 2

A.8 4-Bit Ripple-carry Adders

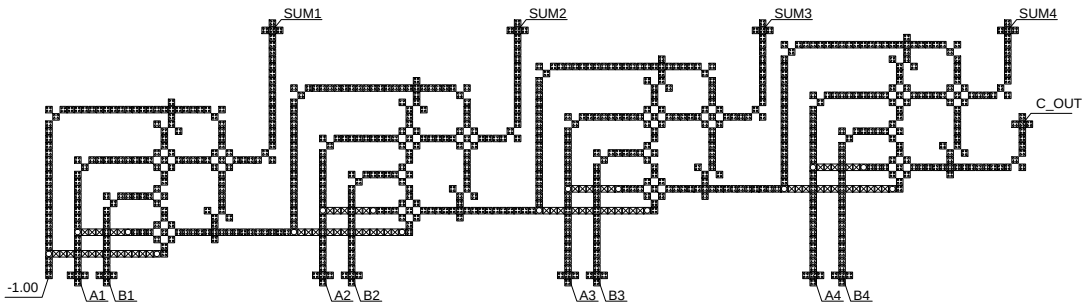
RCA1 - Regular



Number of cells: 519

Latency: 4

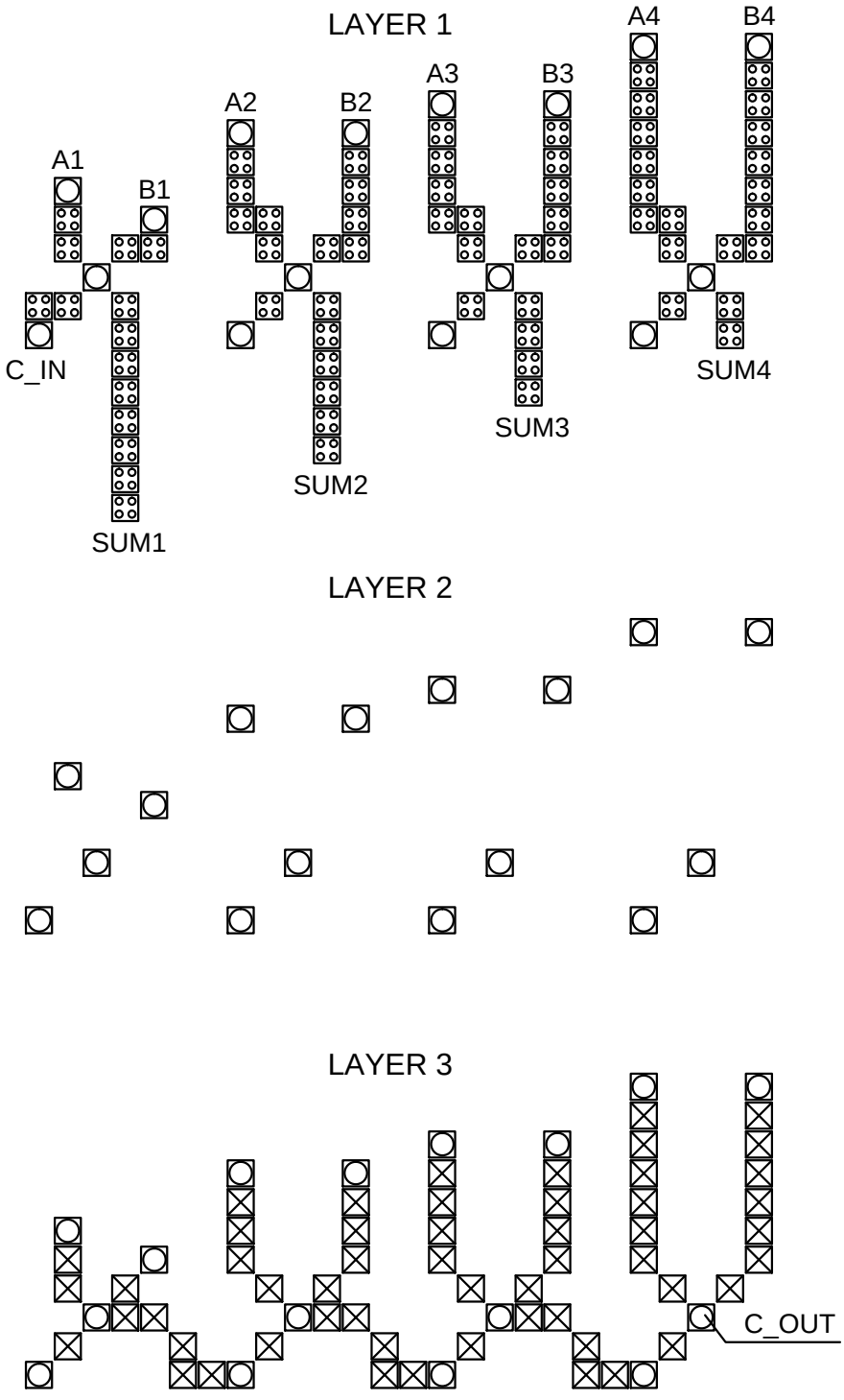
RCA3 - Modified



Number of cells: 909

Latency: 4

RCA2 - Roohi et al



Number of cells: 169

Latency: 2

APPENDIX B – Simulation Results - Structural Defects

B.1 Sequential Probability Model Tests

B.1.1 Individual Defect Classes

Number of iterations:
- Dislocation: 4
- Dopant: 4
- Interstitial: 4
- Vacancy: 1

Number of simulations: $I \times C$

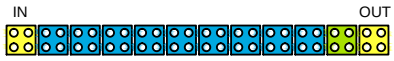
Where:
I: Number of iterations
C: Number of cells

B.1.1.1 Error-free Simulations Rates

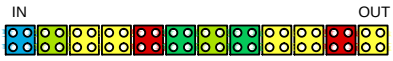
Table 8 – Error-free Simulations Rates - Individual Defect Classes

	Dislocation	Dopant	Interstitial	Vacancy
WIR1	83.33	39.58	95.83	66.67
BWI1	81.25	35.42	100.00	66.67
FO21	89.06	31.25	92.19	68.75
FO31	78.75	12.50	93.75	65.00

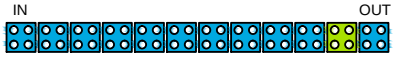
B.1.1.2 Heat Maps



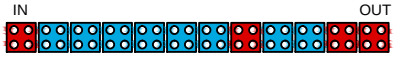
(a) WIR1 under dislocation defects.



(b) WIR1 under dopant defects.

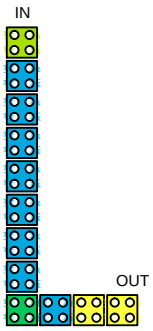


(c) WIR1 under interstitial defects.

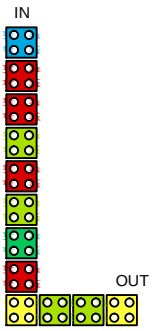


(d) WIR1 under vacancy defects.

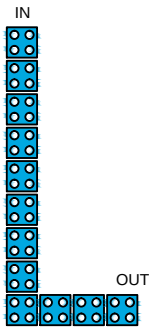
Figure 33 – WIR1 under individual defect classes



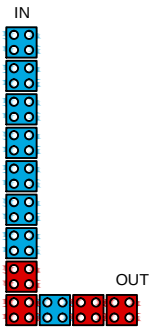
(a) BWI1 under dislocation defects.



(b) BWI1 under dopant defects.



(c) BWI1 under interstitial defects.



(d) BWI1 under vacancy defects.

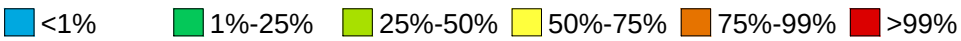
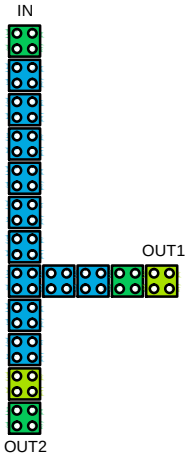
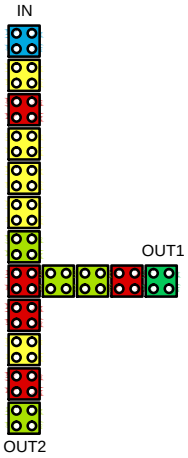


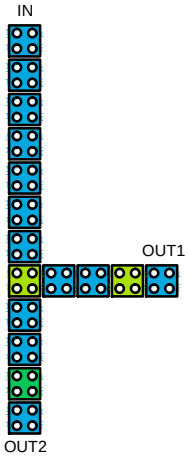
Figure 34 – BWI1 under individual defect classes



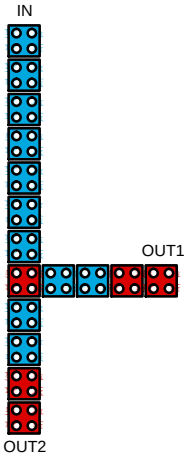
(a) FO21 under dislocation defects.



(b) FO21 under dopant defects.



(c) FO21 under interstitial defects.



(d) FO21 under vacancy defects.

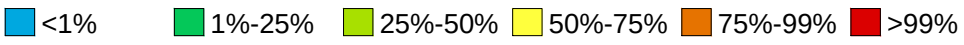
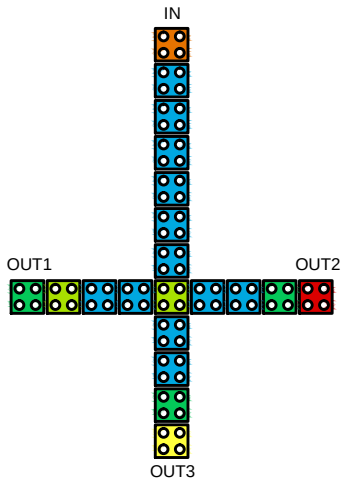
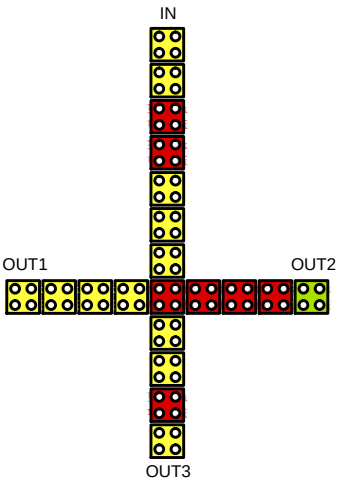


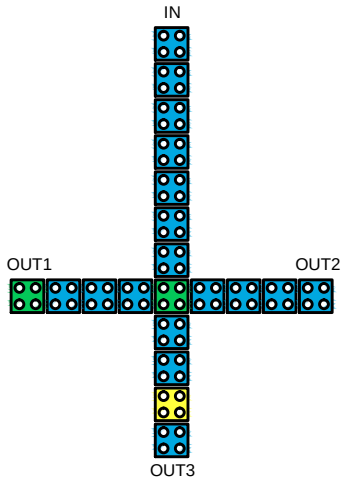
Figure 35 – FO21 under individual defect classes



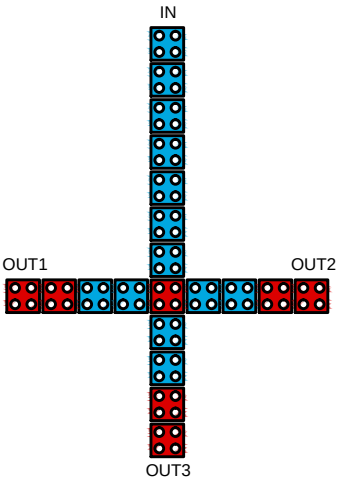
(a) FO31 under dislocation defects.



(b) FO31 under dopant defects.



(c) FO31 under interstitial defects.



(d) FO31 under vacancy defects.

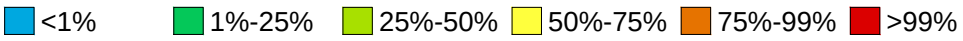


Figure 36 – FO31 under individual defect classes

B.1.2 Combined Defect Classes

Number of iterations:
- Wire: 16
- Bend wire: 16
- Fanout of 2: 16
- Fanout of 3: 16
- Inverter: 4
- 3-input Majority gate : 4
- Full Adder: 4

Number of simulations: $I \times C$

Where:
I: Number of iterations
C: Number of cells

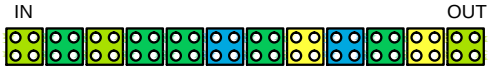
B.1.2.1 Error-free Simulations Rates

Table 9 – Error-free Simulations Rates - Combined Defect Classes

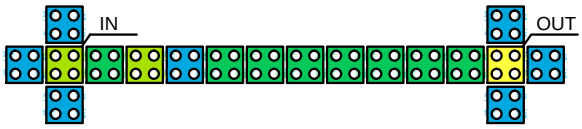
	Regular	Robust*	Modified
Wire	72.40	-	86.46
Bend wire	70.83	-	87.85
Fanout of 2	72.27	-	85.16
Fanout of 3	64.38	-	88.75
Inverter	65.63	89.58	90.63
3-input Majority gate	55.36	92.98	74.36
Full adder	66.20	46.74	68.34

∗ Inverter: INV2 (BEARD, 2006)
∗ 3-input Majority gate: MAJ2 (FIJANY; TOOMARIAN, 2001)
∗ Full adder: ADD2 (ROOHI; DEMARA; KHOSHAVI, 2015)

B.1.2.2 Heat Maps



(a) WIR1 under combined defects.



(b) WIR2 under combined defects.

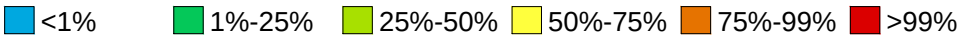
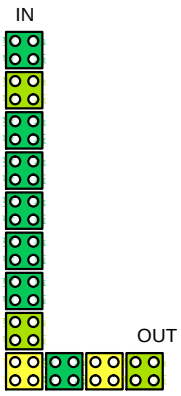
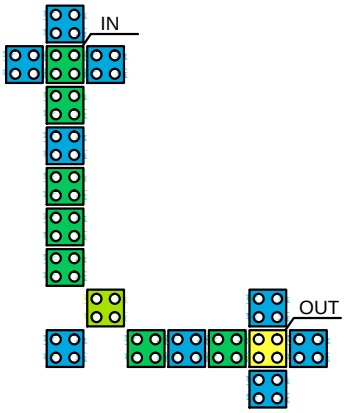


Figure 37 – WIR1 and WIR2 under combined defects



(a) BWI1 under combined defects.



(b) BWI2 under combined defects.

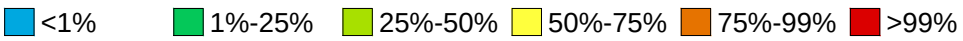
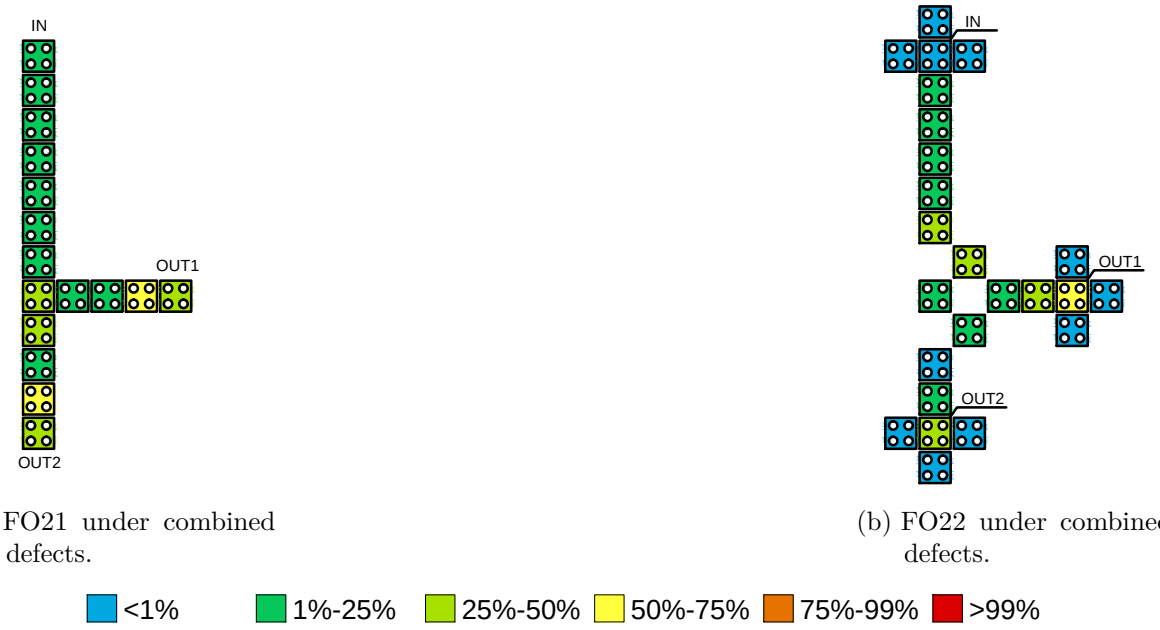


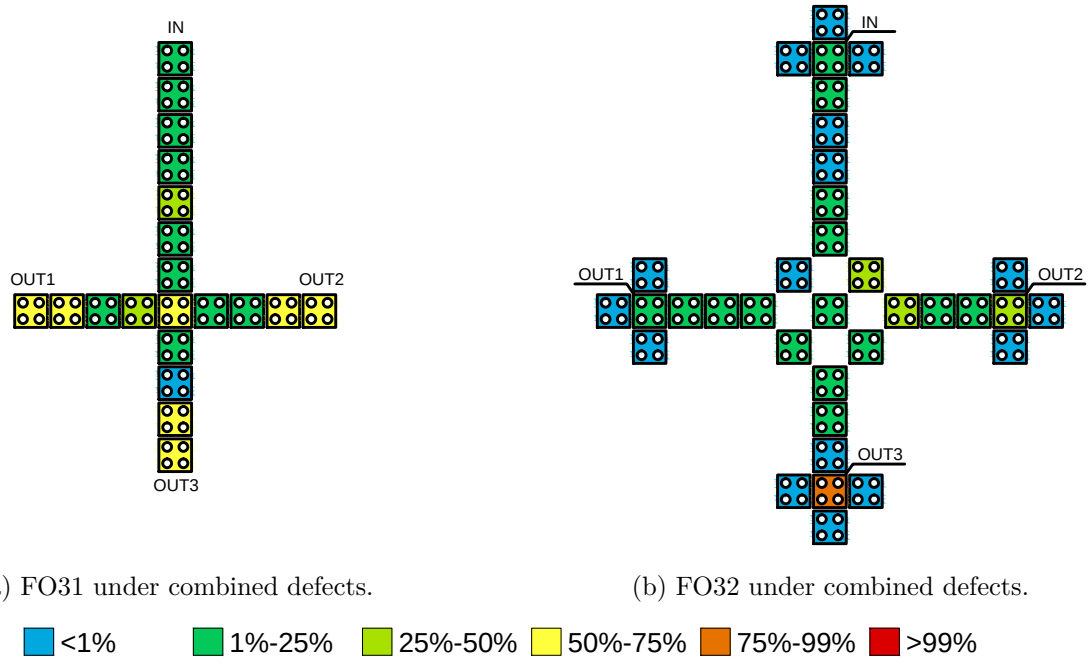
Figure 38 – BWI1 and BWI2 under combined defects



(a) FO21 under combined defects.

(b) FO22 under combined defects.

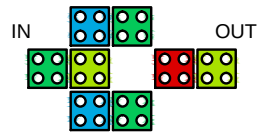
Figure 39 – FO21 and FO22 under combined defects



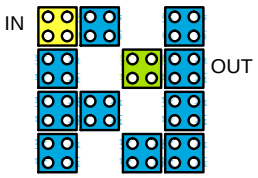
(a) FO31 under combined defects.

(b) FO32 under combined defects.

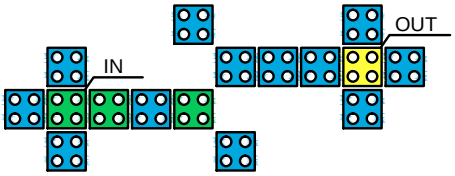
Figure 40 – FO31 and FO32 under combined defects



(a) INV1 under combined defects.



(b) INV2 under combined defects.



(c) INV3 under combined defects.

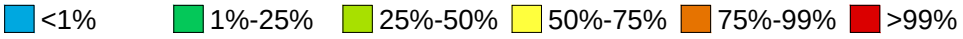
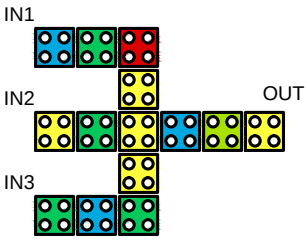
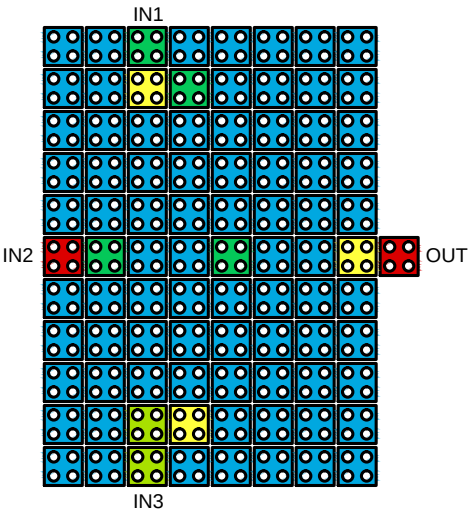


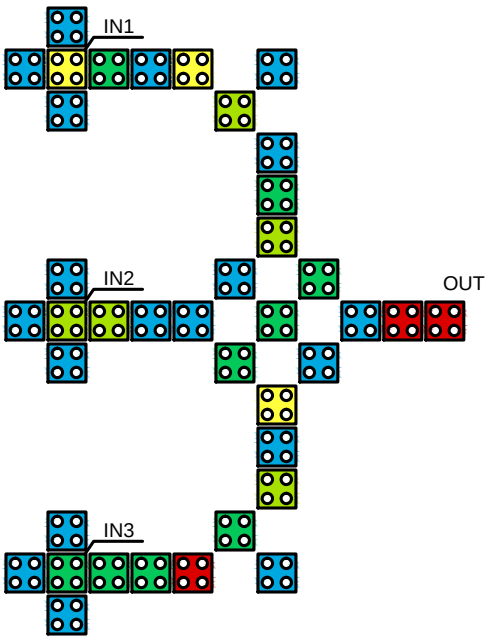
Figure 41 – INV1, INV2 and INV3 under combined defects



(a) MAJ1 under combined defects.



(b) MAJ2 under combined defects.



(c) MAJ3 under combined defects.

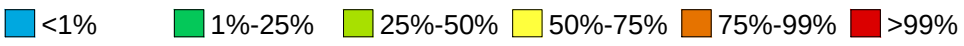
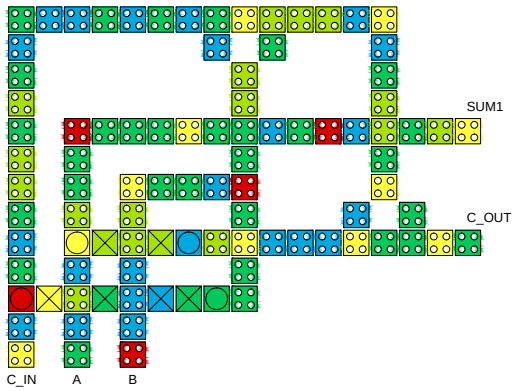
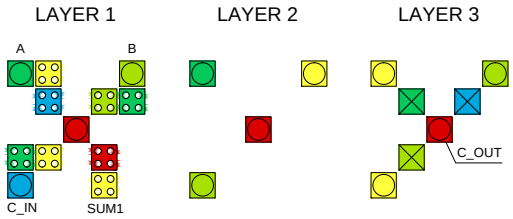


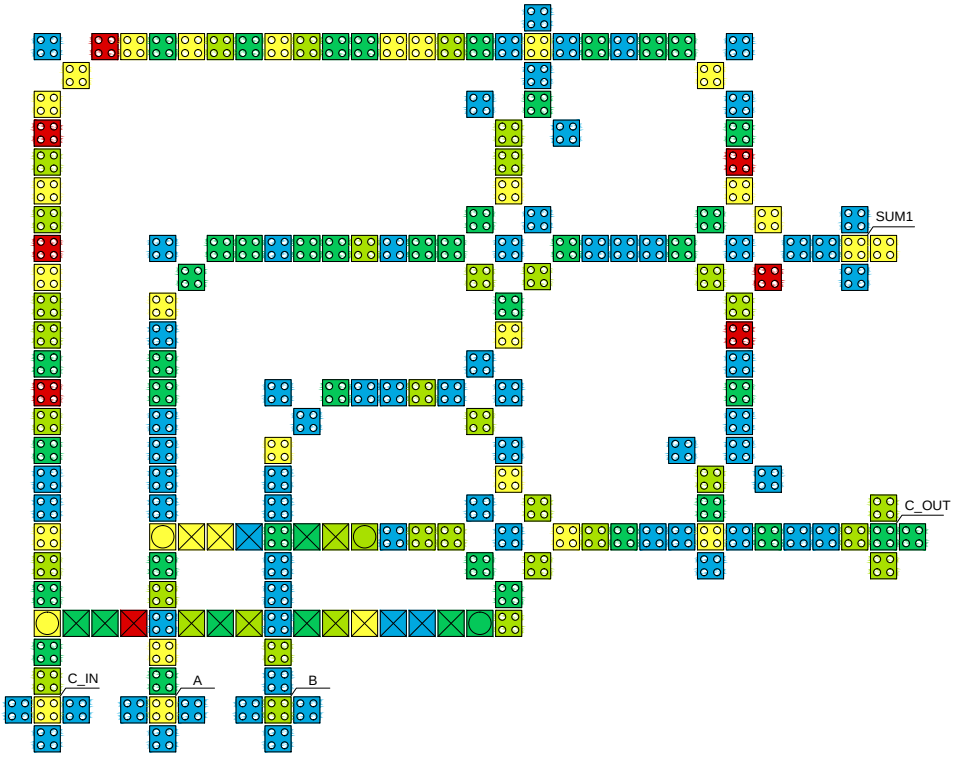
Figure 42 – MAJ1, MAJ2 and MAJ3 under combined defects



(a) ADD1 under combined defects.



(b) ADD2 under combined defects.



(c) ADD3 under combined defects.

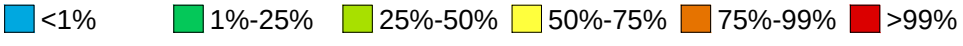


Figure 43 – ADD1, ADD2 and ADD3 under combined defects

B.2 Uniform Probability Model Tests

B.2.1 Wire

B.2.1.1 Dislocation defects

Defect classes selected: • Dislocation
Probability settings: 1/NC

Where:
N: Number of cells
C: Number of defect classes selected

Table 10 – Error-free percent for wire under dislocation defects

	Error-free (%)	Iterations counter
WIR1	87.27	322
WIR2	94.12	306

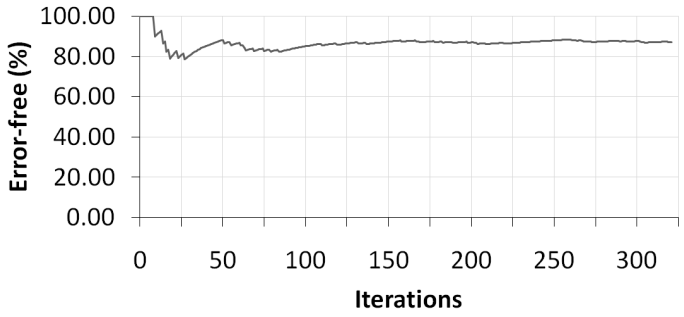


Figure 44 – Error-free percent x Iterations for WIR1 under dislocation defects

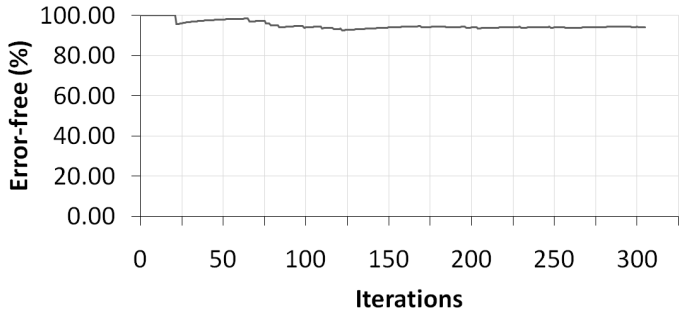


Figure 45 – Error-free percent x Iterations for WIR2 under dislocation defects

B.2.1.2 Dopant defects

Defect classes selected: • Dopant
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 11 – Error-free percent for wire under dopant defects

	Error-free (%)	Iterations counter
WIR1	59.48	427
WIR2	66.32	389

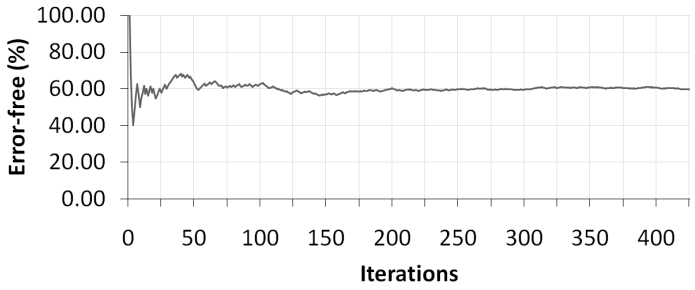


Figure 46 – Error-free percent x Iterations for WIR1 under dopant defects

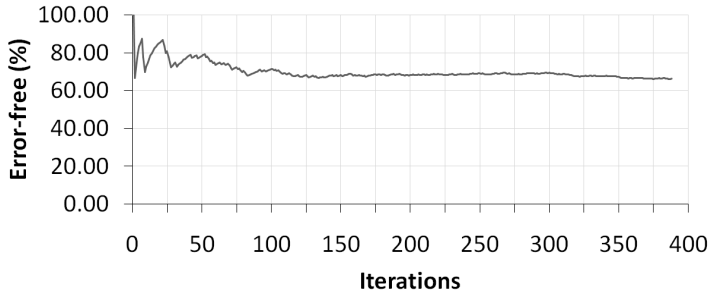


Figure 47 – Error-free percent x Iterations for WIR2 under dopant defects

B.2.1.3 Interstitial defects

Defect classes selected: • Interstitial
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 12 – Error-free percent for wire under interstitial defects

	Error-free (%)	Iterations counter
WIR1	98.53	273
WIR2	100.00	101

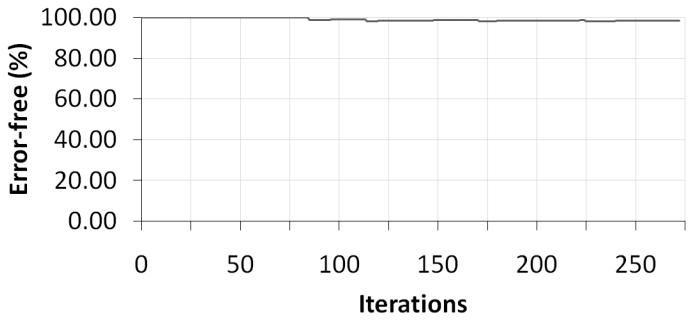


Figure 48 – Error-free percent x Iterations for WIR1 under interstitial defects

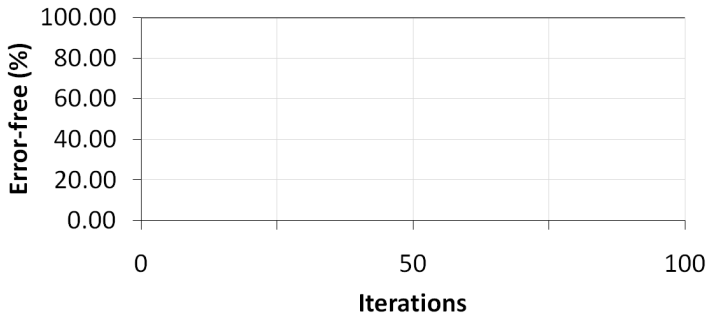


Figure 49 – Error-free percent x Iterations for WIR2 under interstitial defects

B.2.1.4 Vacancy defects

Defect classes selected: • Vacancy
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 13 – Error-free percent for wire under vacancy defects

	Error-free (%)	Iterations counter
WIR1	76.19	357
WIR2	90.37	322

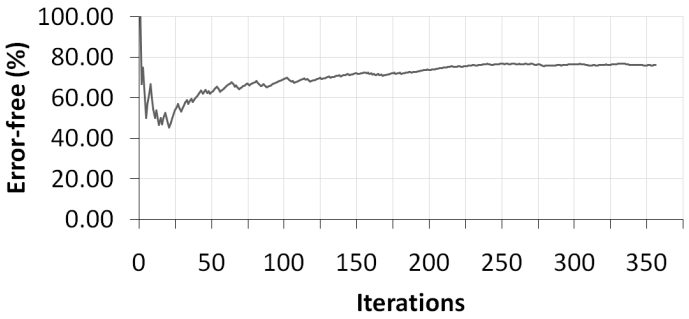


Figure 50 – Error-free percent x Iterations for WIR1 under vacancy defects

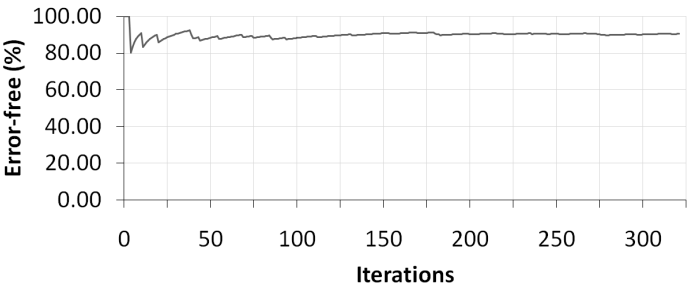


Figure 51 – Error-free percent x Iterations for WIR2 under vacancy defects

B.2.2 Bend Wire

B.2.2.1 Dislocation defects

Defect classes selected: • Dislocation
Probability settings: 1/NC

Where:
N: Number of cells
C: Number of defect classes selected

Table 14 – Error-free percent for bend wire under dislocation defects

	Error-free (%)	Iterations counter
BWI1	86.35	315
BWI2	92.48	306

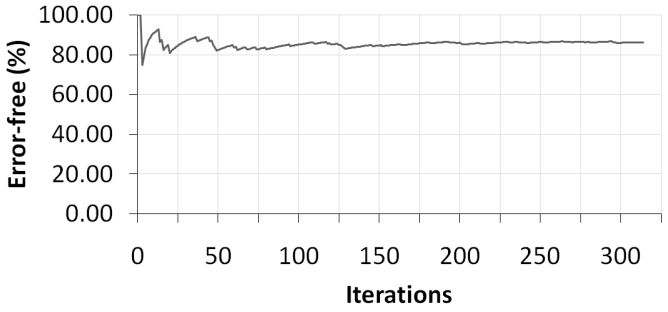


Figure 52 – Error-free percent x Iterations for BWI1 under dislocation defects

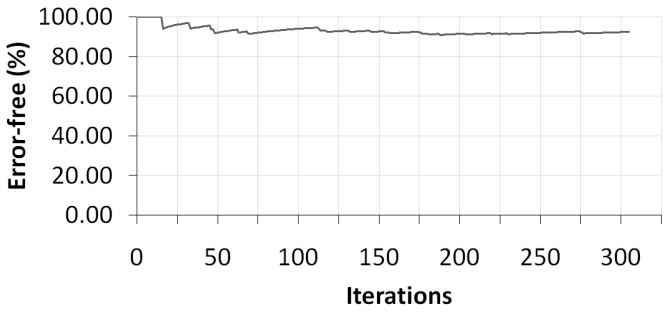


Figure 53 – Error-free percent x Iterations for BWI2 under dislocation defects

B.2.2.2 Dopant defects

Defect classes selected: • Dopant
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 15 – Error-free percent for bend wire under dopant defects

	Error-free (%)	Iterations counter
BWI1	64.83	238
BWI2	74.53	369

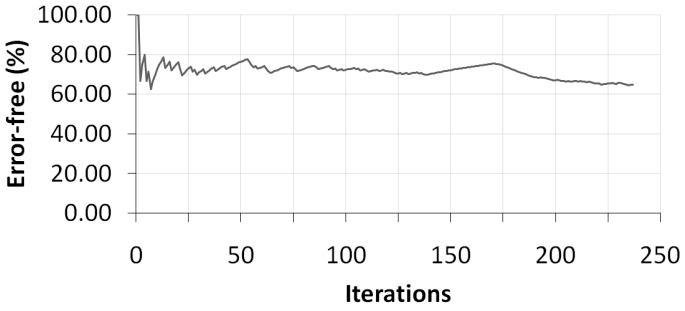


Figure 54 – Error-free percent x Iterations for BWI1 under dopant defects

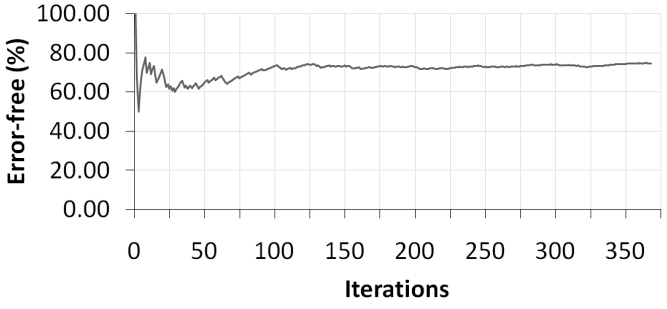


Figure 55 – Error-free percent x Iterations for BWI2 under dopant defects

B.2.2.3 Interstitial defects

Defect classes selected: • Interstitial
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 16 – Error-free percent for bend wire under interstitial defects

	Error-free (%)	Iterations counter
BWI1	98.31	119
BWI2	100.00	101

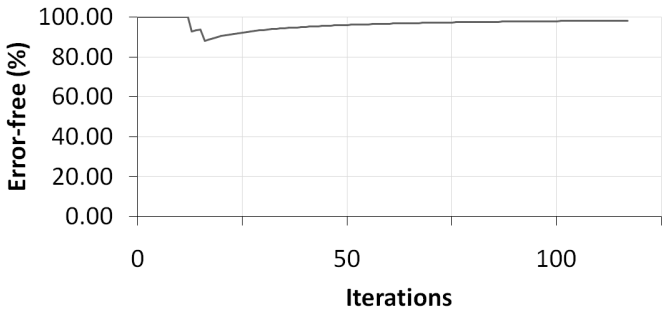


Figure 56 – Error-free percent x Iterations for BWI1 under interstitial defects

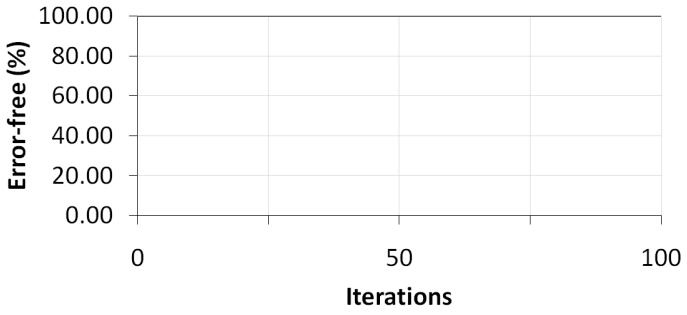


Figure 57 – Error-free percent x Iterations for BWI2 under interstitial defects

B.2.2.4 Vacancy defects

Defect classes selected: • Vacancy
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 17 – Error-free percent for bend wire under vacancy defects

	Error-free (%)	Iterations counter
BWI1	77.56	361
BWI2	99.07	108

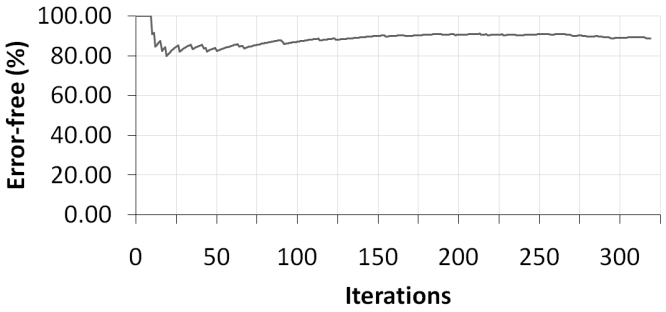


Figure 58 – Error-free percent x Iterations for BWI1 under vacancy defects

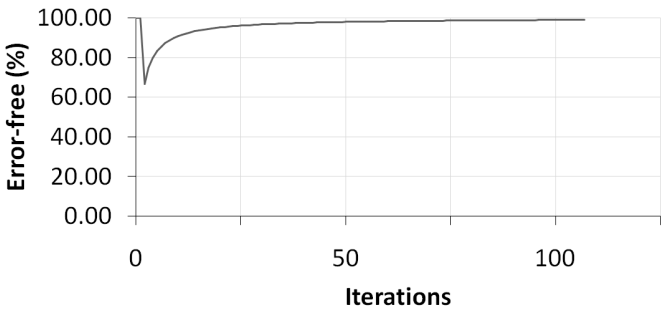


Figure 59 – Error-free percent x Iterations for BWI2 under vacancy defects

B.2.3 Fanout of 2

B.2.3.1 Dislocation defects

Defect classes selected: • Dislocation
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 18 – Error-free percent for fanout of 2 under dislocation defects

	Error-free (%)	Iterations counter
FO21	87.58	314
FO22	92.48	307

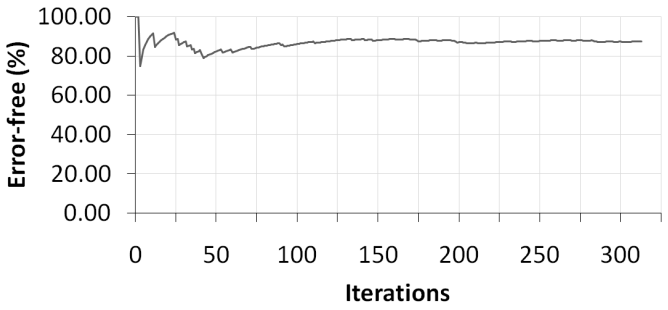


Figure 60 – Error-free percent x Iterations for FO21 under dislocation defects

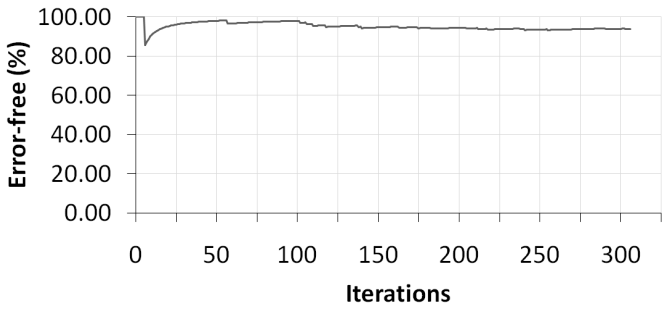


Figure 61 – Error-free percent x Iterations for FO22 under dislocation defects

B.2.3.2 Dopant defects

Defect classes selected: • Dopant
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 19 – Error-free percent for fanout of 2 under dopant defects

	Error-free (%)	Iterations counter
FO21	54.03	472
FO22	74.53	375

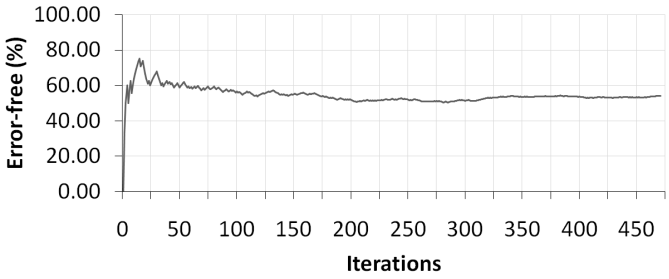


Figure 62 – Error-free percent x Iterations for FO21 under dopant defects

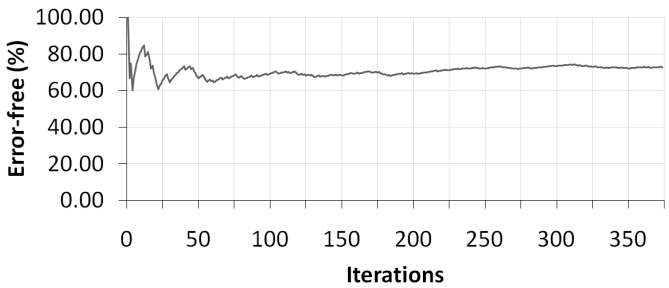


Figure 63 – Error-free percent x Iterations for FO22 under dopant defects

B.2.3.3 Interstitial defects

Defect classes selected: • Interstitial
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 20 – Error-free percent for fanout of 2 under interstitial defects

	Error-free (%)	Iterations counter
FO21	92.11	304
FO22	100.00	101

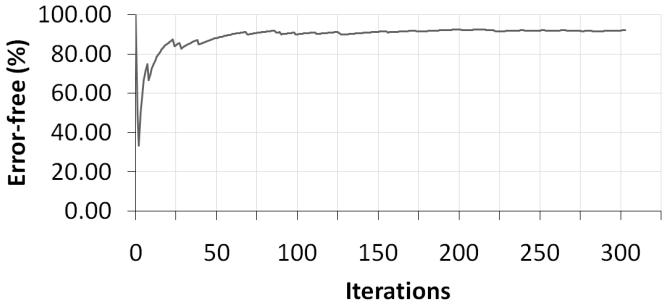


Figure 64 – Error-free percent x Iterations for FO21 under interstitial defects

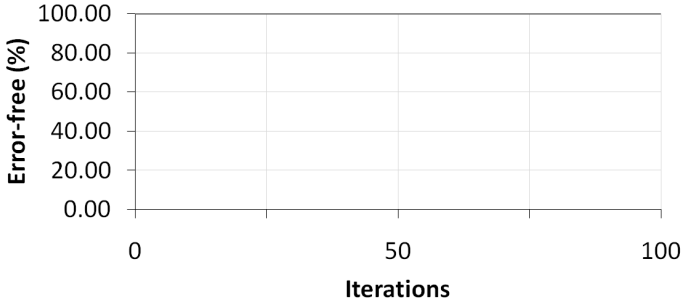


Figure 65 – Error-free percent x Iterations for FO22 under interstitial defects

B.2.3.4 Vacancy defects

Defect classes selected: • Vacancy
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 21 – Error-free percent for fanout of 2 under vacancy defects

	Error-free (%)	Iterations counter
FO21	83.04	336
FO22	99.08	101

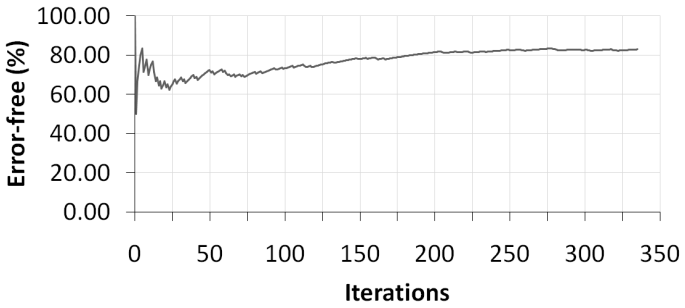


Figure 66 – Error-free percent x Iterations for FO21 under vacancy defects

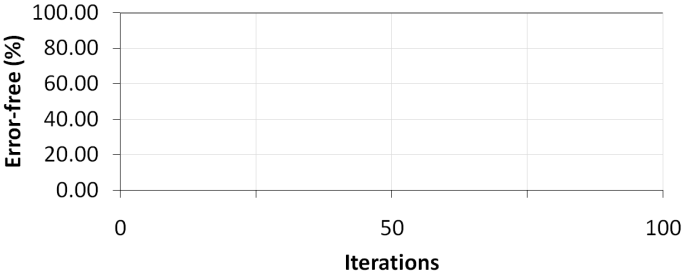


Figure 67 – Error-free percent x Iterations for FO22 under vacancy defects

B.2.4 Fanout of 3

B.2.4.1 Dislocation defects

Defect classes selected: • Dislocation
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 22 – Error-free percent for fanout of 3 under dislocation defects

	Error-free (%)	Iterations counter
FO31	81.87	331
FO32	92.62	298

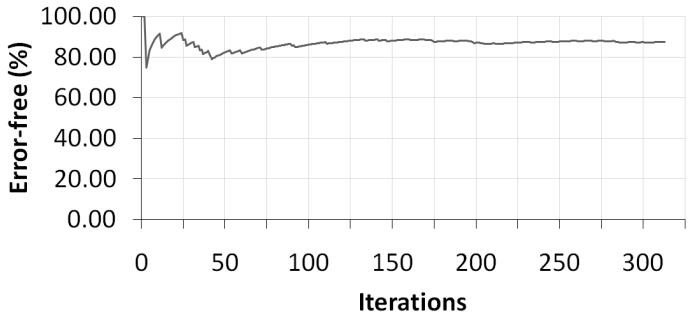


Figure 68 – Error-free percent x Iterations for FO31 under dislocation defects

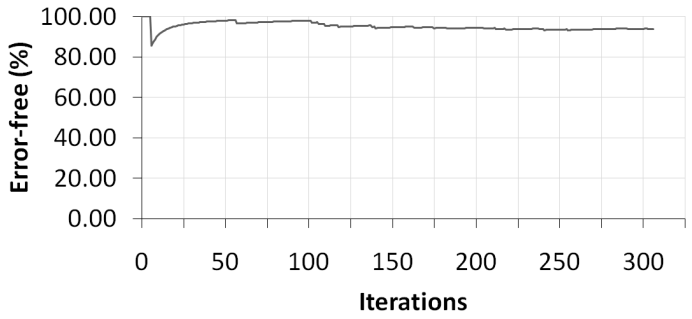


Figure 69 – Error-free percent x Iterations for FO32 under dislocation defects

B.2.4.2 Dopant defects

Defect classes selected: • Dopant
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 23 – Error-free percent for fanout of 3 under dopant defects

	Error-free (%)	Iterations counter
FO31	54.91	468
FO32	68.51	397

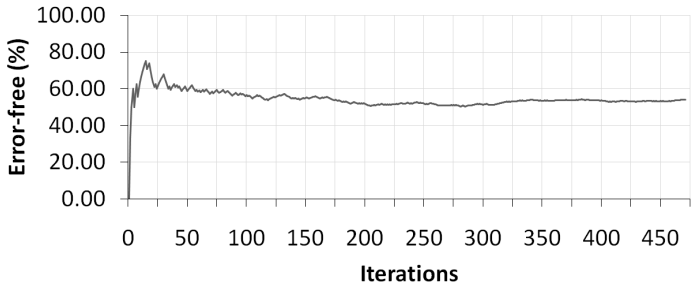


Figure 70 – Error-free percent x Iterations for FO31 under dopant defects

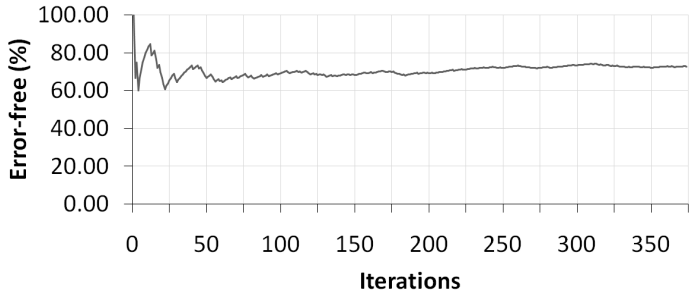


Figure 71 – Error-free percent x Iterations for FO32 under dopant defects

B.2.4.3 Interstitial defects

Defect classes selected: • Interstitial
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 24 – Error-free percent for fanout of 3 under interstitial defects

	Error-free (%)	Iterations counter
FO31	91.96	286
FO32	100.00	101

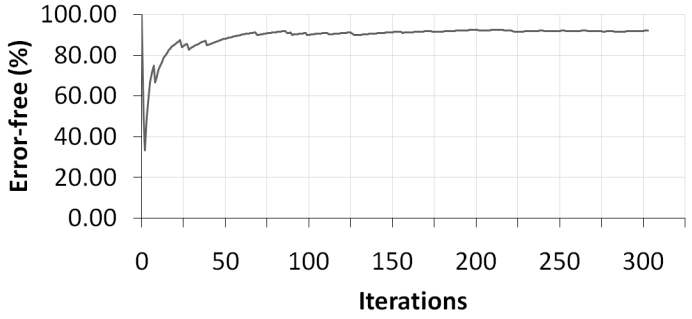


Figure 72 – Error-free percent x Iterations for FO31 under interstitial defects

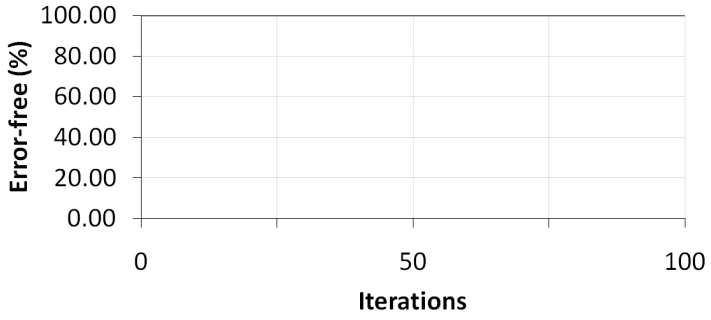


Figure 73 – Error-free percent x Iterations for FO32 under interstitial defects

B.2.4.4 Vacancy defects

Defect classes selected: • Vacancy
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 25 – Error-free percent for fanout of 3 under vacancy defects

	Error-free (%)	Iterations counter
FO31	81.14	350
FO32	98.91	184

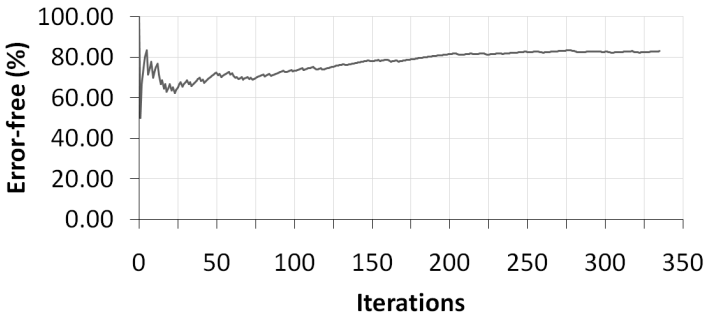


Figure 74 – Error-free percent x Iterations for FO31 under vacancy defects

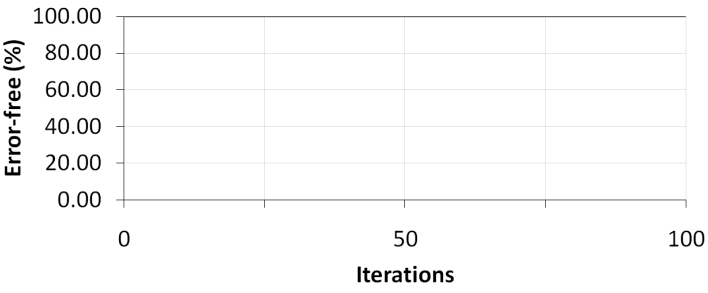


Figure 75 – Error-free percent x Iterations for FO32 under vacancy defects

B.2.5 Inverter

B.2.5.1 Dislocation defects

Defect classes selected: • Dislocation
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 26 – Error-free percent for inverter under dislocation defects

	Error-free (%)	Iterations counter
INV1	79.31	348
INV3	91.75	303

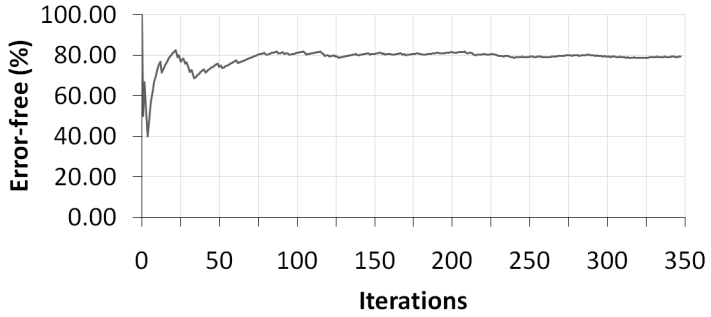


Figure 76 – Error-free percent x Iterations for INV1 under dislocation defects

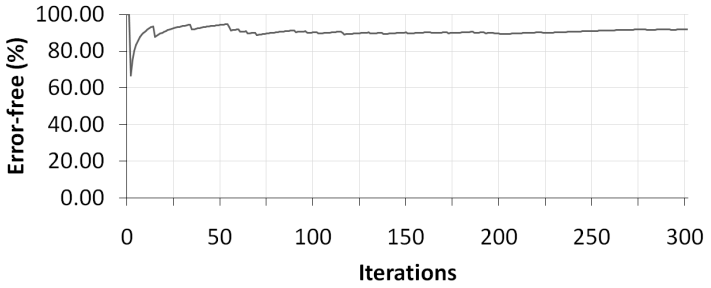


Figure 77 – Error-free percent x Iterations for INV3 under dislocation defects

B.2.5.2 Dopant defects

Defect classes selected: • Dopant
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 27 – Error-free percent for inverter under dopant defects

	Error-free (%)	Iterations counter
INV1	69.26	367
INV3	79.24	342

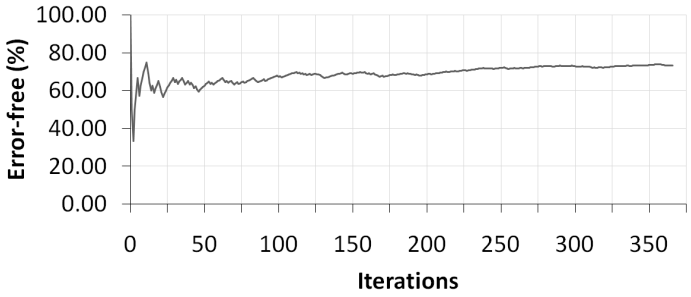


Figure 78 – Error-free percent x Iterations for INV1 under dopant defects

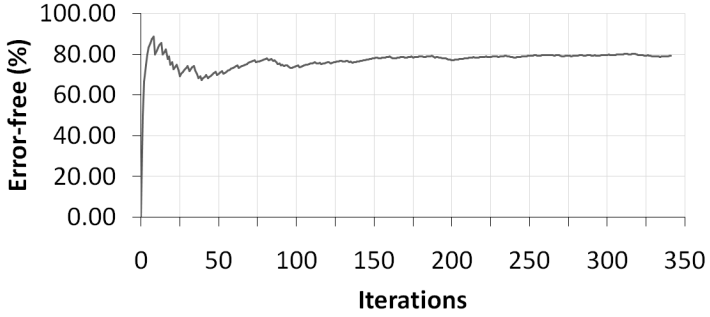


Figure 79 – Error-free percent x Iterations for INV3 under dopant defects

B.2.5.3 Interstitial defects

Defect classes selected: • Interstitial
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 28 – Error-free percent for inverter under interstitial defects

	Error-free (%)	Iterations counter
INV1	94.59	312
INV3	100.00	101

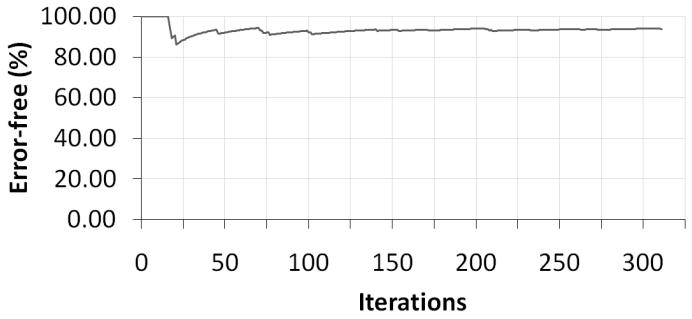


Figure 80 – Error-free percent x Iterations for INV1 under interstitial defects

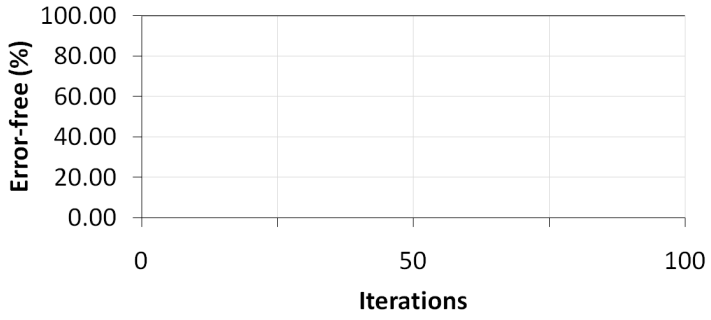


Figure 81 – Error-free percent x Iterations for INV3 under interstitial defects

B.2.5.4 Vacancy defects

Defect classes selected: • Vacancy
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 29 – Error-free percent for inverter under vacancy defects

	Error-free (%)	Iterations counter
INV1	67.00	397
INV3	90.88	307

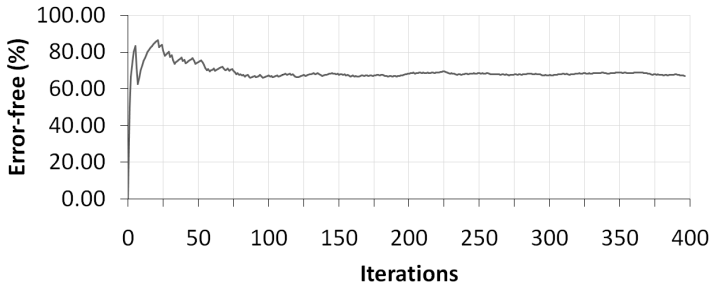


Figure 82 – Error-free percent x Iterations for INV1 under vacancy defects

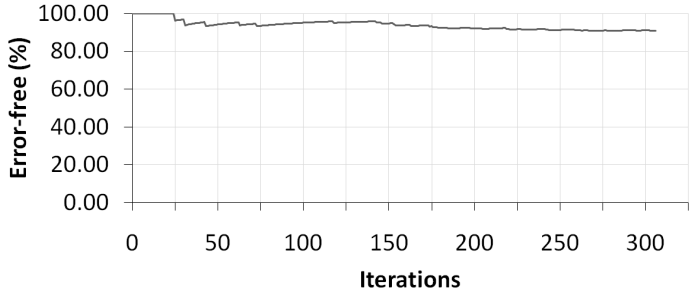


Figure 83 – Error-free percent x Iterations for INV3 under vacancy defects

B.2.6 3-input Majority gate

B.2.6.1 Dislocation defects

Defect classes selected: • Dislocation
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 30 – Error-free percent for 3-input majority gate under dislocation defects

	Error-free (%)	Iterations counter
MAJ1	70.78	402
MAJ2	94.20	273

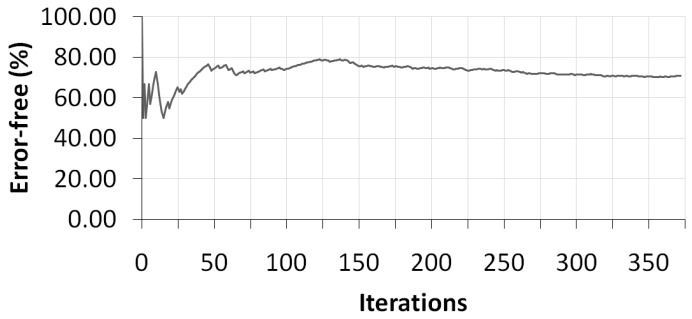


Figure 84 – Error-free percent x Iterations for MAJ1 under dislocation defects

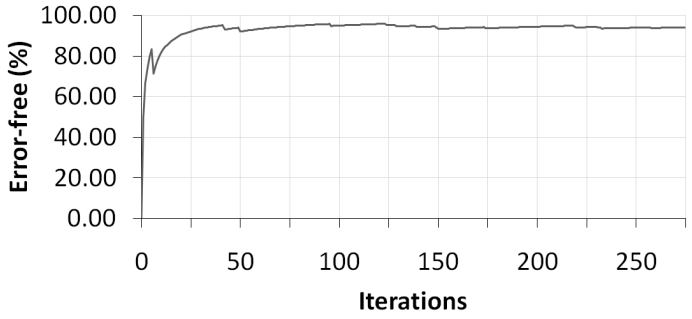


Figure 85 – Error-free percent x Iterations for MAJ3 under dislocation defects

B.2.6.2 Dopant defects

Defect classes selected: • Dopant
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 31 – Error-free percent for 3-input majority gate under dopant defects

	Error-free (%)	Iterations counter
MAJ1	49.69	487
MAJ2	62.81	406

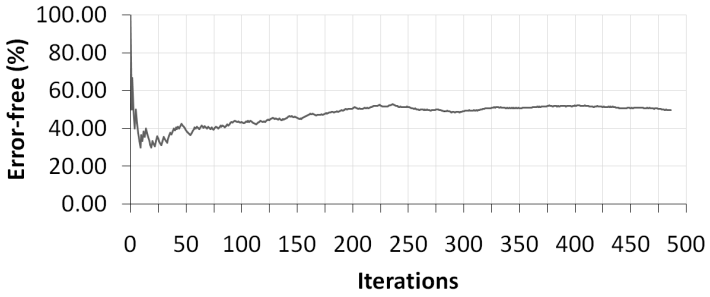


Figure 86 – Error-free percent x Iterations for MAJ1 under dopant defects

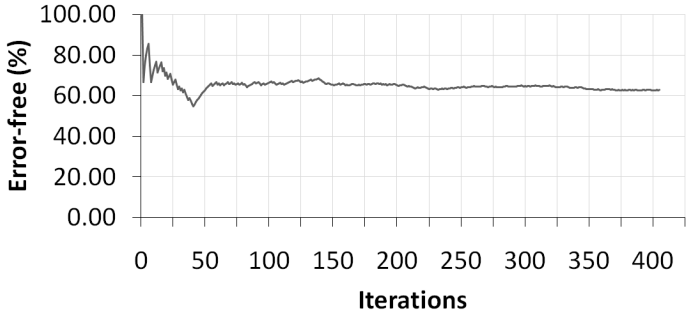


Figure 87 – Error-free percent x Iterations for MAJ3 under dopant defects

B.2.6.3 Interstitial defects

Defect classes selected: • Interstitial
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 32 – Error-free percent for 3-input majority gate under interstitial defects

	Error-free (%)	Iterations counter
MAJ1	91.67	312
MAJ2	98.11	264

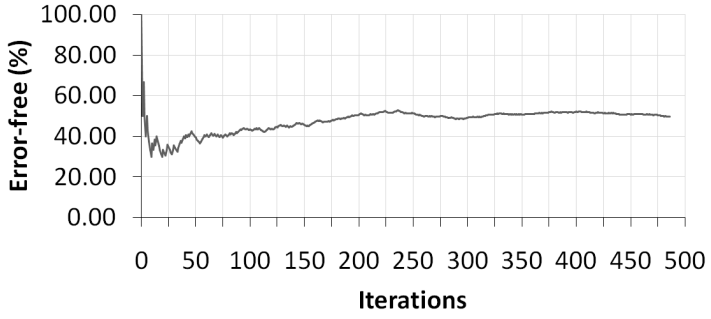


Figure 88 – Error-free percent x Iterations for MAJ1 under interstitial defects

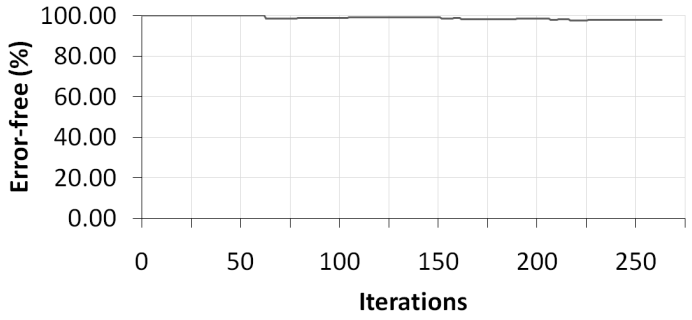


Figure 89 – Error-free percent x Iterations for MAJ3 under interstitial defects

B.2.6.4 Vacancy defects

Defect classes selected: • Vacancy
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 33 – Error-free percent for 3-input majority gate under vacancy defects

	Error-free (%)	Iterations counter
MAJ1	52.93	478
MAJ2	76.52	362

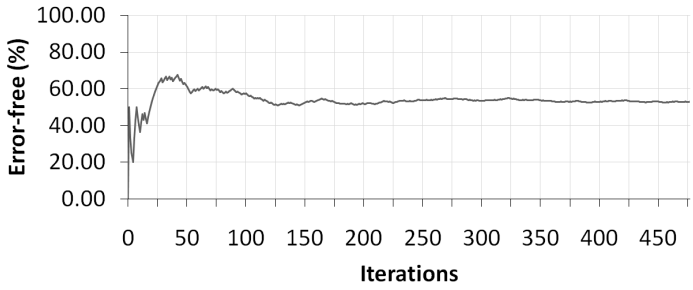


Figure 90 – Error-free percent x Iterations for MAJ1 under vacancy defects

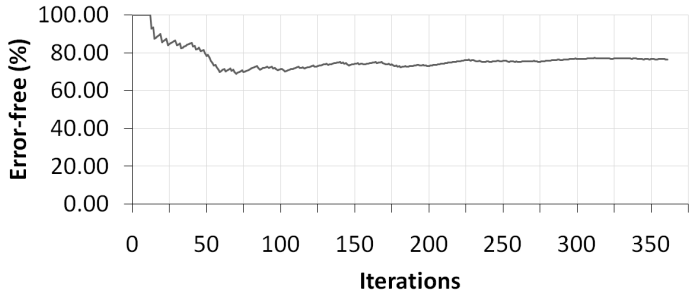


Figure 91 – Error-free percent x Iterations for MAJ3 under vacancy defects

B.2.7 Full Adder

B.2.7.1 Dislocation defects

Defect classes selected: • Dislocation
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 34 – Error-free percent for full adder under dislocation defects

	Error-free (%)	Iterations counter
ADD1	85.67	335
ADD3	86.77	325

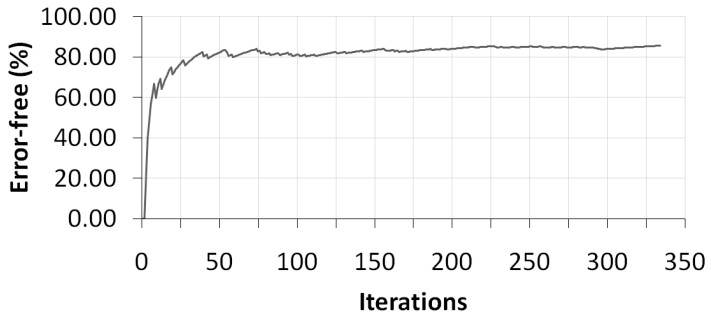


Figure 92 – Error-free percent x Iterations for ADD1 under dislocation defects

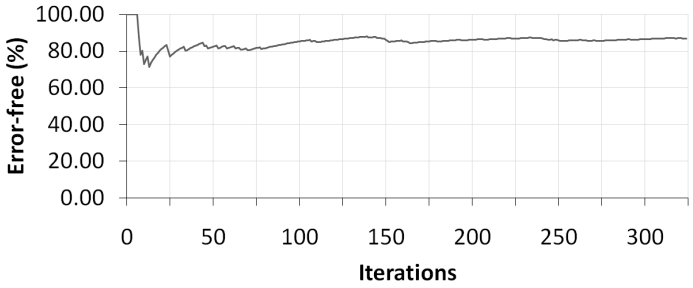


Figure 93 – Error-free percent x Iterations for ADD3 under dislocation defects

B.2.7.2 Dopant defects

Defect classes selected: • Dopant
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 35 – Error-free percent for full adder under dopant defects

	Error-free (%)	Iterations counter
ADD1	53.65	479
ADD3	56.57	386

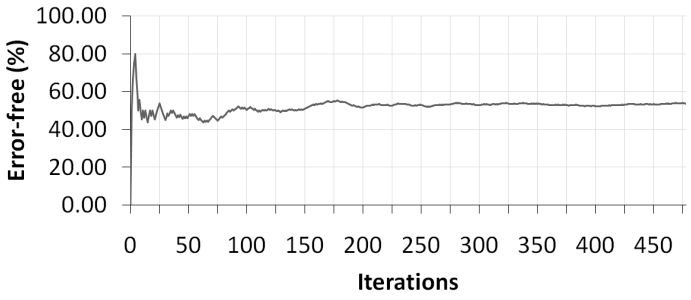


Figure 94 – Error-free percent x Iterations for ADD1 under dopant defects

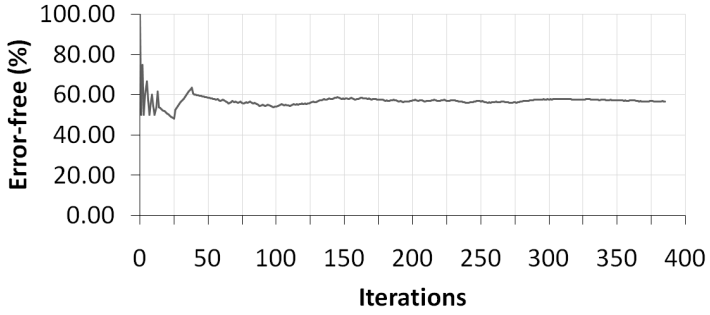


Figure 95 – Error-free percent x Iterations for ADD3 under dopant defects

B.2.7.3 Interstitial defects

Defect classes selected: • Interstitial
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 36 – Error-free percent for full adder under interstitial defects

	Error-free (%)	Iterations counter
ADD1	93.29	313
ADD3	94.48	308

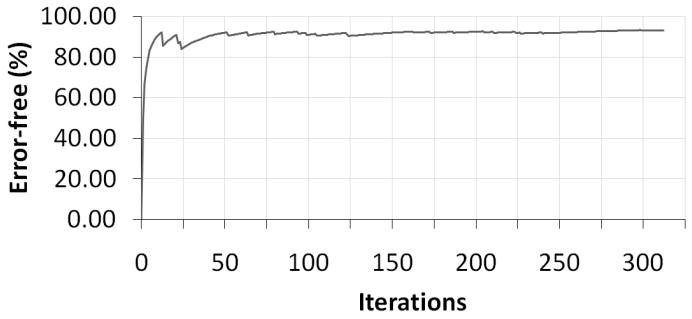


Figure 96 – Error-free percent x Iterations for ADD1 under interstitial defects

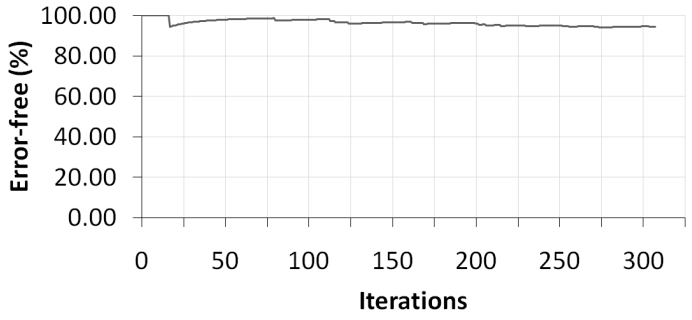


Figure 97 – Error-free percent x Iterations for ADD3 under interstitial defects

B.2.7.4 Vacancy defects

Defect classes selected: • Vacancy
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

Table 37 – Error-free percent for full adder under vacancy defects

	Error-free (%)	Iterations counter
ADD1	54.57	460
ADD3	63.96	419

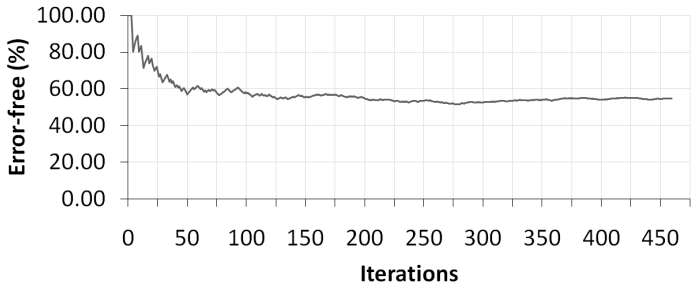


Figure 98 – Error-free percent x Iterations for ADD1 under vacancy defects

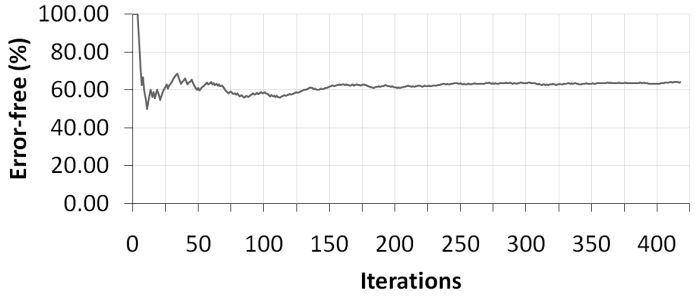


Figure 99 – Error-free percent x Iterations for ADD3 under vacancy defects

B.2.8 4-Bit Ripple-carry Adder

B.2.8.1 Combined defects

Defect classes selected:
- Dislocation
- Dopant
- Interstitial
- Vacancy

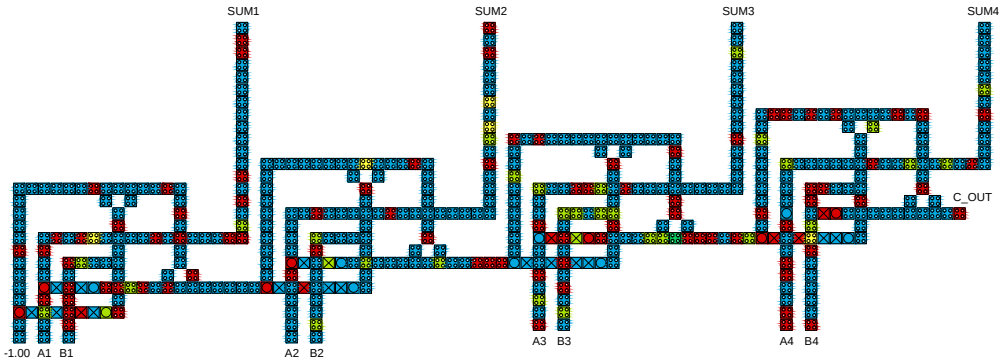
Probability settings: $1/NC$

Where:
N: Number of cells
C: Number of defect classes selected

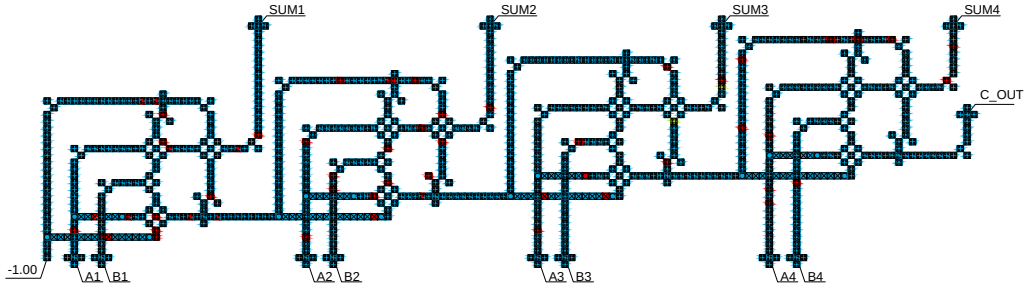
Table 38 – Error-free percent for 4-Bit Ripple-carry adder under combined defects

	Error-free (%)	Iterations counter
RCA1	72.27	299
RCA2	64.93	223
RCA3	80.53	230

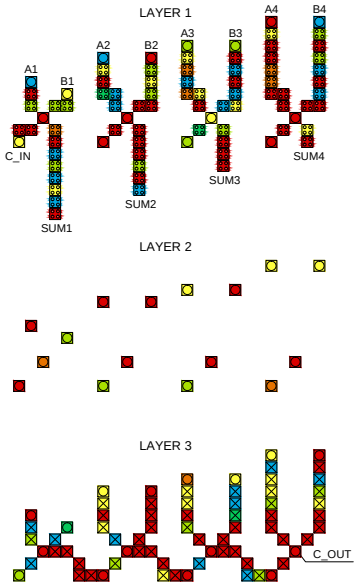
B.2.8.1.1 Heat maps



(a) RCA1 under combined defects.



(b) RCA3 under combined defects.



(c) RCA2 under combined defects.

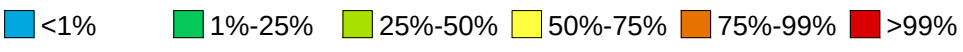


Figure 100 – RCA1, RCA2 and RCA3 under combined defects

B.2.8.1.2 Error-free percent x Iterations

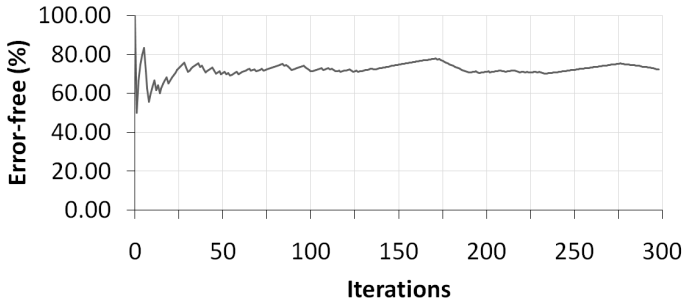


Figure 101 – Error-free percent x Iterations for RCA1 under combined defects

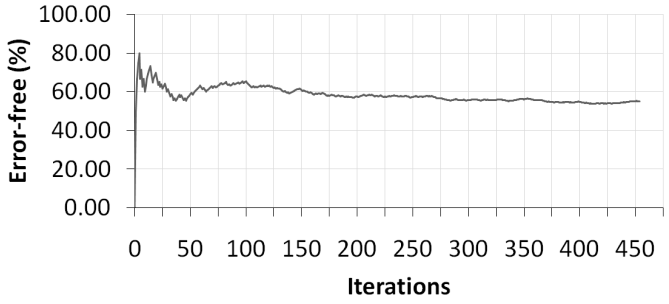


Figure 102 – Error-free percent x Iterations for RCA2 under combined defects

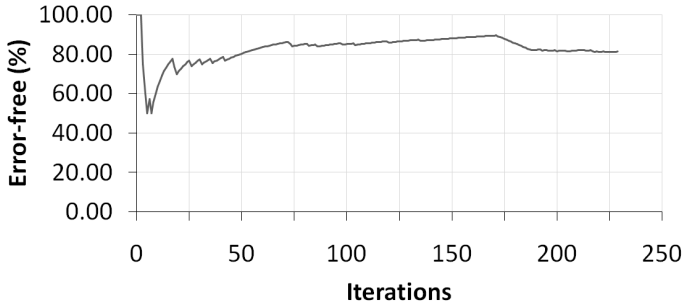


Figure 103 – Error-free percent x Iterations for RCA3 under combined defects

APPENDIX C – Simulation Results - Phase-Shifted Clock Signals

C.1 Wire

Range of shifts: 0.00° to 90.00°

Range divisions: 24

Maximum number of iterations per division: 1000

C.1.1 Synchronous clock signals ($\alpha = 0$ %)

Table 39 – Error-free simulation rates for QCA wires with phase-deviated synchronous clock signals ($\alpha = 0$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	199	0	100.00 %
2	3.75° to 7.50°	165	0	100.00 %
3	7.50° to 11.25°	159	0	100.00 %
4	11.25° to 15.00°	169	0	100.00 %
5	15.00° to 18.75°	180	0	100.00 %
6	18.75° to 22.50°	159	0	100.00 %
7	22.50° to 26.25°	154	0	100.00 %
8	26.25° to 30.00°	172	0	100.00 %
9	30.00° to 33.75°	161	0	100.00 %
10	33.75° to 37.50°	153	0	100.00 %
11	37.50° to 41.25°	163	42	74.23 %
12	41.25° to 45.00°	166	29	82.53 %
13	45.00° to 48.75°	155	33	78.71 %
14	48.75° to 52.50°	155	37	76.13 %
15	52.50° to 56.25°	143	35	75.52 %
16	56.25° to 60.00°	180	53	70.56 %
17	60.00° to 63.75°	172	43	75.00 %
18	63.75° to 67.50°	158	40	74.68 %
19	67.50° to 71.25°	178	51	71.35 %
20	71.25° to 75.00°	178	30	83.15 %
21	75.00° to 78.75°	175	46	73.71 %
22	78.75° to 82.50°	184	58	68.48 %
23	82.50° to 86.25°	173	72	58.38 %
24	86.25° to 90.00°	149	56	62.42 %

Average error-free rate for indexes 1 to 12: 92.45 %
Average error-free rate for indexes 13 to 24: 72.30 %
Average error-free rate for overall shift : 84.38 %

C.1.2 Asynchronous clock signals ($\alpha = 10$ %)

Table 40 – Error-free simulation rates for QCA wires with phase-deviated asynchronous clock signals ($\alpha = 10$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	133	0	100.00 %
2	3.75° to 7.50°	174	0	100.00 %
3	7.50° to 11.25°	176	0	100.00 %
4	11.25° to 15.00°	159	0	100.00 %
5	15.00° to 18.75°	159	0	100.00 %
6	18.75° to 22.50°	162	0	100.00 %
7	22.50° to 26.25°	167	0	100.00 %
8	26.25° to 30.00°	167	0	100.00 %
9	30.00° to 33.75°	179	0	100.00 %
10	33.75° to 37.50°	176	0	100.00 %
11	37.50° to 41.25°	170	0	100.00 %
12	41.25° to 45.00°	178	6	96.63 %
13	45.00° to 48.75°	181	51	71.82 %
14	48.75° to 52.50°	151	32	78.81 %
15	52.50° to 56.25°	155	48	69.03 %
16	56.25° to 60.00°	158	37	76.58 %
17	60.00° to 63.75°	184	40	78.26 %
18	63.75° to 67.50°	155	38	75.48 %
19	67.50° to 71.25°	168	47	72.02 %
20	71.25° to 75.00°	180	40	77.78 %
21	75.00° to 78.75°	177	50	71.75 %
22	78.75° to 82.50°	174	50	71.26 %
23	82.50° to 86.25°	149	45	69.80 %
24	86.25° to 90.00°	168	56	66.67 %

Average error-free rate for indexes 1 to 12: 99.70 %
Average error-free rate for indexes 13 to 24: 73.30 %
Average error-free rate for overall shift : 86.50 %

C.1.3 Asynchronous clock signals ($\alpha = 20$ %)

Table 41 – Error-free simulation rates for QCA wires with phase-deviated asynchronous clock signals ($\alpha = 20$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	177	0	100.00 %
2	3.75° to 7.50°	212	0	100.00 %
3	7.50° to 11.25°	150	0	100.00 %
4	11.25° to 15.00°	167	0	100.00 %
5	15.00° to 18.75°	180	0	100.00 %
6	18.75° to 22.50°	171	0	100.00 %
7	22.50° to 26.25°	172	0	100.00 %
8	26.25° to 30.00°	152	0	100.00 %
9	30.00° to 33.75°	147	0	100.00 %
10	33.75° to 37.50°	158	0	100.00 %
11	37.50° to 41.25°	167	0	100.00 %
12	41.25° to 45.00°	147	0	100.00 %
13	45.00° to 48.75°	182	43	76.37 %
14	48.75° to 52.50°	173	24	86.13 %
15	52.50° to 56.25°	168	46	72.62 %
16	56.25° to 60.00°	162	47	70.99 %
17	60.00° to 63.75°	179	69	61.45 %
18	63.75° to 67.50°	168	52	69.05 %
19	67.50° to 71.25°	167	47	71.86 %
20	71.25° to 75.00°	160	59	63.13 %
21	75.00° to 78.75°	177	51	71.19 %
22	78.75° to 82.50°	163	70	57.06 %
23	82.50° to 86.25°	147	35	76.19 %
24	86.25° to 90.00°	154	49	68.18 %

Average error-free rate for indexes 1 to 12: 100.00 %
Average error-free rate for indexes 13 to 24: 70.40 %
Average error-free rate for overall shift : 85.20 %

C.1.4 Asynchronous clock signals ($\alpha = 30$ %)

Table 42 – Error-free simulation rates for QCA wires with phase-deviated asynchronous clock signals ($\alpha = 30$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	153	0	100.00 %
2	3.75° to 7.50°	158	0	100.00 %
3	7.50° to 11.25°	148	0	100.00 %
4	11.25° to 15.00°	172	0	100.00 %
5	15.00° to 18.75°	146	0	100.00 %
6	18.75° to 22.50°	183	0	100.00 %
7	22.50° to 26.25°	177	0	100.00 %
8	26.25° to 30.00°	174	0	100.00 %
9	30.00° to 33.75°	162	0	100.00 %
10	33.75° to 37.50°	192	0	100.00 %
11	37.50° to 41.25°	168	0	100.00 %
12	41.25° to 45.00°	167	0	100.00 %
13	45.00° to 48.75°	164	31	81.10 %
14	48.75° to 52.50°	170	40	76.47 %
15	52.50° to 56.25°	187	55	70.59 %
16	56.25° to 60.00°	170	27	84.12 %
17	60.00° to 63.75°	159	49	69.18 %
18	63.75° to 67.50°	173	65	62.43 %
19	67.50° to 71.25°	159	66	58.48 %
20	71.25° to 75.00°	165	52	68.48 %
21	75.00° to 78.75°	171	40	76.61 %
22	78.75° to 82.50°	159	52	67.30 %
23	82.50° to 86.25°	168	46	72.62 %
24	86.25° to 90.00°	155	50	67.74 %

Average error-free rate for indexes 1 to 12: 100.00 %
Average error-free rate for indexes 13 to 24: 71.35 %
Average error-free rate for overall shift : 85.68 %

C.1.5 Asynchronous clock signals ($\alpha = 40$ %)

Table 43 – Error-free simulation rates for QCA wires with phase-deviated asynchronous clock signals ($\alpha = 40$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	156	0	100.00 %
2	3.75° to 7.50°	177	0	100.00 %
3	7.50° to 11.25°	165	0	100.00 %
4	11.25° to 15.00°	175	0	100.00 %
5	15.00° to 18.75°	178	0	100.00 %
6	18.75° to 22.50°	156	0	100.00 %
7	22.50° to 26.25°	180	0	100.00 %
8	26.25° to 30.00°	170	0	100.00 %
9	30.00° to 33.75°	158	0	100.00 %
10	33.75° to 37.50°	156	0	100.00 %
11	37.50° to 41.25°	156	0	100.00 %
12	41.25° to 45.00°	173	0	100.00 %
13	45.00° to 48.75°	155	39	74.84 %
14	48.75° to 52.50°	159	44	72.33 %
15	52.50° to 56.25°	156	45	71.15 %
16	56.25° to 60.00°	192	43	77.60 %
17	60.00° to 63.75°	144	38	73.61 %
18	63.75° to 67.50°	142	32	77.46 %
19	67.50° to 71.25°	195	56	71.28 %
20	71.25° to 75.00°	185	65	64.86 %
21	75.00° to 78.75°	154	43	72.08 %
22	78.75° to 82.50°	160	44	72.50 %
23	82.50° to 86.25°	182	66	63.74 %
24	86.25° to 90.00°	176	51	71.02 %

Average error-free rate for indexes 1 to 12: 100.00 %
Average error-free rate for indexes 12 to 24: 71.70 %
Average error-free rate for overall shift : 85.85 %

Table 44 – Wire - Error-free rates

Hold phase time increasing	Average error-free rate for indexes 1 to 12	Average error-free rate for indexes 13 to 24	Average error-free rate for overall shift
0 %	96.45 %	72.30 %	84.38 %
10 %	99.70 %	73.30 %	86.50 %
20 %	100.00 %	70.40 %	85.20 %
30 %	100.00 %	71.35 %	85.68 %
40 %	100.00 %	71.70 %	85.85 %

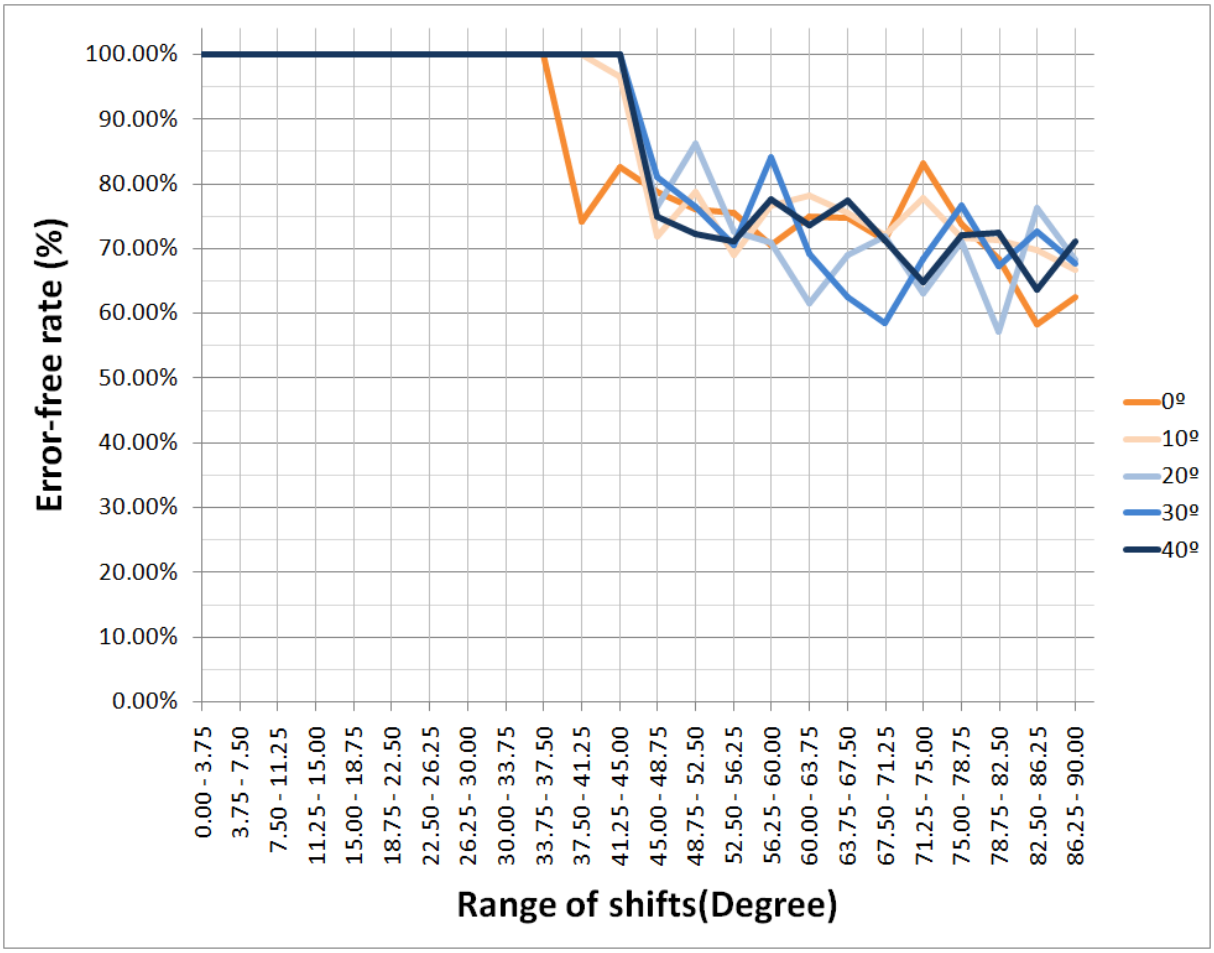
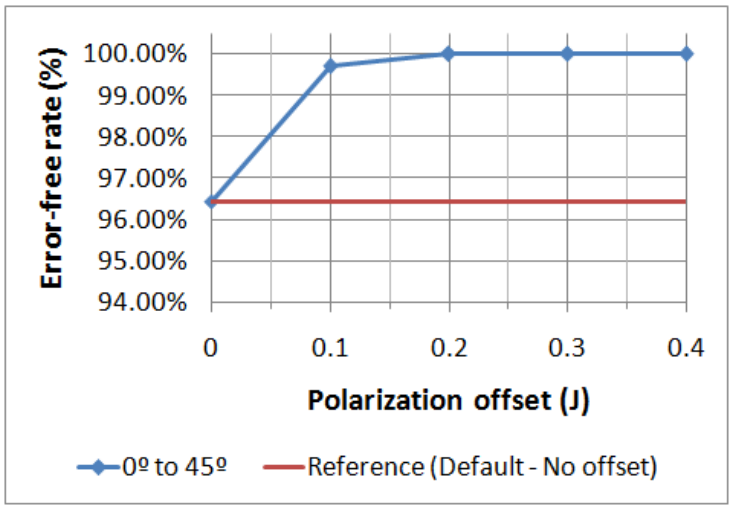
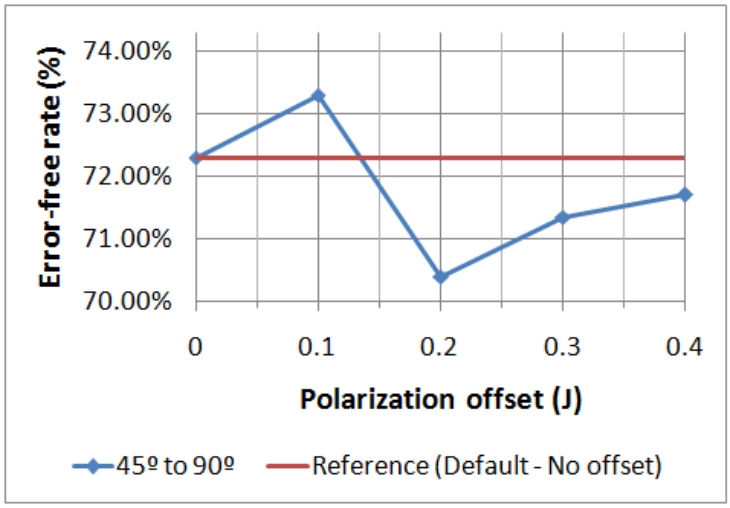


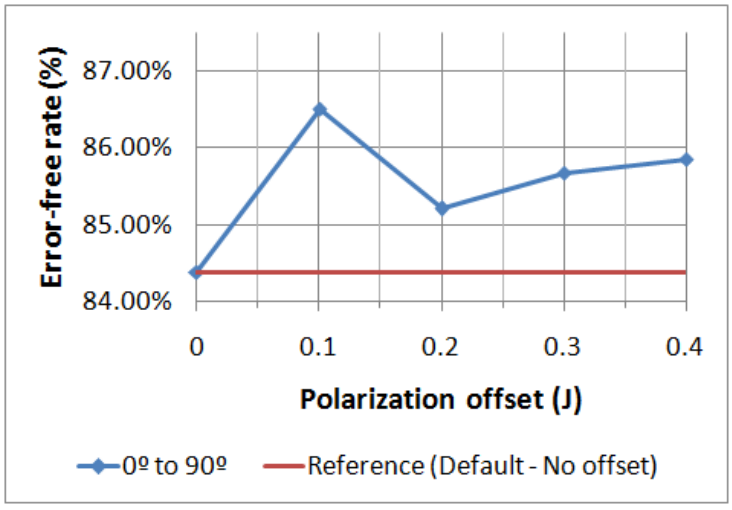
Figure 104 – Wire - % Success X Range of shifts



(a) Error free simulations (%) X Polarization offset (J) - Average error-free rate for indexes 1 to 12



(b) Error free simulations (%) X Polarization offset (J) - Average error-free rate for indexes 13 to 24



(c) Error free simulations (%) X Polarization offset (J) - Average error-free rate for overall shift

Figure 105 – Wire - Error free simulations (%) X Polarization offset (J)

C.2 Bend Wire

Range of shifts: 0.00° to 90.00°

Range divisions: 24

Maximum number of iterations per division: 1000

C.2.1 Synchronous clock signals ($\alpha = 0$ %)

Table 45 – Error-free simulation rates for QCA bend wires with phase-deviated synchronous clock signals ($\alpha = 0$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	150	0	100.00 %
2	3.75° to 7.50°	168	0	100.00 %
3	7.50° to 11.25°	171	0	100.00 %
4	11.25° to 15.00°	177	0	100.00 %
5	15.00° to 18.75°	183	0	100.00 %
6	18.75° to 22.50°	173	0	100.00 %
7	22.50° to 26.25°	167	0	100.00 %
8	26.25° to 30.00°	191	0	100.00 %
9	30.00° to 33.75°	164	0	100.00 %
10	33.75° to 37.50°	165	2	98.79 %
11	37.50° to 41.25°	146	29	80.14 %
12	41.25° to 45.00°	145	33	77.24 %
13	45.00° to 48.75°	157	40	74.52 %
14	48.75° to 52.50°	168	73	56.55 %
15	52.50° to 56.25°	189	97	48.68 %
16	56.25° to 60.00°	170	94	44.71 %
17	60.00° to 63.75°	167	72	56.89 %
18	63.75° to 67.50°	152	78	48.68 %
19	67.50° to 71.25°	165	76	53.94 %
20	71.25° to 75.00°	151	70	53.64 %
21	75.00° to 78.75°	177	80	54.80 %
22	78.75° to 82.50°	155	87	43.87 %
23	82.50° to 86.25°	163	106	34.97 %
24	86.25° to 90.00°	186	122	34.41 %

Average error-free rate for indexes 1 to 12: 96.80 %
Average error-free rate for indexes 13 to 24: 50.25 %
Average error-free rate for overall shift : 73.53 %

C.2.2 Asynchronous clock signals ($\alpha = 10$ %)

Table 46 – Error-free simulation rates for QCA bend wires with phase-deviated asynchronous clock signals ($\alpha = 10$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	133	0	100.00 %
2	3.75° to 7.50°	174	0	100.00 %
3	7.50° to 11.25°	176	0	100.00 %
4	11.25° to 15.00°	159	0	100.00 %
5	15.00° to 18.75°	159	0	100.00 %
6	18.75° to 22.50°	162	0	100.00 %
7	22.50° to 26.25°	167	0	100.00 %
8	26.25° to 30.00°	167	0	100.00 %
9	30.00° to 33.75°	179	0	100.00 %
10	33.75° to 37.50°	176	0	100.00 %
11	37.50° to 41.25°	170	0	100.00 %
12	41.25° to 45.00°	178	6	96.63 %
13	45.00° to 48.75°	185	51	72.43 %
14	48.75° to 52.50°	175	77	56.00 %
15	52.50° to 56.25°	167	73	56.29 %
16	56.25° to 60.00°	157	86	45.22 %
17	60.00° to 63.75°	144	79	45.14 %
18	63.75° to 67.50°	159	81	49.06 %
19	67.50° to 71.25°	166	82	50.06 %
20	71.25° to 75.00°	164	88	46.34 %
21	75.00° to 78.75°	155	81	47.74 %
22	78.75° to 82.50°	185	93	49.73 %
23	82.50° to 86.25°	170	94	44.71 %
24	86.25° to 90.00°	173	104	39.88 %

Average error-free rate for indexes 1 to 12: 99.70 %
Average error-free rate for indexes 13 to 24: 50.55 %
Average error-free rate for overall shift : 75.13 %

C.2.3 Asynchronous clock signals ($\alpha = 20$ %)

Table 47 – Error-free simulation rates for QCA bend wires with phase-deviated asynchronous clock signals ($\alpha = 20$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	157	0	100.00 %
2	3.75° to 7.50°	148	0	100.00 %
3	7.50° to 11.25°	155	0	100.00 %
4	11.25° to 15.00°	159	0	100.00 %
5	15.00° to 18.75°	152	0	100.00 %
6	18.75° to 22.50°	201	0	100.00 %
7	22.50° to 26.25°	160	0	100.00 %
8	26.25° to 30.00°	168	0	100.00 %
9	30.00° to 33.75°	172	0	100.00 %
10	33.75° to 37.50°	158	0	100.00 %
11	37.50° to 41.25°	195	0	100.00 %
12	41.25° to 45.00°	175	0	100.00 %
13	45.00° to 48.75°	154	46	70.13 %
14	48.75° to 52.50°	159	58	63.52 %
15	52.50° to 56.25°	166	78	53.01 %
16	56.25° to 60.00°	171	102	40.35 %
17	60.00° to 63.75°	150	72	52.00 %
18	63.75° to 67.50°	174	83	52.30 %
19	67.50° to 71.25°	161	76	52.80 %
20	71.25° to 75.00°	167	74	55.69 %
21	75.00° to 78.75°	196	99	49.49 %
22	78.75° to 82.50°	176	97	44.89 %
23	82.50° to 86.25°	176	96	45.45 %
24	86.25° to 90.00°	150	62	58.67 %

Average error-free rate for indexes 1 to 12: 100.00 %
Average error-free rate for indexes 13 to 24: 52.85 %
Average error-free rate for overall shift : 76.43 %

C.2.4 Asynchronous clock signals ($\alpha = 30$ %)

Table 48 – Error-free simulation rates for QCA bend wires with phase-deviated asynchronous clock signals ($\alpha = 30$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	186	0	100.00 %
2	3.75° to 7.50°	158	0	100.00 %
3	7.50° to 11.25°	173	0	100.00 %
4	11.25° to 15.00°	167	0	100.00 %
5	15.00° to 18.75°	142	0	100.00 %
6	18.75° to 22.50°	155	0	100.00 %
7	22.50° to 26.25°	184	0	100.00 %
8	26.25° to 30.00°	161	0	100.00 %
9	30.00° to 33.75°	174	0	100.00 %
10	33.75° to 37.50°	161	0	100.00 %
11	37.50° to 41.25°	165	0	100.00 %
12	41.25° to 45.00°	174	1	99.43 %
13	45.00° to 48.75°	176	48	72.73 %
14	48.75° to 52.50°	174	75	56.90 %
15	52.50° to 56.25°	162	85	47.53 %
16	56.25° to 60.00°	167	66	60.48 %
17	60.00° to 63.75°	166	79	52.41 %
18	63.75° to 67.50°	153	72	52.94 %
19	67.50° to 71.25°	170	91	46.47 %
20	71.25° to 75.00°	168	79	52.98 %
21	75.00° to 78.75°	168	88	47.62 %
22	78.75° to 82.50°	152	79	48.03 %
23	82.50° to 86.25°	171	90	47.37 %
24	86.25° to 90.00°	173	70	59.54 %

Average error-free rate for indexes 1 to 12: 99.95 %
Average error-free rate for indexes 13 to 24: 53.90 %
Average error-free rate for overall shift : 76.93 %

C.2.5 Asynchronous clock signals ($\alpha = 40$ %)

Table 49 – Error-free simulation rates for QCA bend wires with phase-deviated asynchronous clock signals ($\alpha = 40$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	178	0	100.00 %
2	3.75° to 7.50°	170	0	100.00 %
3	7.50° to 11.25°	162	0	100.00 %
4	11.25° to 15.00°	171	0	100.00 %
5	15.00° to 18.75°	154	0	100.00 %
6	18.75° to 22.50°	185	0	100.00 %
7	22.50° to 26.25°	168	0	100.00 %
8	26.25° to 30.00°	164	0	100.00 %
9	30.00° to 33.75°	166	0	100.00 %
10	33.75° to 37.50°	148	0	100.00 %
11	37.50° to 41.25°	164	0	100.00 %
12	41.25° to 45.00°	170	0	100.00 %
13	45.00° to 48.75°	167	118	29.34 %
14	48.75° to 52.50°	152	113	25.66 %
15	52.50° to 56.25°	170	136	20.00 %
16	56.25° to 60.00°	160	131	18.13 %
17	60.00° to 63.75°	168	138	17.86 %
18	63.75° to 67.50°	178	136	23.60 %
19	67.50° to 71.25°	176	141	19.89 %
20	71.25° to 75.00°	155	120	22.58 %
21	75.00° to 78.75°	190	151	20.53 %
22	78.75° to 82.50°	154	120	22.08 %
23	82.50° to 86.25°	157	126	19.75 %
24	86.25° to 90.00°	173	135	21.97 %

Average error-free rate for indexes 1 to 12: 100.00 %
Average error-free rate for indexes 12 to 24: 21.75 %
Average error-free rate for overall shift : 60.88 %

Table 50 – Bend wire - Error-free rates

Hold phase time increasing	Average error-free rate for indexes 1 to 12	Average error-free rate for indexes 13 to 24	Average error-free rate for overall shift
0 %	96.80 %	50.25 %	73.53 %
10 %	99.70 %	50.55 %	75.13 %
20 %	100.00 %	52.85 %	76.43 %
30 %	99.95 %	53.90 %	76.93 %
40 %	100.00 %	21.75 %	60.88 %

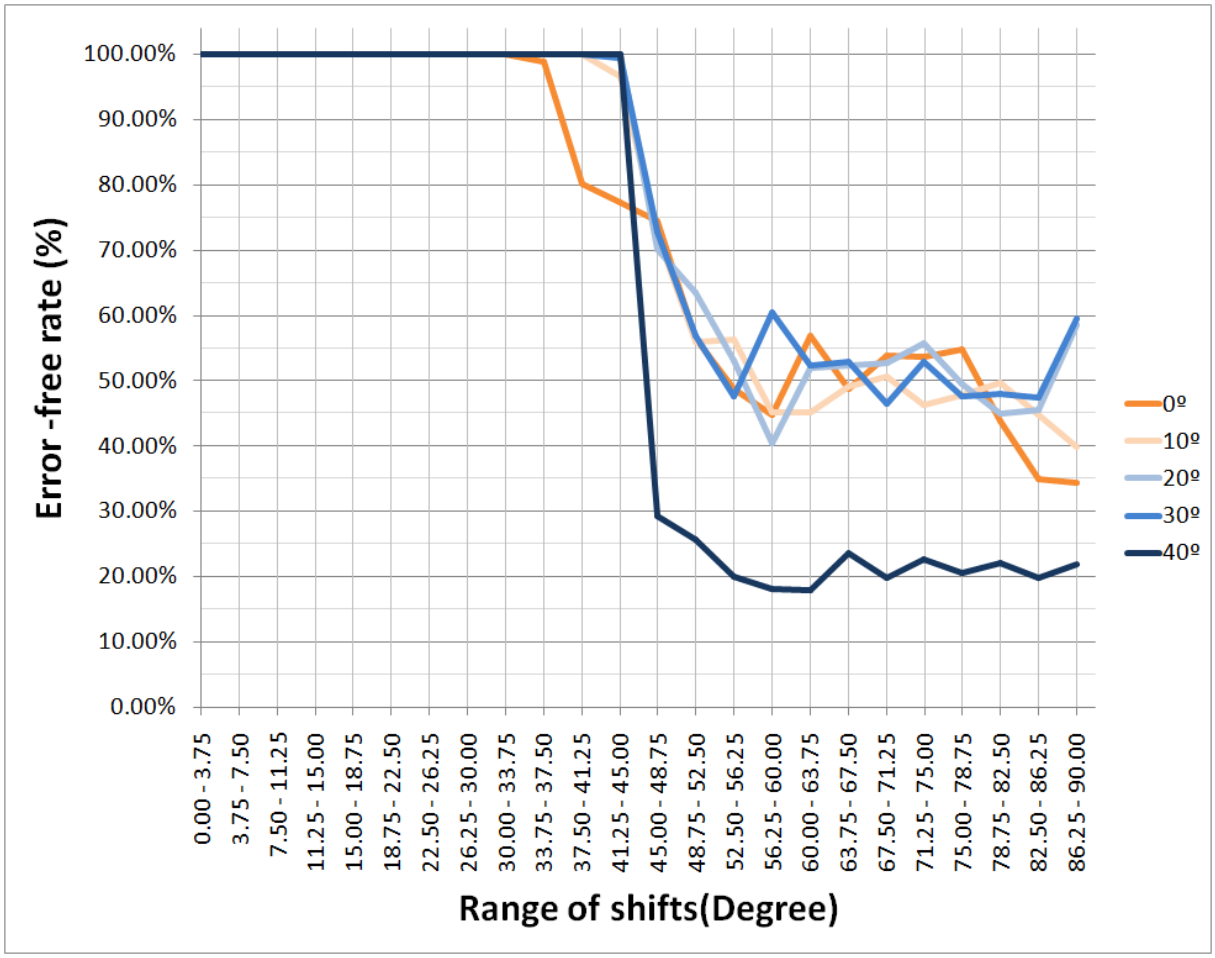
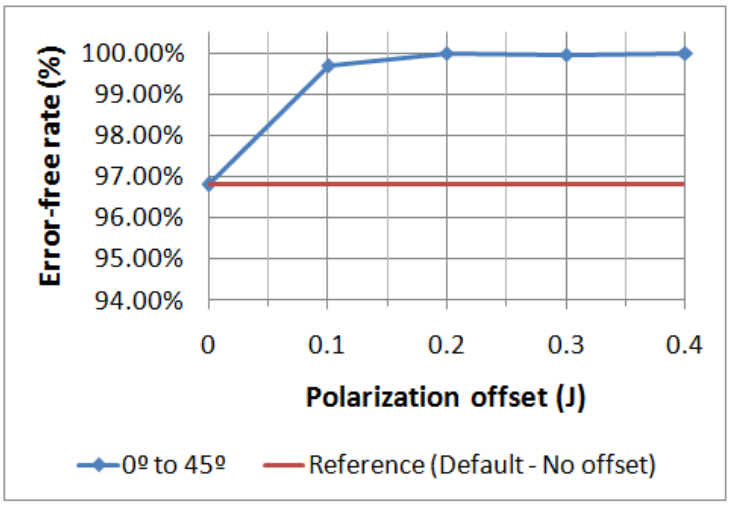
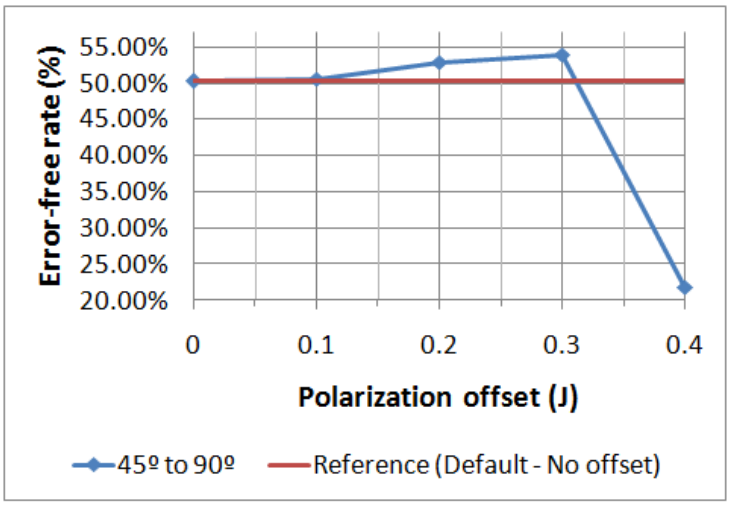


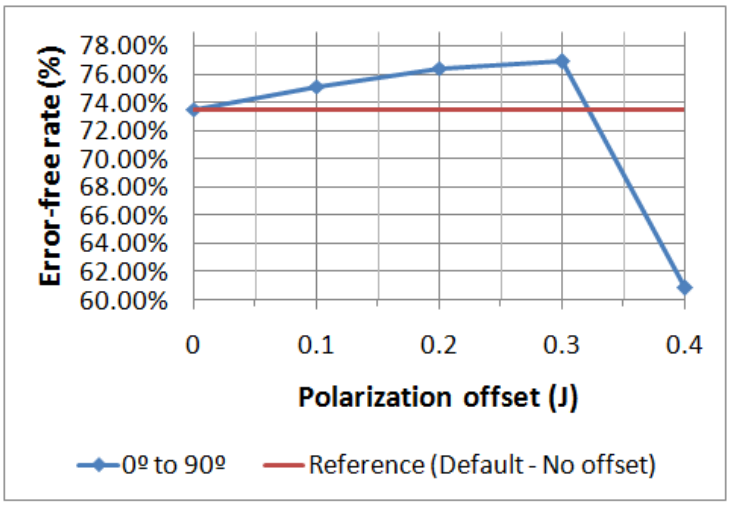
Figure 106 – Bend wire - % Success X Range of shifts



(a) Error free simulations (%) X Polarization offset (J) - Average error-free rate for indexes 1 to 12



(b) Error free simulations (%) X Polarization offset (J) - Average error-free rate for indexes 13 to 24



(c) Error free simulations (%) X Polarization offset (J) - Average error-free rate for overall shift

Figure 107 – Bend wire - Error free simulations (%) X Polarization offset (J)

C.3 Fanout of 2

Range of shifts: 0.00° to 90.00°

Range divisions: 24

Maximum number of iterations per division: 1000

C.3.1 Synchronous clock signals ($\alpha = 0$ %)

Table 51 – Error-free simulation rates for QCA Fanout of 2 with phase-deviated synchronous clock signals ($\alpha = 0$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	177	0	100.00 %
2	3.75° to 7.50°	158	0	100.00 %
3	7.50° to 11.25°	175	0	100.00 %
4	11.25° to 15.00°	153	0	100.00 %
5	15.00° to 18.75°	152	0	100.00 %
6	18.75° to 22.50°	138	0	100.00 %
7	22.50° to 26.25°	196	0	100.00 %
8	26.25° to 30.00°	179	0	100.00 %
9	30.00° to 33.75°	173	0	100.00 %
10	33.75° to 37.50°	164	0	100.00 %
11	37.50° to 41.25°	172	40	76.74 %
12	41.25° to 45.00°	163	38	76.63 %
13	45.00° to 48.75°	181	41	77.35 %
14	48.75° to 52.50°	168	92	45.24 %
15	52.50° to 56.25°	175	86	50.86 %
16	56.25° to 60.00°	156	81	48.08 %
17	60.00° to 63.75°	171	84	50.88 %
18	63.75° to 67.50°	167	87	47.30 %
19	67.50° to 71.25°	166	88	46.33 %
20	71.25° to 75.00°	175	83	52.57 %
21	75.00° to 78.75°	163	71	56.44 %
22	78.75° to 82.50°	150	80	46.67 %
23	82.50° to 86.25°	175	112	36.00 %
24	86.25° to 90.00°	153	95	37.91 %

Average error-free rate for indexes 1 to 12: 96.10 %
Average error-free rate for indexes 13 to 24: 50.00 %
Average error-free rate for overall shift : 73.05 %

C.3.2 Asynchronous clock signals ($\alpha = 10$ %)

Table 52 – Error-free simulation rates for QCA Fanout of 2 with phase-deviated asynchronous clock signals ($\alpha = 10$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	167	0	100.00 %
2	3.75° to 7.50°	165	0	100.00 %
3	7.50° to 11.25°	174	0	100.00 %
4	11.25° to 15.00°	153	0	100.00 %
5	15.00° to 18.75°	192	0	100.00 %
6	18.75° to 22.50°	181	0	100.00 %
7	22.50° to 26.25°	149	0	100.00 %
8	26.25° to 30.00°	155	0	100.00 %
9	30.00° to 33.75°	178	0	100.00 %
10	33.75° to 37.50°	149	0	100.00 %
11	37.50° to 41.25°	165	0	100.00 %
12	41.25° to 45.00°	172	0	100.00 %
13	45.00° to 48.75°	173	44	74.57 %
14	48.75° to 52.50°	166	99	40.36 %
15	52.50° to 56.25°	176	91	48.30 %
16	56.25° to 60.00°	163	80	50.92 %
17	60.00° to 63.75°	151	80	47.02 %
18	63.75° to 67.50°	161	91	43.48 %
19	67.50° to 71.25°	186	109	41.40 %
20	71.25° to 75.00°	181	97	46.41 %
21	75.00° to 78.75°	170	74	56.47 %
22	78.75° to 82.50°	173	83	52.02 %
23	82.50° to 86.25°	147	72	51.02 %
24	86.25° to 90.00°	153	79	48.37 %

Average error-free rate for indexes 1 to 12: 99.70 %
Average error-free rate for indexes 13 to 24: 50.55 %
Average error-free rate for overall shift : 75.13 %

C.3.3 Asynchronous clock signals ($\alpha = 20$ %)

Table 53 – Error-free simulation rates for QCA Fanout of 2 with phase-deviated asynchronous clock signals ($\alpha = 20$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	174	0	100.00 %
2	3.75° to 7.50°	163	0	100.00 %
3	7.50° to 11.25°	178	0	100.00 %
4	11.25° to 15.00°	173	0	100.00 %
5	15.00° to 18.75°	156	0	100.00 %
6	18.75° to 22.50°	144	0	100.00 %
7	22.50° to 26.25°	167	0	100.00 %
8	26.25° to 30.00°	168	0	100.00 %
9	30.00° to 33.75°	174	0	100.00 %
10	33.75° to 37.50°	155	0	100.00 %
11	37.50° to 41.25°	178	7	96.07 %
12	41.25° to 45.00°	170	37	78.24 %
13	45.00° to 48.75°	157	65	58.60 %
14	48.75° to 52.50°	159	81	49.06 %
15	52.50° to 56.25°	184	91	50.54 %
16	56.25° to 60.00°	177	81	54.24 %
17	60.00° to 63.75°	173	80	53.76 %
18	63.75° to 67.50°	164	73	55.49 %
19	67.50° to 71.25°	179	99	44.69 %
20	71.25° to 75.00°	165	86	47.88 %
21	75.00° to 78.75°	159	82	48.43 %
22	78.75° to 82.50°	155	83	46.45 %
23	82.50° to 86.25°	180	90	50.00 %
24	86.25° to 90.00°	148	71	52.03 %

Average error-free rate for indexes 1 to 12: 97.80 %
Average error-free rate for indexes 13 to 24: 50.90 %
Average error-free rate for overall shift : 74.35 %

C.3.4 Asynchronous clock signals ($\alpha = 30$ %)

Table 54 – Error-free simulation rates for QCA Fanout of 2 with phase-deviated asynchronous clock signals ($\alpha = 30$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	184	0	100.00 %
2	3.75° to 7.50°	148	0	100.00 %
3	7.50° to 11.25°	179	0	100.00 %
4	11.25° to 15.00°	172	0	100.00 %
5	15.00° to 18.75°	156	0	100.00 %
6	18.75° to 22.50°	173	0	100.00 %
7	22.50° to 26.25°	160	0	100.00 %
8	26.25° to 30.00°	173	0	100.00 %
9	30.00° to 33.75°	157	8	94.90 %
10	33.75° to 37.50°	158	44	72.15 %
11	37.50° to 41.25°	188	55	70.74 %
12	41.25° to 45.00°	152	41	73.03 %
13	45.00° to 48.75°	170	74	56.47 %
14	48.75° to 52.50°	170	91	46.47 %
15	52.50° to 56.25°	173	102	41.04 %
16	56.25° to 60.00°	161	82	49.07 %
17	60.00° to 63.75°	165	83	49.70 %
18	63.75° to 67.50°	163	82	49.69 %
19	67.50° to 71.25°	149	83	44.30 %
20	71.25° to 75.00°	181	95	47.51 %
21	75.00° to 78.75°	175	93	46.86 %
22	78.75° to 82.50°	172	70	59.30 %
23	82.50° to 86.25°	155	80	48.39 %
24	86.25° to 90.00°	166	78	53.01 %

Average error-free rate for indexes 1 to 12: 92.60 %
Average error-free rate for indexes 13 to 24: 43.35 %
Average error-free rate for overall shift : 70.98 %

C.3.5 Asynchronous clock signals ($\alpha = 40$ %)

Table 55 – Error-free simulation rates for QCA Fanout of 2 with phase-deviated asynchronous clock signals ($\alpha = 40$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	180	0	100.00 %
2	3.75° to 7.50°	169	0	100.00 %
3	7.50° to 11.25°	158	0	100.00 %
4	11.25° to 15.00°	172	0	100.00 %
5	15.00° to 18.75°	189	0	100.00 %
6	18.75° to 22.50°	159	0	100.00 %
7	22.50° to 26.25°	153	13	91.50 %
8	26.25° to 30.00°	152	31	79.61 %
9	30.00° to 33.75°	173	41	76.30 %
10	33.75° to 37.50°	153	44	71.24 %
11	37.50° to 41.25°	165	40	75.76 %
12	41.25° to 45.00°	177	37	79.10 %
13	45.00° to 48.75°	153	44	71.24 %
14	48.75° to 52.50°	188	115	38.83 %
15	52.50° to 56.25°	136	73	46.32 %
16	56.25° to 60.00°	174	111	36.21 %
17	60.00° to 63.75°	165	92	44.24 %
18	63.75° to 67.50°	196	107	45.41 %
19	67.50° to 71.25°	186	91	51.08 %
20	71.25° to 75.00°	153	72	52.94 %
21	75.00° to 78.75°	157	76	51.59 %
22	78.75° to 82.50°	170	72	57.65 %
23	82.50° to 86.25°	151	73	51.66 %
24	86.25° to 90.00°	171	76	55.56 %

Average error-free rate for indexes 1 to 12: 89.70 %
Average error-free rate for indexes 12 to 24: 49.90 %
Average error-free rate for overall shift : 69.80 %

Table 56 – Fanout of 2 - Error-free rates

Hold phase time increasing	Average error-free rate for indexes 1 to 12	Average error-free rate for indexes 13 to 24	Average error-free rate for overall shift
0 %	96.10 %	50.00 %	73.05 %
10 %	100.00 %	50.05 %	75.03 %
20 %	97.80 %	50.90 %	74.35 %
30 %	92.60 %	49.35 %	70.98 %
40 %	89.70 %	49.90 %	69.80 %

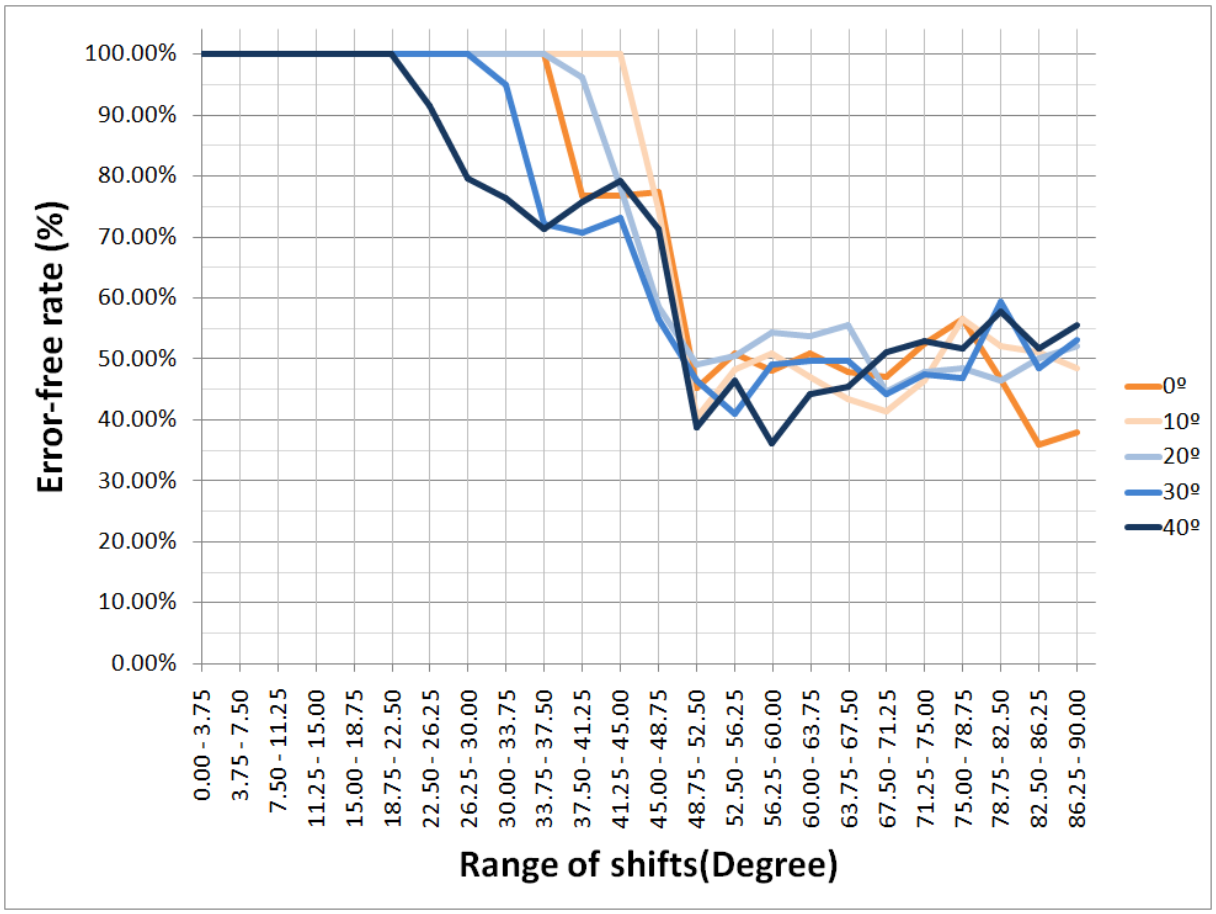
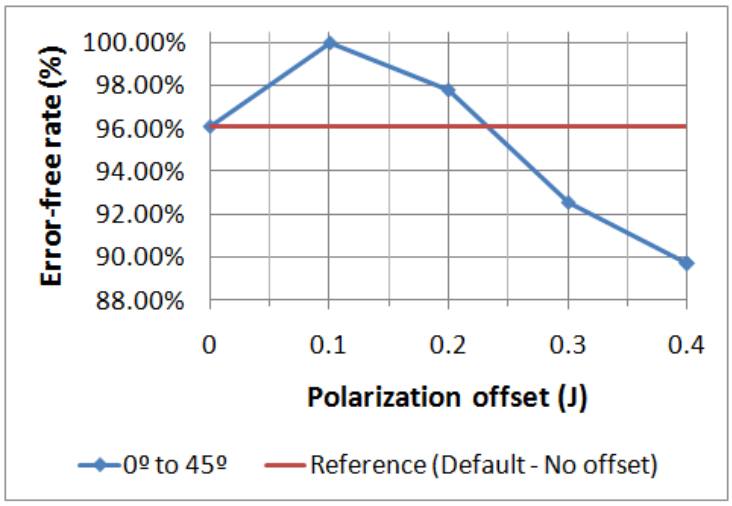
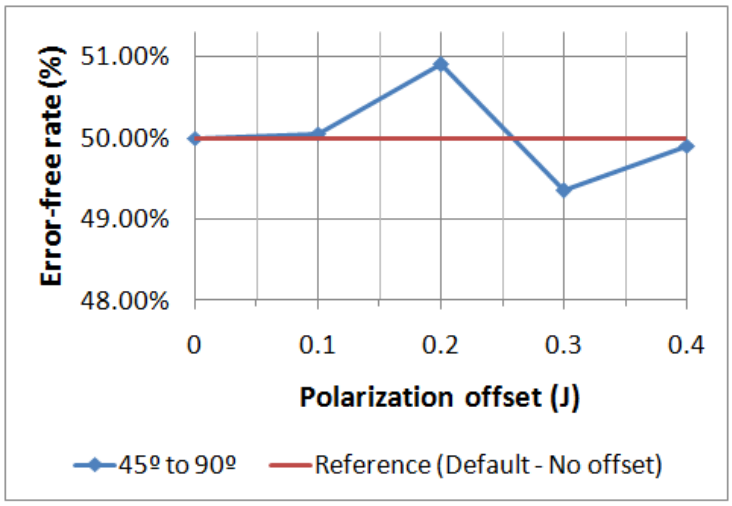


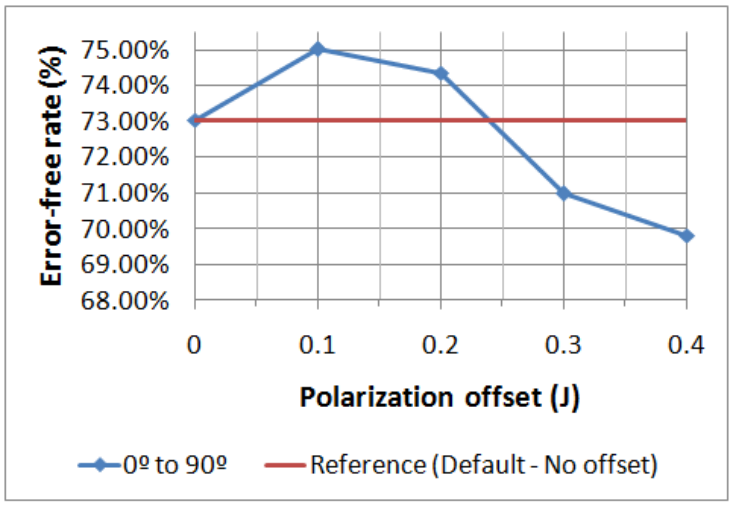
Figure 108 – Fanout of 2 - % Success X Range of shifts



(a) Error free simulations (%) X Polarization offset (J) - Average error-free rate for indexes 1 to 12



(b) Error free simulations (%) X Polarization offset (J) - Average error-free rate for indexes 13 to 24



(c) Error free simulations (%) X Polarization offset (J) - Average error-free rate for overall shift

Figure 109 – Fanout of 2 - Error free simulations (%) X Polarization offset (J)

C.4 Fanout of 3

Range of shifts: 0.00° to 90.00°

Range divisions: 24

Maximum number of iterations per division: 1000

C.4.1 Synchronous clock signals ($\alpha = 0$ %)

Table 57 – Error-free simulation rates for QCA Fanout of 3 with phase-deviated synchronous clock signals ($\alpha = 0$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	174	0	100.00 %
2	3.75° to 7.50°	151	0	100.00 %
3	7.50° to 11.25°	168	0	100.00 %
4	11.25° to 15.00°	179	0	100.00 %
5	15.00° to 18.75°	156	0	100.00 %
6	18.75° to 22.50°	167	0	100.00 %
7	22.50° to 26.25°	164	0	100.00 %
8	26.25° to 30.00°	169	0	100.00 %
9	30.00° to 33.75°	174	0	100.00 %
10	33.75° to 37.50°	162	0	100.00 %
11	37.50° to 41.25°	169	42	75.15 %
12	41.25° to 45.00°	167	45	73.05 %
13	45.00° to 48.75°	163	39	76.07 %
14	48.75° to 52.50°	158	83	47.47 %
15	52.50° to 56.25°	172	89	48.26 %
16	56.25° to 60.00°	181	93	48.62 %
17	60.00° to 63.75°	148	71	52.03 %
18	63.75° to 67.50°	165	89	46.06 %
19	67.50° to 71.25°	171	88	48.54 %
20	71.25° to 75.00°	180	74	58.89 %
21	75.00° to 78.75°	171	79	53.80 %
22	78.75° to 82.50°	152	70	53.95 %
23	82.50° to 86.25°	163	98	39.88 %
24	86.25° to 90.00°	176	116	34.09 %

Average error-free rate for indexes 1 to 12: 95.65 %
Average error-free rate for indexes 13 to 24: 50.55 %
Average error-free rate for overall shift : 73.10 %

C.4.2 Asynchronous clock signals ($\alpha = 10$ %)

Table 58 – Error-free simulation rates for QCA Fanout of 3 with phase-deviated asynchronous clock signals ($\alpha = 10$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	169	0	100.00 %
2	3.75° to 7.50°	181	0	100.00 %
3	7.50° to 11.25°	163	0	100.00 %
4	11.25° to 15.00°	163	0	100.00 %
5	15.00° to 18.75°	161	0	100.00 %
6	18.75° to 22.50°	158	0	100.00 %
7	22.50° to 26.25°	168	0	100.00 %
8	26.25° to 30.00°	169	0	100.00 %
9	30.00° to 33.75°	180	0	100.00 %
10	33.75° to 37.50°	170	0	100.00 %
11	37.50° to 41.25°	150	0	100.00 %
12	41.25° to 45.00°	168	0	100.00 %
13	45.00° to 48.75°	159	38	76.10 %
14	48.75° to 52.50°	196	99	49.49 %
15	52.50° to 56.25°	184	91	50.54 %
16	56.25° to 60.00°	157	88	43.95 %
17	60.00° to 63.75°	171	98	42.63 %
18	63.75° to 67.50°	151	74	50.99 %
19	67.50° to 71.25°	164	77	53.05 %
20	71.25° to 75.00°	166	76	54.22 %
21	75.00° to 78.75°	153	70	54.25 %
22	78.75° to 82.50°	165	84	49.09 %
23	82.50° to 86.25°	173	79	54.34 %
24	86.25° to 90.00°	161	87	45.36 %

Average error-free rate for indexes 1 to 12: 100.00 %
Average error-free rate for indexes 13 to 24: 51.95 %
Average error-free rate for overall shift : 75.98 %

C.4.3 Asynchronous clock signals ($\alpha = 20$ %)

Table 59 – Error-free simulation rates for QCA Fanout of 3 with phase-deviated asynchronous clock signals ($\alpha = 20$ %).

Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	171	0	100.00 %
2	3.75° to 7.50°	174	0	100.00 %
3	7.50° to 11.25°	171	0	100.00 %
4	11.25° to 15.00°	155	0	100.00 %
5	15.00° to 18.75°	162	0	100.00 %
6	18.75° to 22.50°	173	0	100.00 %
7	22.50° to 26.25°	139	0	100.00 %
8	26.25° to 30.00°	153	0	100.00 %
9	30.00° to 33.75°	171	0	100.00 %
10	33.75° to 37.50°	200	0	100.00 %
11	37.50° to 41.25°	169	28	83.43 %
12	41.25° to 45.00°	162	34	79.01 %
13	45.00° to 48.75°	157	65	58.60 %
14	48.75° to 52.50°	159	81	49.06 %
15	52.50° to 56.25°	184	91	50.54 %
16	56.25° to 60.00°	177	81	54.24 %
17	60.00° to 63.75°	173	80	53.76 %
18	63.75° to 67.50°	164	73	55.49 %
19	67.50° to 71.25°	179	99	44.69 %
20	71.25° to 75.00°	165	86	47.88 %
21	75.00° to 78.75°	159	82	48.43 %
22	78.75° to 82.50°	155	83	46.45 %
23	82.50° to 86.25°	180	90	50.00 %
24	86.25° to 90.00°	148	71	52.03 %

Average error-free rate for indexes 1 to 12: 96.90 %
Average error-free rate for indexes 13 to 24: 50.90 %
Average error-free rate for overall shift : 73.90 %

C.4.4 Asynchronous clock signals ($\alpha = 30$ %)

Table 60 – Error-free simulation rates for QCA Fanout of 3 with phase-deviated asynchronous clock signals ($\alpha = 30$ %).

Range Index	Shifts Interval	Iterations	Errors	Error-free Rate
1	0.00° to 3.75°	167	0	100.00 %
2	3.75° to 7.50°	172	0	100.00 %
3	7.50° to 11.25°	193	0	100.00 %
4	11.25° to 15.00°	137	0	100.00 %
5	15.00° to 18.75°	160	0	100.00 %
6	18.75° to 22.50°	160	0	100.00 %
7	22.50° to 26.25°	157	0	100.00 %
8	26.25° to 30.00°	148	0	100.00 %
9	30.00° to 33.75°	192	30	84.38 %
10	33.75° to 37.50°	163	40	75.46 %
11	37.50° to 41.25°	148	37	75.00 %
12	41.25° to 45.00°	203	60	70.44 %
13	45.00° to 48.75°	162	67	58.64 %
14	48.75° to 52.50°	151	79	47.68 %
15	52.50° to 56.25°	155	81	47.74 %
16	56.25° to 60.00°	169	91	46.15 %
17	60.00° to 63.75°	185	86	53.51 %
18	63.75° to 67.50°	168	89	47.02 %
19	67.50° to 71.25°	161	76	52.80 %
20	71.25° to 75.00°	165	83	49.70 %
21	75.00° to 78.75°	173	89	48.55 %
22	78.75° to 82.50°	173	86	50.29 %
23	82.50° to 86.25°	181	99	45.30 %
24	86.25° to 90.00°	157	74	52.87 %

Average error-free rate for indexes 1 to 12: 91.65 %
Average error-free rate for indexes 13 to 24: 50.00 %
Average error-free rate for overall shift : 70.83 %

C.4.5 Asynchronous clock signals ($\alpha = 40$ %)

Table 61 – Error-free simulation rates for QCA Fanout of 3 with phase-deviated asynchronous clock signals ($\alpha = 40$ %).

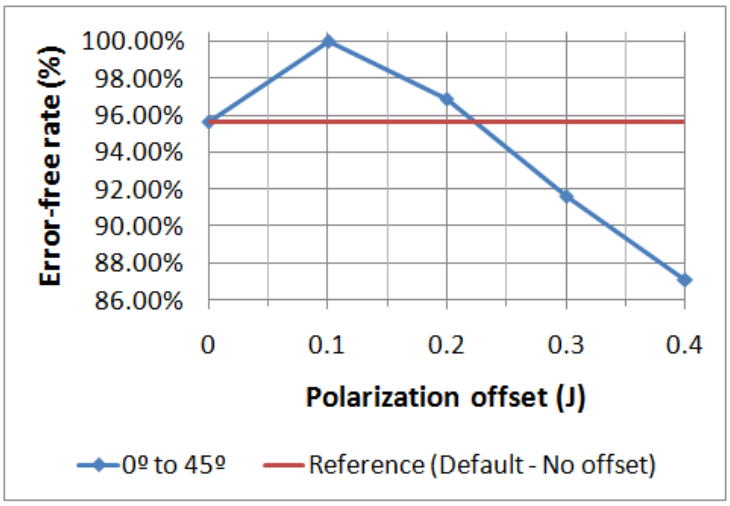
Range Index	**Shifts Interval**	**Iterations**	**Errors**	**Error-free Rate**
1	0.00° to 3.75°	154	0	100.00 %
2	3.75° to 7.50°	144	0	100.00 %
3	7.50° to 11.25°	170	0	100.00 %
4	11.25° to 15.00°	178	0	100.00 %
5	15.00° to 18.75°	158	0	100.00 %
6	18.75° to 22.50°	188	0	100.00 %
7	22.50° to 26.25°	151	33	78.15 %
8	26.25° to 30.00°	176	53	69.89 %
9	30.00° to 33.75°	171	53	69.01 %
10	33.75° to 37.50°	151	32	78.81 %
11	37.50° to 41.25°	181	47	74.03 %
12	41.25° to 45.00°	178	40	77.53 %
13	45.00° to 48.75°	171	60	64.91 %
14	48.75° to 52.50°	177	101	42.94 %
15	52.50° to 56.25°	184	112	39.13 %
16	56.25° to 60.00°	149	83	44.30 %
17	60.00° to 63.75°	153	88	42.48 %
18	63.75° to 67.50°	187	98	47.59 %
19	67.50° to 71.25°	177	86	51.41 %
20	71.25° to 75.00°	165	76	53.94 %
21	75.00° to 78.75°	161	70	56.52 %
22	78.75° to 82.50°	146	73	50.00 %
23	82.50° to 86.25°	168	85	49.40 %
24	86.25° to 90.00°	162	80	50.62 %

Average error-free rate for indexes 1 to 12: 87.10 %
Average error-free rate for indexes 12 to 24: 49.40 %
Average error-free rate for overall shift : 68.25 %

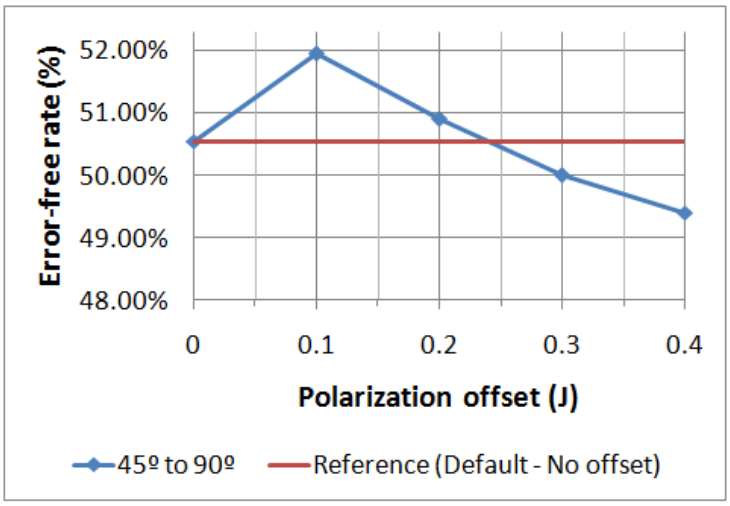
Table 62 – Fanout of 3 - Error-free rates

Hold phase time increasing	Average error-free rate for indexes 1 to 12	Average error-free rate for indexes 13 to 24	Average error-free rate for overall shift
0 %	95.65 %	50.55 %	73.10 %
10 %	100.00 %	51.95 %	75.98 %
20 %	96.90 %	50.90 %	73.90 %
30 %	91.65 %	50.00 %	70.83 %
40 %	87.10 %	49.40 %	68.25 %

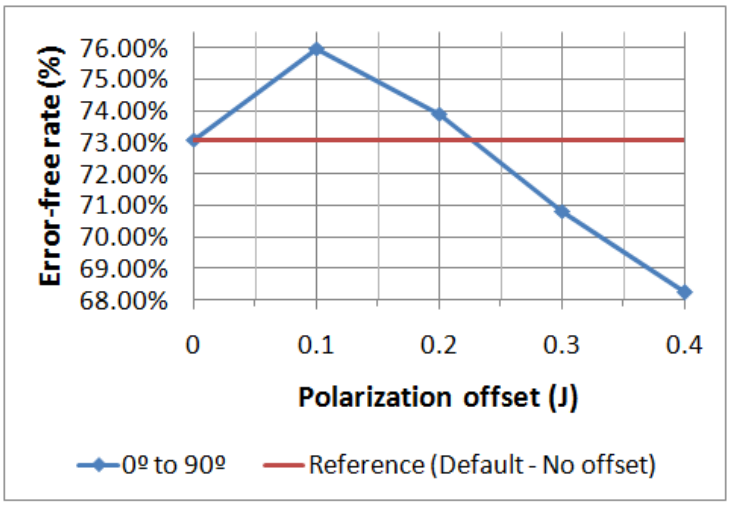
Figure 110 – Fanout of 3 - % Success X Range of shifts



(a) Error free simulations (%) X Polarization offset (J) -Average error-free rate for indexes 1 to 12



(b) Error free simulations (%) X Polarization offset (J) -Average error-free rate for indexes 13 to 24



(c) Error free simulations (%) X Polarization offset (J) -Average error-free rate for overall shift

Figure 111 – Fanout of 3 - Error free simulations (%) X Polarization offset (J)