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A COMPREHENSIVE ANALYSIS OF DESIGN AND PERFORMANCE OF POWER CONVERTERS FOR BATTERY ENERGY STORAGE SYSTEMS

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À minha família, amigos e mentores

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Resumo

O uso de sistemas de armazenamento de energia em baterias conectados à rede elétrica tem aumentado em todo o mundo. No cenário de alto nível de penetração de fontes renováveis de energia na geração distribuída, os sistemas de armazenamento desempenham um papel importante para combinar um fornecimento de energia sustentável com uma fonte de energia despachada confiável. Diferentes topologias de sistemas para conversão de energia são empregadas para conectar as baterias à rede, geralmente usando conversores de estágio único. No entanto, a tensão da bateria varia de acordo com seu estado de carga, o que pode introduzir grandes variações na tensão do barramento cc. Portanto, o estágio cc/ca deve ter suas chaves de potência projetadas para suportar essa variação de tensão. Uma tensão controlável no barramento cc é obtida inserindo um estágio cc/cc para conectar as baterias ao estágio cc/ca. Entre os conversores cc/cc, o conversor bidirecional intercalado tem sido amplamente utilizado devido ao baixo ripple da corrente de entrada e saída. No entanto, o *trade-off* entre custo e otimização no projeto pela inserção do estágio cc/cc é pouco explorado na literatura. Portanto, este trabalho apresenta uma metodologia de análise, considerando a variação da tensão da bateria e sua influência no projeto e na eficiência do sistema de conversão de energia para sistemas de armazenamento de energia em baterias. Ademais, é proposto um projeto de sistema de conversão de energia orientado para a classe de tensão das chaves, eficiência e custo. Além disso, é analisado a estrutura de controle para diferentes topologias de conversores para sistemas de armazenamento. As abordagens de projeto e comparação de conversores para sistemas de armazenamento de energia em baterias são investigadas nos resultados simulados e experimentais. Os resultados indicam as vantagens e desvantagens das topologias investigadas. Além disso, o controle de conversores conectados à rede para sistemas de armazenamento de energia em referenciais estacionários tem sido investigado em diversos trabalhos na literatura. Um dos desafios deste método é o cálculo das referências atuais em função das referências de potência. Em alguns trabalhos, esse problema foi resolvido com base nas equações da teoria da potência instantânea descritas em referenciais estacionários. No entanto, esta abordagem pode levar a erros de regime permanente na potência injetada se houver algum erro na malha de controle de corrente, que é o foco desta investigação. Assim, este trabalho propõe um controle de potência em malha fechada para estágios dc/ac conectados à rede controlados em referencial estacionário. Esta estratégia é investigada experimentalmente em duas configurações de sistemas de conversão de energia para sistemas de armazenamento de energia de bateria. **Palavras-chaves**: SAEB, Bateria de Chumbo-Ácido, Conversor Bidirecional, Conversor Entrelaçado, Módulo de Potência IGBT, Eficiência, Custo, Classe de Tensão.

Abstract

The use of grid-connected battery energy storage systems has increased around the world. In the scenario of high penetration of renewable energy sources in distributed generation, storage systems play an important role in combining a sustainable energy supply with a reliable dispatched energy source. Different power electronics topologies for power conversion systems are employed to connect batteries to the grid, usually using single-stage converters. However, the battery voltage varies depending on its state of charge, introducing significant variations in the dc-link voltage. Therefore, the dc/ac stage must have its power switches to support this voltage variation. A controllable voltage on the dc-link is obtained by inserting a dc/dc converter stage to connect the batteries to the dc/ac stage. Among dc/dc converters, the bidirectional interleaved converter has been widely used due to the low ripple of the input and output current. However, the trade-off between cost and design optimization by insertion the cc/cc stage is less explored in the literature. Therefore, this work presents an analysis methodology, considering the variation of battery voltage and its influence on the design and efficiency of the energy conversion system for battery energy storage systems. Furthermore, a power conversion system design oriented to the switch voltage class, efficiency and cost is proposed. The simulated and experimental results investigate the design and comparison approaches of converters for battery energy storage systems. The results indicate the advantages and disadvantages of the investigated topologies. Furthermore, the control of grid-connected converters for energy storage systems in stationary references has been investigated in several works in the literature. One challenge of this method is the calculation of current references as a function of power references. In some works, this problem was solved based on the instantaneous power theory equations described in stationary references. However, this approach can lead to steady-state errors in the injected power if there is an error in the current control loop, which is the focus of this investigation. Therefore, this work proposes a closed-loop power control for grid-connected dc/ac stages controlled in a stationary frame of reference. This strategy is experimentally investigated in two configurations of energy conversion systems for battery energy storage systems.

Keywords: BESS, Lead-Acid Battery, Bidirectional Converter, Interleaved Converter, IGBT power module, Efficiency, Cost, Blocking Voltage.

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List of Abbreviations and Acronyms

BESS	Battery Energy Storage Systems
PCS	Power Conversion System
R&D	Research and Development
SOC	State of Charge
DAB	Dual-Active-Bridge
THD	Total Harmonic Distortion
PWM	Pulse Width Modulation
PI	Proportional-Integral
AWPI	Anti-Windup Proportional-Integral
PCC	Point of Common Coupling
DSOGI	Second-Order Generalized Integrator
PLL	Phase-Locked Loop
SVPWM	Space Vector Pulse Width Modulation
PR	Proportional-Resonant
IGBT	Insulated Gate Bipolar Transistors
MMC	Modular Multilevel Converter
VSI	Voltage Source Inverter

ZSI	Z-Source Inverter
qZSI	Quasi-Z-Source Inverter
NPC	Neutral-Point Clamped
ANPC	Active Neutral-Point Clamped
CHB	Cascaded H-Bridge
DSP	Digital Signal Processor
GPIO	General Purpose Input/Output

Contents

1 Introduction

1.1 Contextualisation

The cost reduction of battery technologies and high connection level of photovoltaic and wind energy generation in the electrical power systems contribute to the growth of battery energy storage system (BESS) around the world (REN21, 2020). Photovoltaic and wind electricity generation accounts for a significant part of the energy matrix of several countries. Therefore, BESS plays a key role in combining a sustainable power supply with a reliable dispatchable generation. This is a challenge when renewable sources are used due to the intermittent energy generation (Chen et al., 2009).

Furthermore, the BESS can contribute to several grid services, which increases the viability of this system. The grid services can be classified into four groups (Akhil et al., 2013a). The first group is the bulk energy service, where high storage energy is required, such as:

- Time Shifting (Arbitrage): This is an expression to designate energy trade. The electric energy is bought and stored during low-cost periods to be later sold when the cost of energy is higher. Therefore, the profit is built-in in this energy price difference (Walawalkar; Apt; Mancini, 2007; Abdelrazek; Kamalasadan, 2016; Xu et al., 2016).
- Peak Shaving: The BESS goal is to supply energy during short-term demand increase, which reduces the overall cost of demand charges. The BESS is usually charged of light load periods in the system. (de Salis et al., 2014; Prasatsap; Kiravittaya; Polprasert, 2017);
- Load leveling: This service is based on energy storage charging during light load levels and discharging in high demand. While peak shaving is used to remove the energy demand peak, load leveling aims to smooth the load profile, mainly aiming to reduce the higher cost generation during high load period (Mehr; Masoum; Jabalameli, 2013).

The second grid service group is related to the BESS operation modes to keep the stability and security of the power supply. The main ancillary services are:

- Black Start: The BESS is used to power up the transmission and distribution lines and bring power plants online after a grid failure (Xu et al., 2015). Therefore, the black-start service can be understood as a restoration of the power functions of the electrical power system without requesting external transmission lines;

- Spinning Reserve: This service is related to the energy reserve available for the system operator in a short period to meet demand in case of a sudden drop in the generation or load increase. The spinning reserve is the first reserve used when there is an energy deficit. In the electrical power system, this reserve is available, increasing the power output of online generators by the torque increase. Therefore, BESS can also be used to provide this energy reserve. Generally responding within 10 seconds to maintain the system frequency (Xu et al., 2016; Knap et al., 2016);

- Non-spinning Reserve: This is the second energy reserve that may be offline but can be brought online after a short delay. This energy reserve can also be imported from BESS intended for other services (Knap et al., 2016);

- Voltage support: The electrical grid operators establish that the voltage in the system is kept within a limited range. The reactive power control performs the voltage regulation in the system, and thus this ancillary service can also be performed by BESS spread over the grid (Cifuentes et al., 2019);

- Support the intermittent Renewable Generation Plants: Through the BESS, the intermittent energy generation of renewable sources can be smoothed at an appropriate variation level. This service reduces the voltage variations that photovoltaic and wind generation cause in the electrical power systems due to intermittency (Li; Hui; Lai, 2013; Abdelrazek; Kamalasadan, 2016).

The next group involves the infrastructure service and it is described below:

- Transmission and distribution (T&D) upgrade deferral (Eyer, 2009; Garcia-Garcia; Paaso; Avendano-Mora, 2017): If there is a new high energy demand at a specific point in the T&D lines, the utility needs to adapt its infrastructure to support this demand. However, this is expensive and usually complex, as it may be necessary to upgrade T&D devices to support the new power flow. An alternative is the installation of BESS near the high demand grid point, reducing the impacts on T&D devices. As a result, the upgrade of the T&D infrastructure can be delayed or avoided.

The last group of the main services that can be performed by BESS is related to customer energy management services, which involves:

- Power quality: this service aims to protect the online energy customers against short duration power quality issue, such as variations in voltage magnitude, variation around the fundamental frequency, power factor correction, low harmonic distortion level in the grid voltage and current (Akhil et al., 2013a).

- Power supply reliability: This service can support energy customers during total power supply loss from the utility. This service is widely discussed in the study of microgrids (Xu; Chen, 2011).

Fig. 1 summarizes these grid services linked with the respective beneficiary. The entire system presents benefits with the BESS grid service. However, there are directly and indirectly beneficiaries. For example, the support for renewable power generation plants benefits both the power plant and the utility directly, while peak shaving directly benefits the consumers. As can be seen, the utility is the one that has more services linked with direct benefits through the BESS.

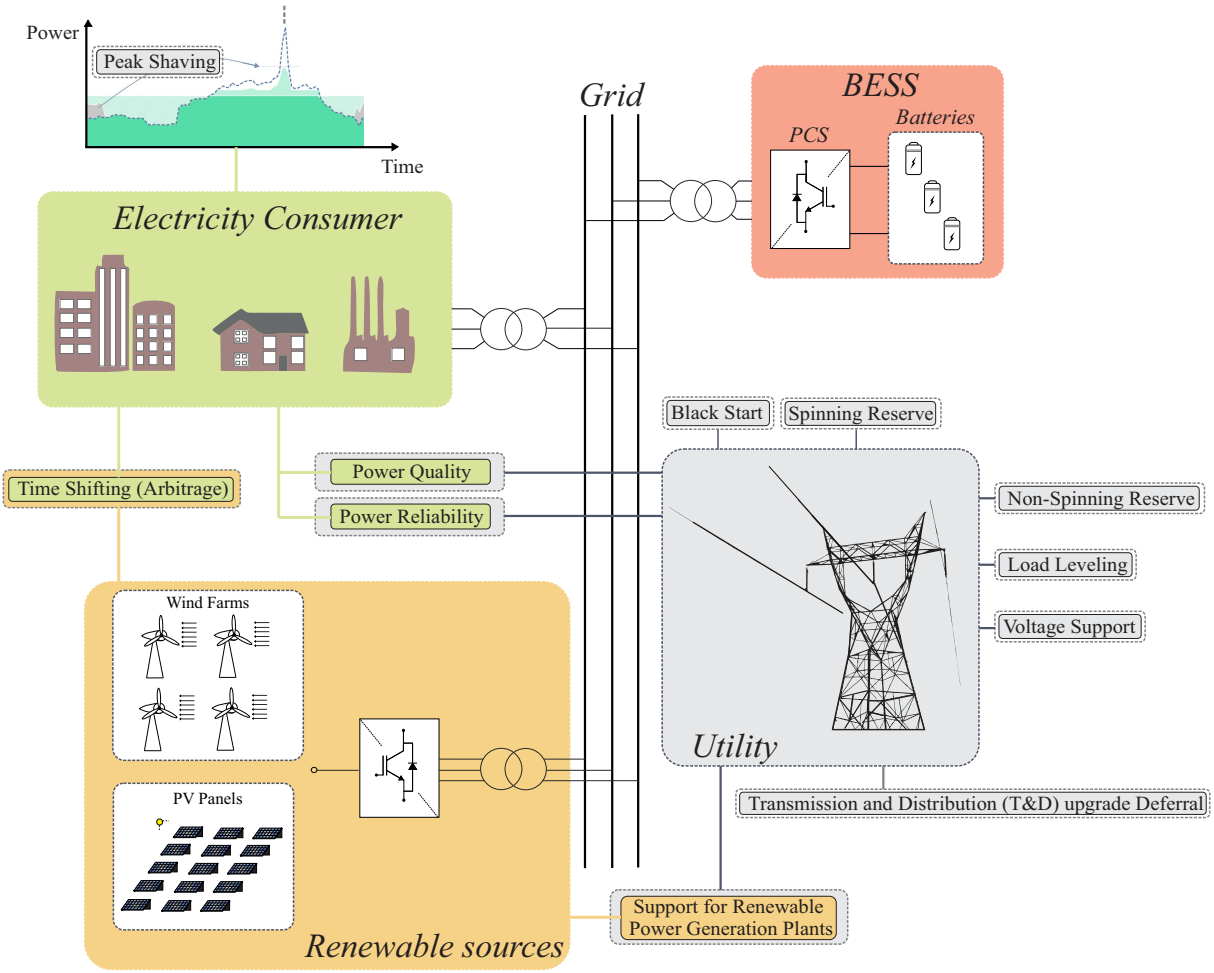


Figure 1 – Services performed by BESS linked with the agent with the higher direct benefit. (Source: own representation)

1.2 Power Conversion System for BESS

An important point for grid-connected BESS performing grid services with the best cost/benefit relation is the power conversion system (PCS) and its relationship with

the battery bank arrangement. The nominal voltage of the electrochemical battery cells is much lower than the grid connection voltage. Generally, the nominal voltage of lead-acid and lithium-ion battery cells are between 2.05 V/cell and 4 V/cell (Horiba, 2014; May; Davidson; Monahov, 2018). Therefore, the cells are connected in series to achieve a voltage level closer to the grid voltage. However, the number of batteries is determined during the BESS design, which depends on the power or energy necessary for the desired application. The battery bank voltage changes with its state of charge (SOC), both decrease in the discharging process and increase in the charging process.

The PCS design for BESS depends mainly on the battery arrangement and the grid voltage level. The batteries can be connected directly to the dc-link, forming a single-stage PCS. In this configuration, the total battery bank voltage must have a minimum dc-link voltage to ensure the power flow between the BESS and the power grid, even with the battery voltage variation. It is worth mentioning that dc-link voltage presents a direct relationship to the grid voltage (Huber; Kolar, 2017). In the PCS with single-stage conversion, the battery bank introduces a significant voltage variation in the dc-link due to the SOC variation and the power switches of the dc/ac stage must support this battery bank voltage range (Wang et al., 2016).

When the battery bank voltage does not have the minimum value for the dc-link, an additional dc/dc stage is necessary to step-up the voltage of the batteries. Furthermore, the dc/dc stage allows a controllable dc-link voltage, which optimizes the design of the dc/ac converter stage power switches for a given voltage level.

The interest of researches to compare PCS for BESS application has been increasing in recent years with several publications, as presented in Stecca et al. (2020). Pires et al. (2014) describes several converter topologies for BESS, including non-isolated and isolated dc/dc converters. Wang et al. (2016) performs an interesting comparison between BESS PCS about the efficiency and costs. The dc/ac stage is based on the two-level or multi-level topologies. However, only a dc/dc converter based on the dual-active-bridge is analyzed in the results. Chatzinikolaou and Rogers (2017) analyses the efficiency and reliability of the dc/ac stage with battery voltage balancing circuits, however, the dc/dc stage is not considered. Díaz-González et al. (2020) approaches some dc/ac and dc/dc converters in relation to the efficiency, reliability and fault tolerance.

There are few works in the literature that discuss the effect of the battery charging-discharging process and SOC variation on the PCS design and efficiency. These points are essential and must be taken into account in the PCS design, since the semiconductors voltage class and, consequently, the power losses and costs may be affected. Furthermore, there are few discussions about the influence of using dc/dc stage in BESS converters regarding the efficiency and cost of the system. Thus, it is important to analyze the advantages and disadvantages when dc/dc stage is employed.

This work studies the multiport dc/dc stage, which is interesting to distribute the energy between two or more converters (Da Silva et al., 2016; Chen; Lu; Rout, 2018). The first analyzed multiport converter presents bidirectional dc/dc converters connected in parallel, as shown in Fig. 2(a). The association of dc/dc converters in parallel mode is widely discussed in literature (Moayedi et al., 2015; Mondal et al., 2016; Jiang; Liu, 2021). An advantage of this structure is that if one converter fails, it can be removed from the system effortlessly. This can be easily achieved due to the natural independence operation between the converters, characteristic of the parallel connection. A disadvantage is the high voltage step-up ratio required for a low input voltage, which occurs in low SOC levels of the battery bank.

The second multiport dc/dc stage is the series connection of converters, as shown in Fig. 2(b) (Vighetti; Ferrieux; Lembeye, 2012; Mukherjee; Strickland, 2016; Sun et al., 2020). The advantage of this structure is the sum of the output voltage of the converters, allowing the lower voltage step-up ratio required if compared to the parallel structure (Bratcu et al., 2011). However, there are challenges in the control strategy and power structure. This structure requires an equal output current in each dc/dc converter.

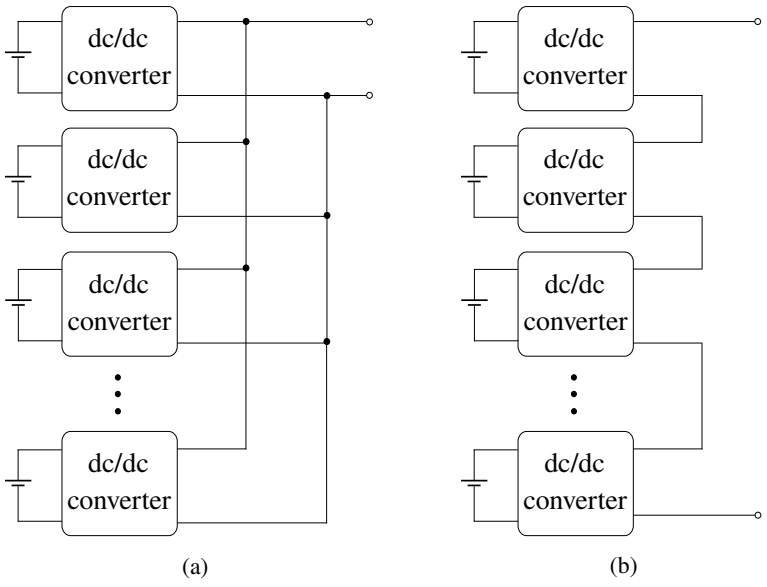


Figure 2 – Multiport dc/dc converter structures studied in this work. (a) Parallel connection of dc/dc converters. (b) Series connection of dc/dc converters. (Source: own representation)

This work provides a study of these two approaches to multiport dc/dc converters. These converter arrangements are gaining more attention in recent years due to the ability to operate with hybrid systems, where sources with different characteristics can be connected to each dc/dc converter (Shan et al., 2019).

1.3 Power Control Realization for BESS

The main aspect of battery voltage and current control is about the battery charge stages (Hunter; Ed Matthews, 2020). Generally, both Li-ion and lead-acid batteries present similar charge stages composed of the constant current mode (CCM), which is featured by the fast charge stage. Furthermore, there is a constant voltage mode (CVM) known as taper mode. The challenge of the battery control is the switching between the discharge/charge control loop and to accomplish the charge stages (Abu Eldahab; Saad; Zekry, 2016; Altaf; Egardt; Mardh, 2017). It is important to mention that the control loop switches can cause transients with current and voltage peaks in the system. Generally, the constant current mode is achieved through the current, power, or duty cycle saturation, avoiding the control switching between the CCM and CVM (Chen; Lai, 2012).

Most of BESS services involve the control of active or reactive power in the grid. Generally, the reactive power is controlled in the outer-loop of the dc/ac stage control strategy. The inner-loop, responsible for controlling the dc/ac stage current, can be implemented in different reference frames, such as synchronous rotating (dq), stationary ($\alpha\beta$) and (abc) reference frames (Brandao et al., 2019). Reference Montero, Cadaval and Gonzalez (2007) concludes that synchronous reference frames are most sensitive to voltage distortions and unbalances in the point of common coupling (PCC).

Generally, the dc/ac stage controls the active power indirectly through the dc-link voltage control. The literature presents two main approaches to control this voltage. The first one is controlling directly the measured value (Yang; Zhou; Blaabjerg, 2016). The second approach is controlling the square value of the measurement (Yazdani; Iravani, 2010). Generally, the square voltage-based method is associated with the instantaneous power theory (IPT) to calculate the dc/ac stage reference currents in stationary reference frame. The advantage of using the square dc-link voltage-based method along with the stationary reference frame and IPT, are listed below (Cupertino; Pereira, 2021):

- This control strategy presents a normalization by grid voltage amplitude, improving the dynamic of the dc-link voltage during sags;
- This strategy does not require Park transformation;
- Less sensitive to voltage distortions and unbalances in the PCC;
- This strategy presents active power reference explicitly, which is helpful for current dynamic saturation.

Due to these advantages, the dc/ac stage control loop based on stationary reference frame has become widely used. Therefore, this work adopts this strategy to control the

dc/ac stage of the BESS PCS. However, this strategy requires some improvements in power control, as demonstrated in this work.

1.4 Motivations and Contributions

1.4.1 Motivations

This work fits the PCS study applied to BESS in two topics. The first one aims to contribute to understand the main factors that influence the design, efficiency and costs of BESS PCS. The second one aims to contribute to the advance in power control for BESS PCS.

There are few works discussing the effect of the battery charge and discharge and SOC variation on the PCS design and efficiency. This fact is an essential issue, because the battery bank voltage variation affects the PCS design. It must be taken into account in the design because it affects the blocking voltage of the power switches and, consequently, the power losses and costs.

Furthermore, there are few discussions about the influence of using dc/dc stage in BESS converters on the efficiency and cost of the system. Thus, a study is interesting to verify the advantages and disadvantages when dc/dc stage is employed.

The lead-acid battery technology is used to evaluate the PCS for BESS in this work. This technology was chosen due to its high commercial appeal in the world and presence in applications involving uninterruptible power supply and grid support (Akhil et al., 2013b).

Another important point is the control strategy used in PCS for BESS application. The control of grid-connected dc/ac stage in stationary reference frame has been investigated in several works in literature. One of the challenges of this method is in the computation of the current references as a function of power references. Generally, it is used instantaneous power theory equations to calculate the reference currents in the stationary reference (Xavier et al., 2019). This approach is an open loop solution and can lead to a steady-state error in the active and reactive power components if the current control presents any errors.

For this reason, Cupertino and Pereira (2021) proposed a control strategy in a closed loop for reactive power, however, experimental validation is required. Furthermore, in some cases the active power must be controlled directly by the dc/ac stage. Generally, this approach is adopted when the dc/dc converters of the PCS are connected in series. This structure has been gaining attention for BESS application due to the low step-up ratio if compared to the parallel converter structure (Mukherjee; Strickland, 2016). In this case, the dc-link voltage is controlled by the dc/dc stage, and the dc/ac stage directly

controls the active and reactive power exchanged with the grid. Therefore, a closed loop control strategy is also required for the active power component.

1.4.2 Contributions

In view of the above discussions, the main contributions are listed below:

- A methodology of analysis considering the battery voltage variation and its impact on PCS design and efficiency. This voltage variation has relation with the IGBT power module design for the dc/ac stage, when the battery bank is directly connected to the dc-link;
- Comparison of the cost/benefit relation of using dc/dc stage for different PCS topologies. For this analysis, a global efficiency index and efficiency map are proposed to determine the performance of a BESS system during a battery bank discharge and charge cycle;
- Proposal of a methodology for PCS design for BESS oriented toward voltage class of power semiconductors, efficiency and cost;
- Proposal of a closed loop for active power control applied in the control strategy based on stationary reference frame and IPT for BESS application.

This work is inserted in the research and development (R&D) project D722 "Análise de Arranjo Técnico e Comercial baseado em uma Planta Piloto de Sistema Distribuído de Armazenamento de Energia em Alimentador Crítico da Rede de Distribuição de 13,8 kV".

1.4.3 Methodology

The methodologies to achieve these goals are:

- Firstly, the BESS is mathematically modeled including the PCS control and the battery bank for studies in simulation environment;
- Simulation results in PLECS environment using computational BESS model and including the power losses calculation model of the converters;
- Levelized cost of storage for long term cost estimation;
- Experimental validations are carried out on the BESS test bench designed for the R&D project D722.

1.5 Text Organization

This Ph.D thesis is organized in 7 chapters. Chapter 1 presents the motivation and contributions of this work. Chapter 2 presents the main PCS and power electronics topologies for BESS approached by the literature and market. Furthermore, the battery modelling is presented. Chapter 3 presents the power electronics topologies studied in this work and discusses the influence of battery voltage variation on the dc/ac stage design when the battery bank is directly connected to the dc-link. Furthermore the PCS design for BESS oriented toward voltage class of power semiconductors, efficiency and cost is presented. Chapter 4 presents the control structure analysis for each compared PCS. In this chapter, the contribution of power control strategy for BESS PCS is described. Chapter 5 presents a case study of a 100 kW BESS in simulation environment, comparing various PCS topologies in terms of efficiency and cost. Chapter 6 presents the experimental results of the PCS for BESS using the prototype designed for the R&D project D722. Finally, Chapter 7 presents the conclusions and the future developments of this work.

2 Power Conversion System Topologies for BESS

In this chapter, it is presented and defined the main PCS topologies studied in this work. It is presented a literature and market review to reinforce the motivation of this work. Furthermore, it is shown and defined the lead-acid battery modelling used and the methodology to estimate the PCS power losses. Finally, the PCS efficiency calculation methodology is presented.

2.1 PCS Topologies

The schematic of the convectional PCS topologies for the grid-connected BESS is shown in Fig. 3. A common point among the topologies is the output filter for connection to the grid, responsible for attenuating the frequency harmonic generated by the semiconductor switching. These PCSs are classified into four groups:

- PCS topology with only dc/ac stage (T1): The batteries are directly connected to the bidirectional dc/ac stage (Tan; Li; Wang, 2013). The main advantage lies in the simplicity and the low cost of this configuration. However, this system requires several batteries in series to reach the necessary dc-link voltage. Generally, in this system, it is common to have few battery strings and several batteries in series, increasing reliability concerns because if a battery cell fails, the whole string is compromised. For this reason, bypass circuits can be employed in the batteries to overcome this drawback (Baronti et al., 2012). However, these additional circuits increase the system cost and hardware complexity, especially if several batteries are connected in series. Another reliability concern is about the dc/ac stage, if it fails, the entire system is affected. The control of the stage is responsible for performing all grid functions and the charging and discharging of the batteries.

- PCS Topology with dc/dc and dc/ac stages (T2) (Schupbach; Balda, 2003; Ponnaluri et al., 2005): This monolithic system presents a bidirectional dc/dc converter linked with an dc/ac stage. This system allows connecting fewer batteries in series due to the voltage step-up and step-down characteristic of the dc/dc converter. This possibility is important if there is no sufficient battery voltage to directly connect the battery bank to the dc-link. Furthermore, the T2 can also be an attractive solution to avoid several batteries in series, increasing the battery bank reliability since if

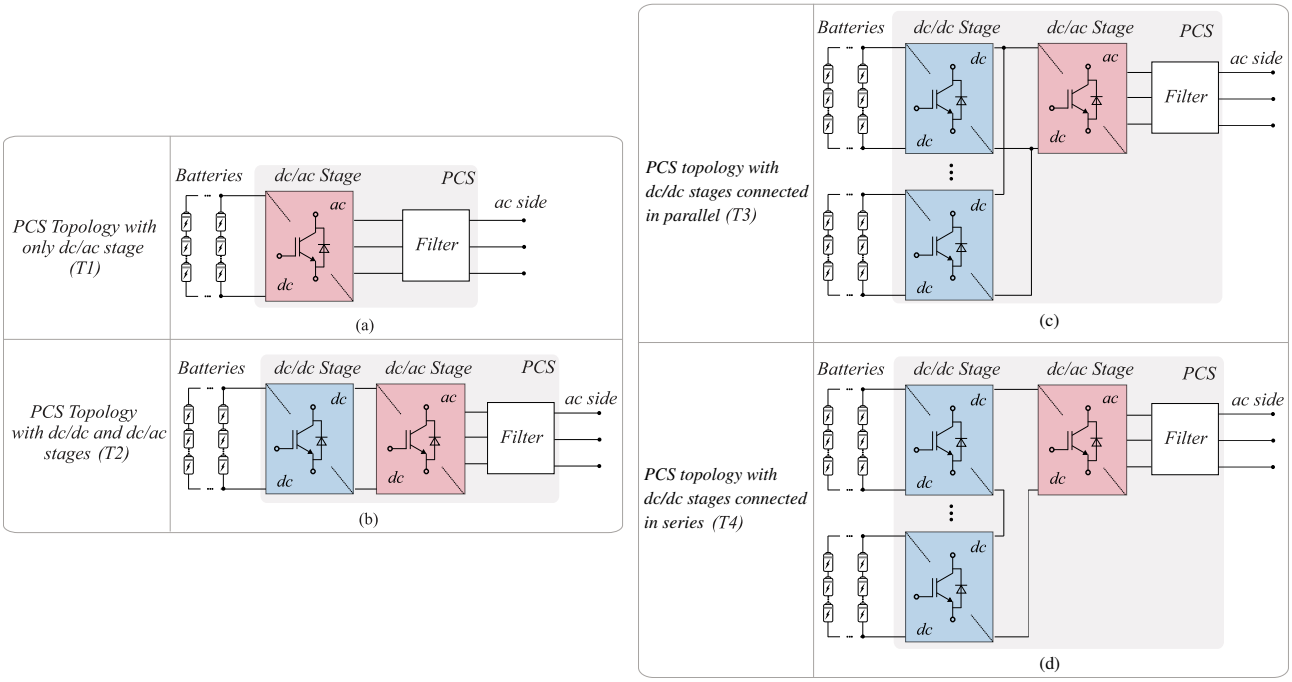


Figure 3 – Schematic of the PCSs topologies for the grid-connected BESS.(a) Single dc/ac stage. (b) Single pair of dc/dc and dc/ac stages. (c) Dc/dc stages connected in parallel. (d) Dc/dc stages connected in series, (Source: own representation)

one battery fails, only one string is affected and the other can still work. With this configuration, the system control can be divided among the converters. The control of charge and discharge of the batteries can be associated with the dc/dc converter and the dc/ac stage controls the grid services. However, the number of power switches is higher than the PCS with only one dc/ac stage. Furthermore, if one stage fails, the BESS can not work.

- PCS topology with dc/dc stages connected in parallel (T3) (Vazquez et al., 2010): This topology concentrates all the system power in only one dc/ac stage, with two or more dc/dc converters in parallel. In this configuration, the output voltage of each dc/dc stage is equal and the currents can be different. For this reason, this dc/dc stage arrangement allows an independent operation between the battery banks, making this converter ideal for hybrid power sources or for using different battery technologies at each stage. Another positive point of this arrangement is that if a converter or string battery fails, the other dc/dc stages can continue generally operating without having to interrupt the entire system to carry out maintenance.

- PCS topology with dc/dc stages connected in series (T4) (Bragard et al., 2010): Unlike T3, this PCS configuration has two or more dc/dc converters connected in series. The main advantage of the series connection of the dc/dc converters is the lower step-up and down ratio than the parallel connection, since the sum of each

converter voltage is equal to the dc-link voltage (Bratcu et al., 2011). However, the control system becomes more complex because a voltage balance strategy between the converters is required to ensure the independent operation between them (Mukherjee; Strickland; Varnosfaderani, 2014).

The guide IEEE Std 2030.2.1™-2019, for design, operation and maintenance of battery energy storage system, highlights the topologies T1, T2 and T3 as the common PCS topologies for BESS (IEEE, 2019). However, the PCS topology T4 is attracting more BESS designer attention due to its efficiency and reliability, as the patent Qahouq (2014). Tab. 1 shows some examples of PCS solution manufacturers that provide some topologies covered in this work.

Table 1 – PCS solution manufacturers that provides some topologies covered in this work. (Source: own representation)

PCS Topology	PCS Manufacturer	Reference
T1	ABB	(Cicio, 2017)
T2	Enercon	(Argyris, 2018)
T3	S&C Electric	(S&C Electric, 2016)

Selecting the power electronics topologies for each PCS stage is important for designers since each topology has inherent advantages and disadvantages. In the following subsections, some topologies of power electronics for both dc/ac and dc/dc stages are presented and each topology that will focus on the analysis of this work.

2.2 Power Electronics for dc/ac Stage

There are two main dc/ac stage groups: two-level and multi-level topologies (Chakraborty; Kramer; Kroposki, 2009; Soong; Lehn, 2014). The first one has the main advantage of simplicity of implementation, control and high commercial maturity. The second one has been gaining more attention in the market, mainly for medium grid voltage applications, and has the advantage of high efficiency and good fault-tolerance capability (Maharjan et al., 2010; Trintis; Munk-Nielsen; Teodorescu, 2010).

The voltage source inverter (VSI), Z-source inverter (ZSI) and quasi-Z-source inverter qZSI, shown in Fig. 4, are two-level inverters for the dc/ac stage of BESS. For the grid connection, it is used a output low-pass filter in order to attenuate the injected harmonics.

The traditional VSI based on full-bridge structure is a widely used dc/ac stage topology due to its hardware and control simplicity. However, the voltage source needs to be higher than the ac voltage. Therefore, the VSI operates as a step-down converter when

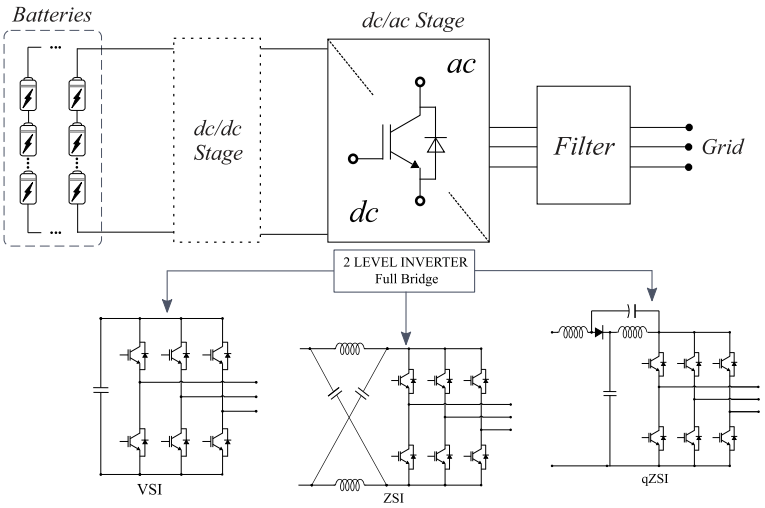


Figure 4 – Conventional topologies of two-level inverters for the BESS connection to the grid. (Source: own representation)

the active power is injected or as a step-up converter for the rectifier mode. Therefore, if the battery bank voltage is smaller than ac grid voltage, the dc/dc converter is necessary.

ZSI and qZSI were designed to overcome this disadvantages inherent of the VSI topology (Fang Zheng Peng, 2003; Anderson; Peng, 2008). These dc/ac stage topologies can operate in step-down and step up in both directions. Therefore, due to these characteristics, many works have used the ZSI to integrate renewable energy sources with batteries and connect them to the grid, which prevents additional dc/dc stage and reduces the number of semiconductors in the system (Cintron-Rivera et al., 2011; Liu et al., 2013).

Among multilevel topologies, the three-level neutral-point clamped (NPC) is another widely used topology for BESS applications (Arifujjaman, 2015; Tabart et al., 2018), as shown in Fig. 5. The advantage of this dc/ac stage topology is the possibility of using power switches with lower blocking voltage and improving the harmonic performance with reduced output filter requirements. This goal is possible due to the clamping of the half dc-link voltage by the clamping diodes, which reduces the power switch voltage requirement.

Similar structures to the conventional NPC are also widely used. The flying capacitor topology uses capacitors instead of clamping diodes to divide the dc voltage input (Meynard et al., 2002). The active NPC (ANPC) topology is another structure that uses electronic switches to perform the voltage clamping (Li et al., 2009). These two topologies are shown in Fig. 5. Further redundancies in the switching states and better capacitor voltage balancing are advantages of these topologies than the topology with diode clamping. Furthermore, the ANPC topology has a higher number of semiconductor switches, which affects the system total cost. More levels of these converters can also be employed, reducing the requirements of the filtering and blocking voltage of power switches (Wang et al., 2017).

However, this approach also increases the control complexity and number of components.

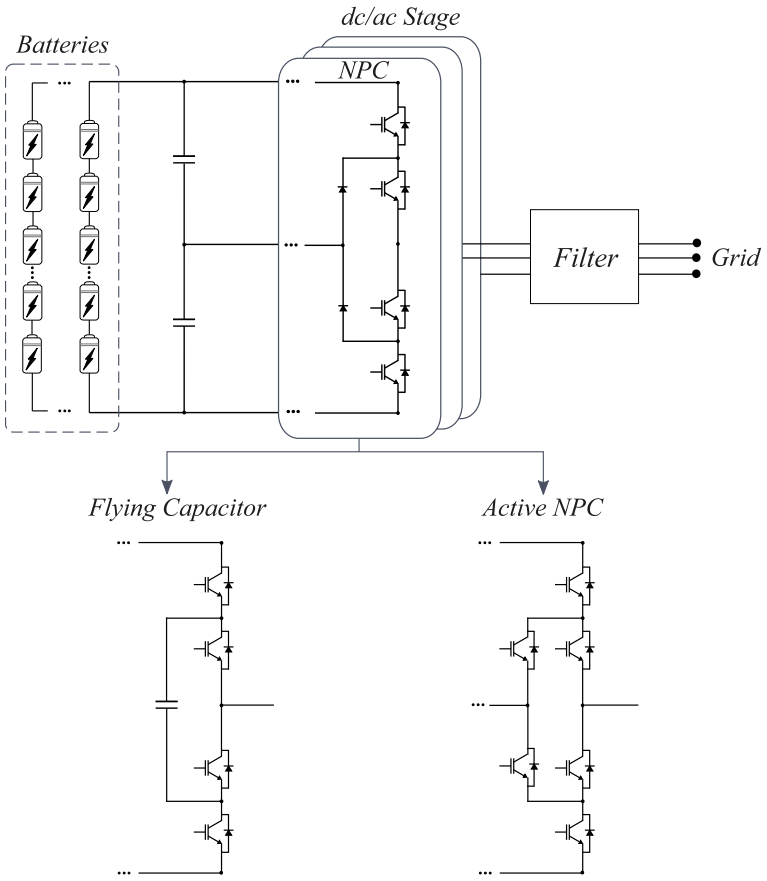


Figure 5 – Three-level dc/ac stage topologies. (Source: own representation)

Multilevel topologies have been highlighted in recent years for BESS application(Marzo et al., 2021; Ma et al., 2021). The cascaded H-bridge converter (CHB) and the modular multilevel converter (MMC) are two highly discussed multilevel topologies in storage applications.

The CHB, shown in Fig. 6, is composed of of several cells of single-phase H-bridge connected in series in each phase (Hagiwara; Akagi, 2009; Kawakami et al., 2014). This dc/ac topology is presented in the literature as star configuration, as shown in Fig. 6(a), or as delta configuration, as shown in Fig. 6(b). Reference Kawakami et al. (2014) shows the development of a 500 kW real-scale star CHB for BESS, with successful test results. Each H-bridge regulates each battery power flow (or battery string) connected to its dc-link. The advantages of the CHB topologies are the inherent advantages of multilevel topologies, such as low blocking voltage requirements of the power switches, fault-tolerant, low-frequency switching operation and low filter requirements (Vasiladiotis; Rufer, 2015). The high number of switches and, consequently, high costs, control and hardware complexity are drawbacks of this topology.

The MMC consists of several single-phase chopper cells connected in series at each phase, as shown in Fig. 7 (Vasiladiotis; Cherix; Rufer, 2015). This topology has the same

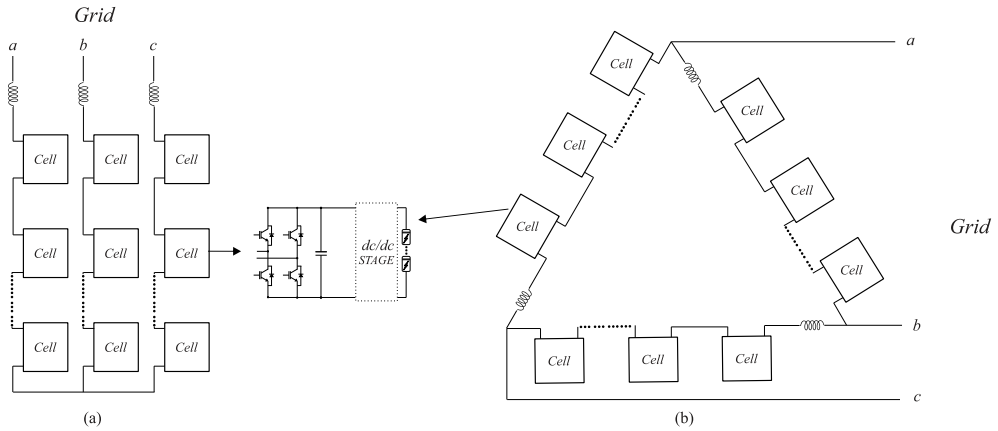


Figure 6 – CHB and its cells composed of single-phase H-bridge. (a) star CHB. (b) delta CHB. (Source: own representation)

advantages inherent to multilevel topologies, as already mentioned for the CHB. This topology presents a flexible disposition of the batteries between the cells of each phase. This topology main advantage is the operation at high grid voltages with low blocking voltage power switches and improved fault-tolerance since if a battery or dc/ac stage cell fails, this can be bypassed and the system can still operate (Cupertino et al., 2020). The MMC showed the highest efficiency, proving to be an interesting solution mainly for a high grid voltage. However, the control complexity and the higher number of electrical components is a drawback of this topology (Wang et al., 2016).

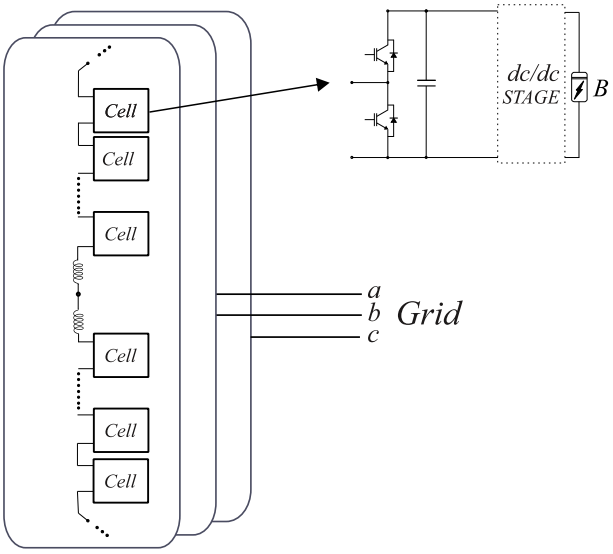


Figure 7 – Schematic of the MMC topology. (Source: own representation)

In this work, the traditional VSI topology is used in the dc/ac stage for BESS PCS application. This topology is chosen due to its market maturity and the control and installation simplicity. Furthermore, the focus of this work is on BESS connected to low voltage grids, which are below the 1000 V.

2.3 Power Electronics for dc/dc Stage

The main bidirectional dc/dc stage topologies for BESS applications are half-bridge, buck-boost and Ćuk converter (Pires et al., 2014). The power electronics structures of these dc/dc converters are shown in Fig. 8. The half-bridge topology is commonly used due to the easy implementation and low control complexity compared to other topologies (Dixon et al., 2010). This converter operates as voltage step-down converter to battery charge and voltage step-up converter to battery discharge (Kollimalla; Mishra; Narasamma, 2014).

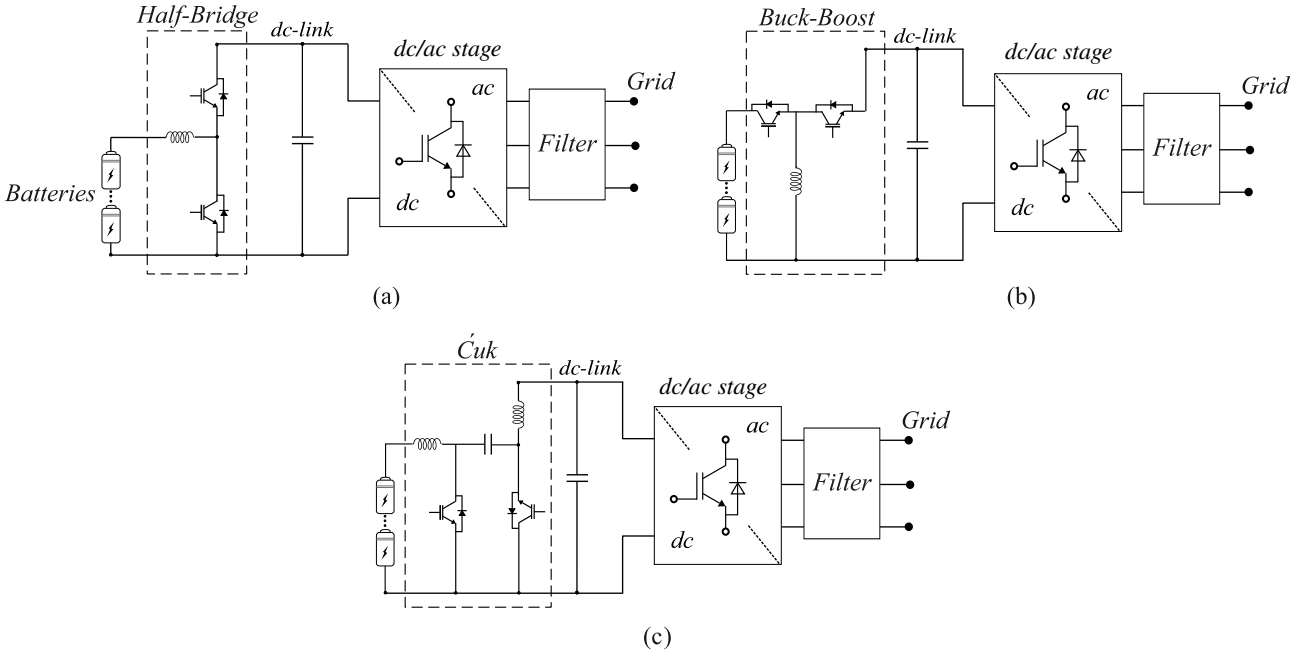


Figure 8 – Main bidirectional dc/dc stage topologies for BESS applications. (a) Half-bridge converter. (b) Buck-Boost converter. (c) Ćuk converter. (Source: own representation)

A variation of the half-bridge converter is the interleaved dc/dc converter, as shown in Fig. 9. It is based on N half-bridge cells in parallel connection, and it is widely discussed in the literature because of the low input and output current ripple, characteristic of multilevel converters (Chen; Lu; Rout, 2018; Da Silva et al., 2016). The low output current is interesting to reduce the required dc-link capacitance (Michal, 2016). The IEEE Std 1491™-2012 warns that a high ripple component on the battery voltage will result in heating, gassing, deterioration of the active plate material (IEEE, 2012). This dc/dc converter is used and detailed in this dissertation for different arrangements.

If galvanic insulation is required, the dual-active-bridge (DAB) topology can be chosen (Zhao et al., 2014), as shown in Fig. 10. This converter topology presents a high-frequency transformer to ensure galvanic isolation between the dc-link and the batteries, replacing the line-frequency transformer, making the energy storage system more

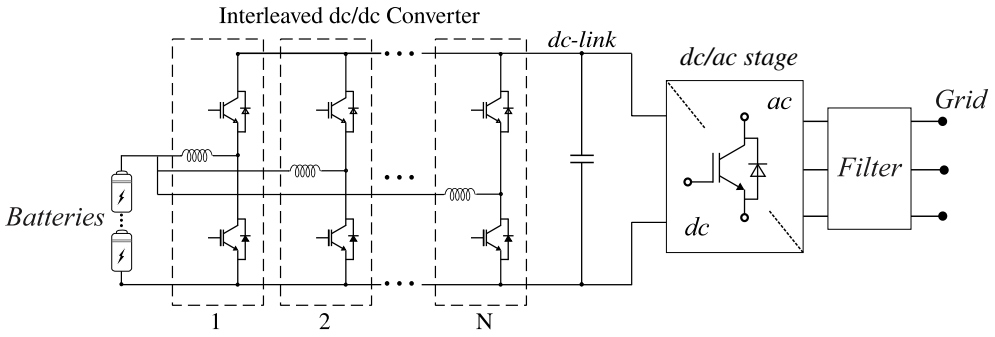


Figure 9 – Interleaved dc/dc converter. (Source: own representation)

compact and flexible (Hung; Hopkins; Mosling, 1993; Inoue; Akagi, 2007). This dc/dc converter is applied in the systems that require a high step-up or down of the voltage between the batteries and dc-link. However, the hardware implementation becomes more complex than the non-isolated dc/dc converters.

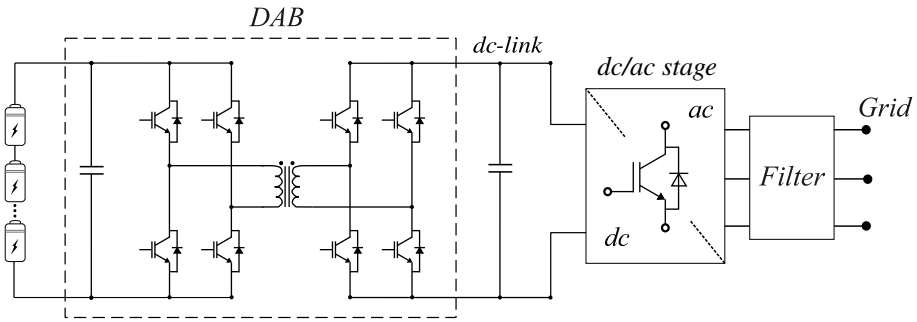


Figure 10 – Dc/dc dual-active-bridge converter. (Source: own representation)

In this work, the dc/dc interleaved converter is used due to the interesting trade-off between the current ripple in batteries and the number of electronic components. Different arrangements of this converter are compared and discussed in terms of efficiency, cost and current ripple.

2.4 Input and Output Current Ripple Cancellation Though Interleaved Converter

This section aims to discuss the characteristic of the interleaved converter and show the advantage of this converter. It is important to highlight that the input and output current ripple depends on the following factors:

- The inductor of each interleaved dc/dc converter cell: this inductor is responsible for limiting the current ripple in each converter cell;

- The number of converter cells: the higher the number of cells, the lower the current ripple in the battery bank, since the ripple in the switching frequency (f_{sw}) of each cell is canceled, leaving only the ripple from (Nf_{sw}). As described below, this ripple cancelation is achieved through phase shifted pulse width modulation (PWM) of the interleaved dc/dc converter.

The inductor for each interleaved cell can be designed in the same way as the boost converter design. Therefore, the inductance is designed considering the boost mode of the bidirectional converter and it is given by (Erickson; Maksimovic, 2001):

$$L = \frac{V_s D}{2\Delta I_L f_s}, \tag{2.1}$$

where V_s is the input voltage or the minimum battery voltage during discharging, D is the duty cycle of each cell, ΔI_L is the current ripple in the inductor of each cell for this operation point and f_s is the switching frequency of each cell. The input apparent current ripple, i.e., the current ripple in the battery using an interleaved converter with N cells is give by (Yang; Zong; Fan, 2017):

$$\Delta I_A = V_o \frac{(1 - D')D'}{LNf_s}, \tag{2.2}$$

where N is the interleaved cells number, V_o is the converter output voltage, Nf_s is the apparent switching frequency of the output current, D' is the apparent duty cycle given by $D' = ND - floor(ND)$.

The normalized apparent current ripple and duty cycles relationship for 1, 2, 3 and 4 cells are shown in Fig. 11. In this case, the individual inductance L is designed to meet 20% of maximum current ripple at duty cycle of 0.5. It is important to highlight that the current ripple design restriction is analyzed in the individual inductor current and the battery current. The reason for that is related to the inductor volume that it is proportional to $LI_{rms}I_{peak}$, where I_{rms} is the RMS value of the ac ripple and I_{peak} is the peak of the current ripple (Ferreira et al., 2020). With a larger number of cells, the individual currents are smaller and therefore the filter volume is reduced. If the battery current ripple is only the design restriction, depending on the number of cells, even an acceptable battery current ripple could lead to a high cell current ripple and, consequently, bulk inductors are necessary (Ferreira et al., 2020).

With this approach, the maximum apparent current ripple with two cells is 10%, 6.66 % for three cells, and 5% for four cells. In both cases, the maximum inductor current ripple is 20%. The duty cycle that the maximum ripple occurs is related to the number of cells, as depicted in Fig. 11.

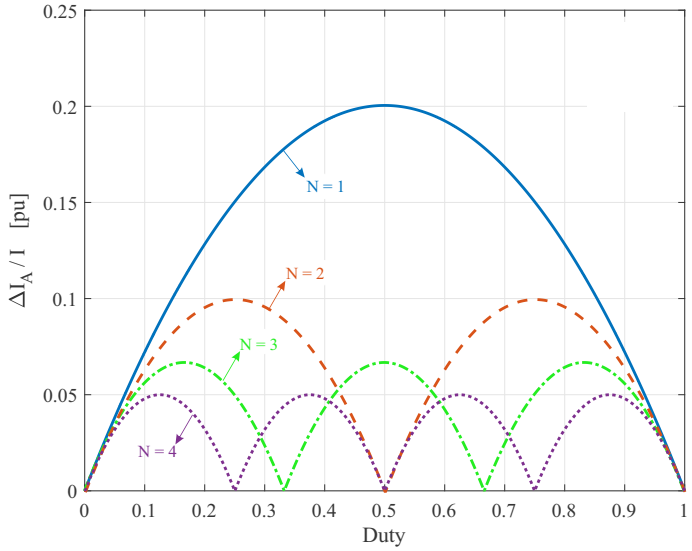


Figure 11 – Input current ripple using interleaved dc/dc converter with 1, 2, 3 and 4 cells. (Source: own representation)

The battery current ripple reduction through the interleaved converter is achieved when the phase between the triangular carries of each cell in the PWM is displaced as:

$$\theta_t = \frac{360^\circ}{N} \tag{2.3}$$

An important feature of the interleaved converter, approach in the literature, is the phase-shedding method. This technique disconnects the interleaved branches to improve the light load efficiency (Su; Liu, 2013; Baek; Choi; Cho, 2013). Therefore, techniques to determine the number of branches indicating for an operation point of a light load are required. It is worth remembering that, disconnecting branches from the interleaved converters can increase the input and output current ripple.

2.5 Battery Model

In this work, the stationary lead-acid battery technology is used to evaluate the PCS for BESS. This technology was chosen due to its high commercial maturity and it is use in applications involving uninterruptible power supply and grid support (Akhil et al., 2013b)

The battery model is essential to simulate the battery behavior under different operating conditions, to predict the battery performance (current, voltage, temperature), to evaluate the safety of the battery in critical situations, to analyze the PCS control strategy and efficiency under different battery operation conditions. The accuracy of the battery model depends on the required analysis. However, generally, the accuracy is inversely linked to the computational effort.

There are three main battery models:

- Mathematical model: This model is usually derived from empirical equations based on Shepherd relation (Shepherd, 1965). This model is commonly used when a simple and not very accurate model is needed, and when it is only necessary to predict the macroscopic battery quantities (current-voltage, temperature). This model advantage is the flexibility to manipulate the equations and the facility to adjust the parameters for different battery characteristics, generally through the battery datasheet curves. Furthermore, this battery model requires a low computational burden.
- Physical-chemical model: This model identifies the battery cell performance and cell optimization with high accuracy and describes macroscopic and microscopic (cell physical-chemical characteristics) quantities (Ramadesigan et al., 2012). It is formed from the partial differential equations to be solved, with a considerable computational burden. Furthermore, the model parametrization is a complicated task.
- Electrical model: This model is based on electrical equivalent circuits and provides the macroscopic battery quantities (He; Xiong; Fan, 2011). It presents a good trade-off between complexity and accuracy. Generally, this model requires experimental realization to achieve the model parametrization.

This work aims to obtain the macroscopic battery quantities with easy parametrization and low computational burden. Therefore, the mathematical model based on the Shepherd equations is used due to the simplicity of obtaining the batteries datasheet parameters without taking experimental measures on the battery (Shepherd, 1965). Based on this model, the lead-acid battery voltage is given by (Tremblay; Dessaint; Dekkiche, 2007):

$$V_{batt} = E_0 - Ri(t) - K\frac{Q}{Q - i_q(t)}\left[i_q(t) + i(t)^*\right] + Exp(t), \tag{2.4}$$

$$V_{batt} = E_0 - Ri(t) - K\frac{Q}{i_q(t) - 0.1Q}i(t)^* - K\frac{Q}{Q - i_q(t)}i_q(t) + Exp(t), \tag{2.5}$$

where:

- V_{batt} = the battery output voltage $[V]$;
- E_0 = the battery constant voltage $[V]$;
- K = the polarisation resistance that represents the resistance between the electrodes and the electrolyte $[\Omega]$;

- Q = the battery capacity $[Ah]$;
- i = the battery output current [A];
- $i_q(t)$ = the actual extracted (discharging) or provided (charging) battery charge $(\int i(t)dt)$ $[Ah]$;
- R = the battery internal resistance $[\Omega]$;
- $i(t)^*$ = the filtered battery output current $[A]$, generally using a low-pass filter.

The $Exp(t)$ equation represents the exponential zone behavior of the battery. This phenomenon is represented for lead-acid battery as:

$$\dot{Exp} = B|i(t)|\left[-Exp(t) + Au(t)\right], \tag{2.6}$$

where $u(t)$ is the charge (1) or discharge (0), A is the exponential voltage constant and B the exponential zone time constant. Tremblay, Dessaint and Dekkiche (2007) and Tremblay and Dessaint (2009) approach the details on how to extract the battery parameters from the datasheet.

The battery voltage and current dynamics during charging and discharging are emulated by this mathematical model, as shown in Fig. 12 for lead-acid technology. Fig. 12(a) shows the battery voltage profile concerning the SOC during the discharging considering a constant discharge current, where V_{fc} is the full charge voltage, V_{nom} is the battery nominal voltage and $V_{cut-off}$ is the cut-off voltage when the battery is fully discharged ($SOC = 0\%$). Fig. 12(b) shows the relationship of the battery voltage and current dynamics with the time during the three-stage charging.

The first stage is the constant current mode (CCM) where a constant current (I_{ch}) is provided for the battery until the battery voltage reaches the charge boost voltage (V_{boost}). The second stage consists to provide the constant voltage V_{boost} for the battery and the current decreases, this stage is the constant voltage mode (CVM). When the current reaches around 10% of the initial discharge current, the float voltage level is provided for the battery and it remains until a new discharge command. This is the third stage or float mode operation. The current and voltage characteristics are generally provided in the lead-acid battery datasheet, thus the parametrization is an easy task.

2.6 Chapter Conclusions

In this chapter, a literature review of the main topologies of PCS for BESS application was performed, indicating the main power electronics topologies for dc/dc and dc/ac stages. This review will serve as a basis for the studies that will be carried out in the next chapters.

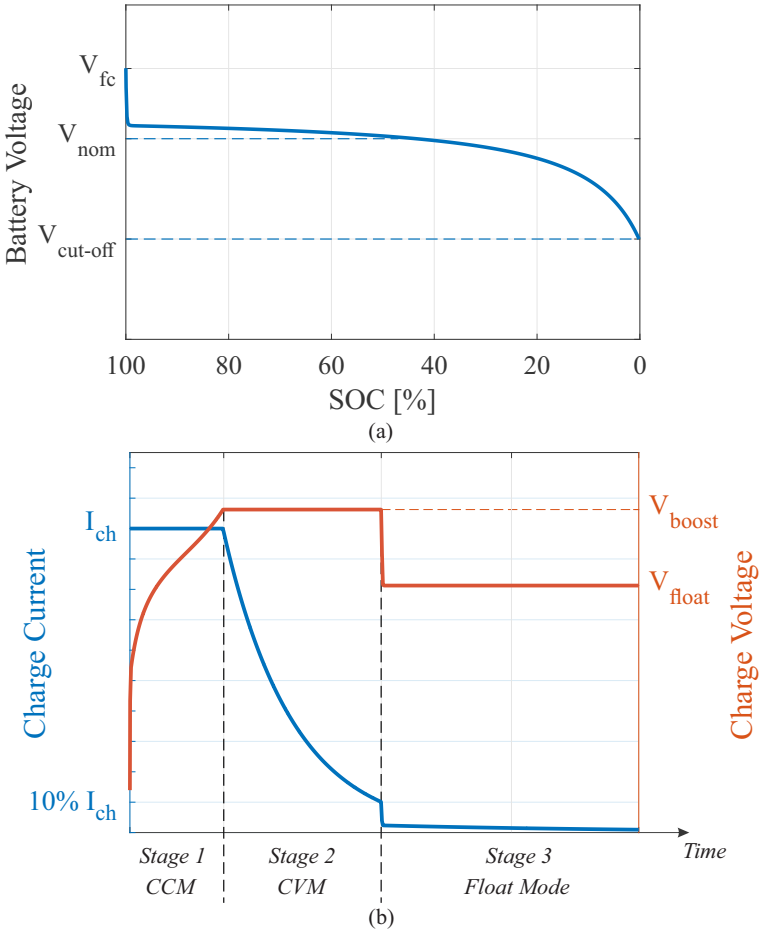


Figure 12 – Voltage and current dynamics of the lead-acid battery during discharging and charging. (a) Voltage dynamic during discharging. (b) Current and voltage profiles during charging. (Source: own representation)

This chapter has pointed out the main topologies based on a single-stage, two-stage, dc/dc stages with converters in parallel and series connection. These topologies will be the focus of the study of this thesis and the system design considering lead-acid batteries will be verified.

For such studies, lead-acid battery technology was modeled through Shepherd mathematical equations and it will be important to estimate the PCS efficiency during the battery charging and discharging and define the procedure of the PCS design for BESS.

3 PCS Design Aspects for BESS

In this chapter, the power electronics topologies for BESS PCS studied in this work are defined. Furthermore, design aspects are proposed, such as the influence of battery voltage variation on the IGBT module solution for the dc/ac stage when the dc/dc stage is employed or not. The system cost estimation methodology of the BESS is approached. Finally, the power structure and control strategy are designed for each PCS.

3.1 Power Electronics Structures

The power electronics topologies used in this work are shown in Fig. 13. These topologies are composed of a two-level dc/ac stage with an LCL filter connected to the grid.

The first power electronics topologies is T1 shown in Fig. 13(a). The main characteristic of this topology is that only dc/ac stage is used and the battery bank is connected directly to the dc-link. This power electronics configuration is suitable if the minimum dc-link voltage is achieved for all SOC operation levels. It is worth remembering that the battery voltage varies with SOC (Wong; Hurley; Wölfle, 2008). Therefore, the BESS designer must choose the dc/ac stage power switches to meet this voltage variation. For example, the minimum battery bank voltage during discharging needs to be enough to connect the dc/ac stage to the grid. However, the switches must block the battery bank voltage at the boost level, about 37% higher than the battery cut-off voltage (Moura, 2021). This fact results in poor switching utilization for this power electronics solution. According to Erickson and Maksimovic (2001), the switching utilization is given by:

$$U = \frac{P_{load}}{S}, \tag{3.1}$$

where P_{load} is the converter load power and S is the switch stress defined as:

$$S = \sum_{j=1}^{k} V_j I_j, \tag{3.2}$$

where V_j is the peak voltage applied to semiconductor switch j, and I_j is the rms current applied to the switch j. Therefore, this utilization relation suggests that in a good design, the voltage and current imposed on the semiconductor devices is minimized, while the load power is maximized.

An alternative to optimize the switching utilization is to use the dc/dc stage, as shown in Fig. 13(b). In this T2 power electronics topology, the battery bank is connected

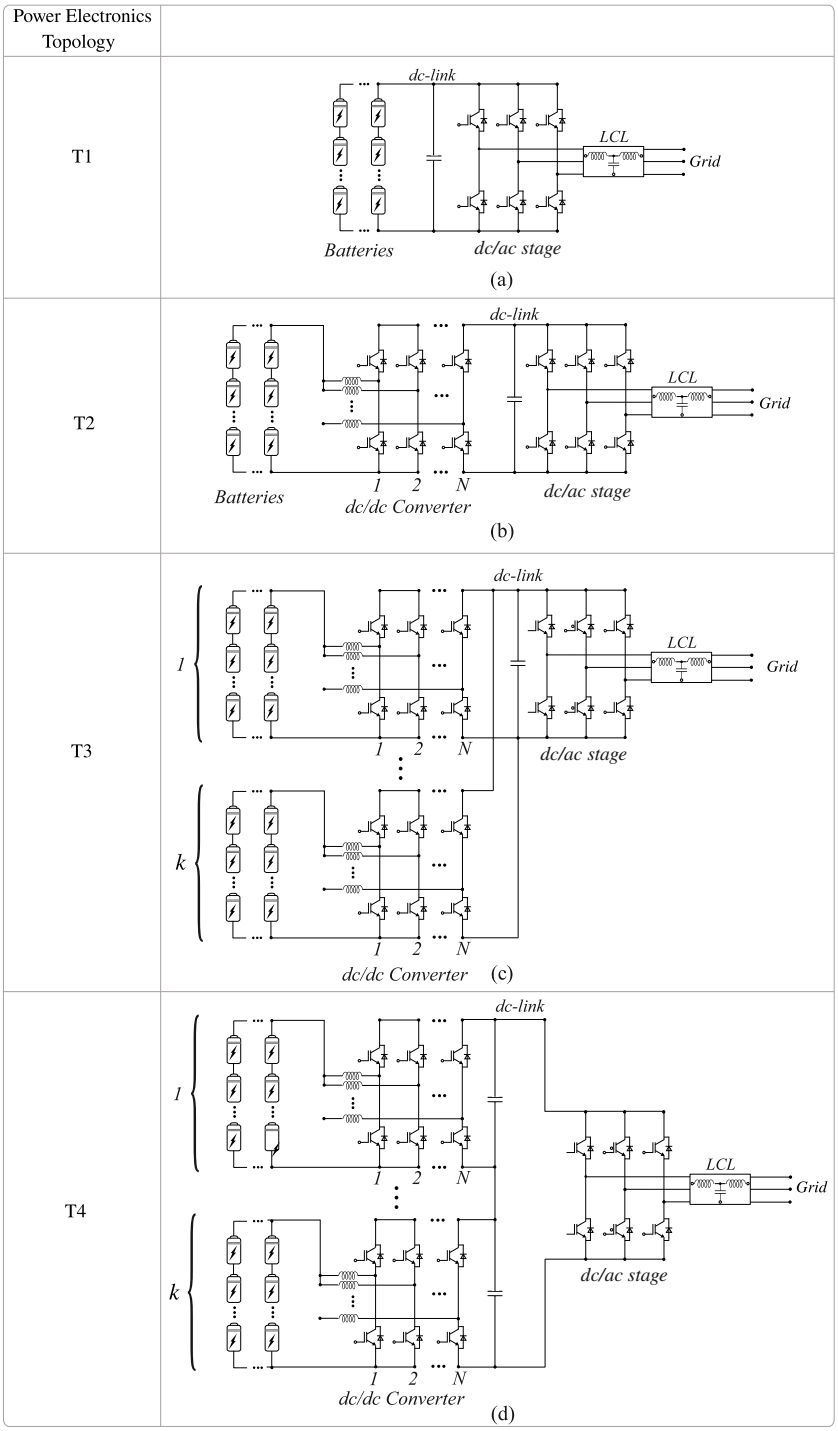


Figure 13 – Power electronics structures applied to BESS based on two-level dc/ac stage and dc/dc converter arrangements. (a) Single stage topology. (b) Interleaved dc/dc converter concentrating all BESS power. (c) Parallel connection of the interleaved dc/dc converters. (d) Series connection of the interleaved dc/dc converters. (Source: own representation)

in an interleaved dc/dc converter. This converter is composed of N half-bridge cells and it operates as a voltage step-up converter during battery discharging and as a voltage step-down converter for charging process.

The battery bank can be divided into more interleaved converters, distributing the power processed by the devices. Therefore, the interleaved converters can be connected in parallel (power electronic topology T3) or series (power electronics topology T4), forming a multi-port dc/dc stage interface with k converters, as shown in Fig. 13(c) and Fig. 13(d), respectively (Pires et al., 2014; Solero; Lidozzi; Pomilio, 2005; Jiang; Fahimi, 2011; Mukherjee; Strickland, 2016).

At a first glance, the parallel connection allows an easy independent operation between the battery banks, with different charges and discharges rates between them, increasing system operational flexibility. Moreover, if one dc/dc converter fails, the system can still operate partially without any complicated intervention, increasing system reliability.

The topology T4 has the main characteristic of output voltage sum. This characteristics leads two design scenarios for T4 in relation to T3:

- Scenario 1: The battery bank configuration and the battery charge for T4 are the same as T3. This battery bank can be adopted in T4 if the maximum battery bank voltage is smaller than the output voltage, even adding the output voltage of the converters. In this scenario, there is an improvement of switching utilization and step-up ratio decrease when using topology T4.
- Scenario 2: The number of batteries in series must be decreased for T4, compared to T3, due to the high dc-link voltage. Therefore, parallel string or the battery charge must increase to obtain the same power o T3. This scenario occurs when it is impossible to connect the same number of batteries with the same charge in series in T4 if compared to T3. This situation can decrease the switching utilization.

These two scenarios for T4 are analyzed in the results. Another important characteristic of the series connection of dc/dc converters is that the current flowing through the converters is the same. Therefore an independent operation between the converters with different discharge and charge rates can be achieved with an output voltage sharing control strategy (Bratcu et al., 2011). For this reason, the control strategy of T4 presents more challenges than the T3 topology. The control analysis is approached in the next chapter.

3.2 Battery Voltage Variation Influence on Semiconductor Blocking Voltage

The minimum dc-link voltage ($V_{dc,min}$) required for two-level dc/ac stage is equal to the peak value of the grid-line voltage, generally plus a reserve of 4% (Islam; Guo;

Zhu, 2014). When the dc/dc stage is not employed, the dc-link voltage changes due to the battery voltage variation. The highest dc/ac converter blocking voltage is the charge boost voltage, and the lowest blocking voltage is correspondent to the minimum allowable battery SOC during discharge process. Hence, the blocking voltage (dc-link voltage) in function of the grid rms voltage is given by:

$$V_{dc(V_g)} = r_b V_{dc,min(V_g)}, \tag{3.3}$$

where $V_{dc,min(V_g)}$ is the minimum dc-link voltage in function of the rms grid voltage (V_g) and r_b is the ratio of the dc-link voltage variation. When the dc/dc stage is not employed, $r_b > 1$ and equal to the ratio between the charge boost voltage and the voltage corresponding to the minimum allowable SOC during discharge. When the dc/dc stage is employed $r_b = 1$, and then $V_{dc(V_g)} = V_{dc,min(V_g)}$.

The power semiconductors of the dc/dc and dc/ac stages are chosen based on the required blocking voltage. The common voltage classes of IGBT modules available in the market are 600 V, 1200 V, 1700 V, and 3300 V for low voltage application. However, only 50%-70% of the semiconductor rated blocking voltage can be utilized to limit the susceptibility to cosmic-ray-induced failures (Dodge, 2007; Huber; Kolar, 2017). The notation γ is used to refer to this device blocking voltage margin.

For the following analysis, a conventional 12 V lead-acid battery characteristic curves are used with charge boost voltage equal to 14.4 V. The battery voltage is equal to 11.52 V in the minimum admissible $SOC = 20\%$ during discharging. Therefore, r_b is 1.25 for the single dc/ac stage is employed. It is important to mention that 63% of the semiconductor rated blocking voltage is used for this analysis.

The blocking voltage (V_{dc}) of the power switches and the grid rms voltage (V_g) relationship, given by Eq. 3.3, is shown in Fig. 14 for the following cases:

- The dc/dc stage is not employed ($\nexists$). The battery bank is connected directly to the dc-link, and it is discharged up to 20% of SOC. The solid red line represents this case;

- The dc/dc converter is employed ($\exists$). This case represents the $V_{dc,min}$ line, since the dc-link is fixed in this value due to the dc/dc stage presence. The dash yellow line represents this case.

The difference between these two cases is due to the r_b value for each case, and it increases with the grid voltage. When the batteries are directly connected to the dc-link, the rate r_b is higher than for the case where a dc/dc stage is employed.

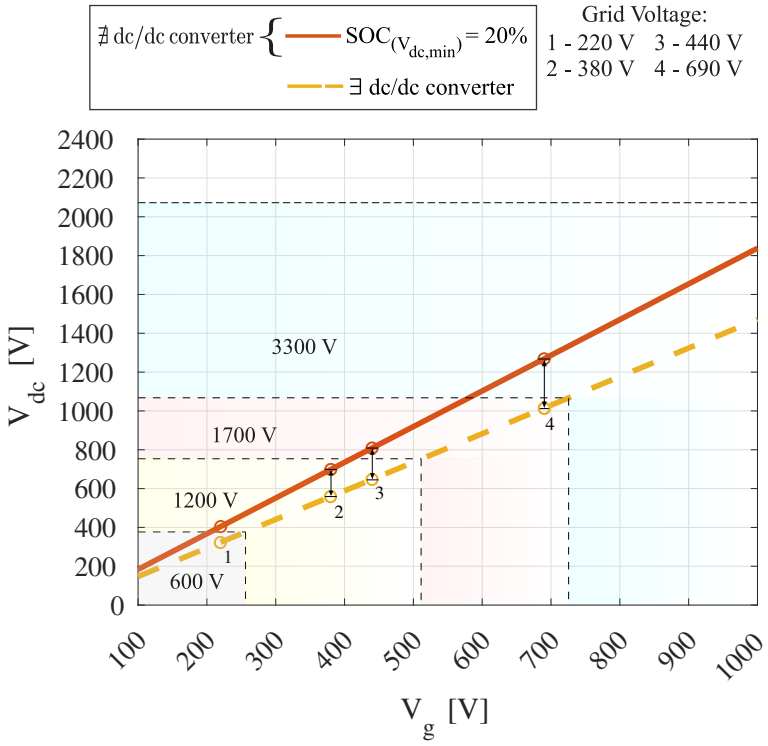


Figure 14 – Blocking voltage requirement for the dc/ac stage IGBT module in relation to the grid voltage for BESS. (Source: own representation)

With the dc/dc converter, the dc-link voltage can be always controlled at the $V_{dc,min}$, and this approach reduces the required voltage class of the dc/ac converter power switches compared to the dc-link voltage without control (without dc/dc stage). The voltage classes of IGBT modules available on the market (600 V, 1200 V, 1700 V, 3300 V) are selected depending on the maximum blocking voltage requirements, i.e, depends on the grid voltage. The points 1, 2, 3 and 4 in Fig. 14 correspond to the main grid levels, 220 V, 380 V, 440 V and 690 V, respectively. For the grid level of 220 V, 440 V and 690 V, the recommended voltage class for dc/ac stage switches is different considering the single or two-stage PCS topology.

For example, considering the 690 V grid voltage, the $V_{dc,min}$ is 1015 V and this voltage level is fixed when the dc/dc stage is employed. In this case, the 1700 V voltage class of the power switches meets the blocking voltage requirements. However, the voltage class must be increased to 3300 V for the single stage PCS topology, since the dc-link voltage can reach 1268 V during charge boost voltage. This voltage class difference can influence the PCS power losses, and an analysis of these cases is important for the converter design. It is worth emphasizing that the absence of dc/dc stage also restricts the minimum number of batteries in series, which restricts the system design.

3.3 PCS Power Losses Calculation Method

The approached BESS efficiency calculation considers the core and copper power losses of all inductors, the switching and conduction losses of the IGBT power modules, and the losses of all capacitors modeled by equivalent series resistance.

The copper losses are represented by the dc ohmic losses in the inductor windings, and it can be given by (Graovac; Purschel, 2009),

$$P_{copper} = R_L \bar{I}_L^2, \tag{3.4}$$

where R_L is the inductor series equivalent resistance and $\bar{I}_L$ is the average current in the inductor. The ac copper losses are neglected, considering that the inductor design reduces the proximity and skin effects.

The core losses are estimated by the improved generalized Steinmetz equation method (iGSE) (Venkatachalam et al., 2002; Mühlethaler; Kolar; Ecklebe, 2011), calculated by the following empirical power equations,

$$P_{core} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt, \tag{3.5}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}, \tag{3.6}$$

where k, α and β are material parameters that have to be empirically determined, known as Steinmetz parameters. Generally, the parameters are provided by the magnetic core manufacturer. B is the flux density and ΔB is the peak-to-peak flux density. θ is the flux angle.

The flux density waveform must be known, and thus the magnetic losses can be computed numerically by Eq. 3.5 and 3.6. B can be obtained from the voltage at the inductor terminals v_L, as given by:

$$B = \frac{1}{N A_c} \int v_L dt. \tag{3.7}$$

where A_c is the cross-sectional area of the inductor core and N is the number of turns.

A constant voltage drop can approximate the conduction losses of the IGBT, and it can be calculated by,

$$P_{CT} = V_{CE}\bar{I}_C, \tag{3.8}$$

where V_{CE} is the IGBT forward voltage drop, and it can be directly obtained from the device datasheet for the current flowing through the IGBT $\bar{I}_C$. Similarly, the conduction losses of the diode can be calculated by,

$$P_{CD} = V_F\bar{I}_D, \tag{3.9}$$

Where V_F is the diode forward voltage drop, and it can be directly obtained from the device datasheet for the current flowing through the diode $\bar{I}_c$.

The switching losses in the IGBT and diode can be calculates based on turn-on and turn-off energy loss given in the datasheet as a function of the currents that flow in these devices, respectively given by,

$$P_{ST} = [E_{on}(\bar{I}_C) + E_{off}(\bar{I}_T)]f_{sw}, \tag{3.10}$$

$$P_{SD} = [E_{rec}(\bar{I}_T)]f_{sw}, \tag{3.11}$$

where f_{sw} is the switching frequency. It is worth noting that the turn-on losses in the diode are normally neglected (Graovac; Purschel, 2009).

The power loss in the electrolytic capacitors is computed by the equivalent series resistance (ESR) provided by the device datasheet as a function of the current frequency (f) that flows in the capacitors. Therefore, the electrolytic capacitor power loss is given by,

$$P_{ecap} = \sum_{f=0}^{F} \bar{I}^2_{CP(f)}ESR_{(f)}, \tag{3.12}$$

where $\bar{I}_{CP(f)}$ is the mean current of each frequency.

The ac film capacitor power loss is computed by an equivalent series resistance value provided by the device datasheet. This resistance does not significantly vary with the frequency. Therefore, the total power loss of the film capacitor is given by:

$$P_{fcap} = \bar{I}^2_{CP,rms}ESR, \tag{3.13}$$

where ($\bar{I}_{CP,rms}$) is the rms value of the capacitor current.

Based on the power losses described above, the PCS efficiency (η) is given by the sum of all power losses divided by the input power, which is the battery bank power during battery discharging and the grid power during battery charging.

A global efficiency index is proposed in this work and it is used to compare PCS topologies performance during a battery charge and discharge cycle. This index is calculated concerning energy losses during this cycle and the system input energy, which is the battery bank energy during discharge and the grid energy during charging. This global efficiency index is given by:

$$\eta_{gi} = \left[1 - \frac{\int_{t_{di}}^{t_{df}} P_{loss(t)}dt + \int_{t_{ci}}^{t_{cf}} P_{loss(t)}dt}{\int_{t_{di}}^{t_{df}} P_{in(t)}dt + \int_{t_{ci}}^{t_{cf}} P_{in(t)}dt}\right] \times 100, \tag{3.14}$$

where t_{di} and t_{df} are the initial and final instant of the discharging, respectively. t_{ci} and t_{cf} are the initial and final instant of the charge instant. $P_{loss}(t)$ is the time-dependent power losses calculated through the methodology described in this section. P_{in} is the input power, which is equal to the battery power during the discharging and equal to the grid during charging. This methodology allows comparing the PCS topologies with a single efficiency value after battery discharge and charge cycle. This efficiency index provides a general overview instead of a fixed efficiency values for an operating point usually provided by manufacturers.

3.4 Cost Calculation Method

The PCSs investment or cost for BESS are compared in this study. Engel et al. (2015), Abu Bakar Siddique et al. (2016) approximate the cost of the semiconductor devices, controls and cabinets as 4 USD/kVA of the installed power, given by:

$$P_{sw} = N_{semi} V_{block} I_{nom}, \tag{3.15}$$

where N_{semi} is the number of semiconductor device (IGBT and diodes), V_{block} is the semiconductor voltage class and I_{nom} is the nominal current.

The cost of the magnetic device is estimated as (Engel et al., 2015):

$$Cost_{mag}[USD] = 818508.3A_p + 4528.8N_{ind}, \tag{3.16}$$

where N_{ind} is the number of inductor, $A_p[m^4]$ is the product of the winding window area and the cross section area of the inductor core.

The cost of the electrolytic and film capacitors are estimated by the follow empirical equations, respectively (Wang et al., 2020):

$$Cost_{e-cap}[USD] = 0.0134C + 0.9815, \tag{3.17}$$

$$Cost_{f-cap}[USD] = 0.209C + 0.7812, \tag{3.18}$$

where C is the capacitance in μF.

The battery cost model was obtained by a market research performed in this work. Lead acid battery costs from Brazil, United State, Europe and Asia were used. The prediction model was obtained through a linear regression based on least squares method, which 91.7% of the proportion of the variation in the cost is predictable from the battery charge. This lead-acid battery cost model is presented in Fig. 15. Therefore, the lead-acid battery cost in USD can be approximated by a linear relation to the battery charge (Ch) and it is given by:

$$Cost_{bat}[USD] = 2.95Ch - 1.75, \tag{3.19}$$

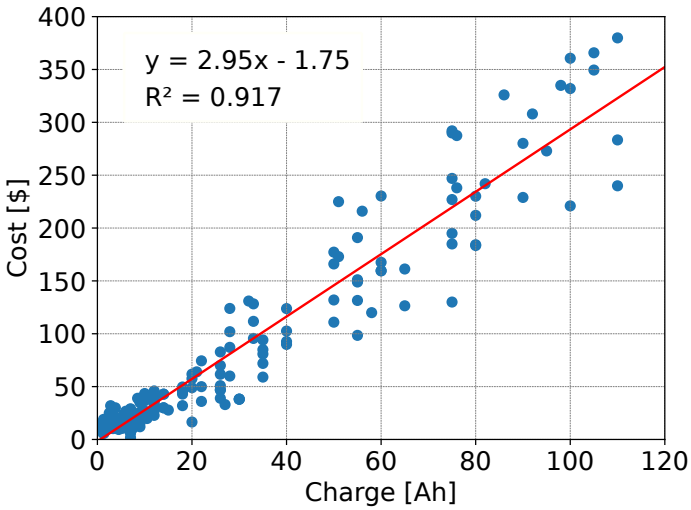


Figure 15 – Lead-acid battery cost estimation in relation to the charge. (Source: own representation)

3.5 Approach to PCS Design for BESS

The flowchart of the PCS design for BESS oriented toward voltage class and efficiency proposed in this work is shown in Fig. 16. The main design inputs are the BESS energy requirements, power requirements and the grid voltage level. With latter, the minimum dc-link voltage is the peak value of the grid voltage plus a reserve of 4%, as discussed in this chapter. The next step is to determine the battery technology, such as lead-acid or lithium-ion batteries, for example. The ratio of the dc-link voltage variation r_b is defined for the case when this voltage is fixed (dc/dc converter is used) or for variable voltage (dc/dc converter is not used). For the last case, the maximum and minimum

operating voltage for the battery technology must be known. Generally, these voltage levels can be found in the battery datasheet.

The following steps are to determine the blocking voltage margin used in the semiconductor devices and find the voltage class of the semiconductors for each r_b condition for each PCS topology. After these procedures, the design of the battery bank is performed according to the BESS energy and power requirements. The global efficiency index is calculated in this design methodology and this indicator can be used for the long-term cost analysis.

The next step is to estimate the initial cost of PCS topologies. Finally, with the initial cost and global efficiency index information for one cycle, the best PCS solution for the project can be determined through a long-term cost analysis. This work recommends using the levelized cost of storage (LCOS), which is the index to represent the entire building and operating cost over the energy involved in c_n cycles of charge and discharge. There are advanced methodologies to calculate the LCOS in the literature with several parameters and indicators (Steckel; Kendall; Ambrose, 2021). As the purpose of this work is not to do a deeper analysis of this topic, a simplified LCOS is used to compare the PCS topologies for BESS given by:

$$LCOS = \frac{CAPEX}{Ec_n\eta_{gi}}, \tag{3.20}$$

where the CAPEX is the capital expenditure and it is associated with the initial cost estimation, E is the nominal energy of the system, c_n is the total cycle number of charge and discharge and η_{gi} is the global efficiency index.

3.6 Chapter Conclusions

The power electronics topologies were defined based on different arrangements of interleaved dc/dc converters. The advantages and disadvantages of parallel and series connections of the dc/dc converters were presented. The parallel connection presents the advantage of simplicity in operation independence between the battery banks. The series connection can improve the switching utilization and operates with a reduced step-up voltage ratio. These differences will be explored with details in the results section.

The study about battery voltage variation impact was presented. The analysis shows that the requirements of the voltage classes of semiconductors switches, especially for the dc/ac stage, can change depending on the PCS topology and the grid voltage level. This fact raises questions about costs and efficiency in the BESS design. Therefore, this work addressed methodologies for efficiency and cost estimation. The global efficiency index was proposed and it is mainly important for long-term cost analysis.

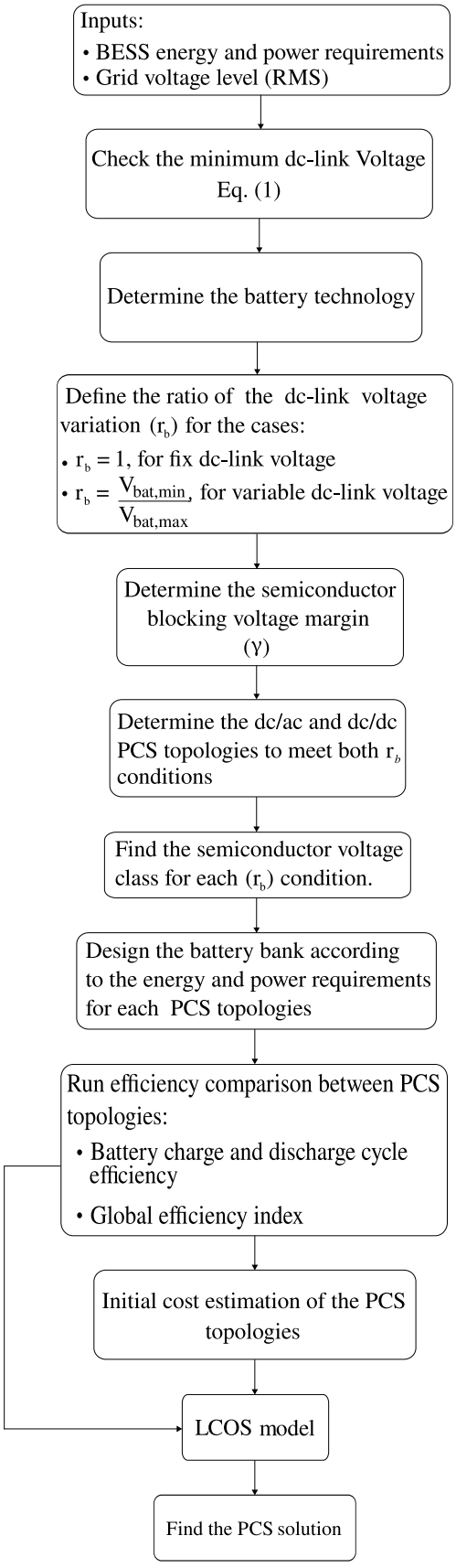


Figure 16 – PCS design for BESS application oriented toward voltage class and efficiency. (Source: own representation)

Finally, a step by step for BESS design oriented toward voltage class and efficiency was presented, where all theory discussed in this chapter is applied in a BESS design procedure. The aim is to define the dc/ac strage voltage class of all PCS topologies and compare the efficiency and long-term cost.

4 Control Structure Design Aspects for BESS

Fig. 17 shows the control structures for the power electronics topologies defined in the previous chapter. All control strategies must comply with the battery and grid control requirements. The battery requirements mainly involve charge modes, such as constant current and voltage modes. The grid requirements involve the services which depend on active and reactive power control.

The control structures are split into dc/ac and dc/dc stages. For the dc/ac stage, the inner loop of all structures controls the inverter side LCL inductor current and it is perfomed in a stationary reference frame ($\alpha\beta$). The current references ($i^*_{\alpha,\beta}$), are calculated by the instantaneous power theory, given by (Akagi; Kanazawa; Nabae, 1984):

$$\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} P^*_n \\ Q^*_n \end{bmatrix}, \tag{4.1}$$

where Q^*_n is the reactive power reference to perform some grid service such as Low-Voltage-Ride-Through or voltage regulation (Yang; Wang; Blaabjerg, 2014; Miñambres-Marcos et al., 2015). The positive sequence on the fundamental frequency of the point of common coupling (PCC) voltage in stationary reference ($v_{\alpha,\beta}$) is calculated by the dual second-order generalized integrator (DSOGI) with the phase-locked loop (PLL). Rodríguez et al. (2006) presents a complete description of the DSOGI-PLL. The inner-loop controls the dc/ac stage current in the stationary reference frame through the current controller G_c, described in the following subsections. The feedforward voltage terms ($v_{\alpha,\beta}$) are added to the G_c output, generating the dc/ac stage reference voltages synthesized using a space vector modulation (SVPWM) (Holmes; Lipo, 2003).

The difference between the dc/ac stage control structure for the power electronic topologies is the outer loop control. The two-stages topologies present differences in the dc/dc stage control. The main characteristics of the power structures for the power electronics topologies are pointed below:

- T1: For single-stage PCS topology (power electronics topology T1), the dc/ac stage control strategy must accomplish the battery and grid service goals, as shown in Fig. 17(a). The outer loop presents the active power control enabled during battery discharging. This power control is a proposal of this work. Furthermore, the outer loop presents the dc-link control based on square voltage value, which is enabled during battery charging. The battery boost voltage (V_{boost}) and the float voltage (V_{float})

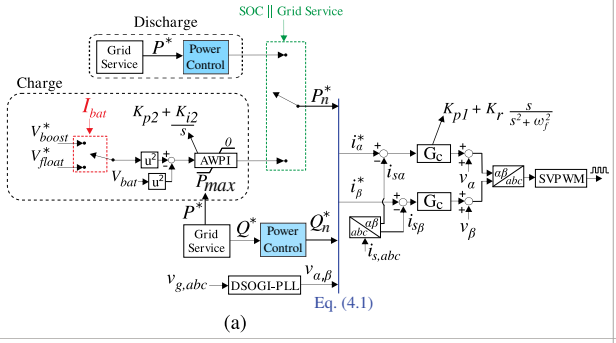
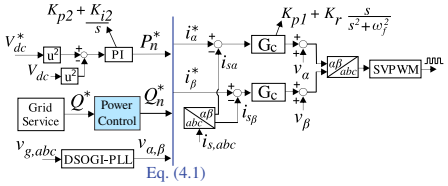
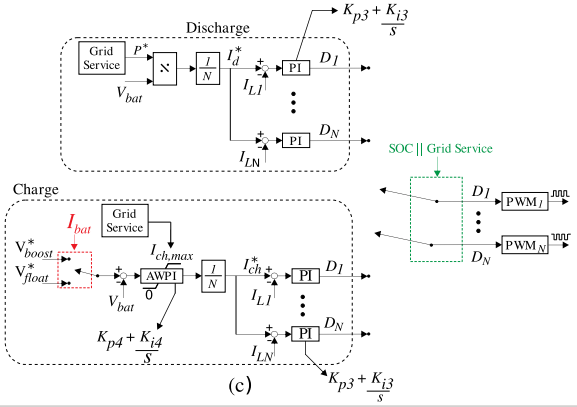
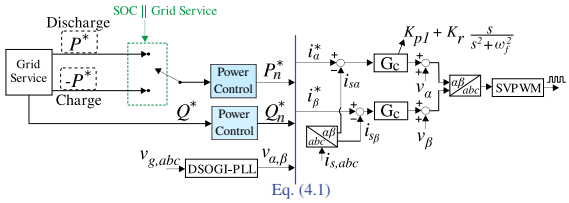
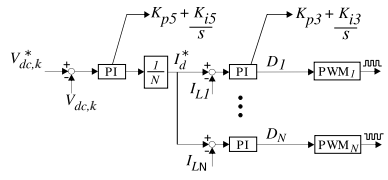
Power Electronics Topology	Control Structures	Stage Control
T1	 (a)	dc/ac stage
T2 and T3	 (b)	dc/ac stage
	 (c)	dc/dc stage
T4	 (d)	dc/ac stage
	 (e)	dc/dc stage

Figure 17 – Control structures of the PCS applied to BESS approached in this work. (a) Dc/ac stage control structure for single stage PCS (T1 topology). (b) Dc/ac stage control structure for T2 and T3 topologies. (c) Dc/dc stage control for T2 and T3 topologies. (d) Dc/ac stage control structure for T4 topology. (e) Dc/dc stage control structure for T4 topology. (Source: own representation)

are the reference and the switching between them depends on the battery current (I_{bat}). This control presents explicitly the active power reference (P_n^*) calculated by an anti-windup proportional-integral (AWPI) controller, saturated in P_{max}, which is the maximum charge power. As already mentioned, the battery charging presents a constant current mode and it is achieved by saturating the active power by the following relation:

$$P^* = P_{max} = I_{ch,max} V_{bat}, \tag{4.2}$$

where $I_{ch,max}$ is the maximum charge current for CCM and V_{bat} is the measured battery voltage. The battery voltage control comes out of saturation when the boost voltage (V_{boost}) is reached and the battery current decreases slowly. The next stage is when the battery current (I_{bat}) reaches 10% of the maximum charge current. At this moment, the battery reference voltage is switched to the float voltage (V_{float}). It is possible to note that the charge and discharge switching depends on the battery SOC level or the grid service algorithm command. Furthermore, in this control strategy, the reactive power is also controlled through the power control strategy proposed in this work. The active and reactive power references are calculated through a grid service algorithm, which the description is out of the scope of this work.

- T2 and T3: For this power electronic topologies, the dc/ac stage outer loop controls the dc-link voltage, as shown in Fig. 17(b). Generally, this voltage is controlled in a constant value equal to the minimum dc-link voltage to connect the BESS to the grid, as seen previously. This voltage control is performed also using the square value base method. The reactive power is also controlled in this control structure with the reference Q^* calculate by a grid service command. The dc/dc stage control presents two loops, one for each battery bank discharge and charge mode, as shown in Fig. 17(c). For discharging, the grid service command provides the active power reference P^*. This power component is divided by the battery bank voltage (NV_{bat}), where N is the cell number of the interleaved converter. The result is the reference current (I_d) for each cell control. The PI controller is used to control the inductor current (I_{LN}) of each converter cell. There is an inner current loop for battery bank charging, similar to the discharge control loop, in which an outer voltage loop calculates the reference current (I_{ch}^*). This outer loop can control the battery bank voltage in boost and float voltage, depending on the battery current (I_{bat}). An AWPI controller with an saturation value of $I_{ch,max}$ ensures the constant current mode during charge. A grid service command provides the saturation current value.

- T4: For the dc/dc converter in series connection, the dc/ac stage outer loop controls the active and reactive power using the control strategy proposed in this work, as shown in Fig. 17(d). The discharge mode is enabled for $P^* > 0$ and the charge mode is enabled for $P^* < 0$. For this power electronics structure, each dc/dc converter

controls its output voltage ($V_{dc,k}$), and the total output voltage of all converters is the dc-link voltage. In this case, the output voltage reference ($V^*_{dc,k}$) for each dc/dc converter is given by:

$$V^*_{dc,k} = V^*_{dc}\frac{V_{bat,k}I_{bat,k}}{P^*}, \tag{4.3}$$

where k is the converter in which the V^*_{dc} is computed and C is the total number of dc/dc converters in series. V_{bat} and I_{bat} represent the battery bank voltage and current, respectively. V^*_{dc} is the total dc-link voltage reference.

Next, the details of all control tuning will be discussed and a complete description of the proposed control strategy for active and reactive power components will be approached.

4.1 Dc/ac Stage Control Modelling

4.1.1 Dc/ac Stage Current Control Modelling

The inner-loop is responsible for controlling the inductor side converter current of the LCL filter, and its modeling is an important issue. The LCL filter capacitor dynamic is neglected to simplify the plant modeling of the inner control loop. This simplification is valid since it is considering only the fundamental frequency component of the current and voltage. Applying the voltage Kirchhoff law, the model of the grid-connected dc/ac stage, in the stationary reference frame, can be represented by:

$$v_{s\alpha,\beta} - R_f i_{s\alpha,\beta} - L_f\frac{di_{\alpha,\beta}}{dt} - v_{\alpha,\beta} = 0, \tag{4.4}$$

where L_f and R_f are the equivalent inductance and equivalent series resistance of the filter, respectively. $v_{\alpha,\beta}$ and $v_{s\alpha,\beta}$ are the grid voltage and the dc/ac stage output voltage in stationary reference frame, respectively. Considering the grid voltage as a system disturbance, the plant model transfer function of the dc/ac stage current control is given by:

$$PL(s) = \frac{i_{s\alpha,\beta}(s)}{v_{s\alpha,\beta}(s)} = \frac{1}{L_f s + R_f}. \tag{4.5}$$

As already mentioned, the dc/ac stage current control is performed in a stationary reference frame, where the dc/ac stage current reference is a sinusoidal signal with grid fundamental frequency (60 Hz). In this case, the PI controller presents a steady-state error due to its limited bandwidth (Cupertino et al., 2013). Therefore, to overcome this drawback, proportional-resonant (PR) controllers have been employed (Yepes et al., 2011; Yang; Zhou; Blaabjerg, 2015). The resonant controller provides an infinite theoretical gain at the resonant frequency and reduces the steady-state error. The transfer function of the PR controller is given by:

$$G_c(s) = K_{p1} + K_r \overbrace{\frac{s}{s^2 + \omega_f^2}}^{R_f(s)}, \tag{4.6}$$

where K_{p1} is the proportional gain, ω_f are resonant frequency tuned at the fundamental frequency, K_r is the resonant gain and $R_f(s)$ is the resonant term responsible for the high gain in the frequency ω_f. K_r value can be tuned to achieve the best compromise between selective filtering and dynamic response.

On the other hand, K_{p1} has a strong effect on the fast transient response through bandwidth regulation. For high K_{p1} values, the dc/ac stage switching frequency affects the current control stability. For this reason, it is common to adopt that the open-loop crossover frequency is lower than a decade below the switching frequency. Yepes et al. (2011) provides an equation to find K_{p1} to ensure this recommendation as follow:

$$K_{p1} = \frac{R_f}{(1-\rho^{-1})\sqrt{2}} \sqrt{2 + 2\rho^{-2} - (1+\sqrt{5})\rho^{-1}}, \tag{4.7}$$

where $\rho = e^{\frac{R_f T_s}{L_f}}$ and T_s is the sampling period.

4.1.2 Power Control Modelling

If the power control block is not used in the dc/ac stage control structure, the power components are in an open loop. Although the simplicity, this approach can present steady-state error in the power components. For this reason, Cupertino and Pereira (2021) proposes the reactive power control loop that allows the control of this power component along with the V_{dc} squared value control method and stationary reference-frame in the current control. The simplified closed-loop block diagram for reactive power control is shown in Fig. 18(a). This control technique adds the measured dc/ac stage reactive power (Q) and compares it with the reference (Q^*). An integrator controller (k_i/s) processes the error between these two components and the output is added to the reference Q^*, equaling this reference to the measured component in steady-state. The result of this control loop is Q_n^* and it is used for IPT to calculate the reference currents for the inner loop.

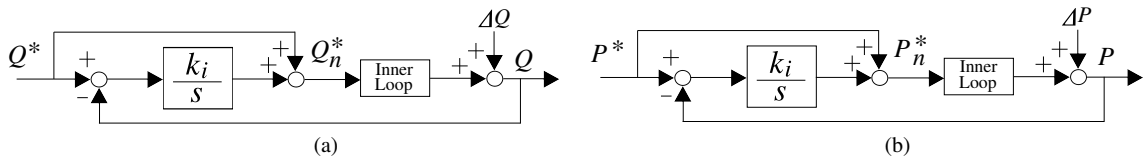


Figure 18 – Simplified closed loop block diagram of the active and reactive power controls.

This thesis expands the study of Cupertino and Pereira (2021) and applies this power control loop for the active power component, which is necessary for the control

structure of the power electronics topologies T1 and T4. This proposed active power control loop is shown in Fig. 18(b). Furthermore, this work presents an analytical study of the error in power components that may appear if the open-loop is used.

4.1.2.1 Design of the Power Controls

As can be seen in Fig. 18, both active and reactive power control loops have a similar structure. Therefore, these control loops have the same design and, consequently, stability and analytical analysis.

The inner loop is designed to be faster than outer-loop control. In such conditions, this gain of this inner loop can be approximated by 1. ΔQ and ΔP is the disturbance that causes steady-state error in the power components concerning the references. For simplicity, the Y nomenclature represents the power components in the analysis below. The output dynamic stiffness, which indicates the effect of the disturbance $\Delta Y(s)$ in the output power component Y, can be found as:

$$\frac{\Delta Y(s)}{Y(s)} = 1 + \frac{k_i}{s}. \tag{4.8}$$

This relationship describes the effect of the disturbance in the output $Y(s)$. Fig. 19 shows the dynamic stiffness magnitude concerning the frequency for range values of k_i. k_i = 0 represents the case when the power components are in open loop, presenting a poor dynamic stiffness. In this case, an unitary magnitude of ΔY causes unitary magnitude error in the output Y in all frequency spectrum. As k_i increases, the dynamic stiffness increases for $s \to 0$ and still is unitary for $s \to \infty$. Therefore, theoretically, the higher the value of k_i, the better the dynamic stiffness.

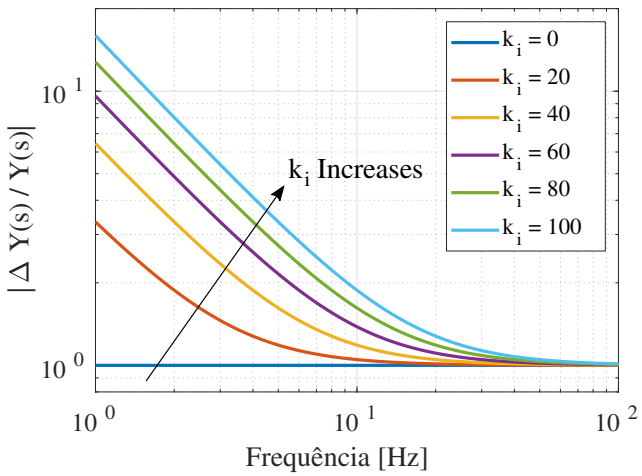


Figure 19 – Dynamic stiffness of the power loops in relation to the integrator gain k_i.

The closed loop transfer function reported in Fig. 18 is given by:

$$\frac{Y^*(s)}{Y(s)} = \frac{k_i}{s + k_i}, \tag{4.9}$$

The pole of this transfer function is:

$$\omega_c = k_i, \tag{4.10}$$

Generally, the inner-loop control is designed one decade bellow the dc/ac stage switching frequency. In order to approximate the inner-loop gain in Fig. 18 to an unitary value, the pole is placed three decades bellow the switching frequency. k_i is defined as:

$$k_i = \frac{2\pi}{1000 T_{sw}}, \tag{4.11}$$

where T_{sw} is dc/ac stage switching period.

Therefore, the control design of the power components is performed to take into account the maximum dynamic stiffness as possible, respecting the limit frequency response in relation to the inner-loop.

4.1.2.2 Error Modelling on the Active and Reactive Power

The active and reactive power errors in steady-state using the open loop approaches are mainly due to the phase or amplitude error from the current control. These errors can occur even if the current control strategy is well-tuned. For example, if the proportional-resonant (PR) controllers tuned at 60 Hz are used and the grid voltage changes the frequency due to any grid instability, the active and reactive power error arises if the open loop approach is employed. To overcome this drawback, adaptive PR controller tunning can be used (Golestan et al., 2018). However, this approach requires considerable computational time processing since the recommended discretization based on Tustin with pre-warping requires the calculation of trigonometric functions in all execution steps (Yepes et al., 2010). The second solution is to use the proposed closed loop strategies for power components control.

The error in the power components can be modeled in function of the phase and amplitude errors in the current control loops. For this purpose, considering the active (P) and reactive (Q) power components injected by the dc/ac stage given by:

$$P = \frac{3}{2}(v_\alpha i_\alpha + v_\beta i_\beta), \tag{4.12}$$

$$Q = \frac{3}{2}(v_\beta i_\alpha - v_\alpha i_\beta), \tag{4.13}$$

where $v_{\alpha\beta}$ is the grid voltage in stationary reference frame, $i_{\alpha\beta}$ is the dc/ac stage side inductor current, in the same reference frame. These voltage and current components are substituted by:

$$v_\alpha = V\cos(\omega t), \tag{4.14}$$
$$v_\beta = V\cos(\omega t - 90), \tag{4.15}$$
$$i_\alpha = (I + \Delta I)\cos(\omega t + \delta + \Delta\theta), \tag{4.16}$$
$$i_\beta = (I + \Delta I)\cos(\omega t - 90 + \delta + \Delta\theta), \tag{4.17}$$

where V is the peak value of grid phase voltage, I is the peak value of the dc/ac stage current, ΔI is the amplitude error of the current controller, $\Delta\theta$ is the phase error of the current controller and δ is the angle of the power factor (PF).

Therefore, the errors in the active and reactive power are given by, respectively:

$$\Delta P = P^* - P = \frac{3}{2}V[(I + \Delta I)\cos(\delta + \Delta\theta) - I\cos(\delta)], \tag{4.18}$$

$$\Delta Q = Q^* - Q = \frac{3}{2}V[(I + \Delta I)\sin(\delta + \Delta\theta) - I\sin(\delta)], \tag{4.19}$$

Considering the same current and voltage amplitudes, the errors depend on the PF angle, the amplitude and phase error of the current control. The errors of the power components are shown in Fig. 20 considering $V = 180\ V$, $I = 16\ A$. The errors of the power components are shown concerning the current control errors ($\Delta\theta$ and ΔI). The power factors equal to 0.707, 0 and 1 are used in this analysis.

It can be noticed that the PF has a great influence on the error plan shape between the cases. For $PF = 0.707$, the $\Delta\theta$ has the predominant influence on the error in both power components compared with ΔI. For $PF = 1$ and 0, the ΔI has a predominant influence on the error.

These analysis confirms that current control errors lead to the errors in the power components and the closed loop is important. The current control error can arise due to the frequency grid variation, discretization problems, bad control tunning, etc.

4.1.3 Dc-link Voltage Control Modelling

The dc/ac stage outer-loop control is responsible for controlling the dc-link voltage. The method based on square voltage method control is employed (Yazdani; Iravani, 2010). The control design is the same in the presence or not of the dc/dc stage. It is worth remembering that for the one stage PCS, the dc link voltage needs to be controlled in the

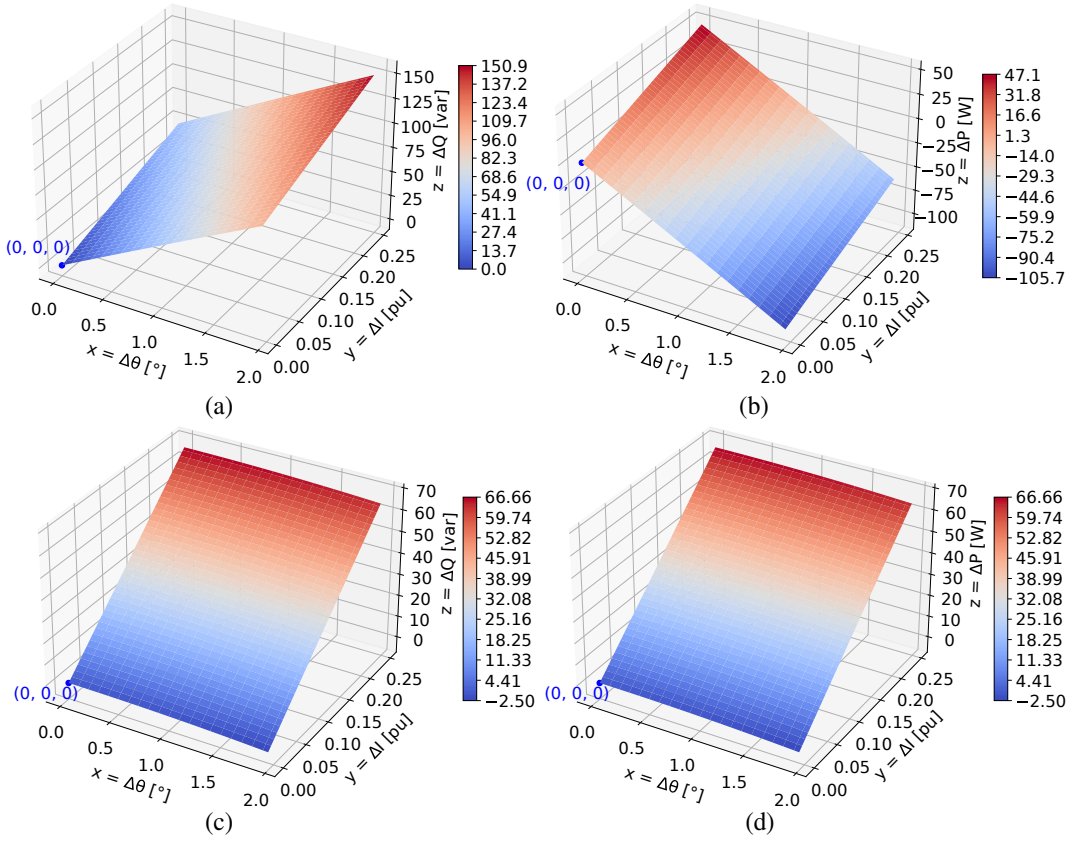


Figure 20 – Active and reactive power error in relation to the phase and amplitude errors of the current control, considering different power factors. (a) Reactive power error for PF = 0.707. (b) Active power error for PF = 0.707. (c) Reactive power error for PF close to zero 0. (d) Active power error for PF = 1.

battery charging in constant voltage mode. The stored energy W in the dc-link capacitor can be expressed as:

$$W = \frac{1}{2} C_{dc} V_{dc}^2, \tag{4.20}$$

where C_{dc} is the capacitance of the dc-link capacitor and V_{dc} is the dc-link voltage. The capacitor instantaneous power (P_C) is equal to the time derivative of the stored energy, as given by:

$$P_c(t) = \frac{dW}{dt} = \frac{1}{2} C_{dc} \frac{dy(t)}{dt}, \tag{4.21}$$

where $y(t) = V_{dc}^2$. Therefore, equation (4.20) can be replaced in equation (4.21) and expressed in the frequency domain given by:

$$P_c(s) = P_{in}(s) - P^*(s) = \frac{1}{2} C_{dc} s y(s). \tag{4.22}$$

where P_{in} is the power injected in the dc-link. When the dc/dc stage is not employed, the P_{in} is equal to the battery bank power. P^* is the control active power reference. Isolating

$y(s)$ in equation (4.22), the following relation is obtained:

$$y(s) = 2\frac{P_{in}(s) - P^*(s)}{sC_{dc}}. \tag{4.23}$$

In such conditions, considering P_{in} as a system disturbance, the plant transfer function is given by:

$$PL(s) = \frac{y(s)}{P^*(s)} = -\frac{2}{sC_{dc}}. \tag{4.24}$$

Considering a PI controller, the controller gains can be calculated by (Buso; Mattavelli, 2006):

$$K_{p2} = \frac{\omega_c \kappa}{\mid PL \mid_{\omega=\omega_c} \sqrt{1 + (\omega_c \kappa)^2}}, \tag{4.25}$$

$$K_{i2} = \frac{\omega_c}{\mid PL \mid_{\omega=\omega_c} \sqrt{1 + (\omega_c \kappa)^2}}, \tag{4.26}$$

where ω_c is the open-loop gain at the crossover angular frequency, $\mid PL \mid_{\omega=\omega_c}$ is the magnitude value at ω_c, and κ is represents the following expression:

$$\kappa = \frac{\tan\left[\frac{\pi(-ph-90+pm)}{180}\right]}{\omega_c}, \tag{4.27}$$

where $ph = \underline{/PL}_{w=w_c}$ is the phase at ω_c and pm is the open-loop phase margin.

4.2 Dc/dc Stage Control Modelling

4.2.1 Battery Voltage and Interleaved dc/dc Stage Current Controls

The schematic of the interleaved converter is shown in Fig. 21. The battery bank is assumed as an inner dc voltage source (E_o) with an internal resistance (R_{bat}). This simplified battery model is adopted to simplify the design of the dc/dc stage controller gains (Manwell et al., 2005). It is assumed that the dc/ac stage performs the dc-link voltage control, and thus this bus is represented by a dc voltage source with a fixed value in V_{dc}. Each interleaved converter cell has an inductive filter with inductance L_i and an equivalent series resistance R_i. The current flowing in the batteries is Ni_L, where N is the number of cells, and i_L is the cell current.

The average current values of each cell (I_L), duty cycle (D) and the output battery voltage (V_{bat}) are used for dc/dc stage control modelling (Erickson; Maksimovic, 2001). Therefore, the following equations can be obtained applying the voltage Kirchhoff law in the circuit shown in Fig. 21:

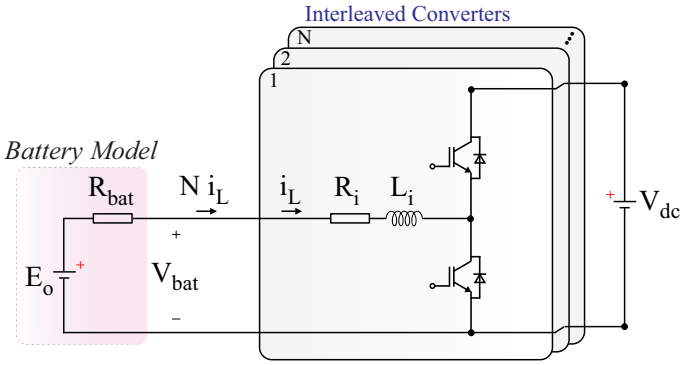


Figure 21 – Schematic of the interleaved converter. (Source: own representation)

$$V_{dc}D - R_iI_L - sL_iI_L - R_{bat}NI_L - E_o = 0, \tag{4.28}$$

$$V_{dc}D - sL_iI_L - R_iI_L - V_{bat} = 0, \tag{4.29}$$

The term E_o is neglected because this is a disturbance in the dc/dc stage control and is not a controlled variable. Furthermore, applying Laplace transformation in equation 4.28 and 4.29, the transfer function with I_L and D relationship is given by:

$$\frac{I_L(s)}{D(s)} = \frac{V_{dc}}{L_is + R_i + NR_{bat}}. \tag{4.30}$$

Isolating the $I_L(s)$ in the equation 4.28 and substituting in equation 4.29. The transfer function with $V_{bat}(s)$ and $I_L(s)$ relationship is given by:

$$\frac{V_{bat}(s)}{I_L(s)} = NR_{bat}, \tag{4.31}$$

Equation 4.30 is the plant transfer function of the dc/dc stage current control. This model and the control is the same for both battery discharging and charging process. Considering the PI controller transfer function $K_{p3} + K_{i3}/s$, the proportional (K_{p3}) and integral (K_{i3}) gains are designed for the pole of the plant transfer function to be canceled by the zero of the PI transfer function. Therefore, the PI gains of the dc/dc stage current control are given by:

$$K_{p3} = \frac{2\pi f_{ci}L_i}{V_{dc}}, \tag{4.32}$$

$$K_{i3} = \frac{2\pi f_{ci}(R_i + NR_{bat})}{V_{dc}}, \tag{4.33}$$

where f_{ci} is the pole frequency of the closed-loop transfer function. It is important to mention that for the series connection of the dc/ dc converters, V_{dc} of Eq. 4.32 and 4.33 represents the dc-link voltage divided between the K connected converters.

Equation 4.31 is the plant transfer function of the dc/dc stage voltage control during discharging process. Considering the PI controller transfer function $K_{p4} + K_{i4}/s$, the proportional (K_{p4}) and integral (K_{i4}) gains are designed by the pole and zero location of the closed-loop transfer function. Therefore, the gains are given by:

$$K_{p4} = \frac{f_{cv2}}{NR_{bat}(f_{cv1} - f_{cv2})}, \tag{4.34}$$

$$K_{i4} = 2\pi f_{cv1} K_{p4}, \tag{4.35}$$

where f_{cv1} is the zero frequency of the closed-loop transfer function and f_{cv2} is the pole frequency.

4.2.2 Dc-link Voltage Control

When dc/dc converters are connected in series, each dc/dc converter controls its output voltage. Therefore, the dc-link voltage is the total output voltage of all converters. The assumption that each dc/dc converter operates isolated from the others is adopted for control modeling simplicity, as shown in Fig. 22. Therefore, the disturbance between the converters is neglected in this control analysis.

The difference between the Fig. 21 and 22 is that the last considers the output capacitor and a output resistance R_0, representing the power demand of the system. Therefore, this is a representation of battery discharge scenario and the dc/dc converter operates step-up the battery voltage (Boost stage).

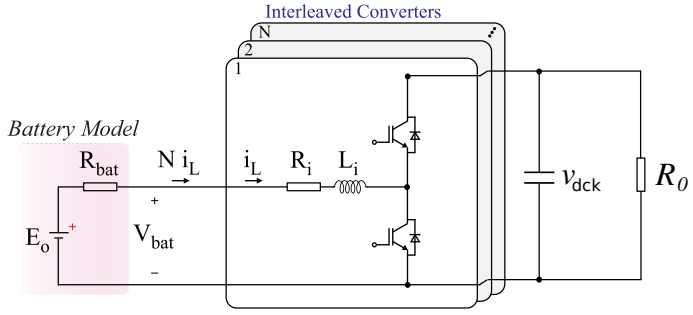


Figure 22 – Simplified system for modeling the output voltage control of the dc/dc converters for series connection. (Source: own representation)

The small signal approach (^) is used for dc/dc converter output voltage (v_{dck}) control design (Erickson; Maksimovic, 2001). This adopted methodology allows linearizing the circuit of the Fig. 22.

Through Kirchhoff current law in the output capacitor node and the small signal approach, the following relation can be obtained:

$$\frac{V_{dck}}{R_0}\hat{d} + ND\hat{i}_L = \hat{v}_{dck}(sC + \frac{1}{R_0}), \tag{4.36}$$

where V_{dck} is the quiescent value of the output voltage, D is the quiescent values of the duty cycle and C is the capacitance of the output capacitor. Furthermore, the following equation can be obtained applying the voltage Kirchhoff law in the circuit shown in Fig. 22.

$$-(L_i s + R_i + NR_{bat})\hat{i}_L - V_{dck}\hat{d} - D\hat{v}_{dck} = 0. \tag{4.37}$$

Isolating $\hat{d}$ in Eq. 4.37, substituting it in Eq. 4.36 and performing mathematical manipulations the following transfer function can be obtained:

$$PL(s) = \frac{\hat{v}_{dck}(s)}{\hat{i}_L(s)} = -\frac{L_i s + R_i + N(R_{bat} - DR_0)}{R_0 C s + D + 1}. \tag{4.38}$$

The above equation is the plant transfer function which relates the output voltage and inductor current of each N cell of the interleaves converter. R_0 can be substituted by:

$$R_0 = \frac{V_{dck}^2}{P_k}, \tag{4.39}$$

where P_k is the processed by each dc/dc converter. In such conditions, considering a PI controller, the controller gains can be calculated by (Buso; Mattavelli, 2006):

$$K_{p5} = \frac{\omega_c \kappa}{\mid PL \mid_{\omega=\omega_c} \sqrt{1 + (\omega_c \kappa)^2}}, \tag{4.40}$$

$$K_{i5} = \frac{\omega_c}{\mid PL \mid_{\omega=\omega_c} \sqrt{1 + (\omega_c \kappa)^2}}, \tag{4.41}$$

where ω_c is the open-loop gain at the crossover angular frequency, $\mid PL \mid_{\omega=\omega_c}$ is the magnitude value at ω_c, and κ is represents the following expression:

$$\kappa = \frac{\tan\left[\frac{\pi(-ph-90+pm)}{180}\right]}{\omega_c}, \tag{4.42}$$

where $ph = \underline{/PL}_{w=w_c}$ is the phase at ω_c and pm is the open-loop phase margin.

4.3 Chapter Conclusions

In this chapter, the main control structure design was presented. The control of all converters was modeled and all necessary gains for the operation of all PC topologies studied in this work were found.

In addition, the power control loop for the dc/ac stage proposed in this work was presented. The steady-state error of the active and reactive powers was modeled and direct dependence of the phase and amplitude error of the current control and the power factor was verified. The validation of this power control loop will be shown in the experimental results.

5 Case Study and Simulation Analysis

In this chapter, a case study is carried out in a simulation environment to compare some PCS topologies for BESS within the design context described in the previous chapters. First, the description of the power electronics structure and control parameters are presented, followed by the efficiency results and cost analysis.

5.1 Description

PCS topologies T1, T2, T3 and T4, shown in Fig. 23, are evaluated in a BESS with power 100 kW and energy 100 kWh in 1C discharge rate. They are simulated using PLECS software to analyze their advantages and disadvantages. Besides, the results are analyzed considering the PCS design for BESS oriented toward voltage class and efficiency. The T2 PCS has an interleaved dc/dc stage with three cells ($N = 3$), and T3 and T4 PCSs has two interleaved dc/dc stages ($K = 2$) with three cells. The dc/dc converters are connected in parallel (T3) and in series (T4). The interleaved dc/dc and dc/ac stage switching frequencies are 12 kH and 6 kHz, respectively.

12 V lead-acid batteries are used, where the main voltage parameters can be seen in Tab. 2. Three batteries charges are used: 60 Ah, 95 Ah and 120 Ah. The BESS is connected to a 690 V grid, hence the minimum dc-link voltage is 1015 V, as shown in Fig. 14. Therefore, the dc-link voltage is controlled at this value when the the dc/dc converter is employed. In all case, the minimum admissible battery SOC during discharge is 20%.

Table 2 – Voltage Parameters for simulated lead-acid battery. (Source: own representation)

Parameter	Value
V_{nom}	12 V
V_{boost}	14.4 V
V_{float}	13.6 V
R_{bat}	5.2 mΩ

The simulation is based on discharging the battery bank at 1C rate, keeping the current in the batteries fixed until the SOC reaches 20 %. After that, the battery bank is charged using the stages described in chapter 2.

The battery charge and arrangement are determined to have the minimum dc/dc converter duty cycle, which ensures the operation close to the maximum efficiency (Erickson; Maksimovic, 2001). Therefore, the battery bank is arranged to have the charge boost voltage close to the dc-link voltage. The battery bank arrangement for each PCS topology is shown in Fig. 23. For topology T1, 88 batteries of 95 Ah are connected in series. This

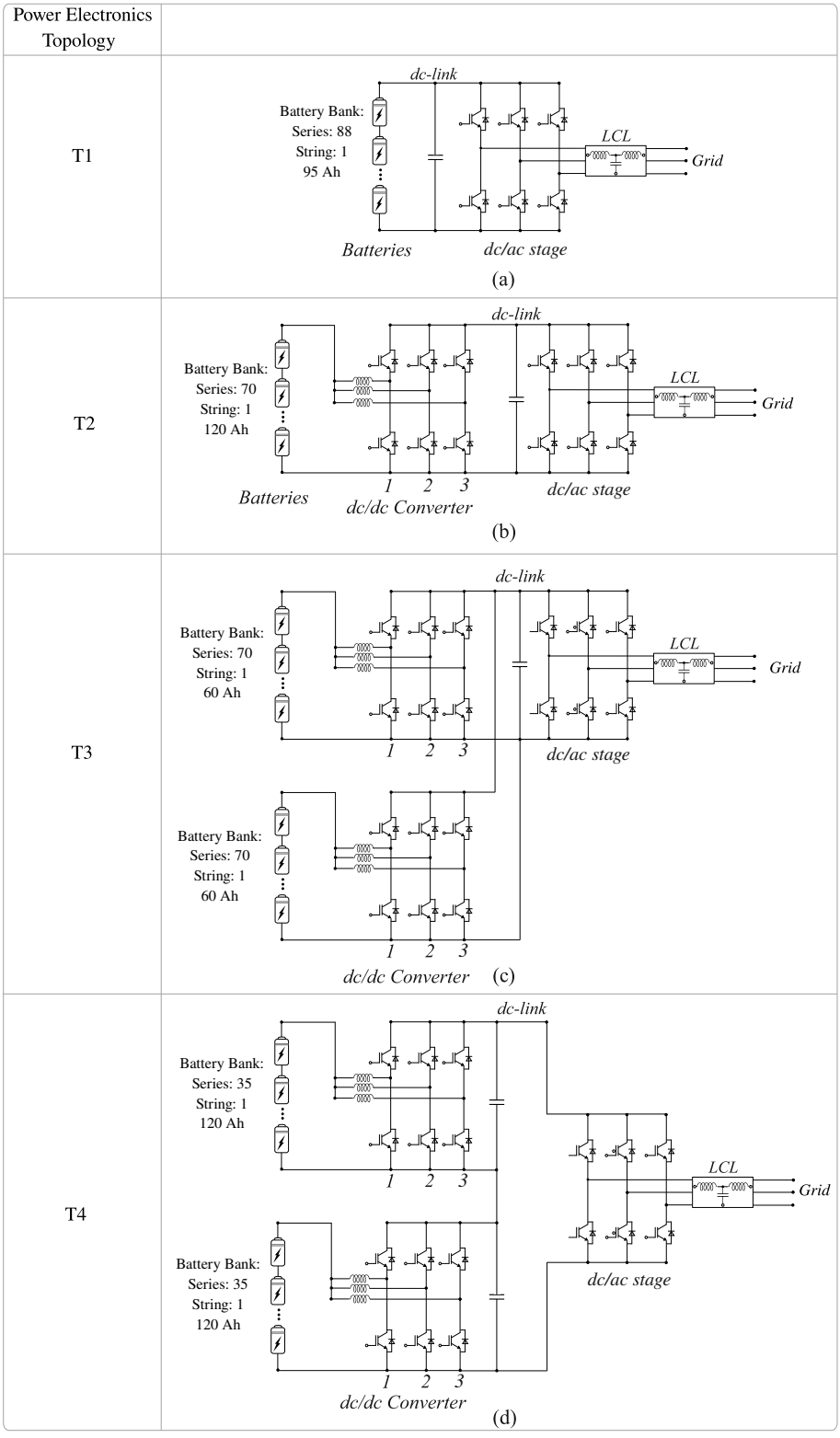


Figure 23 – PCS and power electronics topologies for BESS compared in this work. (Source: own representation)

connection ensures the minimum dc-link voltage (1015 V) in SOC level equal to 20% during the discharge process. For topologies with dc/dc converters, which is the case of T2, T3 and T4, the number of batteries in series is determined to have the minimum

dc-link voltage during boost voltage, ensuring the minimum duty cycle operation. Despite the difference between the number of batteries and their capacity, all systems have 100 kWh, as mentioned previously. The number of batteries and the charge of each one are depended on the configuration of the dc/dc converters. For example, as can be seen, the series connection of the dc/dc converter (T4) requires fewer batteries in series, requiring a higher battery capacity to maintain the same design energy and power, as shown in Fig. 23.

The inductor of each dc/dc converter cell is designed to achieve the same relative value of the inductor current ripple for all PCSs topologies equal to 15% at the nominal operation. The dc inductance and its series equivalent resistance are shown in Tab. 3. The dc inductor physical design for the dc/dc converters is performed using the inductor design tool provided by the manufacturer Magnetics (Magnetics, 2019). The part number of the used Magnetics inductor core, the equivalent series resistance and the number of turns of the inductor are shown in Tab. 3. The Steinmetz parameters for the designed inductor core can be found in Magnetics datasheets.

Table 3 – PCS parameters of the 100 kWh BESS. (Source: own representation)

PCS Topology	LCL Inductance (X/R)	LCL Core Part Number	Number of Turns of the LCL Inductor	LCL Capacitance (ESR)	Dc-link Capacitance Part Number
T1, T2, T3, T4	0.87 mH (17.5 Ω)	58165A2	82	14.5 μF 0.02 Ω	3 mF B43700
PCS Topology	**Dc/ac IGBT Module Part Number**	**Dc/dc IGBT Module Part Number**	**Dc Inductance (R)**	**Dc Inductor Core Part Number**	**Number of Turns of the dc Inductor**
T1	FF200R33KF2C	∄	∄	∄	∄
T2	FF225R17ME4P	FF225R17ME4P	2 mH (64.27 mH)	58165A2	195
T3	FF225R17ME4P	FF150R17ME3G	4 mH (157.66 mH)	58165A2	255
T4	FF225R17ME4P	FF225R17ME4P	1 mH (40.09 mH)	58165A2	128

The IGBT module data for the dc/ac and dc/dc converter are from Infineon. The chosen modules take into account the blocking voltage requirement, analyzed previously, and the maximum junction temperature for safe device operation. For 690 V grid voltage, the module voltage class for the dc/ac module is 3300 V without dc/dc stage, as shown in Fig. 14. However, the used IGBT module voltage class for dc/ac power module can be reduced to 1700 V when dc/dc stage is employed. The part number of the IGBT modules presents the information of the voltage and current. For example, the module FF200R33KF2C presents the nominal current of 200 A and voltage equal to 3300 V. Although the current provided by the part number is nominal, this value is for specific datasheet operation conditions. These modules were selected and verified if the semiconductor junction temperature is within the limits established by the datasheet.

Generaly, the dc-link capacitance is designed to attend the voltage ripple criteria. However, in practice its common to use higher capacitance due to non-ideality of electrolytic

capacitors around the dc/ac stage switching frequency range (Wang et al., 2020), which makes it difficult to control the dc-link voltage. Therefore, the total dc-link capacitance of 3 mF is adopted for all studied PCS topologies in this chapter. This value is commonly used for this BESS power range (Patsios et al., 2016). Nine electrolytic capacitors are used to form the dc-link with three connected in series and three strings, the data from TDK capacitor manufacturer are used to compute the power losses, and the capacitor part number is shown in Tab. 3.

The LCL filter inductors and capacitors are designed following the guideline described in Peña-Alzola et al. (2014). This guideline considers the minimum admissible value of the total harmonic distortion (THD) of the dc/ac stage injected current and the filter power factor. The current THD is set to 0.73% for 0.5 pu of the nominal active power and the filter power factor to 0.99. Therefore, both grid and dc/ac stage side inductor is 0.87 mH, and the filter capacitance is 14.5 μF. The film capacitor data from TDK manufacturer are used, which the capacitor part number is shown in Tab. 3. The ac inductor physical design for the LCL filter is performed using the algorithm proposed in Cota (2016). The part number of the used Magnetics inductor core, the equivalent series resistance and the number of turns of the inductor conductor are shown in Tab. 3.

The PCS controller gains are shown in Tab. 4. The PR gains of the dc/ac stage current control are designed to achieve the open-loop crossover frequency lower than one decade below the switching frequency (6 kHz). The dc-link PI controller gains are calculated to obtain the open-loop crossover frequency lower than a decade below the switching frequency and a phase margin equal to 60°. The PI gains of the dc/dc converter current control are designed to achieve the open-loop crossover frequency lower than a decade below the switching frequency (12 kHz). The PI gains of the battery voltage control are obtained placing the zero of the closed-loop transfer function in 20 Hz and the pole in 1 Hz, using the controller gains equations shown in the control modeling section.

The simulation is based on discharging the battery bank at 1C rate keeping the current in the batteries fixed until the SOC reaches 20%. After that, the battery bank is initially charged by the CCM and then by the CVM when the battery bank voltage reaches the boost voltage. It is important to mention that the dc/dc converters of the systems T3, T5 and T6 are designed to operate in the same duty cycle range. The efficiency of the PCSs is computed as a function of the battery bank SOC during discharge and charge process. Furthermore, the power losses are disregarded to identify the element that most affects the system efficiency.

The parameters required to calculate the cost of each PCS topology are shown in Tab. 5. All these parameters are required by the cost equations shown in Chapter 3.

Table 4 – PCS controller gains. (Source: own representation)

PCS Topology	dc/ac stage Current Control Gains (PR)	Dc-link Voltage Control Gains (PI)	Dc/dc Converter Current Control Gains (PI)	Dc/dc Converter Voltage Control Gains (PI)
T1	$K_{p1} = 6.5$ $K_r = 2000$	$K_{p2} = 0.49$ $K_{i2} = 106.59$	∄	∄
T3	$K_{p1} = 6.5$ $K_r = 2000$	$K_{p2} = 0.49$ $K_{i2} = 106.59$	$K_{p3} = 0.017$ $K_{i3} = 2.69$	$K_{p4} = 0.15$ $K_{i4} = 19.27$
T5	$0.87\ mH$ (17.5 Ω)	$K_{p2} = 0.49$ $K_{i2} = 106.59$	$K_{p3} = 0.017$ $K_{i3} = 5.24$	$K_{p4} = 0.077$ $K_{i4} = 9.64$
T6	$0.87\ mH$ (17.5 Ω)	$K_{p2} = 0.49$ $K_{i2} = 106.59$	$K_{p3} = 0,034$ $K_{i3} = 2.83$	$K_{p4} = 0.31$ $K_{i4} = 38.54$

Table 5 – Physical parameters for PCS cost estimation. (Source: own representation)

Parameters	T1	T2	T3	T4
dc IGBT module $N_{semi}/V_{block}/I_{nom}$	∄	12/1700V/225A	24/1700V/150A	24/1700V/225A
ac IGBT module $N_{semi}/V_{block}/I_{nom}$	12/3300V/200A	12/1700V/225A	12/1700V/225A	12/1700V/225A
dc inductor $A_p\ [m^4]/N_{ind}$	∄	$7.89 \times 10^{-6}/3$	$7.89 \times 10^{-6}/6$	$7.89 \times 10^{-6}/6$
Ac inductor $A_p\ [m^4]/N_{ind}$	$7.89 \times 10^{-6}/6$	$7.89 \times 10^{-6}/6$	$7.89 \times 10^{-6}/6$	$7.89 \times 10^{-6}/6$
dc electrolytic capacitor Capacitance $[mF]$/Number of capacitor	3/9	3/9	3/9	3/9
ac film capacitor Capacitance $[\mu F]$/Number of capacitor	14.5/3	14.5/3	14.5/3	14.5/3

5.2 Simulation Results

The PCS efficiency and battery SOC relationship, during discharge mode in 1C rate, are shown in Fig. 24(a). The T3 presents the highest efficiency, around 94 % even with a higher number of power electronic components in relation to the topology T1. It can be noted that in the discharge process, there is no significant efficiency difference between the PCS T1, T2 and T4 topologies.

The efficiency and battery SOC relationship during the charging process is shown in Fig. 24(b). It is worth noting that the battery charge is usually carried out below the system rated power. The topology T3 still presented the higher efficiency, around 95%. T2 and T4 presented similar efficiency, around 94% and T1 presented the lower efficiency, around 92%. The T1 topology presents a considerable variation in efficiency during a battery operating cycle, even presenting fewer power electronic components.

In this case, the smaller number of electronic components does not affect the efficiency of the T1 topology in comparison to the others. This is because the 3.3 kV dc/ac converter power switches present higher power losses for operation below the rated power. In this case, the PCS topologies with dc/dc stages (T2, T3 and T4) are more efficient than T1 during the battery charge process, since 1.7 kV power switches are used in both the dc/ac and dc/dc converters.

The global efficiency index presented in Eq. 3.14 is applied to each PCS topology during the discharge and charge cycle covered in this case study. This index is based on

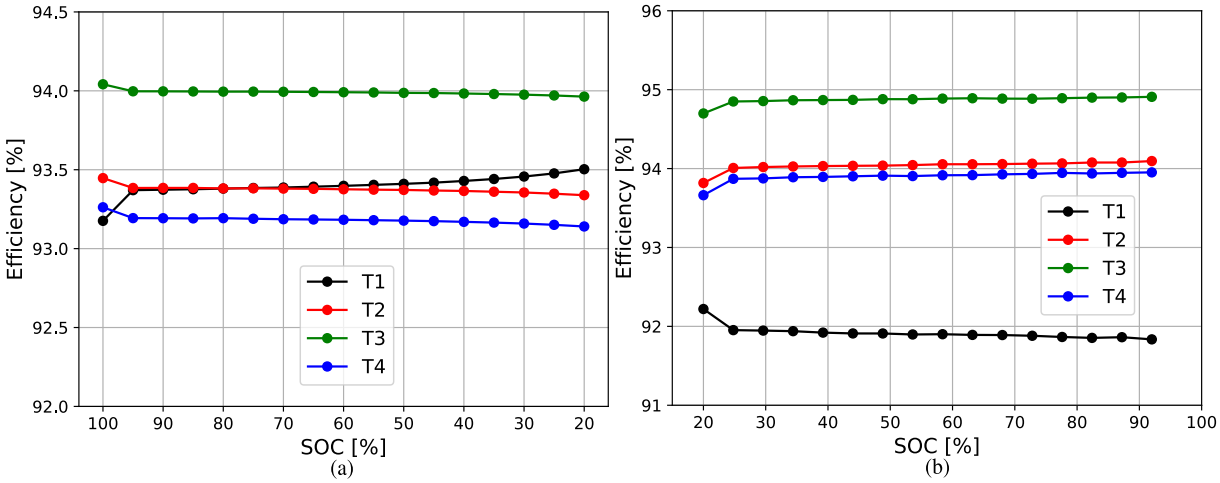


Figure 24 – PCS efficiency and the battery SOC relationship. (a) Discharge process with 1 C rate. (b) Charge process. (Source: own representation)

energy and it is important to verify the system overall performance, since the traditional efficiency calculation shows different behaviors during the discharge and charge process, as shown in Fig. 24. Tab. 6 shows this index for each topology, and it can be noted that the T3 presents the higher global efficiency index and T1 presents the lower global efficiency.

Table 6 – Global efficiency index of each PCS topologies. (Source: own representation)

Topology	Global Efficiency Index
T1	92.62 %
T2	93.69 %
T3	94.42 %
T4	93.52 %

Efficiency maps are used to relate the system operating power and the battery bank SOC. This analysis aims to have a better overview of the performance of the PCS topologies. The efficiency maps for all topologies are shown in Fig. 25. It can be seen that T1 presents a greater efficiency variation with the power and battery SOC variations. This behavior can be noticed by the various color transitions in the efficiency map, as shown in Fig. 25(a) and Fig. 25(b) for battery discharging and charging, respectively. The maximum efficiency achieved for this topology, in this case, is 93.5, approximately. The area of maximum efficiency is for powers above 0.7 pu and battery SOC below the 90%, during discharging. The lowest power region for the T1 occurs in the battery charging and this is the lowest efficient region among all topologies. This fact shows that the used 3.3 kV dc/ac stage power module has low efficiency for powers below the nominal.

The efficiency maps for T2 topology are shown in Fig. 25(c) and Fig 25(d) for battery discharging and charging, respectively. The use of the power switches of 1.7 kV in the dc/ac stage, increases the switch utilization even including more power switches with

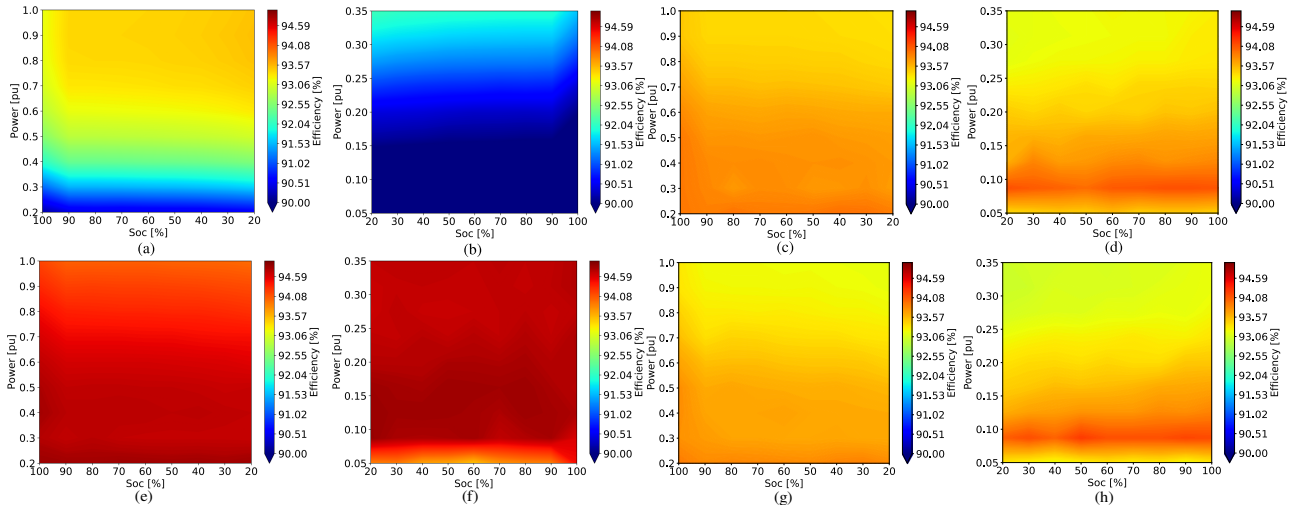


Figure 25 – Efficiency map of the PCS topologies. (a) Battery discharge for T1 topology. (b) Battery charge for T1 topology. (c) Discharge for T2 topology. (d) Charge for T2 topology. (e) Discharge for T3 topology. (f) Charge for T3 topology. (g) Discharge for T4 topology. (h) Charge for T4 topology.

the dc/dc stage presence.

The efficiency maps for T3 topology are shown in Fig. 25(e) and Fig. 25(f) for discharging and charging, respectively. In this case, a low variation of the T3 efficiency can be seen. In this case, of all the configurations, this is the one with the highest switch utilization. This topology presents a homogeneous efficiency and above 94% for most of the power and SOC operating points.

The efficiency maps for T4 topology are shown in Fig. 25(g) and Fig. 25(h) for discharging and charging, respectively. In this case, T4 presents the second lowest efficiency map. In chapter 3, two scenarios were presented, the first in which the switch utilization of T4 is better than T3 and the second the opposite. In this case study, the second scenario occurs, since, for the system power of 100 kWh, a large number of batteries is required. Therefore, it is not feasible to use the same battery charge and the same amount in T4 concerning T3, since the total battery voltage exceeds the dc/dc converter output in T4. To overcome this drawback, the number of batteries is reduced in T4 and the current is increased, canceling out the switching utilization improvement that T4 could provide compared to T3.

The cost estimation for each PCS topology is shown in Fig. 26. The cost is presented per unit with T4 cost as the base (topology with higher cost). The T1 topology presents the lowest cost, being the most part due to the dc/ac stage semiconductor device followed by the ac inductors. The T2 cost is higher than T1 by 0.2 pu, approximately. The T3 cost is higher than T1 by 0.4 pu, approximately. Finally T4 has a cost of 0.1 pu higher than T3. Although the battery charges between the topologies are different, the required number of

battery difference for each topology makes the battery bank cost similar.

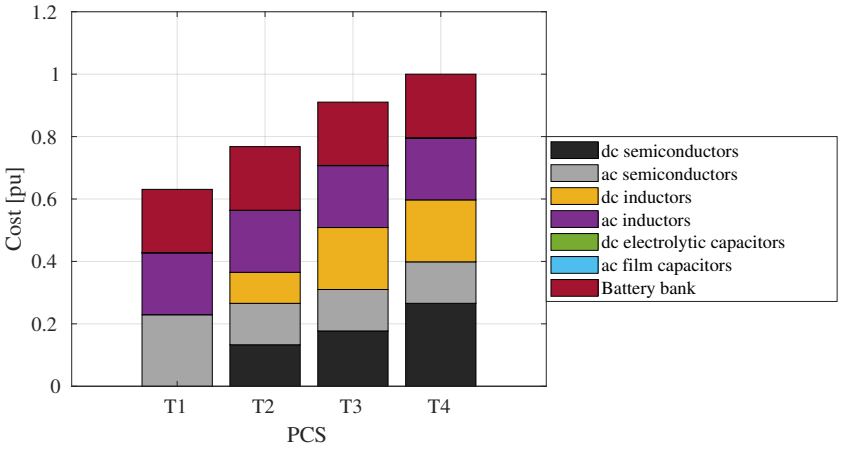


Figure 26 – Cost estimation for each PCS topology. (Source: own representation)

Considering the number of charge/discharge cycles equal to 3000 and the nominal energy of 100 kWh and taking into account the global efficiency index, the LCOS value for each PCS topology is shown in Tab. 7. It can be noted that the T1 topology has the lowest value, even having a lower global efficiency index. The LCOS value follows the same trend to the initial cost. One important point is that the T3 and T4 presents the same number of semiconductors, however, the LCOS value of T4 is higher than T3 due to presence of semiconductors of higher currents, increasing the initial cost of T3.

Table 7 – Estimated levelized cost of storage for the PCS topologies. (Source: own representation)

Topology	LCOS [USD/kWh]
T1	0.2745
T2	0.3303
T3	0.3886
T4	0.4309

5.2.1 Overview Comparison

An overview of the PCS comparison through the parameters is shown in Fig. 27. It can be seen that the global efficiency is approximately equal among the topologies, even with the topology T1 presenting fewer semiconductors and inductors. This can be explained, in this case, due to the higher dc-link voltage in T1 than T2, T3 and T4, and this requires a higher dc/ac stage converter IGBT voltage class for the first topology. Concerning the cost, the T1 is the smallest followed by T2 and T3 topologies. T4 topology presents a higher cost in this case due to the number of higher current power switches. The LCOS for the T1 topology presents the better results, and it can be conclude that even with the lowest global efficiency, the initial costs of this topology still compensates this disadvantage.

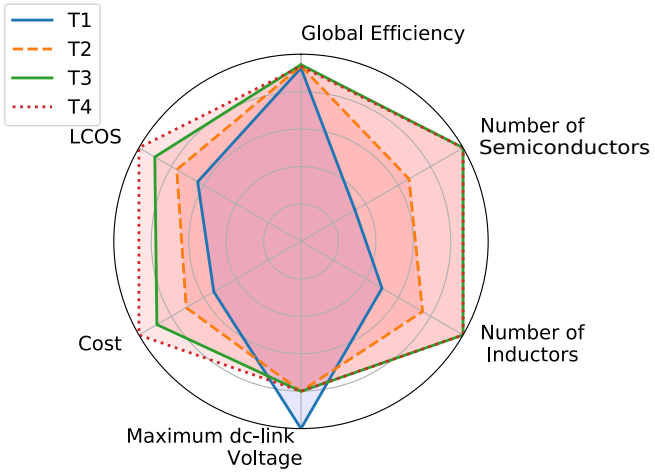


Figure 27 – Overview of the PCS comparison for BESS application. (Source: own representation)

It is worth mentioning that this PCS cost study is a simple estimation. The main costs inherent to the PCS for the BESS application were modeled, but due to each project particularities and market factors, there may be additional costs not modeled in this analysis.

5.3 Chapter Conclusions

This chapter presented a case study to verify the influence of the battery operation point variation on the PCS design and efficiency and compare four topologies for BESS. In this case, the PCS with two dc/dc converter in parallel connection present the higher efficiency, while the PCS without dc/dc converter present the lower efficiency. This can be explained by the use of power switches with a higher voltage class for the single stage converter due to the higher voltage variation of the battery bank. Nonetheless, this last PCS topology presented the lowest levelized cost of storage value based on simplified methodology.

When analyzing the global efficiency, it is clear that the use of more power switches to compose two-stage converters does not always result in lower efficiency compared to single stage converters. The proposed efficiency maps show, in this case, that the two stage converter presents a low efficiency variation with the variation of the operating point of the battery bank, while the PCS with only the dc/ac converter presents a high efficiency variation.

The estimated initial cost analysis showed that the single stage PCS had the lowest cost. It can be seen that the increment of a dc/dc converter can increasing the system cost of 0.2 *pu*. This work shows that in terms of initial costs, the topology with only the dc/ac converter can be interesting. However, this converter will not always present a

greater efficiency due to the variation of battery voltage, requiring a higher voltage class of semiconductor devices for this PCS configuration. Using dc/dc converters, the initial cost can be higher. However, it is a converter that does not have its efficiency affected by the variation in the operating point of the batteries, in addition to requiring fewer batteries in series, which reduces the battery balancing circuits. In the presented case study, the PCS topology with dc/dc converters in parallel connection is an interesting solution.

6 Experimental Bench

6.1 Introduction

This chapter presents the experimental results of the efficiency comparison between the PCS topologies based on dc/dc converters in parallel and series. Futhermore, the results of the power controls for BESS are presented. These results are obtained through a 6 kW test bench developed in this work and inserted in the R&D project D722, "Análise de Arranjo Técnico e Comercial baseado em uma Planta Piloto de Sistema Distribuído de Armazenamento de Energia em Alimentador Crítico da Rede de Distribuição de 13,8 kV".

6.2 Power Structure

The test bench overview and the power structure schematic of the BESS are shown in Fig. 28. This system is formed by two pairs of dc/ac and dc/dc stages, and the last one they are composed of interleaved dc/dc converters with three cells. The dc/ac stages are responsible for interfacing with the grid, and the dc/dc converters connect the batteries to the dc/ac stages. This system is designed to allow different connections between the dc/dc and dc/ac stages.

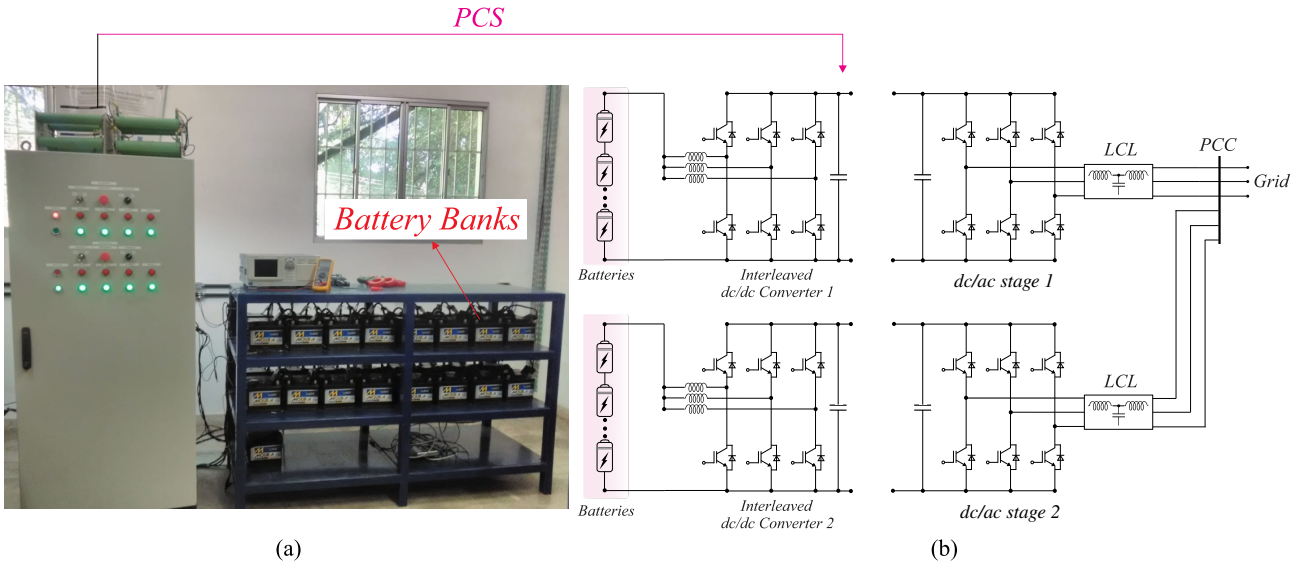


Figure 28 – BESS test bench. (a) Structure Overview. (b) PCS schematic . (Source: own representation)

The dc/dc converters can be connected in parallel or series. The advantage of the series connection is the voltage sum of the two converters, reducing the duty cycle. Thus,

when the battery bank has a low voltage in relation to the minimum voltage required on the dc/dc link, the option is to use the series connection. Otherwise, the parallel connection is commonly used due to the control simplicity. Each dc/dc converter consists of an interleaved converter with three cells, reducing the current ripple in the batteries, allowing a reduction in the input inductors filtering requirements, directly affecting their volume and cost.

Four Semikron B6CI+B1CI+B6U power modules (stacks) are used to assemble the BESS (SEMIKRON, 2008). Each module comprises four branches, each one with two IGBTs, and its maximum RMS current is 50 A, and the maximum blocking voltage equal to 1200 V. Four B43875A5478 electrolytic capacitors compose the dc bus with two connected in series in two strings. This capacitor array totals a capacitance of 4700 μ F and the maximum voltage equal to 900 V. With this power structure it is possible to assemble two three-phase dc/ac stages and two three-phase interleaved dc/dc converters. Fig. 29(a) shows the power electronics structures used in the BESS experimental test. It is possible to see the four SEMIKRON modules, the inductors and capacitors.

This chapter presents the evaluation of the T3 and T4 topologies, as shown in Fig. 29(b). Only one dc/ac stage of the experimental bench is used. The focus of this work is on the dc/dc stage arrangements. In the T3 topology, two dc/dc converters are connected in parallel in the same dc-link with one grid-connected dc/ac stage. Each dc/dc converter presents 16 lead-acid batteries connected in series, forming two independent battery banks. The batteries are from Moura manufactures and the part number is 12MN36. The battery main parameters can be seen in Tab. 8. T4 topology presents two dc/dc converters connected in series with the same battery bank of T3 in each converter. This case represents the scenario one described in Chapter 3 where the battery bank configuration and the battery charge for T4 are the same as T3. This battery bank can be adopted in T4 because the maximum battery bank voltage is smaller than the output voltage, even adding the output voltage of the converters. In this scenario, there is an improvement of switching utilization and step-up ratio decrease when using topology T4.

The dc/ac and dc/dc stages switching frequencies are both $9kHz$, respectively. However, it is worth noting that the phases between the triangular carriers of each dc/dc converter cell in the PWM algorithm are displaced by 120 degrees. Therefore, the apparent switching frequency of the dc/dc converter is 27 kHz. This fact is important to reduce the ripple in the current in the batteries and the converter output current.

The LCL filters are used to attenuate the harmonic orders due to the switching frequency in the injected current into the grid. The grid and dc/ac stage side inductors present inductance equal to 1 mH. The LCL capacitance is 25 μF with damping resistors equal to 1.8 Ω. The filter resonant frequency is 1.43 kHz and the gain at 9 kHz is -64.3 dB. The inductors of the interleaved dc/dc converters present the inductance equal to

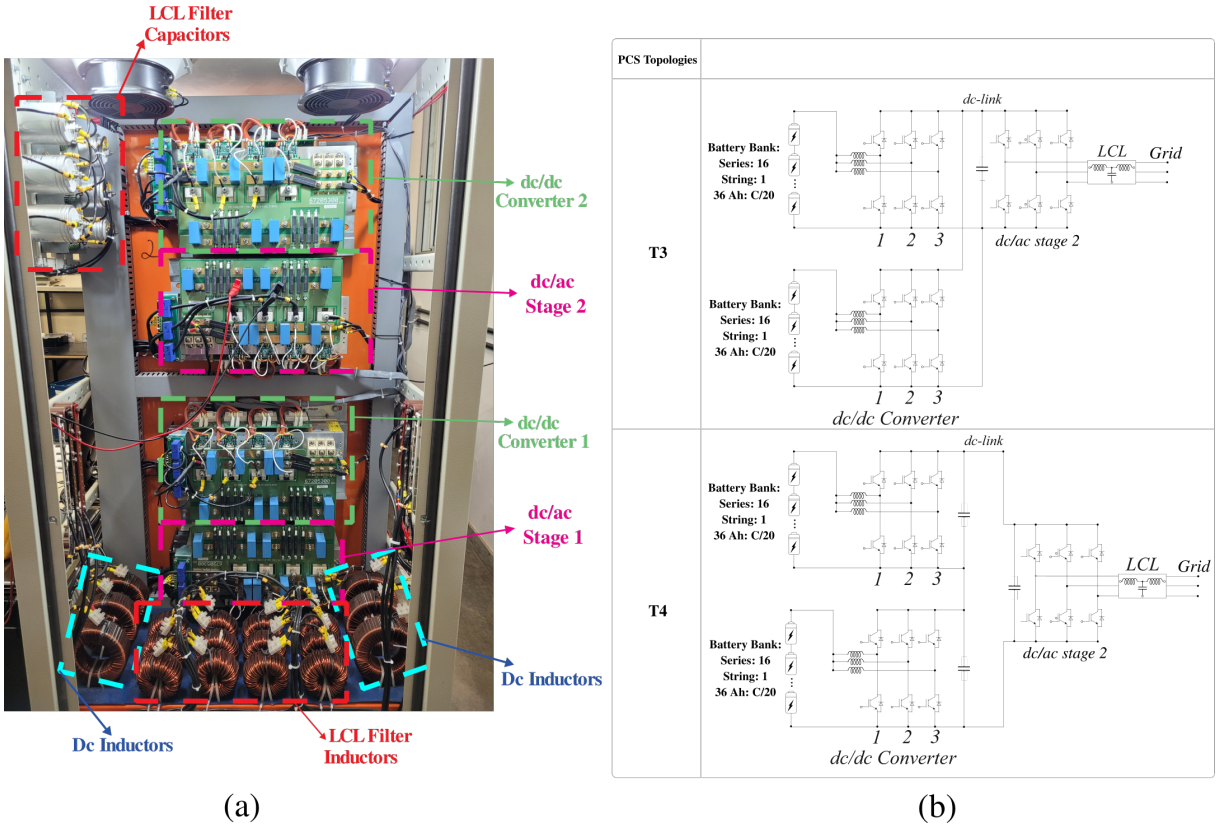


Figure 29 – Power electronics structure overview. (a) Devices of the experimental bench. (b) PCS topologies compared in the experimental test. (Source: own representation)

Table 8 – BESS test bench main parameters. (Source: own representation)

PCS Parameters	Values
Dc/dc converter inductance	4 mH
Dc/dc converter switching frequency	9 kHz
Dc/ac stage switching frequency	9 kHz
Number of interleaved dc/dc converter cells	3
Grid and dc/ac stage side LCL filter inductance	1 mH
Capacitance of each module	4.7 mF
LCL filter capacitance	25 μF
LCL filter damping resistance	1.8 Ω
Grid voltage (RMS)	220 V
Grid frequency	60 Hz
Dc-link voltage	500 V
Nominal current (RMS)	16 A
Battery Parameters	**Value**
Rated Capacity (C/20)	36 Ah
V_{nom}	12 V
V_{boost}	14.4
V_{float}	13.6 V
R_{bat}	7.2 Ω
Maximum charge current	7.2 A

4 mH in each cell. These passives components can be seen in Fig. 29. Tab. 8 shows the BESS test bench main parameters.

6.3 Control System

Two dual core TMDSDOCK28379D kits with the DSP F28379D from Texas Instruments manufacturer are used to implement the system control. The schematic of the division of DSPs and cores is shown in Fig. 30. The CPU 1 and 2 of the DSP 1 controls the dc/ac stage and one dc/dc converter, respectively. CPU 2 of the DSP 2 controls the second dc/dc converter. These two DSPs communicate through UART protocol. This communication is used mainly for series dc/dc converter control.

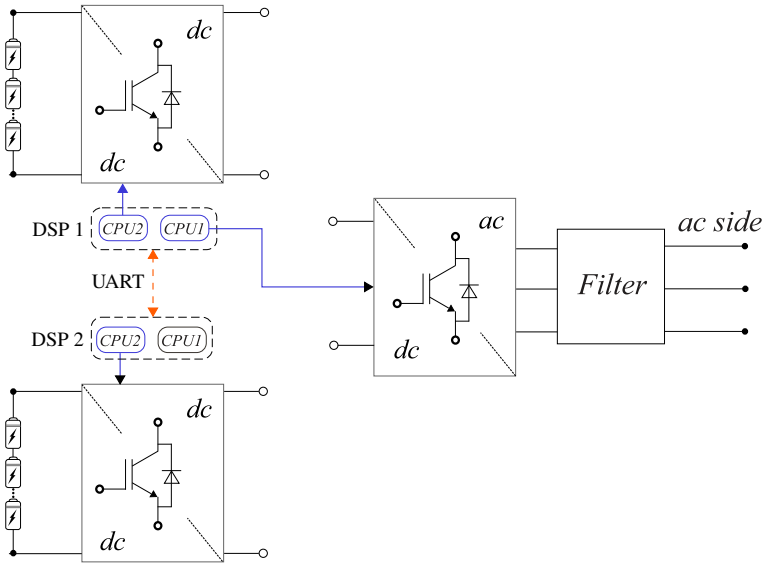


Figure 30 – Schematic of the division of DSP cores between converters. (Source: own representation)

Modular conditioning boards are used to convert and adjust the power system voltage levels to the DSP voltage level, and the system is divided in sub-boards (Cupertino, 2015):

- Relay drive board: This conditioning board intends to control auxiliary relays to open or close the BESS test bench switching contactors. The module can drive up to eight low-power relays;
- Digital inputs board: This board is used to condition the DSP digital inputs, important to check the status of the contactors;
- Digital Outputs board: It has a function similar to the relay drive board, which can be used to analyze the code routine execution time (sampling) or activate other devices incorporated in the bench;
- Analog input board: One of the most important boards of the signal conditioning system is that this board is designed to condition the sensor signals (current and

voltage) to the DSP analog input specifications and the system requirements. Each module has an input for eight sensors;

- PWM board: Another fundamental conditioning board of the system is the PWM board, responsible for activating the converters' switches, being the actuator of the control. The PWM module of the acquisition system is designed for the SEMIKRON SKHI22BH4 Gate Drivers circuits. The module can control up to six arms of IGBT and a protection chopper, making it possible to control up to two three-phase converters, being ideal for the BESS test bench applications.

Each dc/ac and dc/dc stage group has a DSP kit and its conditioning system to receive the sensor signals, to perform the control and actuation on the plant, as shown in Fig. 31.

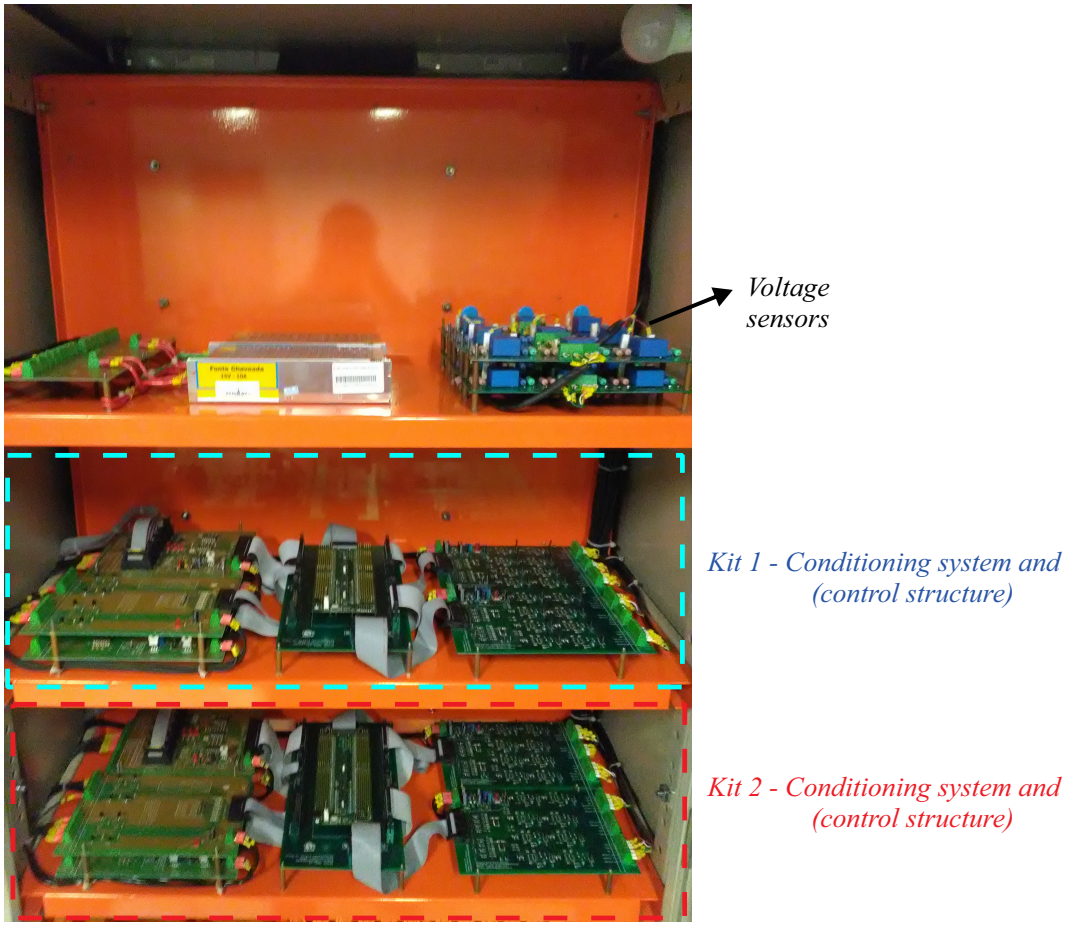


Figure 31 – Signal conditioning system and control structure. (Source: own representation)

6.4 Control Tuning

As already mentioned in the previous chapters, the control strategy must meet the battery charge and discharge requirements. The battery recharge cycle consists of

the CCM and VCM. The control strategies adopted in the BESS experimental bench are similar to the strategies seen in Chapter 4.

The dc/ac stage current inner control loop is designed to track the fundamental component and reject disturbances of the harmonic components present in the grid voltage. Hence, a proportional multi-resonant controller is used, whose open-loop Bode diagram is shown in Fig. 32(a). It is possible to verify that the loop has a high gain and zero phase displacement in the 60 Hz, 300 Hz and 720 Hz components. As can be seen, additional resonant controllers tuned to the fifth and seventh harmonic frequencies were placed in the control of the experiment bench due to the presence of these frequencies in the grid voltage at the system installation site. In this way, it is possible to increase the dynamic stiffness of the control at these frequencies. The loop bandwidth is 900 Hz, a decade below the dc/ac stage switching frequency. This approach allows neglecting the delay in the dc/ac stage actuation since it is much faster than the current control loop action.

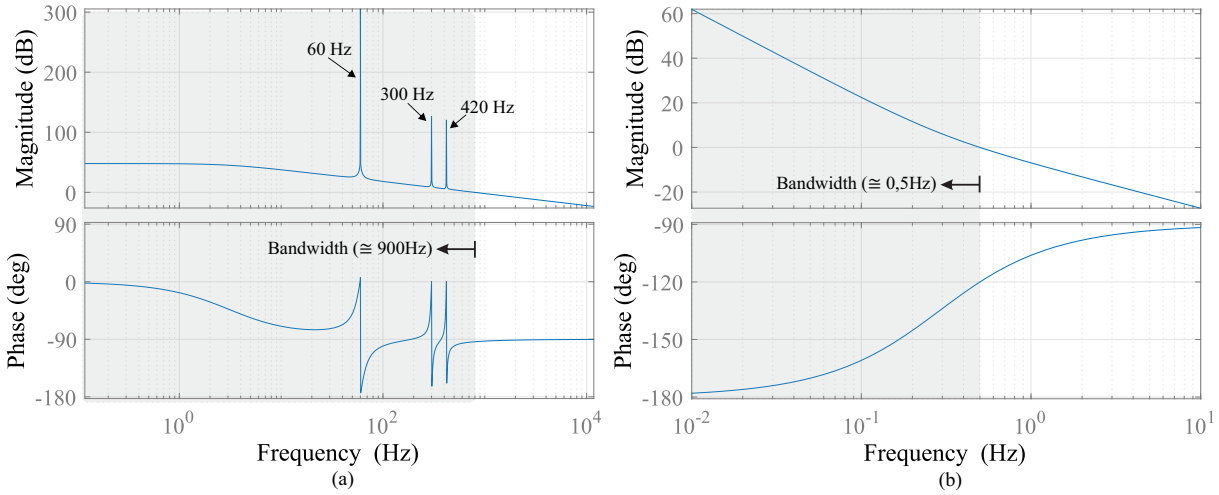


Figure 32 – Open loop Bode diagrams of the dc/ac stage current and dc-link voltage control. (a) Dc/ac stage current control loop. (b) Dc-link voltage control loop. (Source: own representation)

The current reference is calculated by the dc-link voltage control loop, which is performed through the square voltage method. This voltage control loop is an indirect way of controlling the active power, transferring it from the batteries to the grid. The outer-loop is designed to be slower than the inner-loop to simplify the controller design. A proportional-integral controller is used for this control loop, whose Bode diagram of the open-loop is shown in Fig. 32(b). With the aim to suppress the noise in the voltage measurements, a control loop narrow bandwidth is designed, with a value equal to 0.5 Hz.

The dc/dc converter control strategy depends if the batteries are charging and discharging, as shown in Chapter 4. If the discharge process is activated, only dc/dc converter inductor current control is activated. When the charge process is activated, the

dc/dc converter control, for topologies T2 and T3, consists of a current inner control loop and a battery voltage outer control loop.

The battery current control loop designed for the charge and discharge process is the same, as shown in the open-loop transfer function Bode diagram in Fig. 33 (a). The control bandwidth is 900 Hz, a decade below the dc/dc converter switching frequency. The open-loop bandwidth of the battery voltage control is designed to have 0.5 Hz, as shown in the Bode diagram in Fig. 33(b).

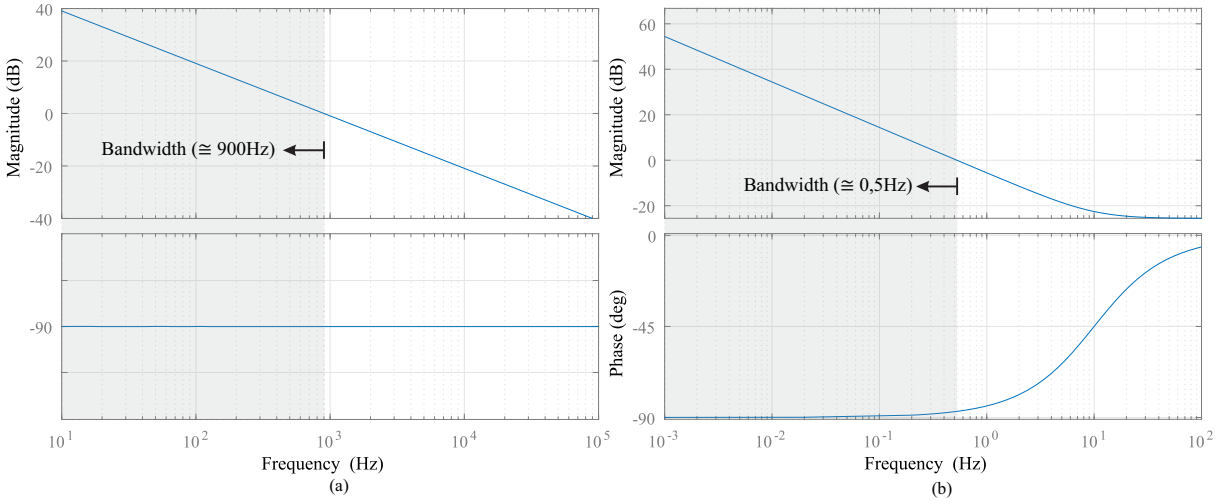


Figure 33 – Open loop Bode diagrams of the battery converter current and voltage control. (a) Battery current control loop. (b) Battery voltage control loop applied in PCS topologies T3 and T4. (Source: own representation)

The open loop Bode diagram for the dc/dc converter voltage output control for topology T4 is shown in Fig. 34. The control bandwidth is 0.02 Hz. This low frequency is explained due to the use of a first order low pass filter of 1 Hz in measuring the output voltage of each dc/dc converter. This filters is necessary to suppress noises.

6.5 Results

First, the dynamics of the system voltages and currents are analyzed through ramp and step variations for system characterization. The second test is to discharge both battery banks with a fixed current equal to 10 A and charge with the maximum current during CCM equal to 5 A. The PCS efficiency is measured during this battery discharge and charge cycle. The experimental PCS efficiency is measured using the digital power meter Yokogawa WT1600 with i1000s FLUKE ac current probes and A622 Tektronix current probes for dc current measure.

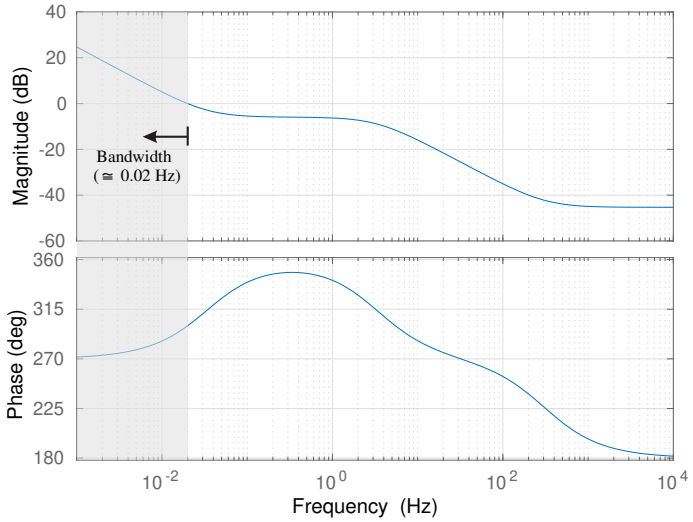


Figure 34 – Open loop Bode diagram of the dc/dc converter voltage output control for topology T4. (Source: own representation)

6.5.1 System characterization

The reference of the dc-link voltage is changed to check the system response. In this step, the dc/ac stage is connected to the grid. Fig. 35(a) shows a ramp variation of the dc-link voltage from 320 V to 400 V. Fig. 35(b) shows the variation of the same voltage from 400 V to 500 V. It can be noted a small overshoot due to the ramp variation.

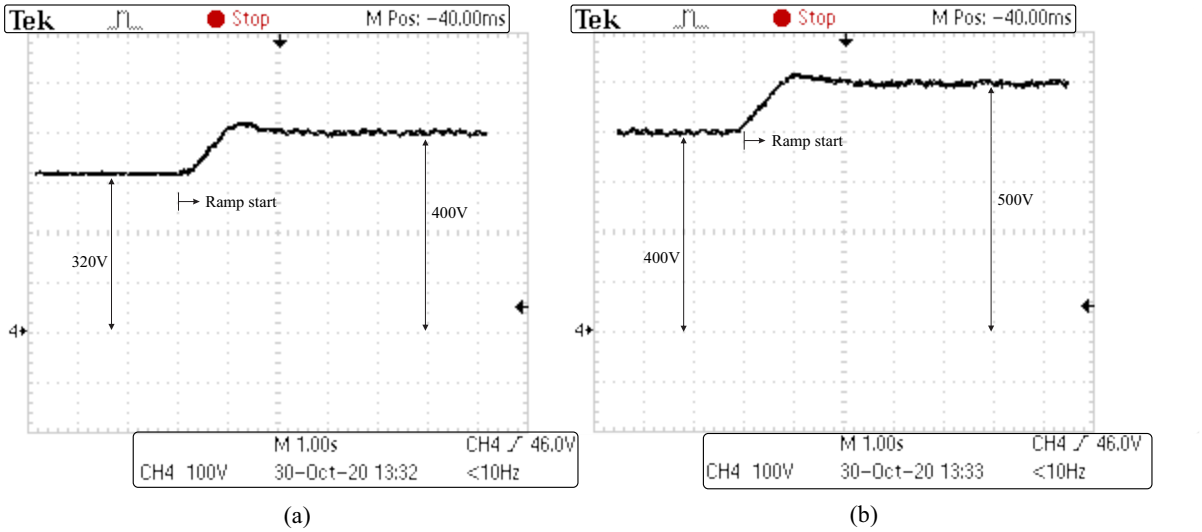


Figure 35 – Dc-link voltage.(a) Ramp variation from 320 V to 400 V. (b) Ramp variation from 400 V to 500 V. (Source: own representation)

The reference of each current battery bank is varied to check the system response. Fig. 36(a) and (b) show the currents in the two battery banks, with a ramp variation from 5 A to 16 A in both. The time for the current to reach a steady-state is approximately 150 ms for both cases, approximately.

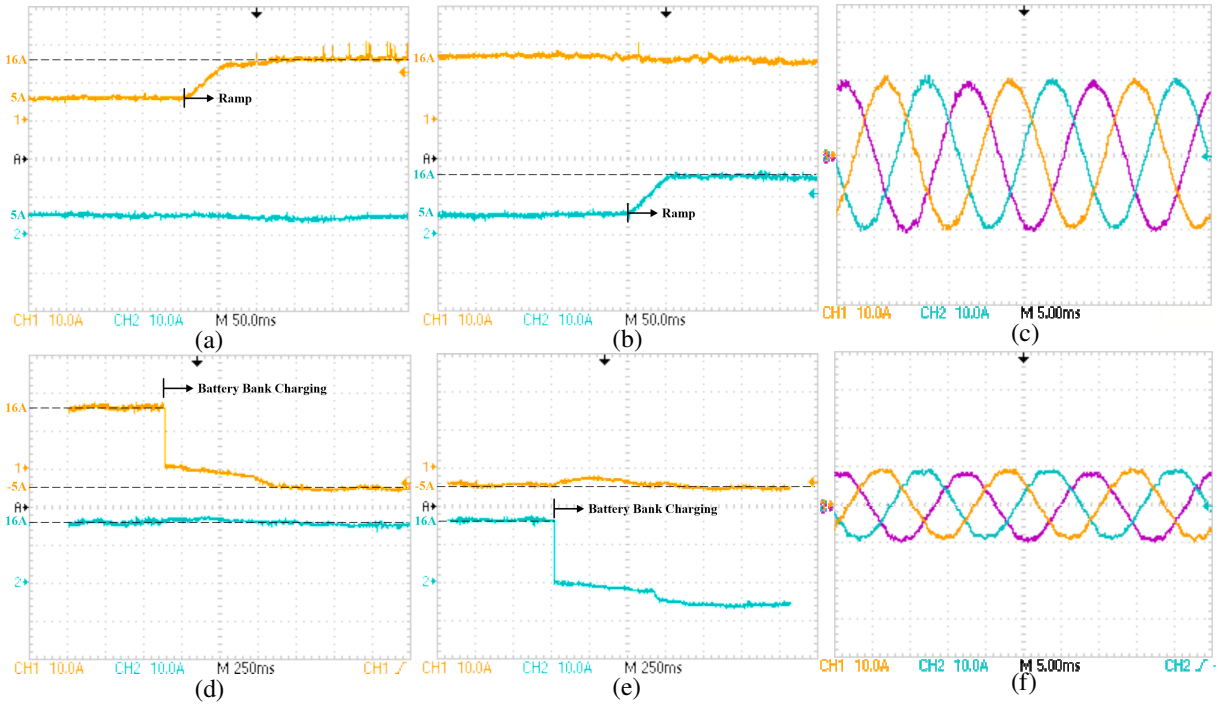


Figure 36 – Current in the two battery banks during discharge/charge and and grid current waveform. (a) Discharging current of the Battery bank 1. (b) Discharging current of the Battery bank 2. (c) Grid current during discharging. (d) Charging current of the Battery bank 1. (e) Charging current of the Battery bank 2. (f) Grid current during CCM charging. (Source: own representation)

Fig. 36(c) shows the three-phase currents when the two battery banks are injecting 16 A each. The current fundamental frequency component is 20 A in amplitude and THD is 3.30 %, approximately. It is possible to see some harmonic frequency distortions in the injected current. However the THD values of the injected current is within the limit of 5% defined by the recommendation IEEE Std 519-2014 (IEEE, 2014).

The battery bank operation mode is changed from discharge to charge process to check the dc/dc converter response control. Hence, the battery bank current is changed from 16 A to −5 A. Fig. 36(d) and (e) show the current step variation. The time for the current to reach the steady-state is 1 s for both cases, approximately.

Fig. 36(f) shows the three-phase current waveform when the two battery banks are charged with 5 A. The fundamental component has an amplitude equal to 9 A and THD is approximately 4.10%, within the IEEE Std 519-1992 limit even with the system operating below the rated power.

6.5.2 Control Validation of the Power Components Under Grid Frequency Deviation

In order to demonstrate the errors that can occur in the dc/ac stage current control, the test bench was supplied with a power source that imposes a frequency of 60.5 Hz. The Regenerative Grid Simulator NHR 9410 is used to perform this frequency variation. This scenario is suitable to validate the power control strategies, emulating a grid frequency deviation around the nominal frequency of 60 Hz. It is worth remembering that the resonant controllers are tuned to 60 Hz. Thus, this deviation in the grid frequency can cause an error in the current controller and, as the power control loops proposed by this work, must reject this disturbance in steady state. The dc/ac stage outer-loop with the reactive and active power components control are designed three decades below the switching frequency, given k_i equal to 57.

The first analysis considers the T3 topology with two interleaved dc/dc converters in parallel. In this case, the reactive power regulation is compared considering the control structure in open and closed loop. Fig 37 shows the reactive power profile considering power factor (PF) equal to 0.707 and reference equal to 3000 var. It can be noticed that the open loop approach presents an error between the measurement and the reference equal to 48 var, while for the closed loop approach, the error of the measured reactive power and the reference is close to zero.

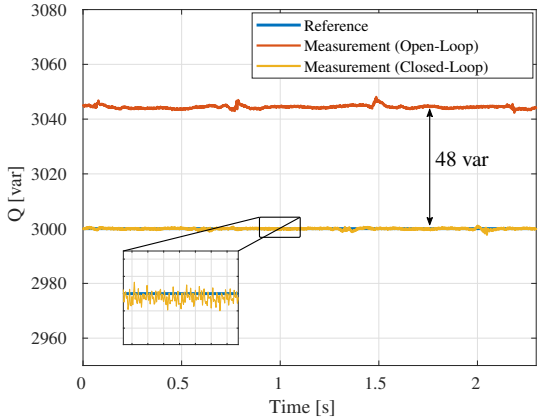


Figure 37 – Reactive power profile considering the power structure composed of two interleaved dc/dc converters in parallel connection and power factor equal to 0.707, considering the reactive power in open and closed loop with reference equal to 3000 var. (Source: own representation)

The reference and measurement current of the dc/ac stage inner loop control are shown in Fig. 38, considering the reactive power open loop approach. The phase error ($\Delta\theta$) between these two components is 0.84 degrees and the amplitude error (ΔI) is 0.03 pu. These errors were estimated through Fast Fourier transform. Through the analytical analysis presented in the previous section, the expected reactive power error is 50.25 var.

This represents an estimation error of 4.7% concerning the measurement value of 48 var, as shown in Fig. 37.

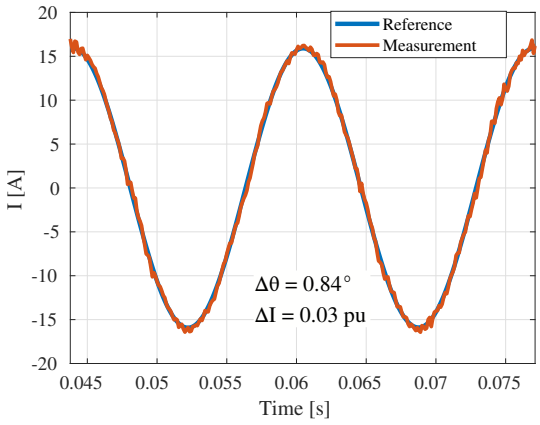


Figure 38 – Reference and measurement current of the dc/ac stage inner loop control. (Source: own representation)

Considering the same power structure, Fig 39 shows the reactive power profile with PF close to zero. The error of the open loop approach reduces to 9 var and this is in line with the analysis shown in Fig. 20(c) since the error variation, in this case, is less than the case of PF equal to 0.707. It is important to note that the closed loop, leads to approximately zero steady-state error.

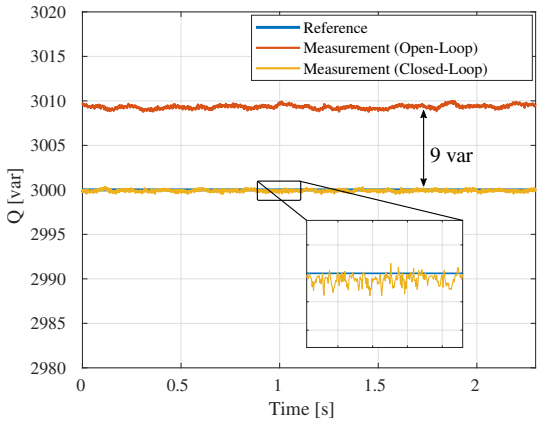


Figure 39 – Reactive power profile considering the power structure composed of two interleaved dc/dc converters in parallel connection and power factor close to 0, considering both open and closed loop. (Source: own representation)

The second analysis considers the structure with two interleaved dc/dc converters in series. For this PCS topology, both active and reactive power are in closed loop and it is compared with traditional scheme in open loop of the power components. Fig 40 shows the active power profile considering PF equal to 0.707 and reference equal to 3000 W. It can be noticed that the open loop approach presents an error between the measurement and the reference equal to 4.5 W, while for the closed loop approach, the error of the measured

active power and the reference is close to zero. It is important to note that the oscillations in the figure Fig 40 are apparent due to the scale of the graph. These oscillations are low and represent approximately 0.2%. Considering the same power structure, Fig 41 shows the active power profile with PF equal to 1. The error of the open loop approach increased to 25.5 W. These results show that the proposed scheme ensures very low steady-state error in the active and reactive power.

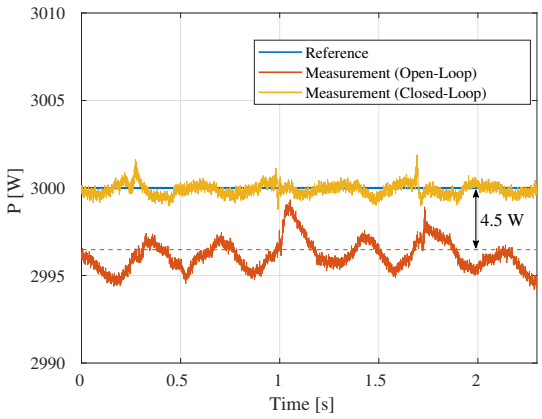


Figure 40 – Active power profile considering the power structure composed of two interleaved dc/dc converters in parallel connection and power factor equal to 0.707, considering the active power in open and closed loop with reference equal to 3000 W. (Source: own representation)

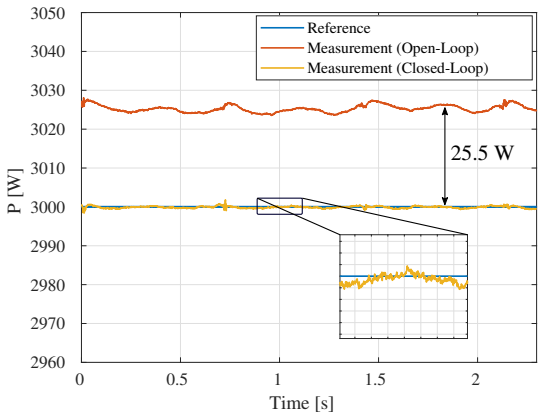


Figure 41 – Active power profile considering the power structure composed of two interleaved dc/dc converters in series connection and power factor equal to 1, considering both open and closed loop. (Source: own representation)

These results show the importance of the power control loop to reduce the steady-state error during a disturbance. The grid frequency deviation around the nominal was used to validate this proposed technique in these results.

6.5.3 PCS Efficiency Analysis During a Battery Charge and Discharge Cycle

A discharge and charge cycle of each battery bank is performed to analyze the PCS efficiency for topology T3 and T4. The efficiencies, current and voltage profiles presented below are obtained through the High Performance Power Analyzer WT1800 from YOKOGAWA.

The battery banks are discharged with a constant current equal to 16 A during 45 minutes in each topology. Fig. 42(a) and (b) show the current and voltage profiles of the battery bank 1 of the T3 topology, respectively. Fig. 42(c) and (d) show the current and voltage profiles of the battery bank 1 of the T4 topology, respectively. The currents and voltages of the battery bank 2 of each topology are not shown because they present similar profiles. The voltages of the battery banks start the discharge with 190 V and end with 180 V, respectively.

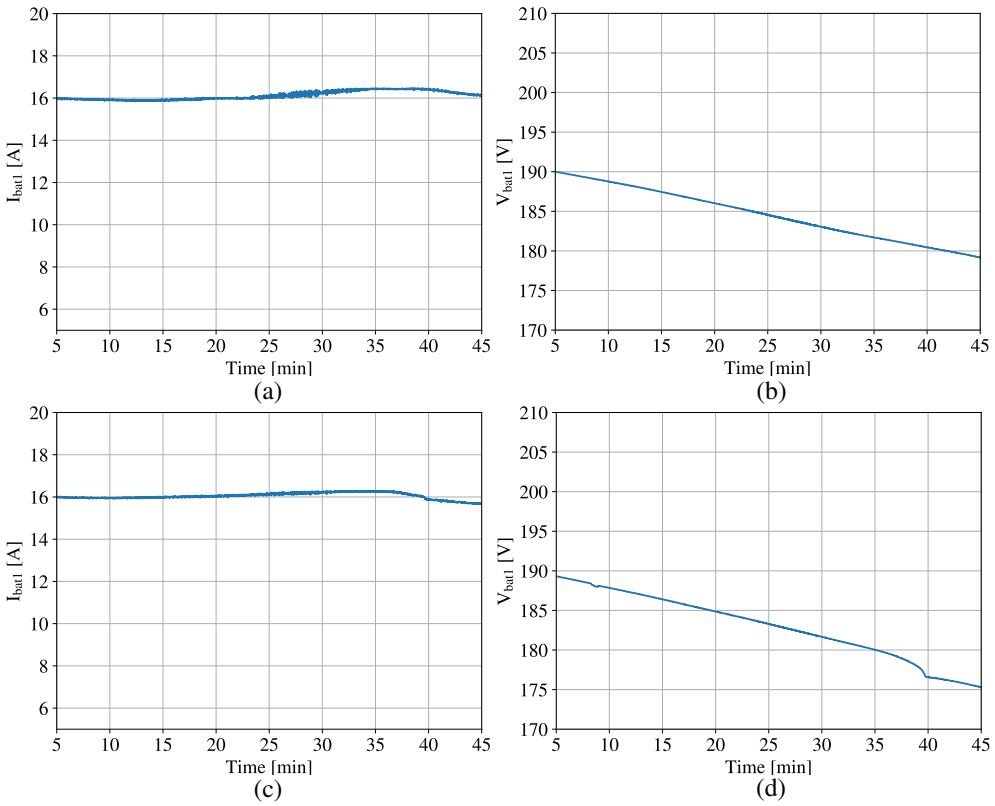


Figure 42 – Current and voltage profile of the battery bank 1 during discharging in both T3 and T4 topology. (a) Battery bank 1 current in T3. (b) Battery bank 1 voltage in T3. (c) Battery bank 1 current in T4. (d) Battery bank 1 voltage in T4. (Source: own representation)

After the discharge cycle, a charge cycle is carried out through CCM. The charging current is fixed at 5 A for 175 minutes approximately. Fig. 43(a) and (b) show the charge current and voltage profiles of the battery bank 1 of the T3 topology, respectively. Fig.

43(c) and (d) present the same profiles for topology T4. The study is finished with a slightly lower charge voltage than boost voltage of 230 V.

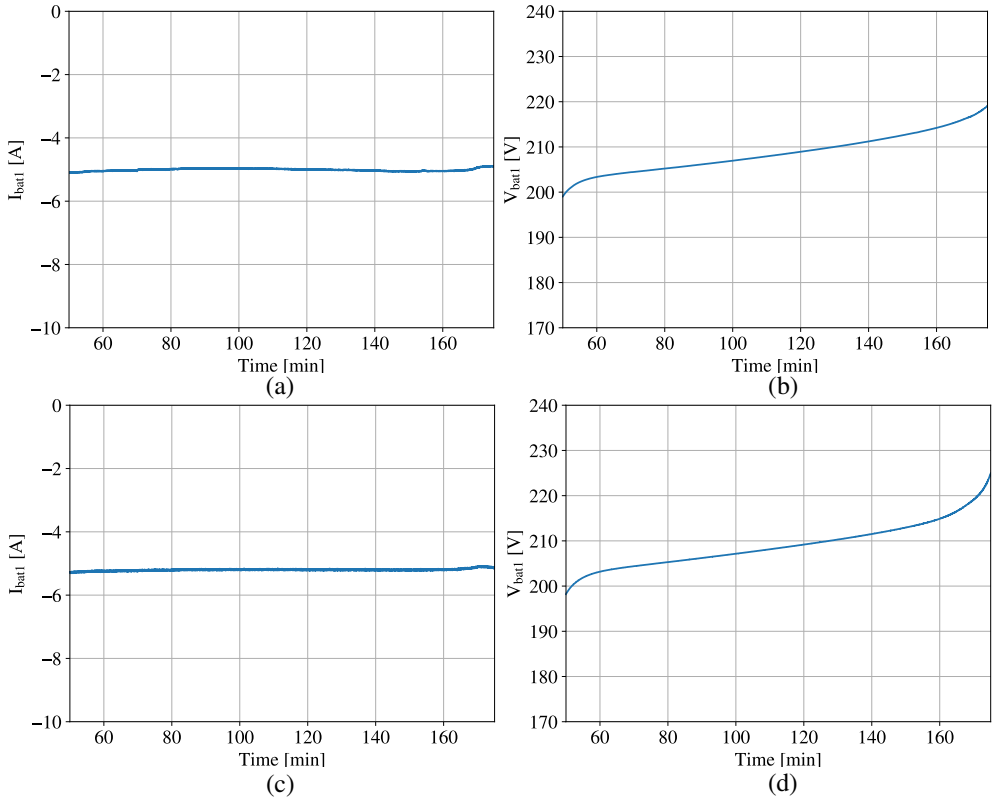


Figure 43 – Current and voltage profile of the battery banks during charge operation process. (a) Battery bank 1 current. (b) Battery bank 1 voltage in T3. (c) Battery bank 2 current in T3. (d) Battery bank 2 voltage in T4. (c) Current waveform injected to the grid in T4. (Source: own representation)

The battery bank 1 and 2 presents the SOC level of 65% at the end of discharging. After that, the charge process up to 100% SOC level. During this cycle, the efficiency for topology T3 is calculated and compared to the the experimental system using the methodology presented in previous sections. For this purpose, the PLECS simulation is performed using the methods described in this work with the experimental test bench parameters.

The experimental and simulation efficiencies during battery discharging and charging for T3 topology are shown in Fig. 44(a) and (b), respectively. The accuracy of the efficiency calculation methodology used in this work is demonstrated. Furthermore, the global efficiency index for experimental setup is 88.14% and for simulation is 89.91%, two close values. Therefore, it is expected that the previous results for the 100 kW case of study are also valid since the behaviour of slight efficiency variation with SOC and difference between charge and discharge are similar.

After performing an efficiency experimental and simulation comparison for T3, this topology is compared with the T4 topology in experimental environment. Fig. 45

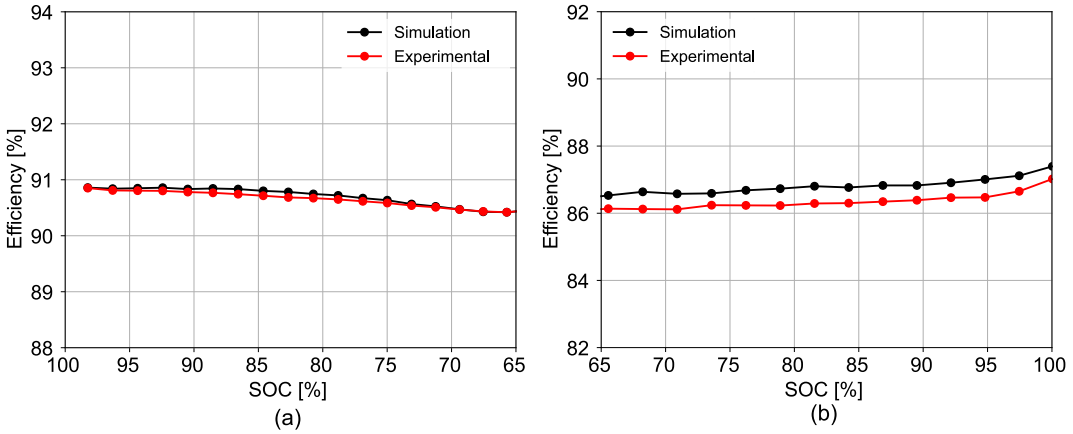


Figure 44 – Comparison between experimental and simulation PCS efficiency and the battery SOC relationship for topology T3. (a) Discharge process. (b) Charge process. (Source: own representation)

shows this comparison, considering the battery discharging (Fig. 45(a)) and charging (Fig. 45(b)). The global efficiency index for T4 is 92.7%. Therefore, the scenario 1 presented in Chapter 3 is predominant in this experimental study. The battery bank configuration and the battery charge for T4 are the same as T3. In this scenario, there is an improvement of switching utilization and step-up ratio decrease using T4 topology. In this situation, the series topology presented higher efficiency due to the lower duty cycle ratio.

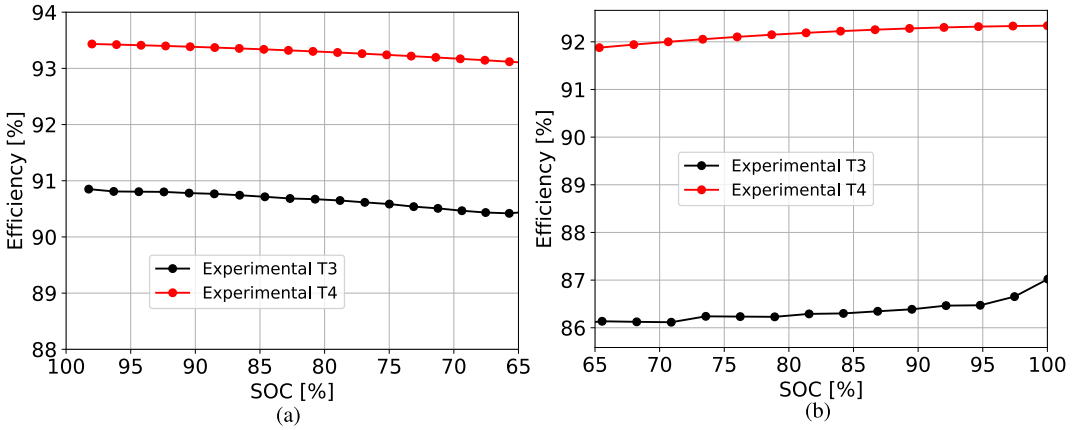


Figure 45 – Comparison between the PCS topologies T3 (parallel dc/dc converters) and T4 (series dc/dc converters). (a) Battery bank discharging. (b) Battery banck charging. (Source: own representation)

It can be noted in the test bench that there is no significant variation in efficiency with the SOC of the batteries, but there is a significant variation in efficiency between charge and discharge processes. This fact can be explained because the discharge is performed below the nominal power of the converters, which are regions of lower efficiency for this PCS configuration and voltage class of the semiconductor switches.

6.5.4 Phase Shedding Approach

The previous results show that for low power operation points, the efficiency of the PCS decreases. The phase shedding method consists in disconnecting some phase branches to improve the converter efficiency during light load conditions. This method can be applied using the efficiency map.

The estimated efficiency map of the experimental bench is shown in Fig. 46, considering 1, 2 and 3 branches in the dc/dc interleaved converter for T3 PCS topology during battery bank discharging. The Plecs software is used to estimated these efficiency maps considering the parameters of the experimental bench.

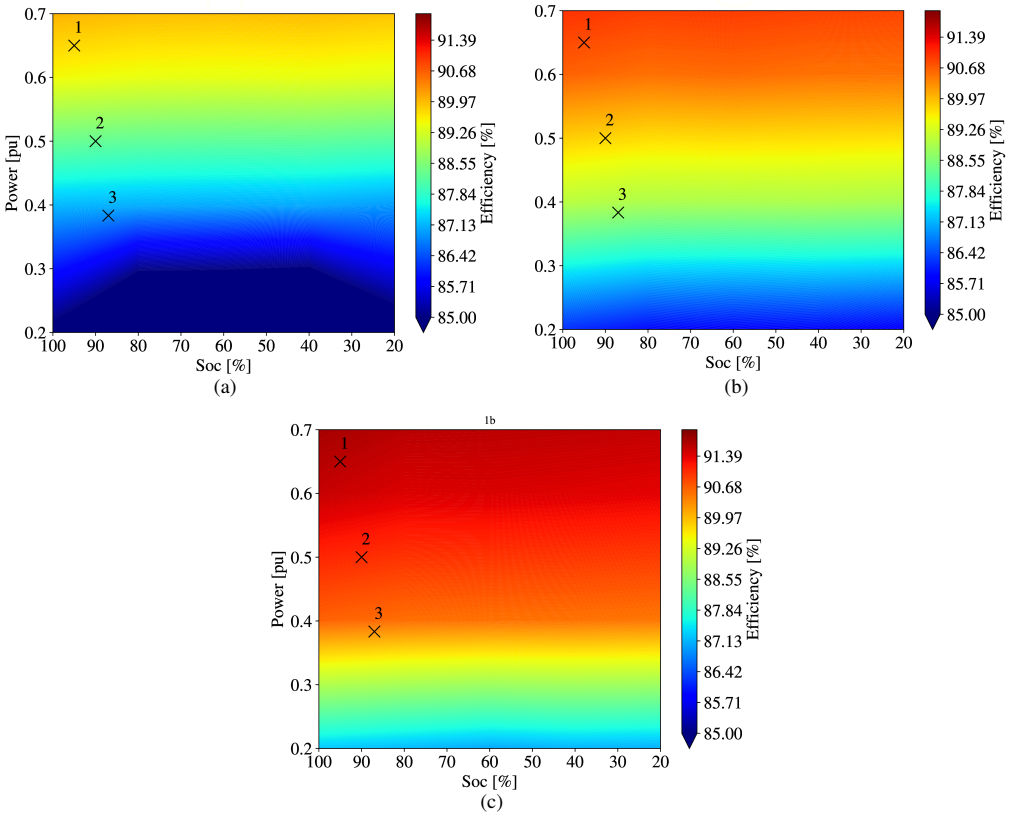


Figure 46 – Calculated efficiency map of the experimental bench for T3 topology phase shedding study, considering battery discharging. (a) Three branches in the interleaved dc/dc converter. (b) Two branches. (c) One branch. (Source: own representation)

Through the color gradient of the efficiency maps for each number of branches, it can be concluded that the efficiency is higher for light load for one branch, two branches and three branches, respectively. In other words, the smaller the number of branches, the greater the efficiency for light load conditions. Therefore, the efficiency map can be used in the control system to create boundary conditions to disconnect the branches.

Three operation points are used to verify the PCS efficiency in the experimental

tests using phase shedding method and comparing it with the calculated efficiency shown in Fig. 46. These three operation points are highlighted in Fig. 46 and they are the same for the three cases of active branch numbers. These three operation points in terms of the battery SOC levels and operation powers are detailed in Tab. 9. It is worth remembering that the nominal power of the system is 6 kW.

Table 9 – Operation points for phase shedding study. (Source: own representation)

Operation point	Battery bank SOC level	Operation power
1	95%	0.65 pu
2	90%	0.50 pu
3	87%	0.38 pu

Fig. 47 shows the efficiency of the experimental T3 topology considering the phase shedding for the three operation points highlighted in Fig. 46. The system efficiency is measured considers different numbers of branches activated (3, 2 and 1). Note that the phase shedding contributes to higher efficiency improvements in low power levels. Therefore, the operation point 3 presents a higher difference in the PCS efficiency considering one branch than the three branches. Note that the efficiencies of the experimental results shown in Fig. 47 is close to the calculated efficiencies shown in Tab. 10.

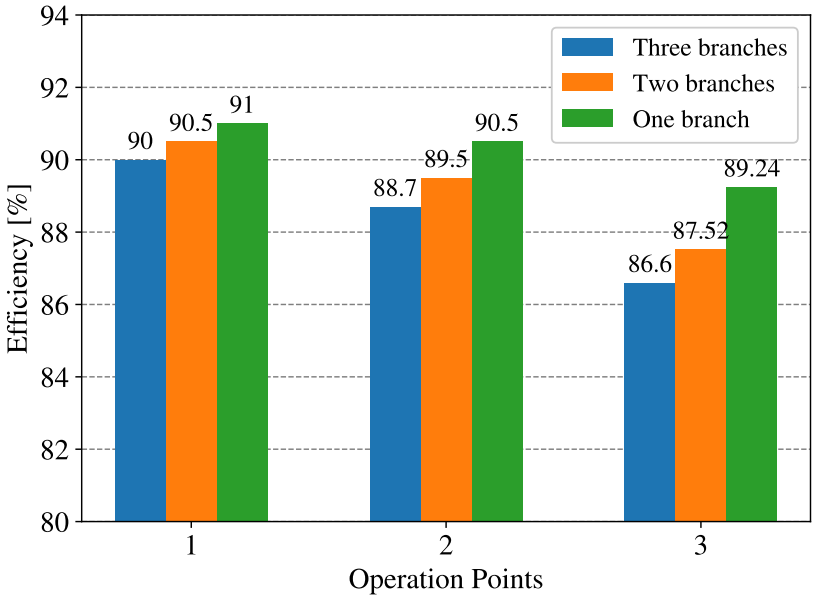


Figure 47 – Efficiency of the experimental T3 topology considering the phase shedding for three operation points. (Source: own representation)

However, disconnecting the branches can bring some disadvantages as well. Decreasing the number of interleaved converter branches can contribute to an increase in the current ripple flowing to the battery banks. Fig. 48(a) shows the battery bank current considering three branches in the interleaved dc/dc converter, considering the operation

Table 10 – Calculated PCS efficiency considering the phase shedding for the three operation points. (Source: own representation)

	3 branches	2 branches	1 branch
Operation point 1	89.50%	90.60%	91,45%
Operation point 2	88.50%	89.40%	90,50%
Operation point 3	86.50%	88.55%	89,60 %

point 3. Fig. 48(b) shows the same current with one branch. An increase in ripple can be noted for the one branch condition as the ripple cancellation capability of the interleaved converter is lost. Thus, there is a trade-off between efficiency improvement and current ripple in the battery banks when the shedding phase technique is applied.

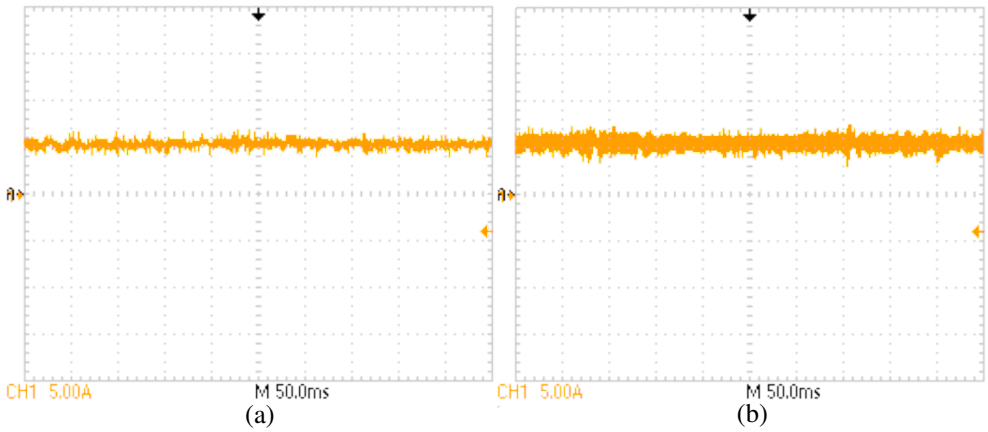


Figure 48 – Battery bank current to verify the ripple considering the phase shedding for the operation point 3. (a) Three branches in the interleaved dc/dc converter. (b) One branch. (Source: own representation)

6.5.5 Chapter Conclusions

This chapter presented the experimental test bench description and results to verify the influence of the battery operation point variation on the PCS efficiency and compare the topology with dc/dc converters in parallel and series connection.

The methodology used for efficiency calculation was validated and the PCS with two dc/dc converters in parallel connection presents a lower efficiency than the series connection. These experimental results show the other case of the one obtained from the simulation result, the serial connection presents a better switching utilization than the parallel topology. This occurs due to the possibility of using the same battery bank and the same battery charge and voltage in both topologies.

Furthermore, the phase shedding technique was presented, in which the branches of the interleaved converter are disconnected under light load conditions to improve the efficiency of the PCS. It can be noted that the efficiency map can be used to delimit

efficiency boundary conditions in relation to the SOC of batteries and power to perform the phase shedding approach.

7 Conclusions and Future Research

7.1 Conclusions

This work proposed an analysis methodology of the influence of the battery voltage variation on the PCS design and efficiency. The influence of battery voltage variation on the IGBT module design for the dc/ac stage was evaluated when the battery bank is directly connected to the dc-link. This approach was compared to the different arrangement of dc/dc interleaved converters with a controllable dc-link voltage, which can allow the use of lower blocking voltage for the dc/ac stage power switches. With this analysis, PCS design for BESS oriented toward voltage class and efficiency. Furthermore, a closed-loop power control was proposed to eliminate the steady-state error in the active power when the current control is implemented in the stationary reference frame. These control errors were modeled to understand the main factors that affect the power control applied in this strategy.

7.1.1 PCS Design Aspects for BESS

The proposed design method can help BESS projects informing the topology more efficiently for a given application and this can feed a more advanced levelized cost of storage methodology to decide the best solution. A simulation case study is presented to exemplify the proposed PCS design and methodology.

In this case, the PCS with two dc/dc converter in parallel connection present the higher efficiency, while the PCS without dc/dc converter present the lower efficiency. This can be explained by the use of power switches with a higher voltage class for the single stage converter due to the higher voltage variation of the battery bank. Nonetheless, this last PCS topology presented the lower levelized cost of storage value based on simplified methodology.

When analyzing the global efficiency, it is clear that the use of more power switches to compose two-stage converters does not always result in lower efficiency compared to single stage converters. The proposed efficiency maps show, in this case, that the two stage converter presents a low efficiency variation with the variation of the operating point of the battery bank, while the PCS with only the dc/ac converter presents a high efficiency variation.

The estimated initial cost analysis showed that the single stage PCS had the lowest cost. It can be seen that the increment of a dc/dc converter can increasing the system cost of 0.2 pu. This work shows that in terms of initial costs, the topology with only

the dc/ac converter can be interesting. However, this converter will not always present a greater efficiency due to the variation of battery voltage, requiring a higher voltage class of semiconductor devices for this PCS configuration. Using dc/dc converters, the initial cost can be higher. However, it is a converter that does not have its efficiency affected by the variation in the operating point of the batteries, in addition to requiring fewer batteries in series, which reduces the battery balancing circuits. In the presented case study, the PCS topology with dc/dc converters in parallel connection is an interesting solution. The experimental results validates the efficiency analysis addressed in this work.

The simulation and experimental analysis show two distinct cases that a BESS designer might come across. The first one shows the case when the dc/dc converters in series connection present the lower switching utilization, presenting the poor efficiency compared to the parallel connection. In an experimental study, the series connection presents better switching utilization than a parallel connection, resulting in better efficiency. The important point is that the arrangement and load of the battery bank have direct interference in the choice of converter for BESS. This fact reinforces the application of this work as an indication to carry out the PCS project for BESS

7.1.2 Power Control Applied to Stationary Reference Frame

These strategies are applied in the dc/ac stage control along with the square dc-link voltage along with stationary reference frame and instantaneous power theory. The experimental results, considering a deviation in the grid rated frequency, show that the steady-state error was reduced using the closed loop for power components in relation to the open loop strategies addressed in the literature. Furthermore, it can be verified that the power component error depend on the power factor and the error of the current control loop. The control strategy proposed in this work is simple to be implemented and guarantees the reduction of the steady-state error in the power components. These errors can arise from several factors, as discretization problems, bad control tunning or grid frequency variation.

7.2 Future Research

From the studies carried out in this work, there are many research ramifications that can be studied in future works. The following themes of study can be addressed by future work:

- Evaluate, development and modeling a PCS arrangement able to operate with the dc/dc converter connected in series or in parallel. This PCS can be adapted to the battery bank and can be switch between the converter arrangements even during

system operation. This converter can detect the scenarios covered by this work and make the decision on the best operation arrangement;

- Analyse the control disturbance of dc/dc converters in series connection. In this case, one converter acts as a disturbance over the others, making the control analysis more complex;

- Include the constant voltage mode capability in the series converter control for battery bank charging.

7.3 List of publications

The approached research have resulted in a following journal publication:

- L. S. Xavier, W. C.S. Amorim, A. F. Cupertino, V. F. Mendes, W. C. Boaventura, H. A. Pereira. “Power Converters for Battery Energy Storage Systems Connected to Medium Voltage Systems: A Comprehensive Review.” in BMC Energy, v. 1, p. 7, November 2019. doi: 10.1186/s42500-019-0006-5.

The author also contributed to the following journal publications in correlated topics:

- L. S. Xavier, A. F. Cupertino, H. A. Pereira and V. F. Mendes, ”Partial Harmonic Current Compensation for Multifunctional Photovoltaic Inverters,” in IEEE Transactions on Power Electronics, vol. 34, no. 12, pp. 11868-11879, Dec. 2019, doi: 10.1109/TPEL.2019.2909394.

- V. M. R. de Jesus, A. F. Cupertino, L. S. Xavier, H. A. Pereira and V. F. Mendes, ”Comparison of MPPT Strategies in Three-Phase Photovoltaic Inverters Applied for Harmonic Compensation,” in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 5141-5152, Sept.-Oct. 2019, doi: 10.1109/TIA.2019.2927924.

- Allan F. Cupertino, Lucas S. Xavier, Erick M.S. Brito, Victor F. Mendes, Heverton A. Pereira, Benchmarking of power control strategies for photovoltaic systems under unbalanced conditions, International Journal of Electrical Power & Energy Systems, Volume 106, 2019, Pages 335-345, ISSN 0142-0615, https://doi.org/10.1016/j.ijepes.2018.10.014.

The published conference papers in correlated topics are cited below per chronological order:

- L. S. Xavier, J. D. S. Zacarias, A. F. Cupertino, H. A. Pereira, D. I. Brandao and V. F. Mendes, "Harmonic Compensation Strategies Applied to Multifunctional Photovoltaic Inverters," 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 2019, pp. 1-6, doi: 10.1109/COBEP/SPEC44138.2019.9065297.

- A. L. P. de Oliveira, L. S. Xavier, J. M. S. Callegari, A. F. Cupertino, V. F. Mendes and H. A. Pereira, "Partial Harmonic Current Compensation Applied to Multiple Photovoltaic Inverters in a Radial Distribution Line," 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 2019, pp. 1-6, doi: 10.1109/COBEP/SPEC44138.2019.9065362.

7.4 Codes and Simulations

The simulations and codes used to obtain the results in Chapters 5 and 6 are present below and they can be used to continuous the study:

- <https://github.com/lsantx/thesis-case-study-chapter5>. This repository presents the complete simulation and codes used in the simulation case study of the Chapter 5;

- <https://github.com/lsantx/BESS-bench-simulation>. This repository presents the complete simulation of the BESS experimental bench in the PLECS software;

- <https://github.com/lsantx/bess-expe-bench>. This repository presents the source code of the BESS experimental bench developed in the code compose studio.

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