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Luis Eduardo Pedraza Caballero

Complementary Photonic Crystal Integrated Logic Devices and Circuits

Belo Horizonte
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Versão Final

Tese apresentada ao Programa de Pós-Graduação em Ciência da Computação da Universidade Federal de Minas Gerais, como requisito parcial à obtenção do título de Doutor em Ciência da Computação.

Orientador: Omar Paranaiba Vilela Neto
Coorientador: Paulo Sérgio Soares Guimarães

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Dissertation presented to the Graduate Program in Computer Science of the Federal University of Minas Gerais in partial fulfillment of the requirements for the degree of Doctor in Computer Science.

Advisor: Omar Paranaiba Vilela Neto
Co-Advisor: Paulo Sérgio Soares Guimarães

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Complementary Photonic Crystal Integrated Logic Devices and Circuits

LUIS EDUARDO PEDRAZA CABALLERO

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Resumo

Nos últimos anos temos testemunhado um incremento na demanda por maior poder computacional para dar suporte a à aplicações do mundo moderno. Portanto, diversas abordagens têm sido investigadas para aprimorar as tecnologias computacionais atuais. Especificamente, a fotônica visa utilizar fótons ao invés de elétrons com a promessa de desenvolver componentes e dispositivos mais eficientes, mais rápidos e de baixo consumo energético. Neste contexto, esta tese explora as propriedades fundamentais de um tipo de dispositivos, conhecidos como os Cristais Fotônicos (CF), com o intuito de projetar circuitos e sistemas fotônicos integrados (CI).

Essencialmente, propomos uma nova abordagem para criar CI baseada na conexão dos switches N e P, dispositivos lógicos complementares baseados em CF (CPCL) equivalentes aos transistores NMOS e PMOS, respectivamente. Estes dispositivos ocupam um área menor que 25 μm $\times$ 15 μm, apresentam uma taxa de perda de energia (ELR) menor que 0,045, tempo de resposta de 50 ps, razão ON-OFF (CR) maior que 6 dB e operam com o mesmo cumprimento de onda de entrada/saída (1550 nm aproximadamente). Suportam deslocamentos na ordem de (λ/28) nas fontes de entrada, mudanças na potência de entrada de $\pm$5 mW e deslocamentos na região das cavidades na ordem dos $\pm$20 nm. Estes resultados garantem as principais características para o cascateamento dos switches, permitindo pela primeira vez a projeção de circuitos e sistemas integrados em CF, superando as limitações e barreiras identificadas em trabalhos prévios.

Projetamos um conjunto de portas lógicas baseadas exclusivamente em CPCL atuando como componentes de hardware base. Apresentamos os desenhos para as portas AND, OR, NAND, NOR, XOR, para o componente FAN-OUT, e adicionalmente os circuitos Half-Adder e Full-Adder (Carry and Sum). Para estes circuitos obtemos um CR maior que 5,5 dB, tempo de resposta menor que 120 ps e um ELR menor que 0,06. Além disso, nossos circuitos ocupam um area menor que 75 μm $\times$ 46 μm.

Considerando o exposto anteriormente, destacamos que o paradigma de computação em CF atinge um nível de abstração mais alto, passando de componentes para CI. De fato, utilizando a abordagem proposta baseada em CPCL, podemos construir qualquer circuito combinacional em CF. Isto representa uma contribuição significativa do nosso projeto para o domínio de portas lógicas e circuitos em CF. Como observação final, os desenhos aqui propostos possuem grande potencial para microfabricação, apresentam baixa dissipação de energia e alta velocidade de processamento de dados.

Palavras-chave: Computação - Teses, Arquitetura de Computadores, Nanocomputação, Cristais Fotônicos, Sistemas Lógicos, Circuitos Integrados

Abstract

In recent years we have seen an increasing demand for higher computational power in order to support modern world applications. Therefore, several approaches have been investigated to improve current computational technologies. Specifically, photonics aims to use photons instead of electrons, promising the development of components and devices with high efficiency, high speed of data processing, and low power consumption. In this context, this thesis explores the fundamental properties of a kind of photonic device, known as Photonic Crystals (PhC), targeting to project photonics systems and integrated circuits (PIC).

Essentially, we proposed a new approach to build IC based on applying switches N and P, Complementary Photonic Crystal Integrated Logic Devices (CPCL), equivalents to NMOS and PMOS transistors, respectively. These devices have a footprint area less than 25 μm $\times$ 15 μm, exhibit an Energy Loss Ratio (ELR) lower than 0.045, a response time of 50 ps, ON-OFF Contrast Ratio (CR) of at least 6 dB and operate within the same input/output wavelength (about 1550 nm). They can support small phase delay ($\lambda/28$) at the input sources, changes in their Input power levels ($\pm$ 5 mW), and hole disorder effects around the cavity ($\pm$ 20 nm), the most sensitive region. These results ensure the main features to connect the CPCL allowing for the first time the development of PhC integrated circuits and systems by their adjacent connection, breaking the limitations of the previous works.

We designed a complete set of logic gates by exclusively applying the CPCL acting as core hardware devices. Specifically, we presented PhC designs for the AND, OR, NAND, NOR, XOR logic gates, for the FAN-OUT component, plus the Half-Adder and Full-Adder (Carry and Sum) circuits. The logic gates and circuits presented here have CR higher than 5.5 dB, a response time of 120 ps, and an ELR lower than 0.06. Additionally, the footprint area is less than 75 μm $\times$ 46 μm for all of our circuits.

Considering the above, we highlight that the PhC computing paradigm reaches a high abstraction level, switching up from components to PIC. Indeed, by using our proposed approach based on CPCL, we can build any combinational circuit in a PhC platform. This is a significant contribution of our project to the domain of logic gates and circuits based on PhC. As a final remark, our circuit designs have great potential for microfabrication, present low energy dissipation, and high speed of data processing.

Keywords: Computer Architecture, Nanocomputing, Photonic Crystals, Logic Systems, Integrated Circuits.

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Chapter 1

Introduction

Nowadays, we live in a highly connected digital society and experiencing the information era. This digital revolution was possible thanks to advances in the semiconductor technology, particularly with the invention of the transistor, followed by the integrated circuit and, finally, the miniaturization of electronic components. The shrinking of these components allows the development of fast, small, portable, and high data storage computers as a result of the fact that billions of transistors can be placed into one single chip [1].

Currently, the physical limitation of conventional CMOS transistors miniaturization and the consequent downfall of Moore's Law have motivated an ongoing pursuit for emerging technologies to aid the development of computational systems able to support the demands of nowadays applications, such as deep learning, big data, internet-of-things (IoT), autonomous driving, datacenters, cryptocurrencies, wearable systems, neuromorphic computing, and many others [2–6]. In order to advance in these applications, low power consumption, high speed of data processing, and low energy dissipation are the main desirable features for the new generation of computational systems [7, 8].

An emerging technology capable of fulfilling digital electronics gaps and achieving the desired features mentioned before is Photonics. In effect, Photonic Crystals (PhCs) appear as a promising platform to perform the fully optical information processing and computing since its discovery and demonstration [9–12]. The PhC ability to control electromagnetic waves, compactness, low power consumption and exceptional confinement of light has opened a large variety of applications for telecommunications, signal processing, biophotonics, and computing [13–17].

1.1 Motivation

Photonics technology has been successfully applied to route a new generation of components for other fields including biochemical detection, medicine, telecommunications, space exploration, and healthcare devices [18–23]. We have recently evidenced an

increasing interest related to the domain of logic gates based on PhC. As a result, different approaches have been applied to achieve devices and components suitable for sensing, signal processing, and computing.

One possible approach to allow logic gates in PhC is the use of the self-collimation (SC) effect. This is a phenomenon where the incident light can propagate along with specific directions through a structure without experiencing any diffraction. In general, building PhC logic gates using the self-collimated beams depends on the Total Internal Reflection (TIR) phenomena. Hence, the operations of the logic gates can be performed by introducing different phase shifts between the incident beams on the input faces of the PhC structure to create constructive or destructive interference at the output faces. Several works have effectively demonstrated different sets of PhC logic gates using this approach [24–27].

Another way to design logic gates applies the Multi-Mode Interference (MMI) effect. In PhC logic gates based on MMI, the input logic values are determined only by the phase of the input signals for each gate. This can be achieved by using Binary Phase Shift Keyed (BPSK) signals, whereas the output logic value is determined by the amplitude of the output signal regardless of its phase. With the proper signal phases of the input signals, they interact together in the MMI area to either generate a signal at the output port, which corresponds to logic 1, or eliminate the signal generation at the output port, which corresponds to logic 0. Then, the logic gates can be performed by the proper parameter selection in addition to the selection of the phases of the input signals [28–31].

Although these works demonstrated effective designs for PhC logic gates, the input phase sensitivity, unequal input/output frequency, and the use of complex structures limit the application for large-scale circuits and also yield to hard fabrication challenges. Thus, a simple, useful, and efficient approach was proposed by controlling the light beam interference effect through the waveguides interference path (WIP). In this scheme, the high transmission state (logic 1) is guaranteed if a constructive interference occurs between the inputs waveguides. This is accomplished by designing an intersection point with a path difference of 0 between them. In contrast, if the designed path difference is one lattice constant, destructive interference occurs between the inputs waveguides at the intersection point, achieving a low transmission state (logic 0). Using this approach, a complete set of PhC logic gates have been proposed theoretically [32–39]. However, high feedback propagation to the inactive inputs, loss of the signal at the output, and different power values representing the same logic state bring troubles to incorporate these devices into an integrated circuit.

Some of the obstacles mentioned before can be solved by introducing nonlinear materials into the PhC structure. The main property of such materials is the change in their refractive index under high-intensity radiation passing over them. Such variations of

the refractive index can cause essential changes, such as the ranges of operating frequencies. Thus, by setting the proper source intensities, logic gates are achieved using this approach [40–44]. Nevertheless, high power consumption, narrow operating frequency bandwidth and slow response time are the main drawbacks of this scheme. Indeed, some other approaches have been applied to design logic gates in PhC, presenting the same previously discussed limitations. Examples of that are: ring-resonator, four-wave mixing, temporal solitons, semiconductor-optical-amplifier (SOA), PhC fiber, topological cavity, and edge states, stimulated Raman scattering, Mach-Zehnder interferometer [37, 45–54].

	SC	**MMI**	**WIP**	**Nonlinear**
Unequal input/output frequency	X	X		
Hard microfabrication	X	X		
Input phase sensitivity	X	X		
Low Contrast Ratio	X	X	X	
High feedback propagation			X	
Large size			X	
Complex phase input synchronization			X	
Narrow operating frequency bandwidth				X
High power consumption				X
Slow response time				X

Table 1.1: Possible approaches applied to project logic gates in PhC and their main drawbacks.

Despite the technological advances achieved in this area, limitations to creating logical systems remain unsolved to concatenate devices and logic gates in order to design integrated circuits. Indeed, it lacks a standard or rule to design devices operating at the same input and output wavelengths, under the same input/output powers levels representing the two binary states and realistic structures for fabrication. In addition, optical transistors, as the core hardware devices of optical gates supporting large-scale integrated circuits for computers, have not been effectively exploited with PhCs. Regarding the successful history of electronic digital circuits, photonic technology may have a similar way to go. Table 1.1 crosses the possible approaches to design logic gates in PhC with their main drawbacks.

1.2 Thesis Statement

Considering the above, this thesis explores the fundamental properties of PhC in order to design devices and components capable of being applied to project integrated circuits and systems.

Thesis Statement. The statement of this research is as follows:

> *The proposed Complementary Photonic Crystal Integrated Logic Devices (CPCL), based on realistic structures for fabrication and equivalents to CMOS technology's NMOS and PMOS logic transistors, acting as PhC core hardware components, allows the development of integrated circuits and systems by their adjacent connection. Moreover, with these components operating at the same input/output frequency and under low energy loss and well-defined power values representing the logic states, the design of integrated circuits at a high abstraction level is ensured.*

1.3 Goals

Our goal is to build the PhC Switches N and P, equivalents to the NMOS and PMOS transistors, respectively, and based on a practical approach for fabrication, in order to support the development of large-scale PhC integrated logic circuits and systems.

More specifically, we pretend to (i) design a PhC structure capable of ensuring single-mode propagation and strong confinement of the electromagnetic mode, (ii) propose an approach to achieve well-defined power representations for the logic states, (iii) design the PhC structures equivalents to the Switches N and P demonstrating their correct operation at the same input/output frequency, with high data processing speed, and under a low energy loss regime, (iv) build PhC integrated logic gates and circuits by applying exclusively the Switches N and P.

1.4 Contributions

The contribution of this work is the design of PhC components together with the theoretical demonstrations of integrated devices and circuits. More precisely, our main contributions are the following. (i) Design of a PhC slab heterostructure that allows single-mode propagation and strong confinement of the electromagnetic mode. (ii) A simple, effective, and efficient approach based on Kerr nonlinear effect to achieve well-defined representations of the logic states 0 and 1, ensuring low energy loss and high data processing speed. (iii) Design and theoretical demonstration of efficient Switches N and P (Complementary Photonic Crystal Integrated Logic Devices), PhC analogous of the NMOS and PMOS logic transistors of the CMOS technology. These devices allow for the first time the development of integrated circuits by their adjacent connection. (iv) Prove the PhC integrated logic gates and circuits built exclusively using the CPCL as core hardware devices via reliable numerical simulations.

1.5 Thesis Organization

This thesis is organized as follows. Chapter 2 presents the foundations for the development of this work, i.e., a theoretical review of what PhC are and their fundamental properties, together with simulation methods. In Chapter 3, we discuss the main and recent works of logic devices using PhC. Chapter 4 details the Complementary Photonic Crystal Integrated Logic Devices. In Chapter 5, we demonstrate how CPCL can be applied to build PhC integrated logic gates and circuits. Chapter 6 presents a discussion of the most relevant achievements of this thesis together with a comparison with other works. Finally, Chapter 7 gathers the main conclusions and describes future works and possible research paths.

Chapter 2

Fundamental Theory

This chapter presents a theoretical review of what PhC are and their fundamental properties. It also covers the kinds of defects that can be introduced in them, the interference and nonlinear effects, and the simulation methods.

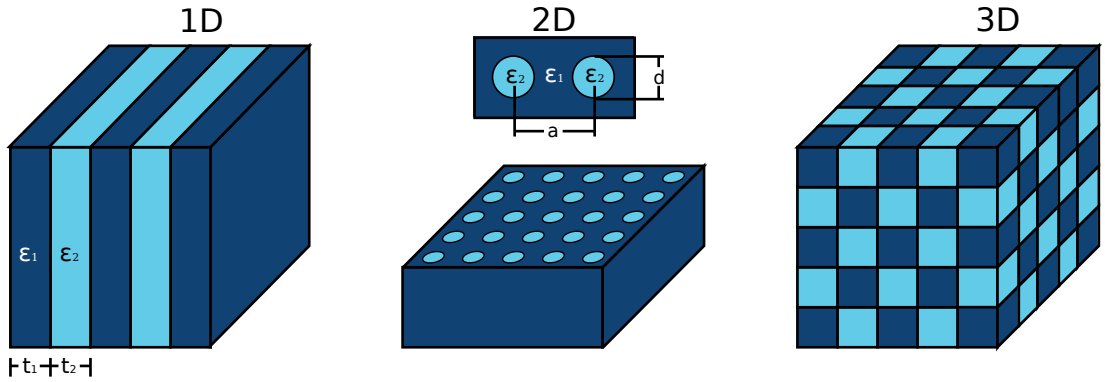
2.1 Photonic Crystals

Photonic crystals (PhC) are devices that have awaken a great interest since their proposal in 1987, and even more after their experimental demonstration in 1991 [9–11]. Fundamentally, PhC are a class of optical structures formed by a periodic modulation of the dielectric function distributed in a specific geometric lattice.

Due to this periodicity, electromagnetic waves are affected by the coherent scattering phenomena when they are launched into the PhC. The scattered waves cause the propagation or reflection of particular frequencies inside the structure, as a result of the constructive and destructive interferences between them. The allowed and forbidden frequencies are associated to the photonic bands (PB) and photonic band gaps (PBG), respectively. Thus, when the incident electromagnetic wave on the crystal has frequency within the PBG, it is completely reflected. Otherwise, if the frequency is in the allowed region (PB), it will propagate inside the PhC [55].

As can be noted, this fact means that PhC operate as optical semiconductor devices and allow us to design insulators or conductors of electromagnetic waves by engineering their geometrical parameters. Photonic crystals can be divided geometrically into three broad categories, namely one-dimensional (1D), two-dimensional (2D), and three-dimensional (3D) structures, as can be appreciated in Figure 2.1.

In 1D PhCs, the periodic modulation of the dielectric function occurs in one direction, while in the other two directions the medium is uniform. A very low number of possible variations can be accomplished, in this case: only the dielectric materials, layer's thicknesses, and the number of layers can be varied [55, 56].



(a) (b) (c)

Figure 2.1: Schematic representation of photonic crystal dielectric distribution in (a) 1D, (b) 2D and (c) 3D. Dark and light colors correspond to two different materials, with different dielectric constant ε_1 and ε_2. Adapted from Ref. [56].

In a 2D photonic crystal structure, the periodicity of the dielectric function occurs in two directions, while in the third the medium is uniform. Consequently, a large variety of configurations can be achieved by varying the dielectric materials, lattice geometry *(square, hexagonal)*, lattice constant a, and shape of the dielectrics *(square, ellipses, triangle)*. Nevertheless, for technological reasons two types of configurations are commonly used: square and hexagonal lattices, illustrated in Figure 2.2. For both cases, good examples are a silicon substrate with etched holes or a system of dielectric rods in air [55].

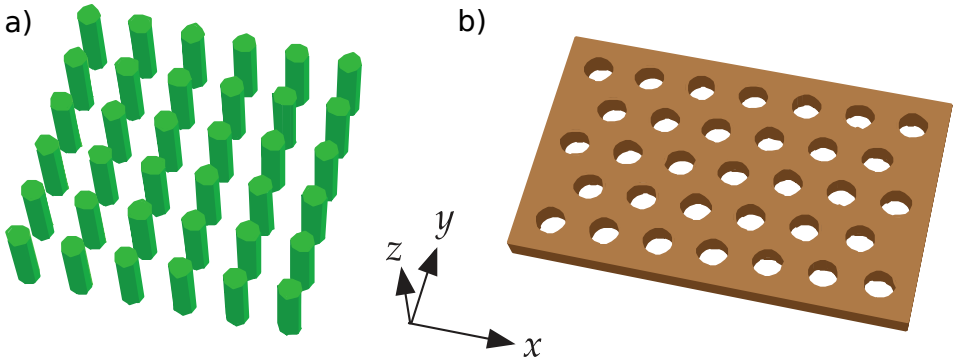


Figure 2.2: 2D photonic crystals lattice configurations. a) A PhC of dielectric rods in air arranged in a square lattice and b) a dielectric substrate with etched holes configured in a hexagonal lattice. Taken from Ref. [56].

The three-dimensional photonic crystals have dielectric modulations along all three directions. With that, the number of possible configurations is much larger. However, these 3D structures are more difficult to fabricate, although they are relatively common in nature. The most known naturally formed 3D PhC is the valuable stone opal [55].

At this point, as in solid state physics, the concept of band diagrams (also called

band structure or dispersion relation) is useful to understand the properties of the structure. A band diagram is a plot of the allowed frequencies as a function of the wave vector, usually along a highly symmetric direction in the reciprocal space (the first Brillouin Zone). Its physical meaning is the connection between the characteristics of the photonic crystal and its properties of propagation (PB) and reflection (PBG) [55, 56]. It can be obtained solving the eigenvalue problem of the master Maxwell equation:

$$\hat{\Theta}H(r) = \left(\frac{\omega}{c}\right)^2 H(r), \tag{2.1}$$

where $H(r)$ is the magnetic field, r is the (cartesian) position vector, ω is a given frequency, c the speed of light, and $\hat{\Theta}$ is the hermitian Maxwell operator, defined as:

$$\hat{\Theta} = \nabla \times \left(\frac{1}{\varepsilon(r)}\nabla \times H(r)\right). \tag{2.2}$$

Here, $\varepsilon(r)$ is the dielectric function and it is the square of the refractive index n. In general ($n = \sqrt{\varepsilon\mu/(\varepsilon_0\mu_0)}$). However, for most dielectric materials of interest, the relative magnetic permeability ($\mu(r) = \mu/\mu_0$) is very close to unity, making n approximately $\sqrt{\varepsilon(r)}$ [56]. Figure 2.3 shows a typical band diagram of a 2D-photonic crystal structure. In this case, it is composed of dielectrics rods embedded in air and arranged in a triangular lattice, as shown schematically on the top right side of the figure.

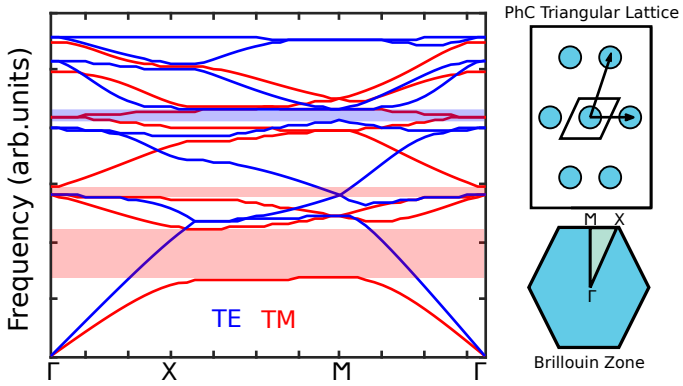


Figure 2.3: Band diagram of a 2D photonic crystal composed of dielectric rods embedded in air, arranged in a triangular lattice. This example exhibits photonic band gaps for two polarizations, transverse magnetic (TM,red) and transverse electric (TE,blue). Adapted from Ref. [57].

In summary, photonic crystals are promising devices considering their properties, which allow the manipulation of photons, like semiconductors allow the control of electrons. Indeed, scientists are now turning to light instead of electrons as the information carriers and have begun imagining photonic integrated circuits which resemble microscopic networks at micrometer length scales. Light has several advantages over the electron, such as it can travel in a dielectric material at much greater speeds, can also carry a larger amount of information per second, the bandwidth of dielectric materials is significantly

larger than that of metals, and light particles (or photons) are not as strongly interacting as electrons, which helps reduce energy losses [58].

2.1.1 Photonic Crystal Slab

Control the light in all three dimensions is the goal of the technological and scientific community. To do that, three-dimensional PhC are the ideal platform to confine and guide the light in the three dimensions. Although there are some advances in the demonstration of 3D PhC, critical steps towards the fabrication of functional and large-scale 3D devices and circuits have not been achieved [59–65].

Two-dimensional PhC embedded into planar dielectric waveguides, known as two-dimensional PhC slabs, have emerged in the last decade as the best candidates for efficiently confining and guiding the electromagnetic fields at optical frequencies in three dimensions. Currently, lithography and etching processes at sub-micron scales are in a very mature and advanced stage, allowing the fabrication of large-area photonic crystal slabs with high-nanometric precision [66–71].

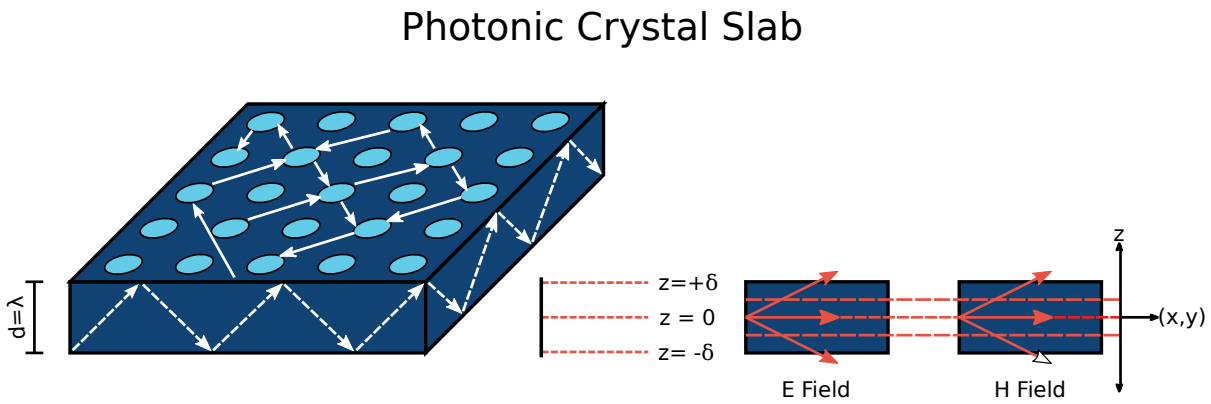


Figure 2.4: Schematic representation of a PhC slab. The dashed lines indicates the TIR mechanism along the z axis. The solid line represent the DBR mechanism on the 2D pattern. The electromagnetic modes on a PhC slab are confined at $z = 0$. Generally, the thickness of the slab is $d \sim \lambda$, where λ is the operating wavelength of the device. Adapted from Ref. [57].

In PhC slabs, the vertical confinement mechanism is given by total internal reflection (TIR), and in-plane the propagation is controlled by the photonic pattern via distributed Bragg reflection (DBR), as shown in Figure 2.4. Photonic band gaps in these systems are thus conditioned by both TIR and DBR mechanisms.

The electromagnetic modes in a PhC slab can be divided into two orthogonal polarizations, known as transverse-electric (TE) and transverse-magnetic (TM). The first

has field components (E_x, E_y, H_z), while the second presents the following components (H_x, H_y, E_z), considering xy as the plane where the photonic pattern is present [57].

In PhC Slabs, in which thickness $d \sim \lambda$, the electromagnetic modes are confined at only one symmetry plane, $z = 0$ (the center of the slab). On the other hand, the finite-thickness condition along the vertical axis in PhC slabs introduces new physical phenomena that are not present in the fully two-dimensional case. Since the space is open outside the PhC slabs, the electromagnetic field is not bounded in this region, and it determines a continuous spectrum. In addition, the electromagnetic field is bounded inside the slab, and the spectrum is discrete. Discrete resonances, i.e., guided modes, can thus interact with the continuous spectrum, i.e., radiative (or leaky) modes, through the vertical boundary, allowing the possibility of energy flux from inside the PhC to outside, and vice versa [56].

2.2 Photonic Crystal Defects

In particular, two types of defects can be introduced in two-dimensional photonic crystals: point defects and line defects, often employed to build cavities and waveguides, respectively.

2.2.1 Photonic Crystal Cavity

A photonic crystal defect is a perturbation of the system that breaks the periodicity of its dielectric function. This can be made removing one or more dielectric features, a dielectric rod or a hole in the structure, or replacing them with other features, whose size, shape or dielectric constant are different from the original.

In effect, if the designed defect has the proper size, shape and dielectric constant to support an electromagnetic mode within the photonic band gap, the light cannot escape from it, and it is trapped into the cavity forming an optical resonator, as illustrated in Figure 2.5. The two most important characteristics of interest in PhC cavities are: the mode volume and the quality factor (Q).

The mode volume is a measure of how tightly the mode is localized into the cavity. It can be determined with the dielectric function and the field function of the electromagnetic mode profile [72].

The quality factor Q is a dimensionless quantity that relates the outgoing power and the electromagnetic energy localized in the cavity. Also, it can be viewed as a measure of the number of optical periods that elapse before the energy decays, i.e., the lifetime of the electromagnetic modes in the cavity [56]. The quality factor of a PhC cavity can be computed using the following relation:

$$\frac{1}{Q} = \frac{P}{\omega_0 U}, \tag{2.3}$$

where P is the outgoing power, ω_0 is the resonant frequency and U is the electromagnetic energy localized in the cavity [56]. A high Q implies a longer lifetime of the electromagnetic waves inside the defect.

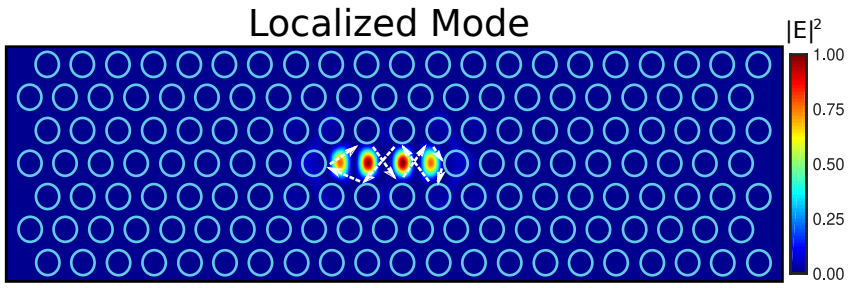


Figure 2.5: PhC cavity. Schematic representation and normalized intensity distribution of a localized mode in a PhC L3 cavity.

High quality factors have been achieved in two-dimensional photonic crystals using the L3 cavity. It is created by removing three holes or rods in the same line of the structure, as shown in Figure 2.5. Values of Q reaching the order of 10^5 have been reported in the literature for L3 cavities [73].

Such kind of cavity has important applications for low threshold lasers, high finesse filters, sensors, cavity quantum electrodynamics as well as filtering, switching, and integrated optical processing when integrated with waveguides [74–82].

2.2.2 Photonic Crystal Waveguide

Another fundamental type of perturbation in a photonic crystal structure is a waveguide. Essentially, a waveguide in a two-dimensional photonic crystal device is a line defect created by removing or changing the properties of one entire dielectric row or column, as shown in Figure 2.6.

The key difference between cavities and waveguides is that, for the former electromagnetic modes can be localized whenever its frequency is in the photonic band gap,

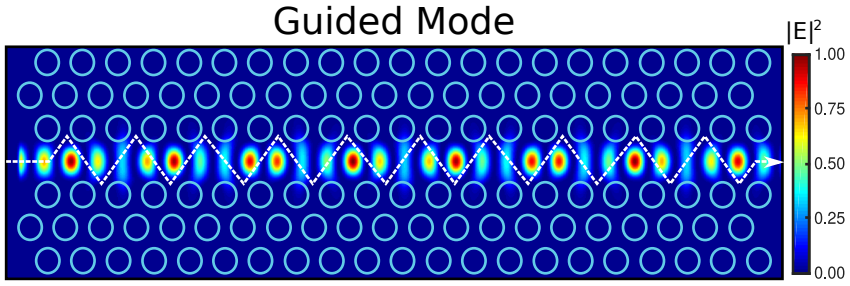


Figure 2.6: Photonic crystal waveguide. Schematic representation and normalized intensity distribution of a guided mode in a PhC waveguide.

while for the latter the behavior of the mode relies on its frequency and wave vector. Thus, a guided mode needs only the combination of wave vector and frequency disallowed in the structure; it is not necessary that frequency alone is disallowed. With this condition, the conservation of the wave vector along the defect allows the propagation of the electromagnetic mode from one side to another, as opposed to being just a region where it is localized [56].

Taking advantage of this, waveguides are used to guide the electromagnetic waves with very high efficiency. Thus, optical devices working in the low losses and low energy-consumption regime for telecommunication purposes can be achieved.

2.2.3 Photonic Crystal Coupled Sytems

A coupled system is one in which the operation of each component is described according to the behavior of the other elements that compose the system.

Waveguides and cavities can form a coupled system in a photonic crystal in order to build efficient frequency filter devices. There are two possible configurations to couple waveguide and cavities in a PhC structure: side-coupled and directly-coupled.

In a waveguide-cavity directly coupled system, the cavity is placed in line with the waveguide, as illustrated in Figure 2.7. Thus, light from the input waveguide couples into the cavity, and the cavity, in turn, couples into the output waveguide allowing the transmission of frequencies near the resonant frequency of the cavity. This system acts as a narrow-band filter device [56, 83].

The transmission spectrum (T) of this system can be estimated using the following function:

$$T(\omega) = \frac{\delta}{\left(\frac{\omega-\omega_0}{\omega_0}\right)^2 + \delta}, \tag{2.4}$$

where ω_0 is the resonant frequency of the cavity and δ is a quantity related to the quality

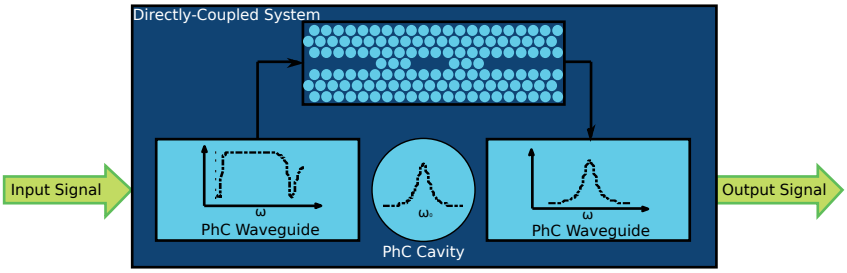


Figure 2.7: Representation of a directly waveguide-cavity coupled system in PhC.

factor as: $1/Q^2$.

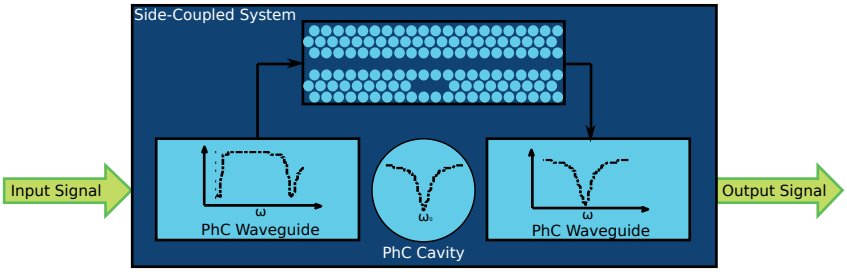


Figure 2.8: Representation of a side waveguide-cavity coupled system in PhC.

On the other hand, in a waveguide-cavity side coupled system, shown in Figure 2.8, the cavity is placed in a line up or down to the waveguide. Thus, the cavity couples with the input and output waveguides reflecting the frequencies around the resonant frequency of the cavity [56, 83]. For this kind of configuration, the transmission spectrum can be computed with the equation:

$$T(\omega) = \frac{\left(\frac{\omega-\omega_0}{\omega_0}\right)^2}{\left(\frac{\omega-\omega_0}{\omega_0}\right)^2 + \delta}. \tag{2.5}$$

These coupled systems have been used successfully to enhance nonlinear effects, frequency filters, absorptive devices and sensors [84].

2.3 Interference Effects in PhC

This section details the interference effects that can be applied in PhC to design logic devices.

2.3.1 Interference Effect Based on MMI

Generally, Multi-Mode Interference (MMI) devices are composed of the access waveguides, the multi-mode region, and the output waveguides. Its operation principle is the self-imaging property. In this, guided modes are excited and interfere constructively or destructively at the MMI region when an input field is launched at the access waveguides. Then, the excited field at the MMI region transmutes periodically along the propagation direction to the output waveguides. Usually, access and output waveguides are single-mode to ensure a high-performance MMI device. On the other hand, the MMI region is a waveguide that supports a large number of modes and where the MMI occurs [85].

2.3.2 Interference Effect Based on Self-Collimation

Self-Collimation (SC) or self-guiding of light in a PhC is a process in which a narrow beam of electromagnetic wave can propagate without any significant broadening or change in the beam profile, and without relying on a bandgap or engineered defects, such as waveguides. This phenomena occurs due to the complex spatial dispersion properties of planar photonic crystal generating anomalous refraction of light. To achieve the SC in a PhC, the allowed wavevectors in the structure and their corresponding frequencies must be as flat as possible to ensure the perpendicularity of the group velocity of light. Thus, launching beams signals with appropriate phases into a SC PhC, the reflected and transmitted can generate constructive or destructive interference [86].

2.3.3 Interference Effect Based on Waveguide Intersection Paths

As described earlier, PhC waveguides are used to guide electromagnetic modes from one place to another. PhC bend waveguides based on square and triangular lattices have been extensively studied and also experimentally demonstrated. Two rules of thumb can be applied to adequately design the intersection path between two PhC waveguides. In general, a path difference of zero implies that constructive interference occurs between the

two input signals. In contrast, a destructive interference will occur if the path difference between the waveguides are one lattice constant [32, 34].

2.4 Kerr Effect in Photonic Crystals

The optical Kerr effect is a kind of phenomena in that a nonlinear material changes its refractive index under high intensity radiation passing over them. This change of the refractive index can be calculated through the following equation:

$$\Delta n = n_0 + n_2 I, \tag{2.6}$$

where n_0 is the linear refractive index, n_2 is the Kerr coefficient and I is the intensity of the electromagnetic wave. Such variations of the refractive index can cause essential changes of device fundamental characteristics [87].

In this way, the best approach to observe the optical Kerr effect in photonic crystals is through a coupled system with a nonlinear cavity. In this kind of system, the introduced nonlinearity induces a change of the refractive index inside the cavity which follows the relation of the Equation 2.6. Besides, it is observed that the cavity resonant frequency shifts proportionally to Δn due to the subsequent growth of the electromagnetic energy inside the resonator [84].

Then, after applying rigorous perturbation theory arguments, the relation between the output and input power in a directly-coupled system can be expressed by the Lorentzian [84]:

$$\frac{P_{out}}{P_{in}} = \frac{1}{1 + (P_{out}/P_0 - \Delta)^2} \tag{2.7}$$

where P_{in} and P_{out} are the input and output powers, P_0 is the characteristic power of the cavity, and Δ relates the resonant frequency (ω_0) with the width of the resonance (Γ), $\Delta = \omega - \omega_0/\Gamma$. For a side waveguide-cavity coupled system, this relation can be expressed as:

$$\frac{P_{out}}{P_{in}} = \frac{(P_{out}/P_0 - \Delta)^2}{1 + (P_{out}/P_0 - \Delta)^2} \tag{2.8}$$

Figures 2.9a and 2.9b show the typical transmission spectrum of a directly and side waveguide-cavity coupled systems, respectively. In general, if the applied input on the waveguide has the proper amount of intensity to put the cavity in the nonlinear regime, then the resonant frequency of the system shifts due to the change in the refractive index of the nonlinear cavity. This variation gives the possibility to design a new class of optical devices such as optical information storage elements, bistables, transistors, and logical elements [78, 88–95].

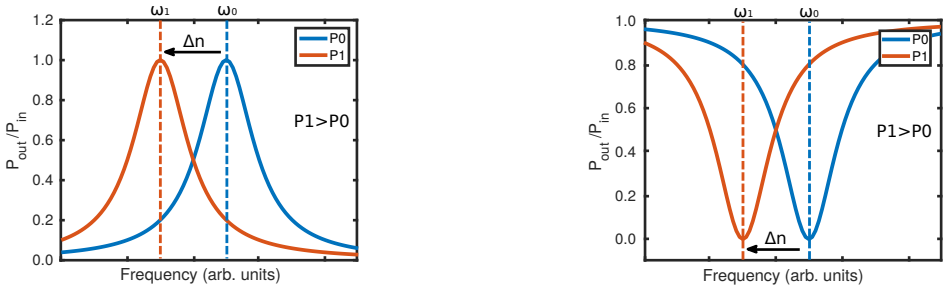


Figure 2.9: Typical transmission spectrum of nonlinear coupled system in photonic crystal for (a) directly waveguide-cavity coupled system and (b) side waveguide-cavity coupled system. For a power P_1 greater than P_0, the resonant frequency of the cavity shifts as a function of the applied input power on the waveguide.

2.5 Simulation Methods

2.5.1 Finite Difference Time Domain Method

The finite difference time domain method (FDTD) is a numerical technique used to solve Maxwell's equations. It can be implemented without using linear algebra which makes it appropriate for rigorous simulations of large scale problems, and structures with non-uniform dielectric distribution and complicated geometries. It is accurate, and sources of numerical error are well understood. Also, FDTD calculates naturally the nonlinear response of an electromagnetic system as it is a time-domain technique [96, 97].

To solve Maxwells equations, FDTD divides space and time into a grid (usually uniform) of discrete points and approximates their derivatives ($\nabla\times$ and $\partial/\partial t$) by finite differences. The propagation in time, in particular, uses a leap-frog scheme where the E fields at time t are computed from the E fields at time $t-\Delta t$ along with the H fields at time $t-\Delta t/2$, and vice versa for H at $t+\Delta t/2$. In this way, the E and H field patterns are marched through time, offset by half of a time step Δt [96–98].

At this time, FDTD starts the field calculations from initial and boundary conditions. Typically, the initial conditions in FDTD are defined by the geometry of the device and a source. FDTD supports a number of different types of sources such as Gaussian, a total-field scattered-field (TF-SF) source, a guided-mode source. A Gaussian source defines a beam of electromagnetic radiation propagating in a specific direction, with the amplitude defined by a Gaussian cross-section of a given width. Total-field scattered-field sources are used to separate the computation region into two distinct regions, one contains the total field (i.e., the sum of the incident field and the scattered field), while the

second region contains only the scattered field. The incident field is a plane wave with a wavevector normal to the injection surface. The mode source is basically a wave used to inject a guided mode into the simulation region [96, 97].

The boundary conditions in FDTD define the behavior of the field at the boundaries of the computation region. Here, it is important to add an absorbing layer for wave equations in order to simulate problems with open boundaries. Currently, the most commonly used is the perfectly matched layer (PML). It is a thin layer that has a high artificial absorption by incorporating fictitious loss terms. In this way, fields decay without being artificially reflected back into the problem space [96, 99].

Finally, to analyze the transmission and reflection spectrum and the power response of a system, FDTD incorporates the concept of monitors. The monitors allow calculating frequency domain quantities from a time-domain simulation. The key point here is to capture the resulting fields in the time domain and use a discrete Fourier transform to yield them into the frequency domain [97]. As a final consideration, it is important to remark that FDTD converges if the Courant stability condition is satisfied. Basically, it estimates the time step by the following equation:

$$c\Delta t \leq \frac{1}{\sqrt{\left(\frac{1}{(\Delta x)^2} + \frac{1}{(\Delta y)^2} + \frac{1}{(\Delta z)^2}\right)}}, \tag{2.9}$$

where Δt is the time step required for converge, c is the speed of light and Δx, Δy and Δz are the linear dimensions of the computation mesh cell.

Nowadays, FDTD is one of the most advanced methods for computation of the field distribution and to study other behaviors such as nonlinearities in photonic crystals. It has also been applied to a large variety of electromagnetic problems [96, 97]. There are some commercial and open source software packages that implements the FDTD method, such as MEEP, OptiFDTD, Lumerical FDTD Solution Tool and RSoft.

2.5.2 Plane Wave Expansion Method

The Plane Wave Expansion (PWE) method is a frequency-domain eigensolver which solves the eigenproblem for the frequencies of a periodic system such as PhC.

The discretization of Equation 2.1 through planewave expansion yields a finite generalized eigenproblem $Ax = \omega^2 Bx$, where A and B are $N \times N$ matrices, x the eigenvector and ω the eigenvalues. Here, the eigenvalues represent the frequencies while the eigenvectors contain amplitude coefficients of the plane wave components [100–102]. In particular, for a one dimensional PhC structure, the plane wave using Fourier series takes

the form:

$$u_k(x) = \sum_{n=-\infty}^{\infty} c_n(k) e^{i\frac{2\pi n}{a}x}, \tag{2.10}$$

where $u_k(x)$ is a periodic function $u_k(x) = u_k(x+a)$, where a is the lattice constant. $c_n(k) = \frac{1}{a}\int_0^a dx e^{-i\frac{2\pi n}{a}x} u_k(x)$ are the complex Fourier series coefficients.

In general, PWE method is best suited to analyze periodic structures with low to moderate index contrast where the size of the unit cell is less than a wavelength. Using the supercell method or absorbing boundary conditions, the PWE can be used to compute eigenmodes of waveguides, resonators, and structures of finite size. It is stable, fully vectorial, and rigorous in the sense that no approximations are made to Maxwells equations other than truncating the number of spatial harmonics representing the fields [100–102]. However, it is very inefficient for modeling metallic structures and can not directly incorporate material dispersion because frequency is the eigenvalue being solved. The PWE method may be the most popular approach for calculating band diagrams of periodic structures like PhC. It is a simple method to implement and enables rigorous analysis of 3D structures [56]. A free software tool called MPB (MIT Photonic Band-gap) is available for this purpose.

Chapter 3

Related Work

PhC structures have been applied to design devices towards the realization of all-optical telecommunication and information systems. Particularly, cavities and waveguides embedded in PhC can be used to design efficient all-optical computational devices with flexible functionalities. Several approaches have been applied to accomplish these PhC devices. Here, we present a literature review of several methods used to perform logic gates in PhC.

3.1 Logic Gates Based on Self-Collimation (SC)

A light beam is partially reflected and partially transmitted when incident on a PhC structure with a self-collimated region. Thus, a phase change occurs in the reflected beam with respect to the transmitted beam. This phase difference dependends on the radius of the dielectrics of SC PhC region. If another light beam with appropriate phase is launched, the reflected and transmitted beams may interfere constructively or destructively. Thus, logic gates based on SC PhC can be achieved by modifying the radii of the dielectrics and introducing different phase shifts between the incident beams at the input faces. Several works using this approach demonstrated a complete set of all-optical logic gates [24–27]. Figure 3.1 shows the schematic structure of the photonic crystal self-collimated device proposed by Zhang et al. [24]. This device is formed by two input faces (I_1, I_2) and two output faces (O_1, O_2). It can operate as OR and XOR logic gates by introducing a certain phase difference between the two beams (incident on the input faces I_1 and I_2). Thus, if the phase difference between the inputs $\phi_1(I_1) - \phi_2(I_2)$ is set as $2k\pi + \pi/2$, the output faces O_1 and O_2 operate as OR and XOR logic gates, respectively.

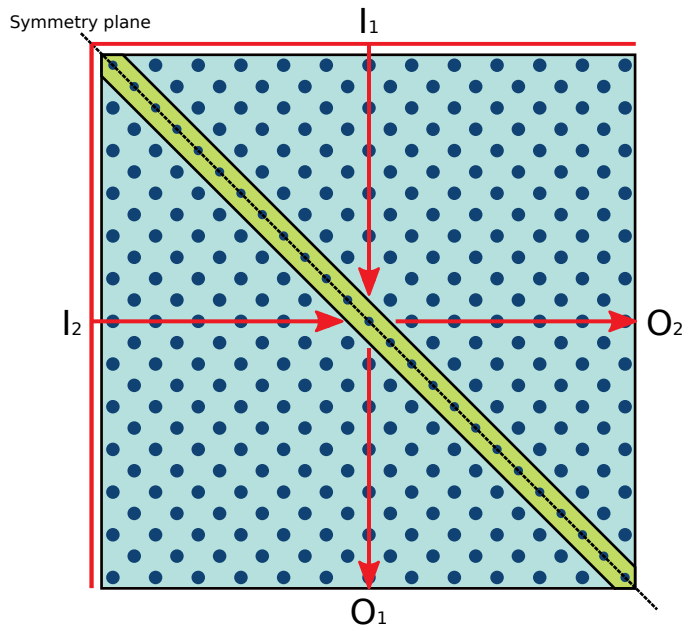


Figure 3.1: Schematic representation of PhC logic device based on self-collimated effect proposed in Ref. [24]. Adapted from Ref. [24].

3.2 Logic Gates Based on MMI (Multi-Mode Interference)

To accomplish logic gates based on MMI, the input logic values need to be determined only by the phase of the input signals for each gate. This can be achieved by using Binary Phase Shift Keyed (BPSK) signals, whereas the output logic value is determined by the amplitude of the output signal regardless of its phase. With the proper signal phases of the input signals, they interact together in the MMI area to either generate a signal, which corresponds to logic 1, or eliminate the signal generation, which corresponds to logic 0 at the output port. Then, the logic gates can be performed by the proper parameters selection in addition to the choice of the phases of the input signals, as demonstrated in the literature [28–31].

Figure 3.2 shows the schematic representation of the PhC MMI device proposed by Liu et al. [29]. It is formed by two input ports (A and B) and two output ports (X and Y). Thus, to achieve the logical functions, two kinds of BPSK signals are injected into each input port. In the case of XNOR gate, logic 1 for the input port A is expressed as signal phase 0, while logic 0 is expressed as signal phase π. Whereas the input port B expresses logic 1 as signal phase $-\pi/2$, while logic 0 is expressed as signal phase $\pi/2$. Similarly, the XOR, OR and NAND gates can be realized by selecting the proper input signal's phase for each logic.

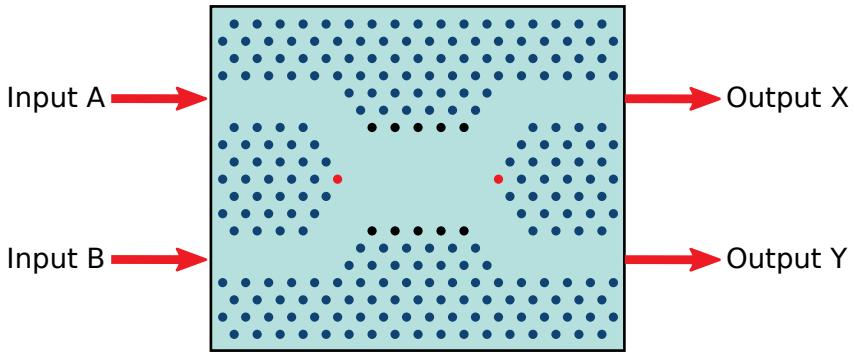


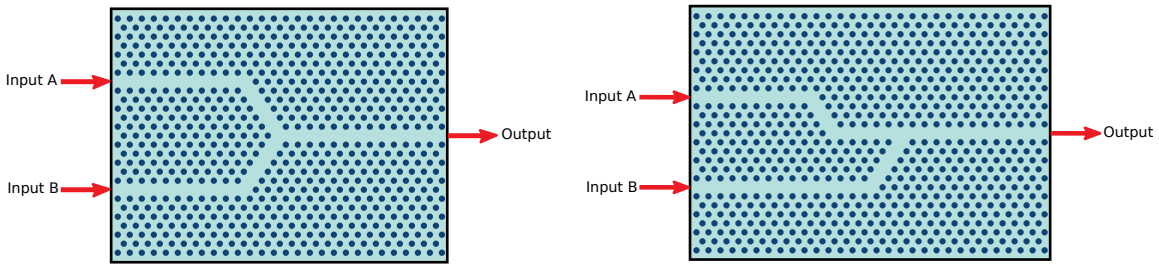
Figure 3.2: Schematic representation of PhC logic device based on MMI proposed in Ref. [29]. Red and black circles represent optimized rods. Adapted from Ref. [29].

3.3 Logic Gates Based on Waveguide Intereference Paths

This is a simple, useful, and effective approach to design logic gates in photonic crystals. In this scheme, the high transmission state (logic 1) is guaranteed if a constructive interference occurs between the input waveguides. This is accomplished by designing an intersection point with a path difference of 0, which generates a phase difference of $2k\pi$ (where $k = 0, 1, 2...$) between input signals. In contrast, if the designed path difference is one lattice constant, it generates a phase difference of $(2k + 1)\pi$, and destructive interference occurs between the inputs signals, achieving the low transmission state (logic 0).

Using this approach, the OR, XOR, NOT, XNOR, and NAND gates have been proposed theoretically by Fu et al. [32]. The structures were designed on a photonic crystal composed of a triangular lattice of cylindrical silicon rods, with a dielectric constant of 11.56, embedded in a background medium of air (refractive index 1). The lattice constant and the diameter of the silicon rods were 875 nm and 495 nm, respectively. The OR logic gate is formed by two intersecting waveguides (inputs) at 10.5×10^3 nm to the cross point between them, forming an angle of 120 and a phase difference of 0, as illustrated in Figure 3.3a. Thus, if a single beam is injected into one of the inputs, the signal light can propagate to the output through the waveguide, and a logical value of 1 can be obtained in the output. When two beams are injected in both input ports simultaneously, constructive interference occurs, and high power is observed in the output. Obviously, when no single beam is injected into any input port, no light comes to the output, corresponding to the logical value of zero.

For the XOR gate, the designed structure consists of two waveguides with one lattice constant of path difference to the cross point between them, as shown in Figure



(a) (b)

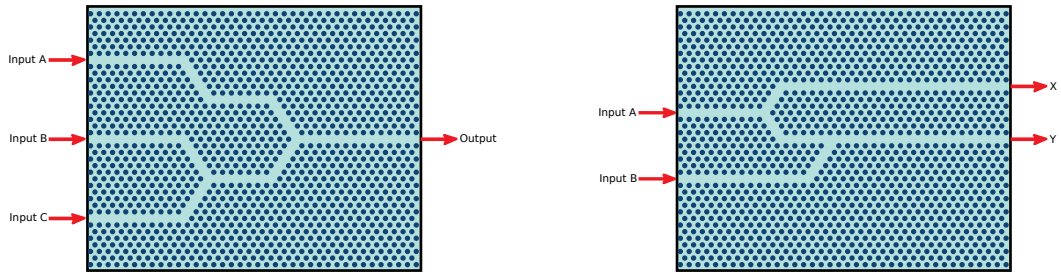
Figure 3.3: Schematic representation of PhC (a) OR and (b) XOR gates proposed in Ref. [32]. Adapted from Ref. [32].

3.3b. At this point, when the inputs are excited simultaneously with a continuous wave source, a phase difference of π generates a destructive interference, and the output signal is approximately zero (0.67 %). On the other hand, if only one input is excited, the output signal is greater than 75%. Thus, considering transmissions greater than 70% and lower than 1% as logic values 1 and 0, respectively, the XOR logic gate was carried out.

The XNOR and NAND gates structures were based on the XOR device, but introducing a control signal in order to generate a high transmission output when no light is injected into the input ports, i.e for the logic input case (0,0)=1. Thus, for these devices, transmission values greater than 85% and lower than 10% have been reported for logic values 1 and 0, respectively. The logic devices proposed can operate at the telecommunication window of 1550 nm and in the low power regime. Also, the author reported the intensity contrast ratio between the output signals for the logic states of 1 and 0 as high as 20 dB.

Using the same parameters, Caballero et al. addressed the Majority and the Feynman gates [103]. The former allows the creation of simple and optimized computational circuits, and the latter is a reversible logic device designed targeting to achieve circuits within the thermodynamic limit of computation. For the Majority gate, illustrated in Figure 3.4a, the authors reported that transmission values at the output greater than 85% and lower than 35% can be interpreted as logic 1 and 0, respectively. For the Feynman gate, shown in Figure 3.4b, the equivalent transmission for the logic 1 was found as high as 40% while transmissions values lower than 10% correspond to the logic 0.

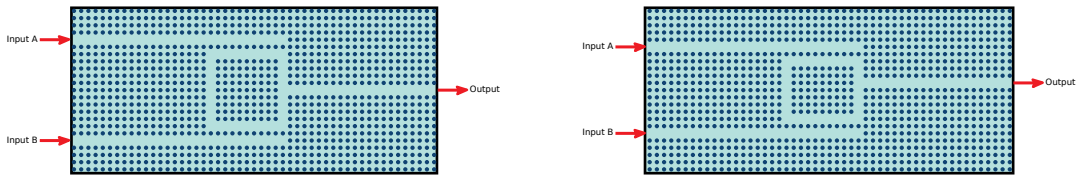
Employing the control interference effect in a two-dimensional photonic crystal composed of a square lattice of cylindrical silicon rods, with a dielectric constant of 11.56, embedded in a background medium of air, D'souza and Mathew demonstrated the operation of the OR, XOR, NOT, and AND logic gates [34]. The parameters of the based structure were 650 nm for the lattice constant and 230 nm for the radii of the rods. The devices are formed by a square ring resonator waveguide with three other linear waveguides which are connected to each other by the ring resonator, as illustrated in Figure 3.5. The principle is that the signal injected into the input waveguides split into two through



(a) (b)

Figure 3.4: Schematic representation of PhC (a) Majority and (b) Feynman gates proposed in Ref. [103]. Adapted from Ref. [103].

the ring resonator. One travels in the clockwise and the other in the counterclockwise direction. If a constructive interference occurs, a larger output energy is obtained at the output and the OR, and AND gates were accomplished. Engineering the ring resonator to produce destructive interference, the XOR and NOT logic gates were also demonstrated. The advantage of these devices is that they can operate at different wavelengths around the 1550 nm window. In addition, a contrast ratio higher than 35 dB was reported by the authors.



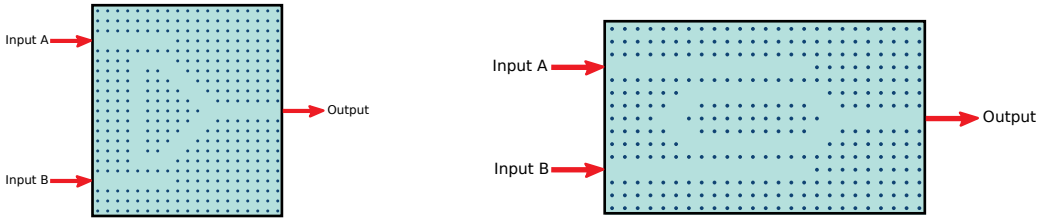
(a) (b)

Figure 3.5: Schematic representation of PhC (a) AND and (b) XOR gates proposed in Ref. [34]. Adapted from Ref. [34].

A methodology to evaluate the effect of structural disorder on photonic crystals logic gates was applied to these devices in order to figure out their robustness and fault tolerance [36]. The study was based on the evaluation of two metrics: the error rate (ER) and the mean absolute deviation of transmission of the error cases (MATEC). ER is the probability that a fabricated photonic crystal logic gate does not accomplish its logic function correctly, and MATEC measures the imperfection degree of the device through the transmission coefficient. The authors found that, for structures with a triangular lattice, regions in the corners and close to the output are more critical to ER and MATEC, respectively. For structures with a square lattice, the intersection regions are the most sensitive for both metrics.

Hussein et al. introduced new designs of all-optical OR, AND, XOR, NOT, NOR, NAND and XNOR logic gates based on the interference effect [38]. The designs were created using 2D square lattice photonic crystal structures of germanium (Ge) rods, with a relative permittivity of 16, embedded in a background of air. The radius of the rods was

set as $0.15a$, where a is the lattice constant and its value was selected as 580 nm to get a operational wavelength of 1550 nm. The interference effect to achieve the logical function is designed via an optical resonator induced for each structure, as shown in Figure 3.6. Optical bit rates ranging from 3.8 to 7.6 Tbps and contrast ratio from 5.036 dB to 12.15 dB were reported in this work.



(a) (b)

Figure 3.6: Schematic representation of PhC (a) AND and (b) OR gates proposed in Ref. [38]. Adapted from Ref. [38].

Caballero et al. accomplished an integrated and compact photonic crystal (PhC) device that can operate as a NAND or NOR logic gate [39], shown in Figure 3.7. It is designed in a PhC slab composed of GaAs/AlGaAs heterostructure and a 2D pattern of a triangular lattice of holes. By modifying target holes on the structure, the NAND or NOR gates can be achieved. The simulation results reported by authors show that the upper power limit to represent the logic 0 is $0.17Pin$, where Pin is the input power. On the other hand, the lower power limit to represent the logic 1 is found to be $0.50Pin$. The NAND and NOR logic gates present a response time of 5 ps, resulting in a clock rate of 200 GHz. They also operate within the C band of the telecommunication window (between 1530 and 1565 nm).

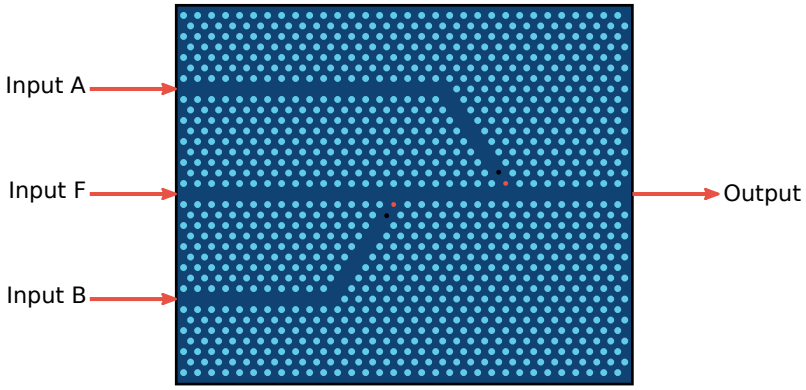


Figure 3.7: Schematic representation of the XY view of the integrated PhC compact device. In this, dark and light colors correspond to two different dielectric constant ε_1 and ε_2, respectively. With $\varepsilon_1 > \varepsilon_2$. Red and black circles represents the target holes to be optimized to achieve the NAND and NOR logic functions in our PhC structure. Adapted from Ref. [39].

3.4 Logic Gates Based on Kerr Effect

To accomplish logic devices using the Kerr effect on PhC, a waveguide-cavity coupled system need to be introduced on the structure and the power of the inputs need to be properly selected.

Using this scheme, a high-contrast all-optical bistable switching was proposed by Yanik et al. [78]. The device is a 2D photonic crystal composed of a square lattice of dielectric rods ($\varepsilon = 12.25$) embedded in air, as illustrated in Figure 3.8. To achieve the optical bistability, a waveguide was side-coupled to a single-mode cavity with instantaneous Kerr nonlinearity. Consequently, the high transmission state is accomplished when the cavity is OFF resonance with the excitation and the field inside the cavity is low, making the decaying field amplitude from the cavity negligible. In contrast, when the field intensity inside the cavity is much higher, it pulls the cavity resonance frequency down to the excitation frequency of the incident field, and the low transmission state is achieved. To prove the correctness of the bistability, a coupled-mode theory was applied and presented excellent agreement with FDTD simulations.

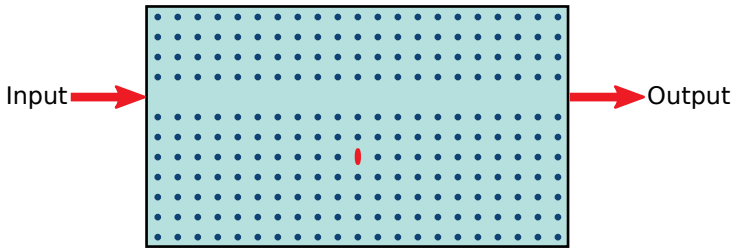


Figure 3.8: Schematic representation of the PhC Switch proposed in Ref. [78]. Red ellipses represent nonlinear materials. Adapted from Ref. [78].

In a following work performed by the same research group, the first all-optical transistor in photonic crystals was proposed [89]. The structure consists of two waveguides, input and control, arranged in a cross geometry. Additionally, a cavity with instantaneous Kerr nonlinearity was inserted in the waveguides intersection, as shown in Figure 3.9. With this configuration, the cross-talk between the waveguides is prohibited due to modal symmetry; consequently, each waveguide couples only to the cavity mode with the same axis symmetry. FDTD simulations were performed to show the transistor operation. Thus, the ON state is reached at 25 ps when the input and control waveguides are excited with input powers about 200 mW/μm. Otherwise, if only the input waveguide is launched, the transistor is on the OFF state. The advantages of the proposed device are the small footprint of a few micrometers squared and the requirement of only a few milliwatts of power at a 10Gbit/s switching rate.

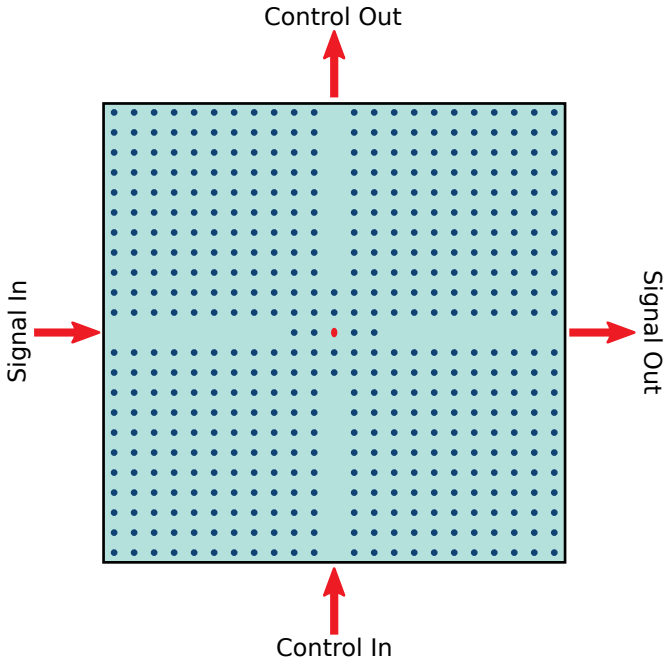


Figure 3.9: Schematic representation of the PhC transistor proposed in Ref. [89]. Red ellipses represent nonlinear materials. Adapted from Ref. [89].

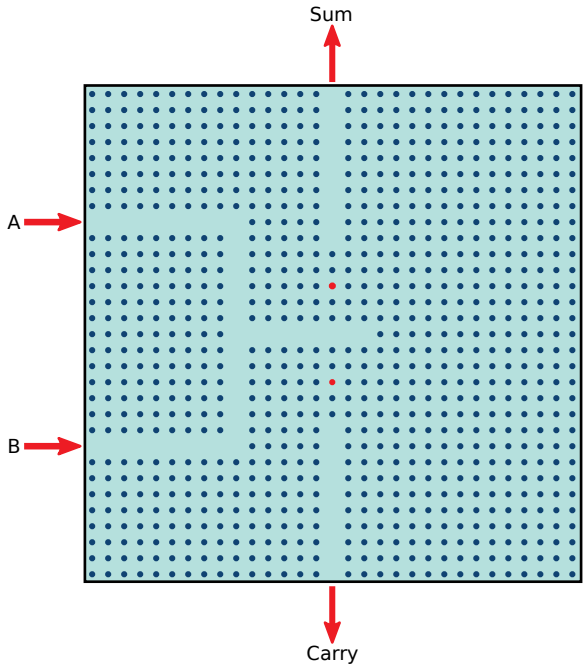


Figure 3.10: Schematic representation of the PhC half adder proposed in Ref. [43]. Red circles represent nonlinear materials. Adapted from Ref. [43].

In the search for useful multipurpose devices, an all-optical half adder based on photonic crystals resonant cavities was proposed by Neisy et al. [43]. The designed structure is composed of a 31×31 square array of dielectric rods ($\varepsilon = 11.97$) immersed in air. Two inputs waveguides and two nonlinear resonant cavities, as can be observed in Figure

3.10, were introduced and optimized to get the correct behavior for the resonant frequencies. To prove the functionality as a half adder, a continuous wave with a wavelength of 1551 nm and an optical intensity of 10 mW/μm^2 is used as input source. Values greater than 70% and lower than 5% were reported to be considered as logic 1 and logic 0, respectively. Compactness and low delay rate of about 3 ps are highlighted as the main advantages of the proposed structure.

In the same direction, a photonic crystal 1-bit full adder was designed by [42]. The structure was developed by cascading two optical 1-bit half-adders. The final structure consists of eight optical waveguides and two nonlinear resonant rings, created inside a rod type two-dimensional photonic crystal with square lattice. The structure has X, Y and Z as input waveguides and, SUM and CARRY as output ports waveguides. The performance and functionality of the adder were validated by means of the FDTD method. Normalized transmission values greater than 60% and less than 5% were considered as logic 1 and logic 0, respectively. In addition, a delay time of 1.5 ps and an overall footprint of about 439μm^2 were reported.

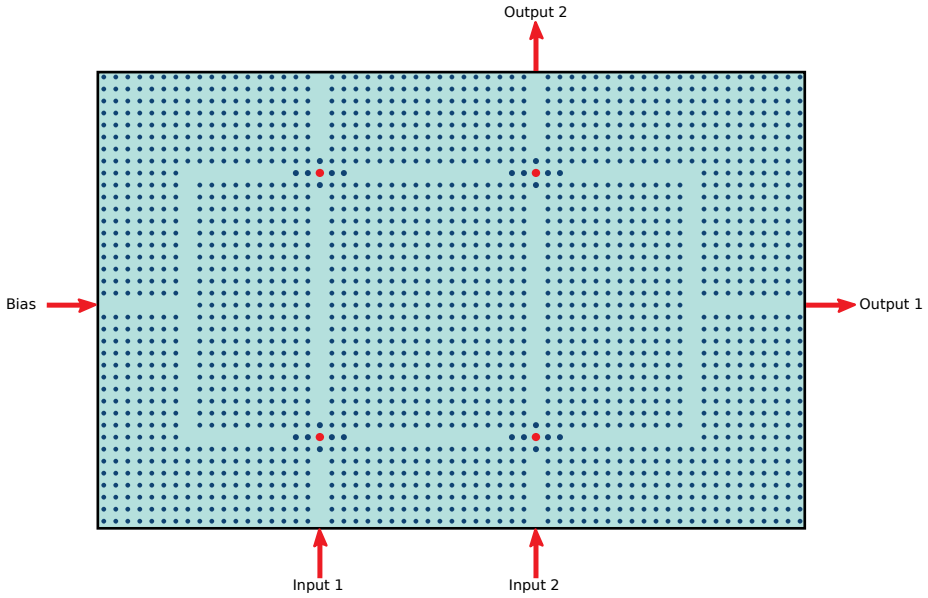


Figure 3.11: Schematic representation of the PhC reversible XOR and XNOR gates proposed in Ref. [44]. Red circles represent nonlinear materials. Adapted from Ref. [44].

The energy dissipation produced by the information loss is currently a concern in the design and fabrication of logic circuits. R. Landauer showed that there is a great amount of energy dissipation inside large scale digital circuits because of information loss, which is an inevitable phenomenon in irreversible logic gates [104]. However, in reversible logic gates, due to one-to-one mapping between the input ports and output ports, it is possible to obtain the state of input ports from the output ports. As a result, no information loss is presented, so the energy dissipation can be reduced. Thus, all-optical reversible XOR and XNOR gates based on electromagnetic scattering phenomenon in

nonlinear photonic crystal structures were reported [44]. The designed devices consist of two cross-connected waveguides acting as inputs and outputs along with some linear and nonlinear defect rods, illustrated in Figure 3.11. A 2DPhC with cubic lattice was used as the fundamental structure. The operation principle to get the XOR reversible logic is to map one of the inputs to one of the outputs, and compute in the second output the conventional XOR operation. For the XNOR, the inverse of one input is mapped to one of the outputs, and the conventional XNOR operation is performed in the second output. The results showed the correct operation of the logic gates for transmission values greater than 65% and lower than 2% considered as logic 1 and logic 0, respectively. The authors also reported a 10 ps of a maximum time delay to get the logic answer.

3.5 Logic Gates Based on Alternatives Approaches

Some other strategies have been addressed to project PhC logic gates. Examples of these are: semiconductor-optical-amplifier (SOA), PhC fiber, topological cavity and edge states, stimulated Raman scattering, Mach-Zehnder interferometer [37, 45–54]. All of these works reviewed here prove that PhC are good candidates to develop computational logic devices with low power consumption, high-efficiency and with high-speed data processing.

3.6 Summary

In this section we discuss the advantages and disadvantages of the strategies to design PhC logic gates, together with a description of the most relevant achievements of this literature review.

PhC logic gates based on self-collimation present small area, fast response, wide operating frequency bandwidth, and low power operation. Indeed, their size can be reduced to the operating wavelength order. They are also independent of light intensity allowing operation in a low power regime. However, they lack a high contrast ratio, and their microfabrication is challenging to achieve since it is hard to control the dispersion relations to achieve the self-collimation effect. Besides, they need phase shifters to synchronize input signals, increasing the device size and limiting their adjacent connection.

Logic Gates (LG) based on this approach can be suitable for hybrid system integration, signal processing, extreme environments sensors, and frequency shifters.

PhC logic gates based on MMI exhibit small size, fast response, large operating frequency bandwidth and low power operation. The compactness of the MMI region ensures their simple configuration, robustness and low loss. In addition, low power operation is accomplished because of their light intensity independence. Nevertheless, they need to adopt different phase values to achieve the logic state representations. This fact brings inconvenience towards the development of integrated circuits because it increases their size and leads to strict fabrication processes. In general, this scheme can be used to project extreme environments sensors, frequency shifters, splitters, demultiplexers and signal processors.

In general, PhC logic gates based on waveguide interference paths have wide operating frequency bandwidth, low power operation, fast response, and reasonable contrast ratio. They are simple designs for two and three inputs logic gates showing high availability and fault tolerance. They can also operate within the entire bandgap of the PhC. Their input power independence also allows the operation in the low power regime with low losses and slight heat dissipation. In contrast, their size typically is in the order of few microns above the operating wavelength. Also, logic gates up to three inputs are challenging to achieve since it is difficult to synchronize and control the phase difference for the light input signals. This fact can also latch their microfabrication. In addition, the feedback propagation to the inactive inputs has limited their application for large scale circuits. In particular, these kinds of devices can be extensively used for applications in signal processing, routing, parallel computing, and hybrid system integration.

Nonlinear PhC logic gates can reach high contrast ratios and are input phase independent. LG based on this approach can have high power operation due to the required optical control pulse to generate the nonlinear effects. Also, the response time and the bandwidth are limited by the nonlinear material and the resonant frequency of the resonator, respectively. LG based on this approach are good candidates for integrated photonic devices, sensors, switching, and signal processing. They can also be applied towards the realization of PhC logic circuits.

Table 3.1 condensates the information achieved in this literature review exploiting the advantages, weakness and possible applications of each method to accomplish logic gates in PhC.

Overall, the development of PhC logic gates has gained attention in recent years due to the importance of these systems to build the future of the fully photonic communication and computer systems. Here, we have evaluated 143 papers related to this subject retrieved from IEEE, IET, AIP, OSA, Elsevier, IOP, Springer. These are summarized in Figure 3.12. It shows the increasing number of papers published per year (see Figure 3.12a), compiled on 75% of journal manuscripts and 25 % proceedings and conference

Logic Gate Method	Advantages	Weakness	Possible Applications
Self-Collimation	Small area Fast response Wide operating frequency bandwidth Low power operation	Low contrast ratio Hard microfabrication Input phase requirement	Hybrid system integration Signal processing Extreme environments sensors Frequency shifters
MMI	Small size Fast response Large operating frequency bandwidth Low power operation	Different phase for logic representation Input phase requirement	Splitters Demultiplexers Signal processing Extreme environments sensors Frequency shifters
Waveguide Interference Paths	Wide operating frequency bandwidth Low power operation Fast response Reasonable contrast ratio	Large size Difficult to synchronize the phase difference	Signal processing Routing Parallel computing Hybrid system integration
Nonlinear Effects	High contrast ratio Input phase independent	Narrow operating frequency bandwidth High power consumption Slow response	Sensors Signal processing Switching Integrated photonics devices Logic circuits

Table 3.1: Summary of the advanced, weakness and possible applications for each PhC logic gates approach.

meetings. As expected, we found that the most used logic gates to build circuits appear at the top of the implementations, as illustrated in Figure 3.12b. On the other hand, Figure 3.12c shows that logic gates are implemented on a PhC lattice configuration of rods on air and holes in a substrate with 83% and 16%, respectively. It can explain the poor number of experimental works (3%) since the former is still a challenging fabrication process. Finally, we found that employed materials are the most common in integrated photonic technology, such as Si, GaAs, SiO_2, AlGaAs, InP, Ag-Polymer, Lithium Niobate, Germanium and Chalcogenide glasses, as illustrated in Figure 3.12d.

We evidenced in this literature review interesting advances in the field of PhC logic gates suitable for a wide range of integrated photonics technology applications, such as signal processing, sensors, telecommunications, routing, and computing. However, it is important to mention that these achievements presented isolated logic devices and components. Thus, it still remains a big challenge to demonstrate PhC integrated circuits by concatenating logic devices to allow the design of microprocessors. We also call attention to the fabrication, and experimental demonstration of the different PhC logic devices explained here. Lastly, we evidenced the lack of a standard methodology to guide the design of PhC integrated circuits since we found that different dimensions, unequal transmission, or power values representing the same logic value can generate undesirable behaviors of the devices within the same approach.

This work intends to address possible solutions to these drawbacks by proposing the Complementary Photonic Crystal Integrated Logic Devices. It consists of two fun-

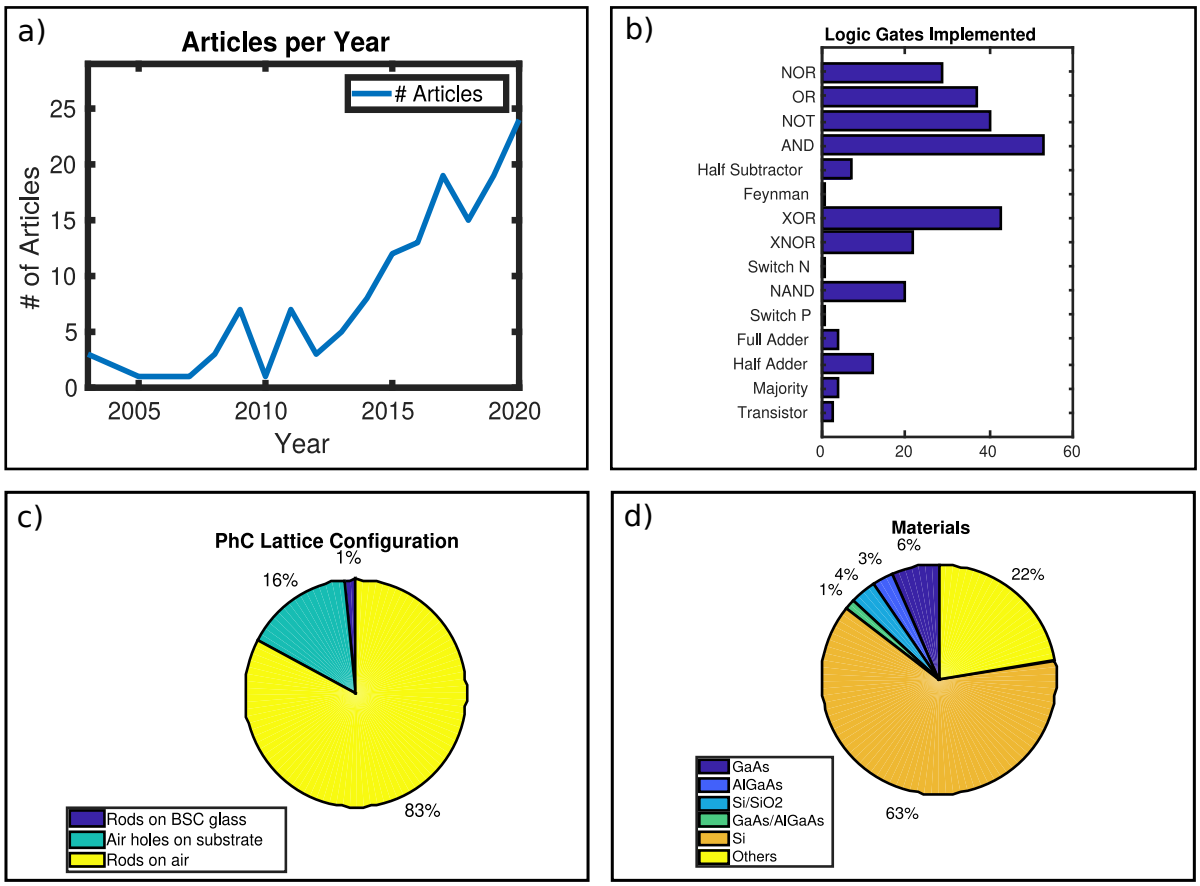


Figure 3.12: Summary of the PhC logic gates literature review. a) Articles published per year. b) Number of logic gates implemented. c) PhC lattice configurations and d) materials used to design logic gates.

damental devices (Switches N and P), PhC analogous to the NMOS and PMOS logic transistors of CMOS technology. We aim to design manufacturable core hardware devices operating at the same input/output frequency, with well-defined power values representing logic states 0 and 1, available to support the development of PhC logic circuits and computational systems. So, we will be able to design logic circuits in a similar way as in conventional digital electronics.

Chapter 4

Complementary Photonic Crystal Integrated Logic Devices

This chapter presents the proposed designs and theoretical demonstration of the Switches N and P (SwN and SwP), PhCs equivalent to NMOS and PMOS logic transistors, respectively. These switches together stand for Complementary Photonic Crystal Integrated Logic (CPCL). For the first time, they allow the development of PhC integrated logic circuits by their adjacent connection, like CMOS transistors for electronic digital circuits.

4.1 Designing the Photonic Crystal Structure

This section details the design of our PhC components including: the slab heterostructure, the 2D pattern and the logic representation approach. Equally important, it describes the simulation setup. All of these components play an important role to achieve the PhC integrated SwN, SwP and circuits.

4.1.1 PhC Slab Heterostructure

In order to design our integrated devices, we first built the slab of our PhC structure. It consists of a GaAs core of 500 nm with 180 nm of $Al_{0.25}Ga_{0.75}As$ cladding on top and down sides, and a 1500 nm buffer of $Al_{0.6}Ga_{0.4}As$, as illustrated in Figure 4.1a. We choose this kind of heterostructure because it exhibits interesting properties for nonlinear systems and monolithic integration, and can be experimentally grown with current fabrication techniques [67]. We then built a ridge waveguide in the PhC slab that we will use as input and output channels for the switches. The width of the ridge was set

as $a\sqrt{3} - 2r$, where a and r will be defined below and are parameters related to the 2D pattern of our PhC structure. Figure 4.1a and 4.1b show the YZ view of its schematic representation and the 3D representation of the PhC waveguide, respectively.

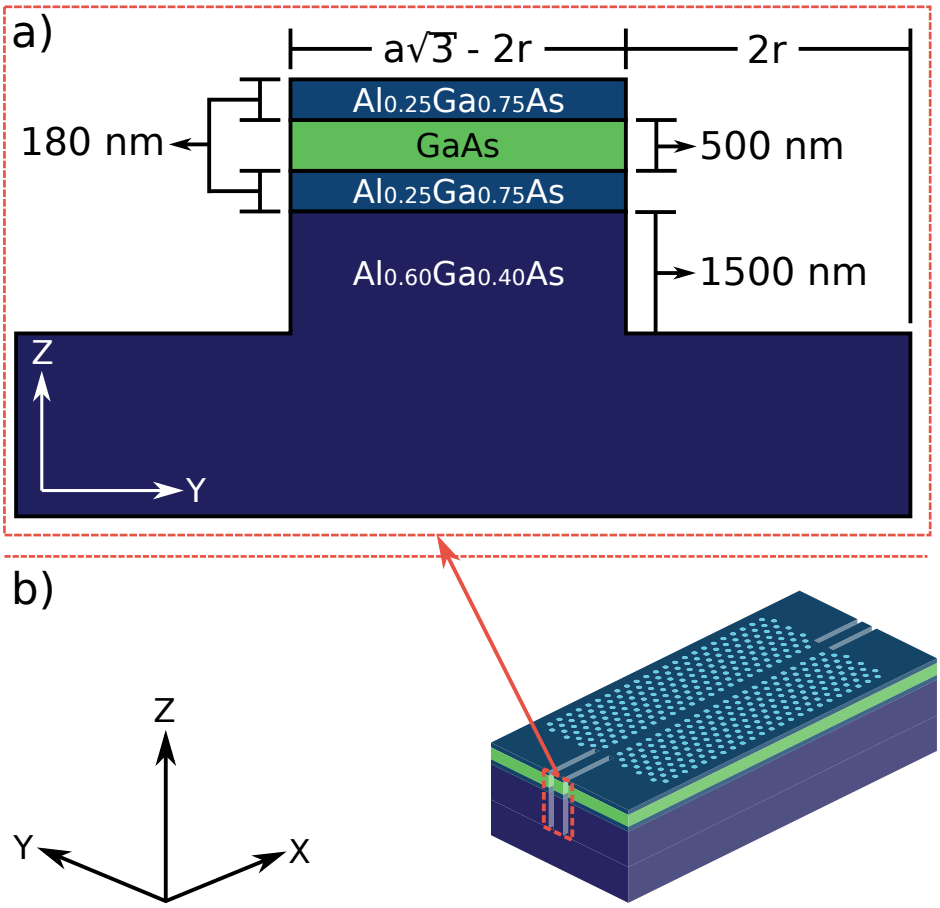


Figure 4.1: a) Design of the integrated PhC slab waveguide. Schematic representation of the YZ view of the Ridge waveguide of our PhC waveguide. b) 3D view of the PhC waveguide.

We evaluated, through the MODE Solutions tool, the effective refractive index (n_{eff}) as a function of the GaAs core width, as illustrated in Figure 4.2. As can be noted, the single-mode cutoff appears at 540 nm. Thus, for a 500 nm of GaAs core width, we guarantee a single-mode propagation because fabrication errors should be less than a few nanometers. For this dimension, we found an n_{eff} of 2.87 with 0.3740 dB/cm of mode loss. The inset of Figure 4.2 shows the intensity distributions and the strong confinement of the fundamental TE00 mode of the ridge waveguide.

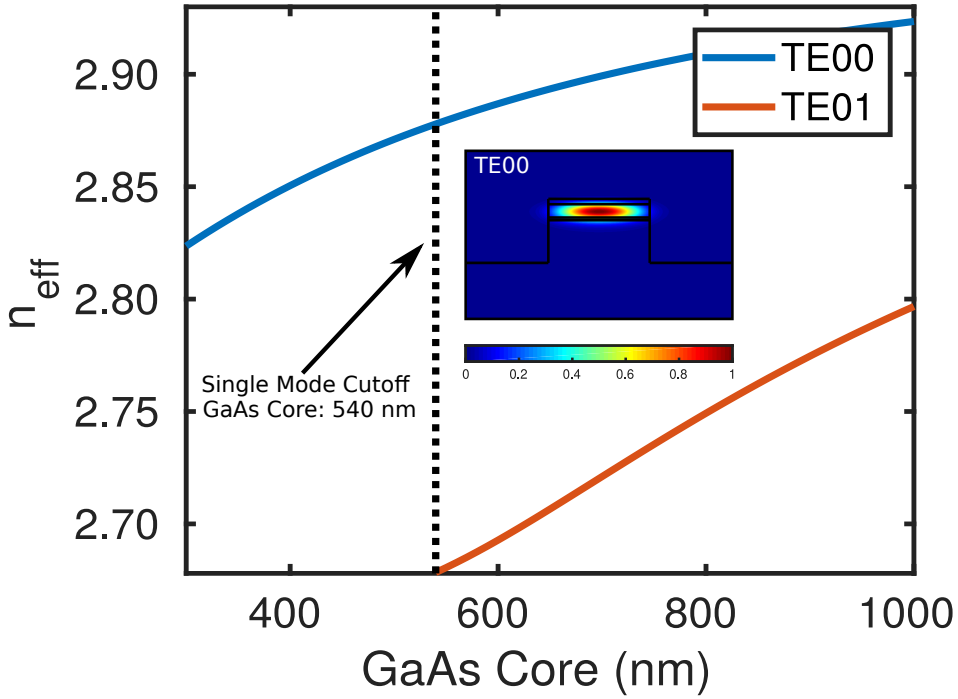


Figure 4.2: The effective refractive index as a function of the GaAs core height. The single-mode cutoff appears at 540 nm of GaAs core height.

4.1.2 PhC 2D Pattern

We then designed the 2D pattern of our PhC structure. It is composed of a triangular lattice of holes with radius $r = 0.31a$, where a is the lattice constant, i.e., the distance between the center of two adjacent holes, embedded in a dielectric medium with refractive index $n = 2.87$. We computed its band diagram employing the MIT Photonic Band Gap (MPB) package [101] finding a TE-like gap of 26% from $0.2514(a/\lambda)$ to $0.3269(a/\lambda)$, as illustrated in Figure 4.3. In effect, to get an operating wavelength of $\lambda = 1550$ nm, which is commonly used in the telecommunication window, we set $a = 420$ nm and $r = 130$ nm.

We also calculated the propagation loss of a PhC waveguide for a length (L) of 250 μm, as illustrated in Figure 4.4a. We found a propagation loss of 0.8238 dB. We then performed a similar calculation for a PhC bend waveguide with L = 250 μm and height (H) of about 11 μm ($15a$), represented in Figure 4.4b. Simulation results showed a propagation loss of 0.9324 dB for this kind of structure. Thus, we ensure low propagation loss considering that the footprint of our devices is less than 80 $\mu m \times 50$ μm.

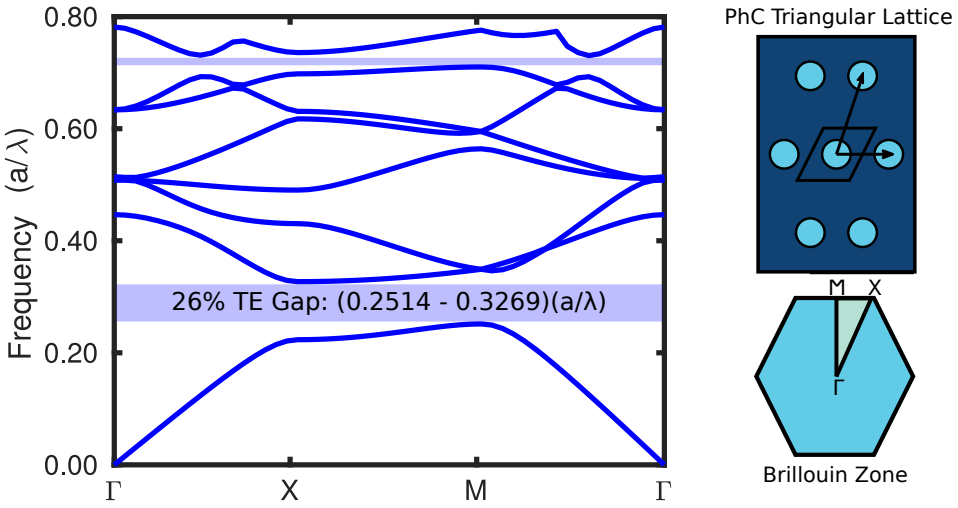


Figure 4.3: Band diagram of our PhC structure composed of triangular lattice of holes embedded in a dielectric medium ($n = 2.87$).

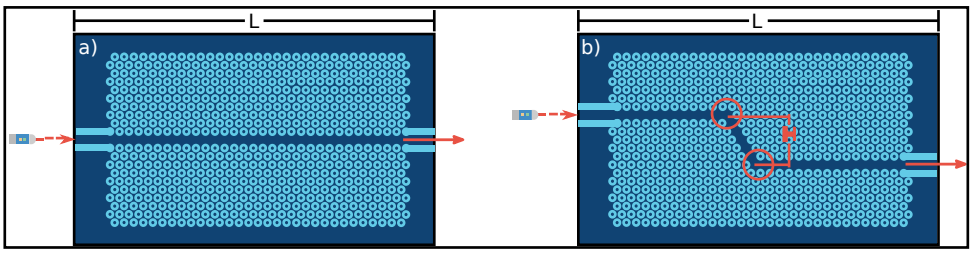


Figure 4.4: a) Schematic representation of the PhC waveguide with length (L) to calculate propagation loss of the strucure. b) PhC bend waveguide, red circles indicates the bends of the structure and the height (H).

4.1.3 PhC Efficient Y-Junction and Splitter

A PhC splitter is a device with the essential function to convert a single-mode signal in the input waveguide symmetrically into two single-mode signals in the output waveguides. Also, it can efficiently work as a junction and couple two different waveguides branches into one. These devices are basic elements used in the field of optical communication to create devices such as beam splitters and wavelength division multiplexing (WDM) systems. In this work, they will be used as a components to build the Switch N and circuits. We fit the Y-Junction proposed by Wilson et al. to our PhC structure since it was experimentally fabricated and based on a similar heterostructure [67]. We found through numerical simulations that the PhC Y-Junction exhibits an output of 86% of the total input applied P_{in}, as illustrated in Figure 4.5. On the other hand, the PhC splitter divides the input power P_{in} into two branches with about $0.43P_{in}$ each, as shown in Figure 4.6.

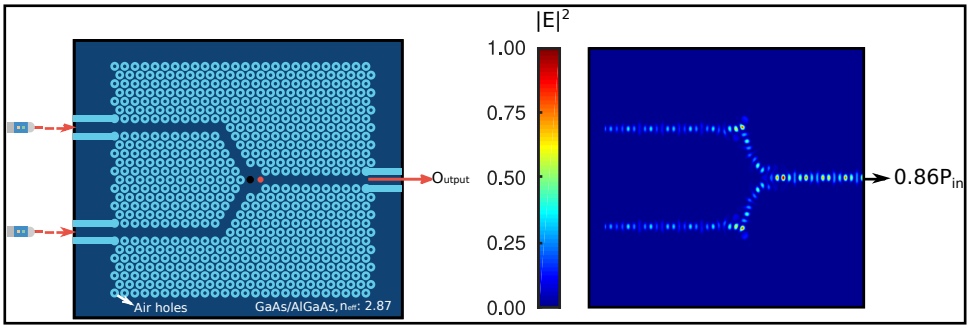


Figure 4.5: Design of the PhC efficient Y-Junction and normalized intensity distribution of the optical propagating mode.

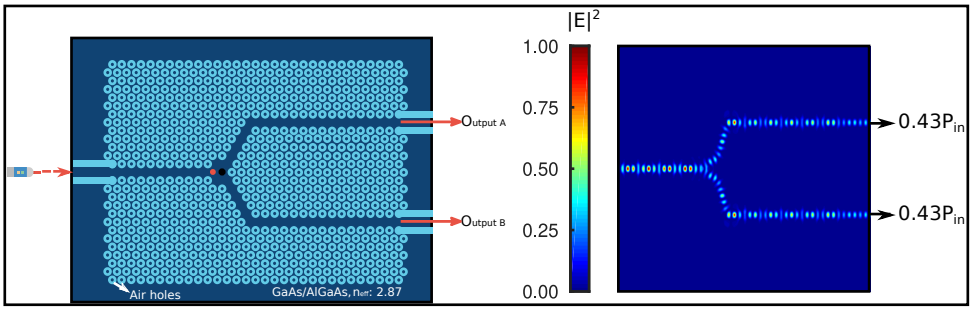


Figure 4.6: Design of the PhC efficient Splitter and normalized intensity distribution of the optical propagating mode.

4.1.4 PhC Logic Representation Approach

In order to achieve the logic state representations, we exploited a PhC nonlinear Waveguide-Cavity side coupled system, previously detailed in Section 2.2.3 and Section 2.4. Figure 4.7 represents the non-linear typical behavior used here to achieve the logic state representations. In this, we can observe that applying an input power P_0 into the system, it will exhibit an absorption peak, corresponding to the resonant frequency of the cavity, ω_0 [blue curve in Fig. 4.7]. By increasing the input power to P_1, the introduced nonlinearity induces a change of the refractive index, Δn, inside the cavity and a downwards shift of its resonant frequency to ω_1 is observed [red curve in Fig. 4.7]. Thus, if we define ω_{op} (close to ω_0) as the input reference frequency, we can have well-defined output power values to represent the logic states 0 and 1 applying a low input power. With this, we are now able to integrate these components into one system and project the switches N and P.

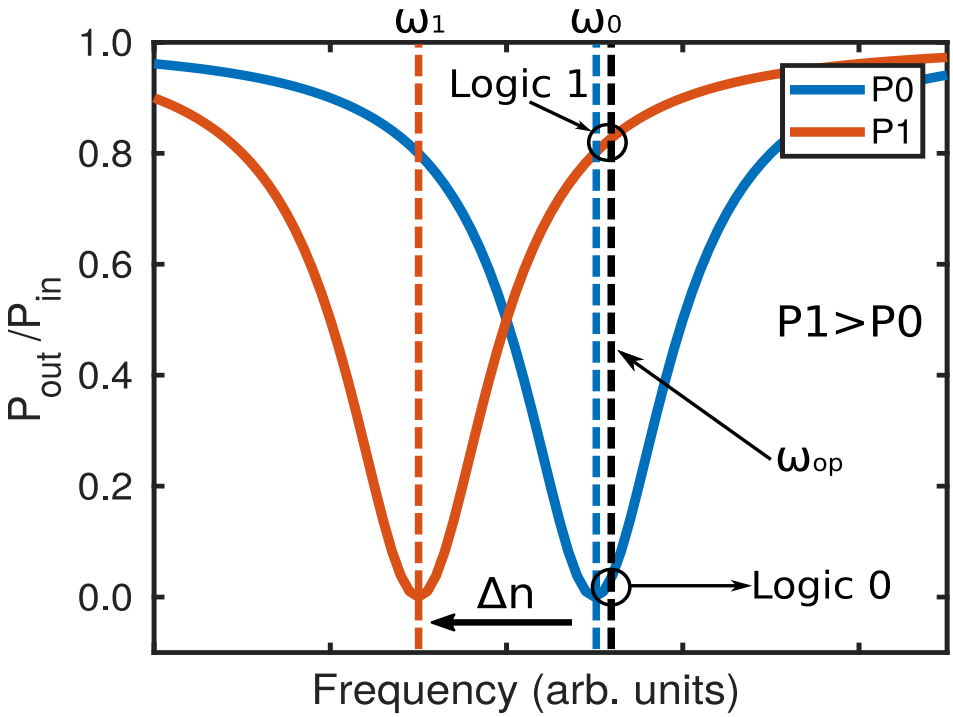


Figure 4.7: PhC approach used to achieve the logic state representations. It shows the typical behavior of a nonlinear cavity-waveguide coupled system in a PhC. A shift to lower frequencies of the cavity resonance frequency (red curve) is observed under high input power (P_1). The blue curve represents the transmission spectrum under low input power (P_0). So, we can achieve well defined representations for Logic 0 and 1.

4.1.5 Simulation Setup

For the design of the devices, gates and circuits, we adopt the Finite-Difference Time-Domain (FDTD) method using the Lumerical FDTD Solution Tool to demonstrate the correct operation of the PhC components, thus ensuring accurate and reliable numerical simulations. First, we set the simulation Courant stability condition in 0.7 with a time step of 0.04 fs and space step of 0.02 μm. The Perfectly Matched Layer (PML) has a thickness of the order of the operating wavelength, i.e., about 1550 nm. Then, we divide the simulation space into three sections: Input (IS), PhC Processing Logic Unit (PPLUS), and Output (OS), as graphically described in Figure 4.8.

In the IS, we place all input sources and input waveguides. So, to represent logic 1, we use a 50 mW Gaussian pulse centered at 193.41 THz (1550 nm) and a full-width of 0.24 THz. On the other hand, the absence of a light signal means logic 0. The PPLUS is the core of the device and where the logic takes place. In this sense, we can add or string the Switches N and P to obtain the desired logic function at the output of our system. Finally, in the OS, we place the output waveguides and the field and power monitors. These monitors collect the field profile in the frequency domain from simulation results

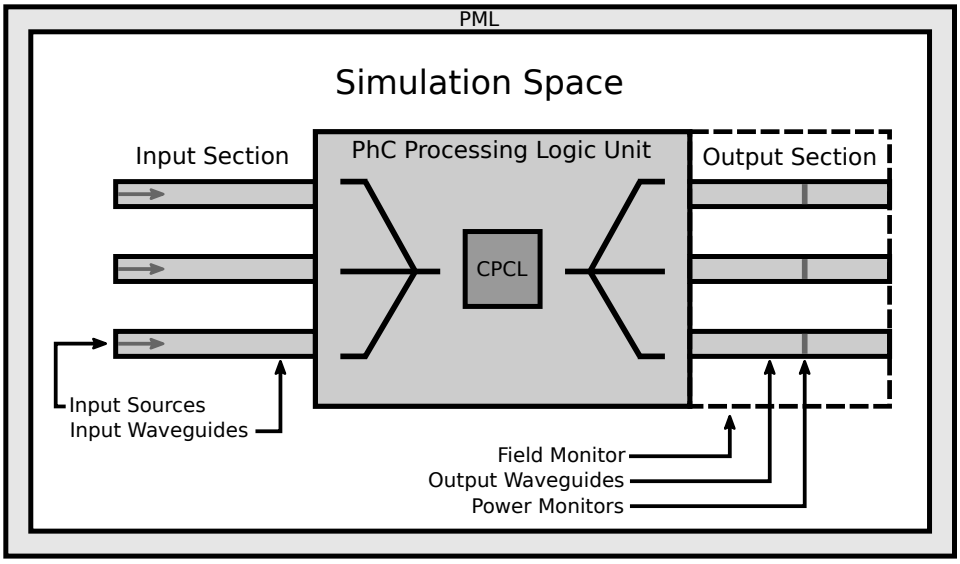


Figure 4.8: Sketch of a typical simulation space of a PhC integrated circuit. It is divided in three sections: Input (IS), PhC Processing Logic Unit (PPLUS) and Output (OS).

across some spatial region within the simulation in the FDTD. Essentially, the E (Electric field), H (Magnetic field), P (Poynting vector) and T (Transmission) as a function of frequency are calculated by applying a Fourier transform on the simulation time collected data. Here, we capture the intensity distribution at the steady-state at $\omega_{op} = 193.45$ THz. In addition, we compute the power value at the output waveguides. Aiming to optimize the computational resources, the monitoring of the intensity distribution system will be carried out in OS. We then analyze the performance of our system, transforming the power response into a logic response. So, we define a high logic threshold (P_1) and power values to represent logic 1. In contrast, power values below the lower threshold (P_0) will represent the logic 0. Then, we proceed to calculate the ON-OFF contrast ratio (CR) of the device, as follow:

$$CR = 10Log_{10}(P_1/P_0)\ dB. \tag{4.1}$$

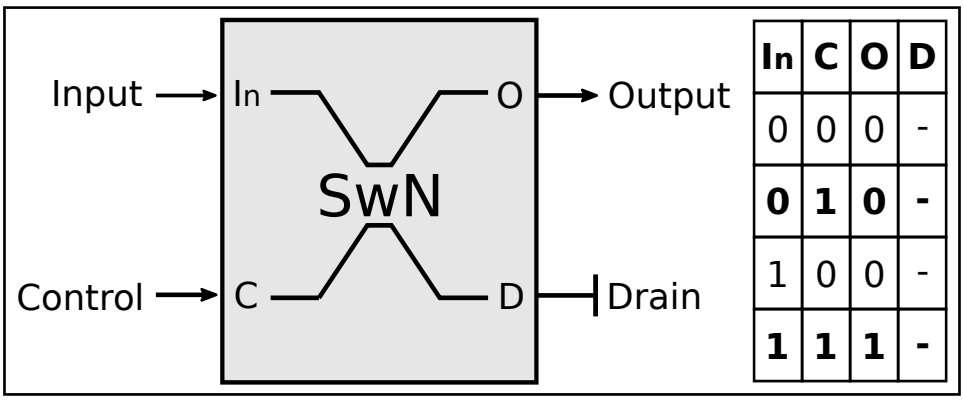
Later we compute the average of the energy loss ratio (ELR) obtained for each input combination. The ELR is defined as follow:

$$ELR = 1 - \frac{\sum Pc}{P_{in}}, \tag{4.2}$$

where $\sum Pc$ is the sum of the computed power at each terminal of the system, i.e., the output, drains, the feedback power at the inputs and the power stored at the cavities. These components will be detailed in the next section. P_{in} is the total input power applied into the system.

4.2 Switch N

The PhC integrated Switch N (SwN) proposed in this work, named in analogy with the NMOS transistor, is composed of four terminals, called input, control, output, and drain, as graphically represented in Figure 4.9. At this point, it is important to mention that the drain is not used in the logic datapath.



In	C	O	D
0	0	0	-
0	**1**	**0**	**-**
1	0	0	-
1	**1**	**1**	**-**

Figure 4.9: Diagram representation of the PhC integrated Switch N (SwN) and its truth table.

The output (O) of the SwN logic function is defined as follow:

$$\text{SwN(In,C)} = \begin{cases} \text{In} & \text{if C is logic 1} \\ 0 & \text{if C is logic 0} \end{cases} \tag{4.3}$$

where In and C are the input and control terminals. The SwN truth table can also be observed in Figure 4.9.

Figure 4.10 shows the designed device to accomplish the SwN logic function in the PhC structure. In this, we first added two ridge waveguides to be used as input and control terminals. Then, we combined them through a PhC waveguide to form a path difference of 0. This fact implies that constructive interference will occur if C and In are active at the same time. Consequently, high power will flow to the output system allowing to represent the logic state 1. On the other hand, if only one source is active, low power will be carried to the output, obtaining logic state 0. Next, we embedded an optimized Y-Junction to reduce the losses due to bend waveguides [67]. The radii of the initial and second holes at the junction are $0.5r$ and $0.75r$, respectively (red and black circles in Fig. 4.10). We also added a modified Y-Splitter to divide the incoming waveguide into two branches: the output and the drain.

We then coupled two nonlinear L3 cavities with the PhC output waveguide branch to accomplish the well-defined logic state representations via Kerr effect. We optimized these cavities to achieve low power operation by shifting left the three holes of their left

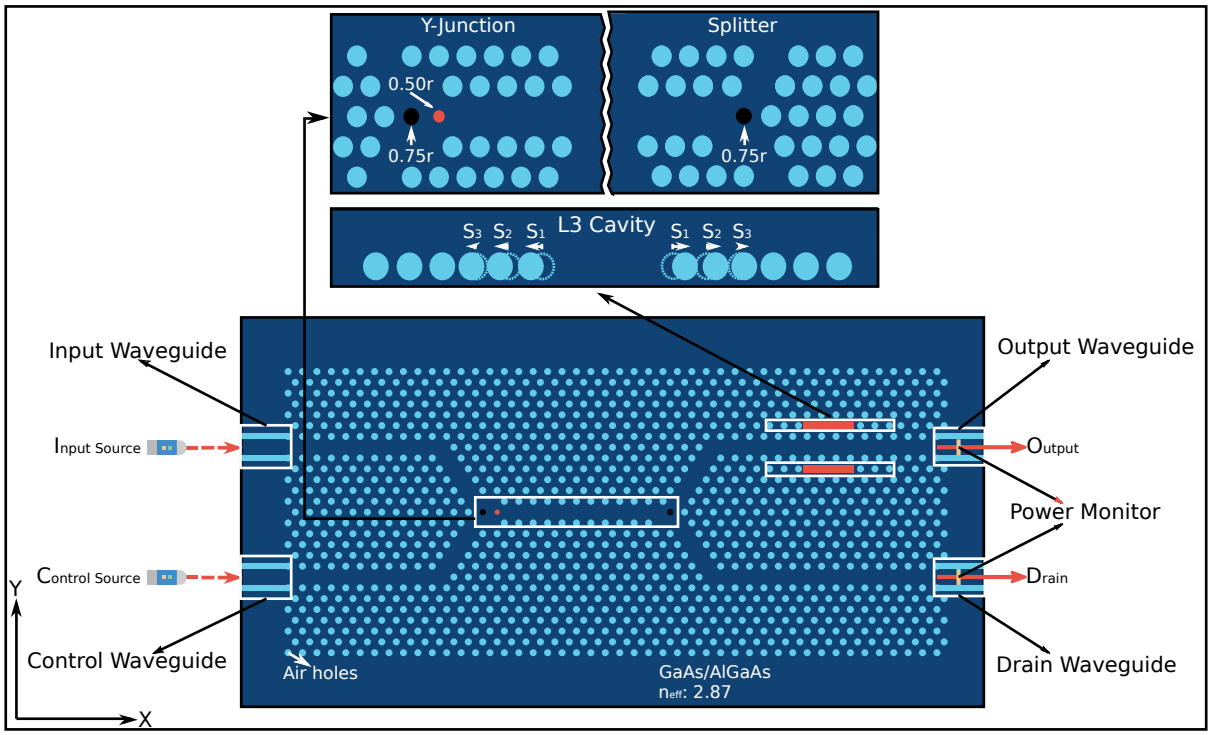


Figure 4.10: Simulated structure of the PhC integrated Switch N (SwN). Black and red circles represent optimized holes with radius $0.75r$ and $0.5r$, respectively. The displacements of the holes around the cavity are $S_1 = 0.33a$, $S_2 = 0.26a$, $S_3 = 0.12a$.

side and mirroring the holes of their right side. The displacements of these holes from left to right are $S_3 = 0.12a$, $S_2 = 0.26a$ and $S_1 = 0.33a$ (See Fig. 4.10). The resonant frequency w_0 and the quality factor Q of each cavity are 193.43 THz (1549.83 nm) and 8402, respectively. We used in the nonlinear area of each cavity a Kerr coefficient of $1.5 \times 10^{-17}\text{m}^2/\text{W}$, which is achievable with nearly instantaneous nonlinearity in AlGaAs below half the electronic bandgap [105]. The drain waveguide modulates the output power, ensuring that the energy value that represents logic value 1 at the Input and Output terminals are very close and helping the logic value 0 at the output to be as low as possible. Finally, we incorporated two power monitors at the output and drain waveguides to compute the outgoing power on them. The chip area of the SwN is (22.26×11.64) μm^2.

First, we only launched the control source into the system to evaluate the logic operation SwN(0,1) = 0. Then, a fraction of the input power is transmitted to the inactive input and the remainder from the Y-Junction to the Y-Splitter. At the output waveguide, we computed 10 mW of power value. Figure 4.11a illustrates the response time and Figure 4.11b shows the OS normalized intensity distribution of the optical propagating mode at 100 ps and 1549.75 nm. The normalization rule applied here consists of scaling the intensity by a factor $\delta = 1/max(A_h)$, where A_h is the maximum value of the intensity distribution with the higher output power. For the SwN, A_h is obtained when the logic operation SwN(1,1) = 1 is carried out. We observed similar behavior for

the logic operation SwN(1,0) = 0, [Figure 4.12a and Figure 4.12b].

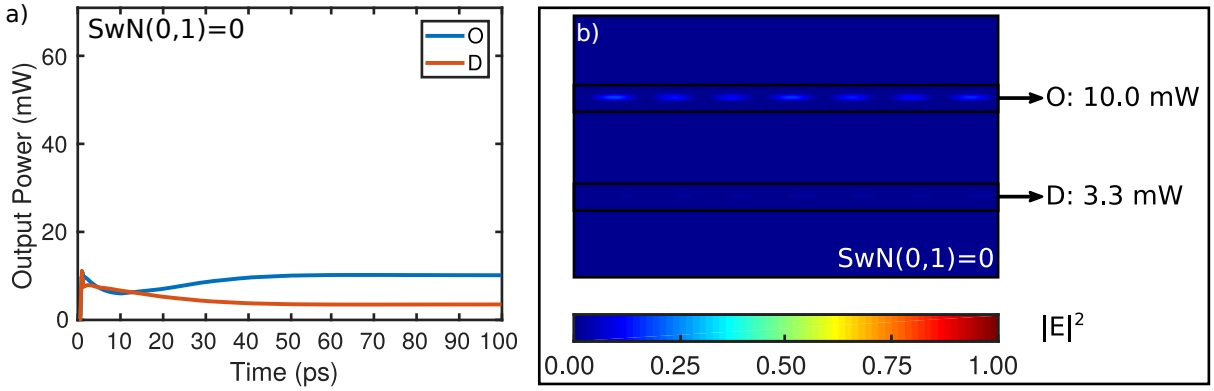


Figure 4.11: Simulation results of the PhC integrated SwN(0,1). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwN(0,1).

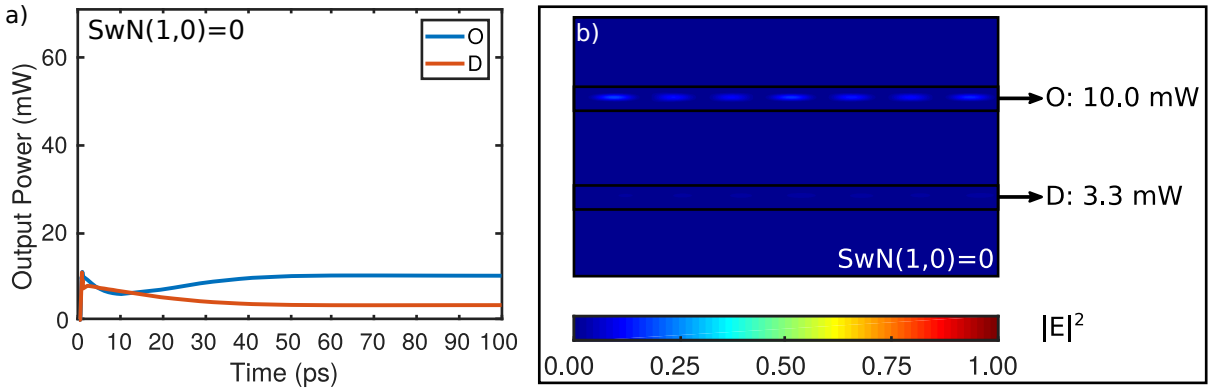


Figure 4.12: Simulation results of the PhC integrated SwN(1,0). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwN(1,0).

When we activated the control and input sources simultaneously, constructive interference occurs at the Y-Junction, and high power passes over the output waveguide. The system gets into the nonlinear regime and an output power value of 60 mW is obtained, an amplification gain of 1.13. This simulation setup corresponds to logic operation SwN(1,1) = 1, [Figure 4.13a and Figure 4.13b].

We finally decreased the inputs power to a value of 5 mW to simulate the logic operation SwN(0,0) = 0. As expected, low output powers were obtained, [Figure 4.14a and Figure 4.14b].

Table 4.1 compiles the input and output power results for the PhC integrated SwN. In summary, we can appreciate that power values lower than 10 mW represent output logic 0 and greater than 50 mW stands for output logic 1. These values mean an ON-OFF contrast ratio (CR) of 6.98 dB. We also found a ELR of 0.034 for this device. In addition to its logical function as a switch, the SwN also operates as an optical amplifier as we can

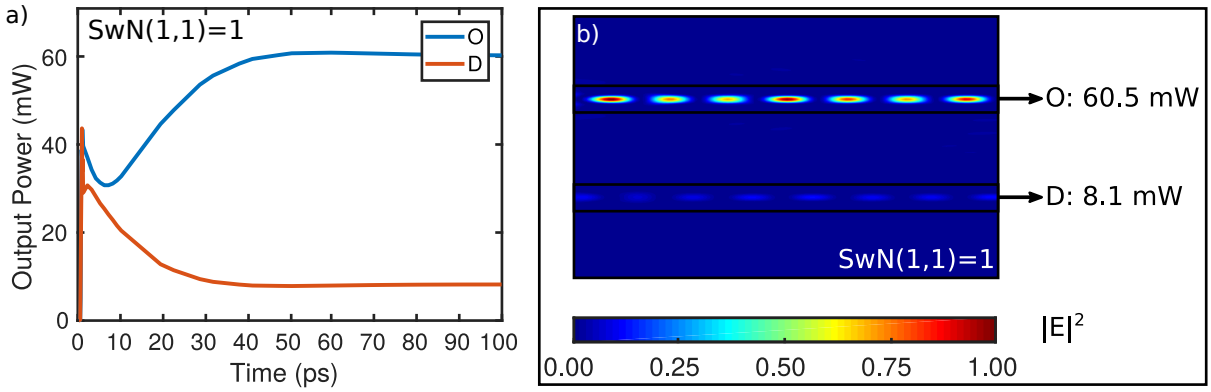


Figure 4.13: Simulation results of the PhC integrated SwN(1,1). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwN(1,1).

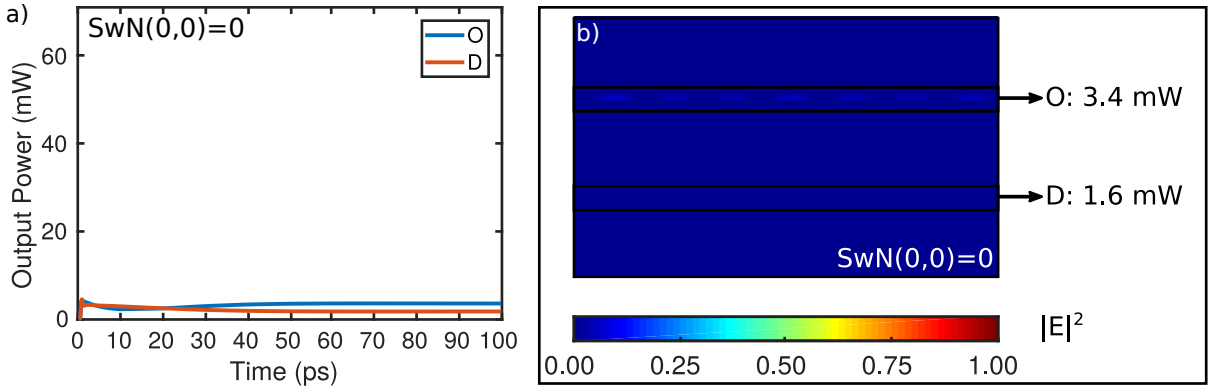


Figure 4.14: Simulation results of the PhC integrated SwN(0,0). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwN(0,0).

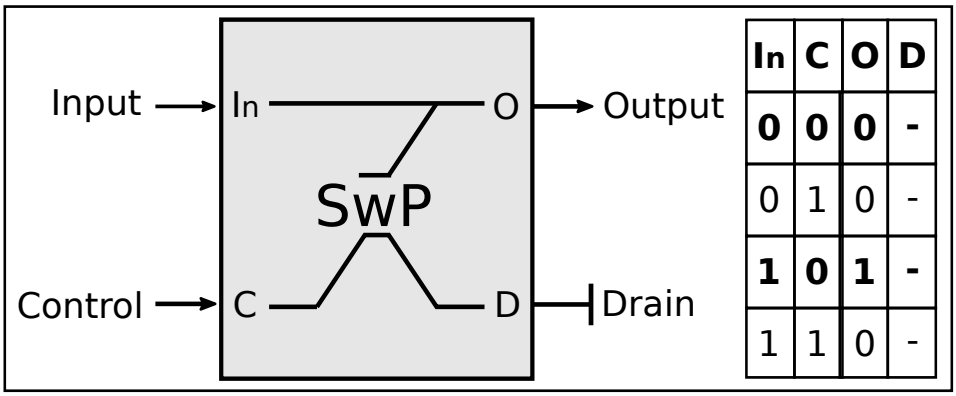
In (mW)	Logic In	C (mW)	Logic C	O (mW)	Logic O
5	0	5	0	3.40	0
0	0	50	1	10.0	0
50	1	0	0	10.0	0
50	1	50	1	60.50	1

Table 4.1: Input (In), Control (C) and Output (O) power results as a function of the input power for the PhC integrated SwN.

reshape a low power signal by modifying the power injected at the control waveguide. It also works as an AND logic gate. We highlight that the SwN presents a clock rate of 20 GHz.

4.3 Switch P

The PhC integrated Switch P (SwP) proposed here, named for its counterpart PMOS transistor, also consists of four terminals: input, control, output, and drain, as represented in Figure 4.15.



In	C	O	D
0	**0**	**0**	**-**
0	1	0	-
1	**0**	**1**	**-**
1	1	0	-

Figure 4.15: Diagram representation of the PhC integrated Switch P (SwP) and its truth table.

The output (O) of the SwP logic function is exactly the complement of the SwN, i.e.:

$$\text{SwP(In,C)} = \begin{cases} \text{In} & \text{if C is logic 0} \\ 0 & \text{if C is logic 1} \end{cases} \tag{4.4}$$

Figure 4.16 shows the designed device to achieve the SwP logic function in the PhC structure. Here, we configured the input and control PhC waveguides to create a path difference of one lattice constant, which generates a destructive interference if both sources are active. At their junction, we introduced an optimized hole with radius $r_a = 0.5r$ (red circle in Figure 4.16). With this, we limit the back reflection to the control terminal when In is active. Therefore, high power goes to the output system, and the representation of the logic state 1 can be achieved. Also, we avoid a high transmission to the output system if C is active but ensuring a strong destructive interference if both sources are launched. These facts allow us to represent the logic state 0. Next, we coupled to the output waveguide two cavities with the same properties of those used in the SwN. Finally, two power monitors are incorporated at the output and drain waveguides. The chip area of the SwP is $(20.58 \times 14.55)\ \mu\text{m}^2$.

Thus, we only activated the control source to simulate the logic operation SwP(0,1) = 0. We obtained a power value of 0.2 mW at the output waveguide. Figure 4.17 illustrates the response time for this case and the OS normalized intensity distribution of the optical propagating mode at the steady-state. For the SwP, A_h is obtained when SwP(1,0) = 1 is performed.

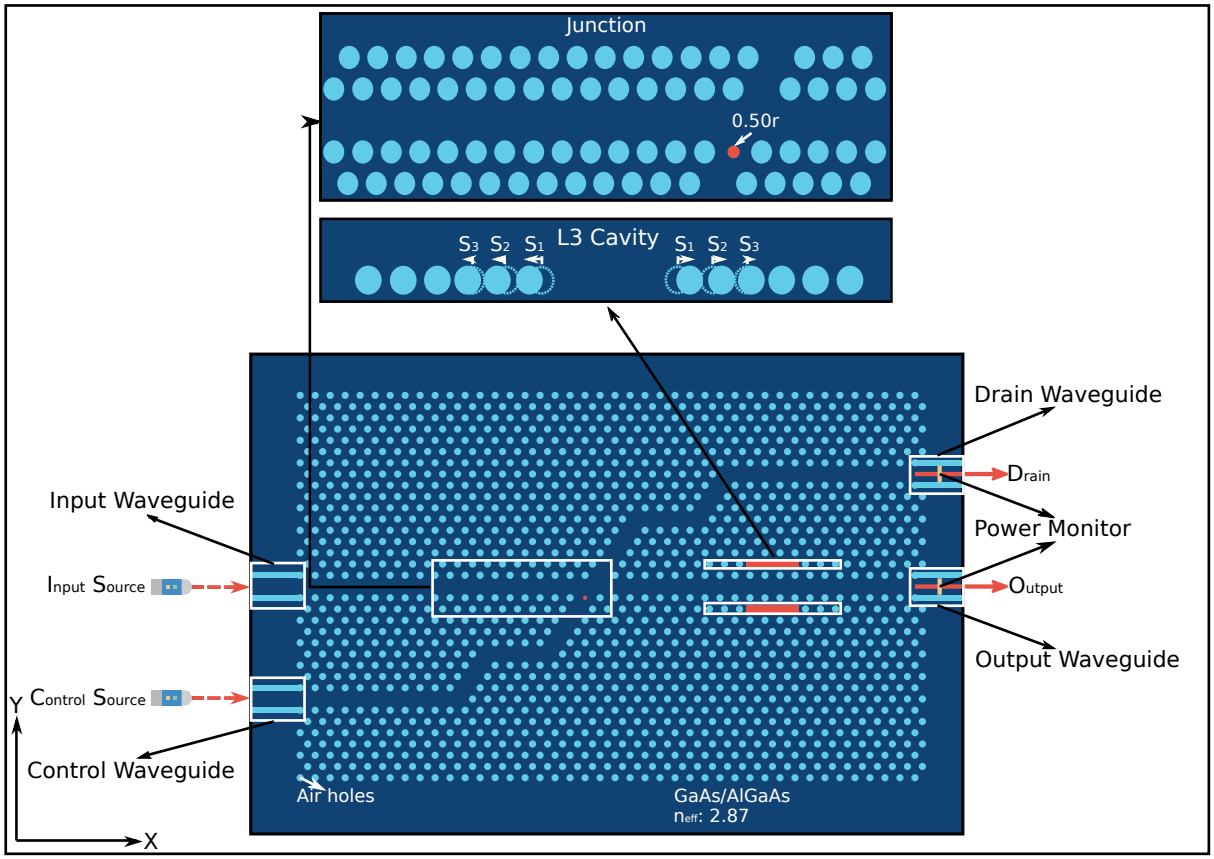


Figure 4.16: Simulated structure of the PhC integrated Switch P (SwP). The red circle represents optimized hole with radius $0.5r$.

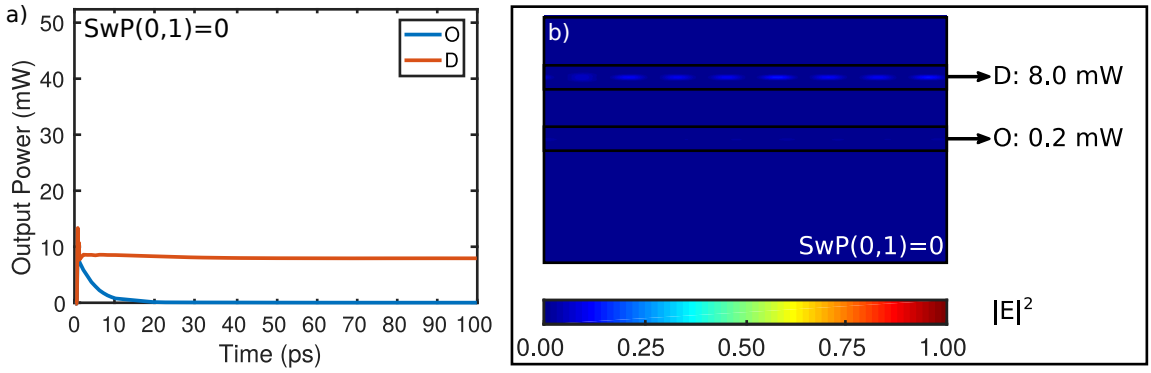


Figure 4.17: Simulation results of the PhC integrated SwP(0,1). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwP(0,1).

When we injected only the input source into the device, high power passes over the output waveguide since the optimized hole limits the back reflection to the control terminal. The device gets into the nonlinear regime, and we computed a power value of 42.5 mW at the output waveguide. This simulation setup corresponds to the logic operation SwP(1,0) = 1, [Figure 4.18a and Figure 4.18b].

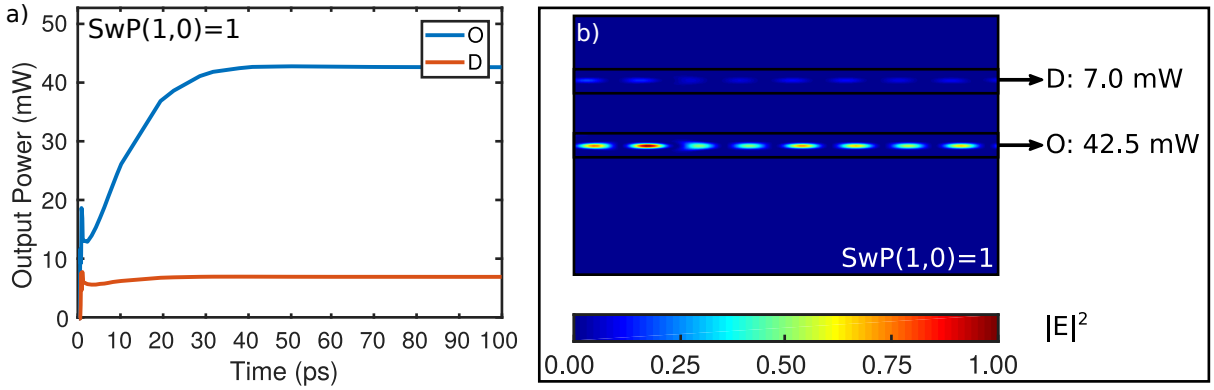


Figure 4.18: Simulation results of the PhC integrated SwP(1,0). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwP(1,0).

To study the logic operation SwP(1,1) = 0, we launched the control and input sources at the same time. At this point, destructive interference occurs at the SwP junction, and low power (9.5 mW) was obtained at the output, [Figure 4.19a and Figure 4.19b].

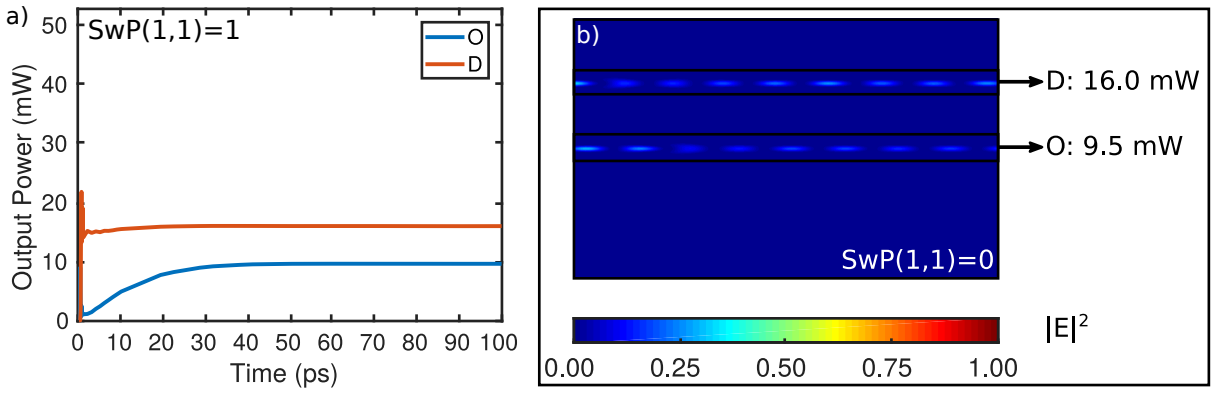


Figure 4.19: Simulation results of the PhC integrated SwP(1,1). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwP(1,1).

We finally simulated the logic operation SwP(0,0) = 0 by decreasing the inputs power to a value of 5 mW. In this case, low output power values were obtained, [Figure 4.20a and Figure 4.20b].

Table 4.2 compiles the input and output power results for the PhC integrated SwP. In summary, we can establish that power values lower than 10 mW and greater than 42

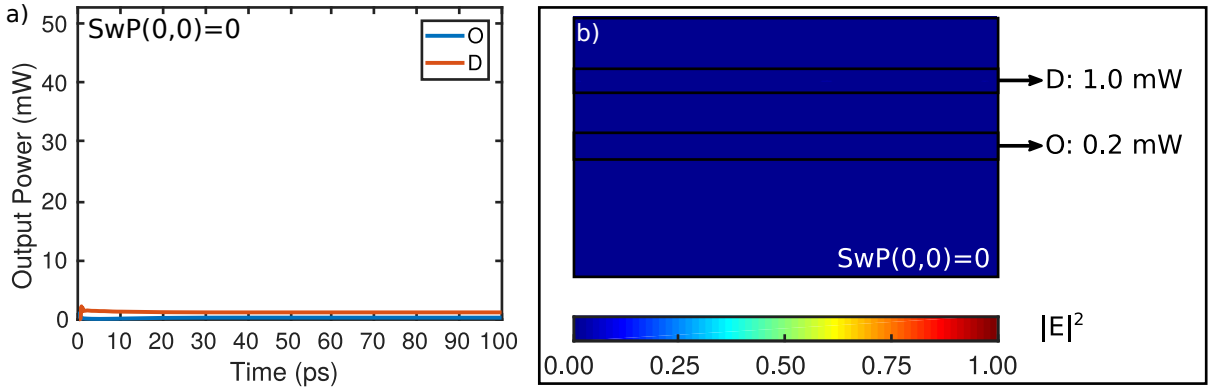


Figure 4.20: Simulation results of the PhC integrated SwP(0,0). a) Response time and b) OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination SwP(0,0).

In (mW)	Logic In	C (mW)	Logic C	O (mW)	Logic O
5	0	5	0	0.20	0
0	0	50	1	0.20	0
50	1	0	0	42.50	1
50	1	50	1	9.50	0

Table 4.2: Input (In), Control (C) and Output (O) power results as a function of the input power for the PhC integrated SwP.

mW represent output logic 0 and 1, respectively. These values mean a CR of 6.23 dB. It also reaches a clock rate of 25 GHz. We found a ELR of 0.045 for this device. Moreover, the SwP can also operate as an optical modulator as we can reduce to a low power signal by modifying the power injected at the control waveguide. Also, it can work as the NOT logic gate by fixing the source at the input terminal always ON, and using the control source as the NOT gate input.

4.4 Power Response Analysis

Here we introduce a wide study of the switches output power responses to better describe the systems and achieve a proper setup for each PhC integrated gate and circuit. Therefore, we perform a set of simulations consisting of all the setups for the Input and Control sources from 0 to 80 mW with power steps of 5 mW.

Figure 4.21 shows the output power response as a function of each Input and Control combination for both the Output and Drain of SwN. We can observe in Figure 4.21a that the greater the Input and Control, the greater the power value at the Output of SwN, reaching a power value of about 118 mW for the SwN(80,80) input setup. This

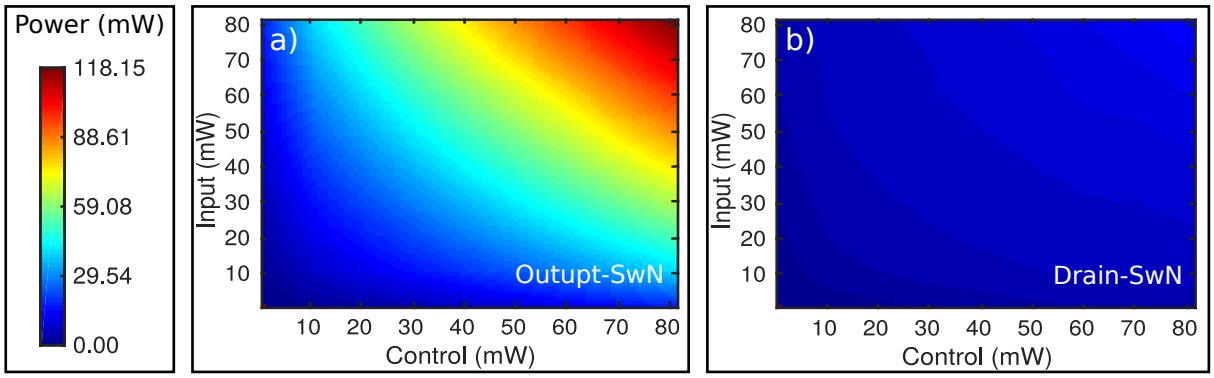


Figure 4.21: Normalized SwN power response as a function of the Input (from 0 mW to 80 mW) and Control (from 0 mW to 80 mW) for the a) Output. The lateral color bar illustrates the maximum and minimum power values obtained at the Output of the SwN when the input setups SwN(80,80) and SwN(0,0) are carried out, respectively. b) Normalized power response to the maximum SwN Output value at the SwN Drain.

result shows that the SwN operates as an optical amplifier since we can modulate the power at the Control to achieve the desired power value to represent a specific logic state. Figures 4.21b also shows an increase in the Drain value, but it is much smaller and can be neglected since it is not used in the logic datapath.

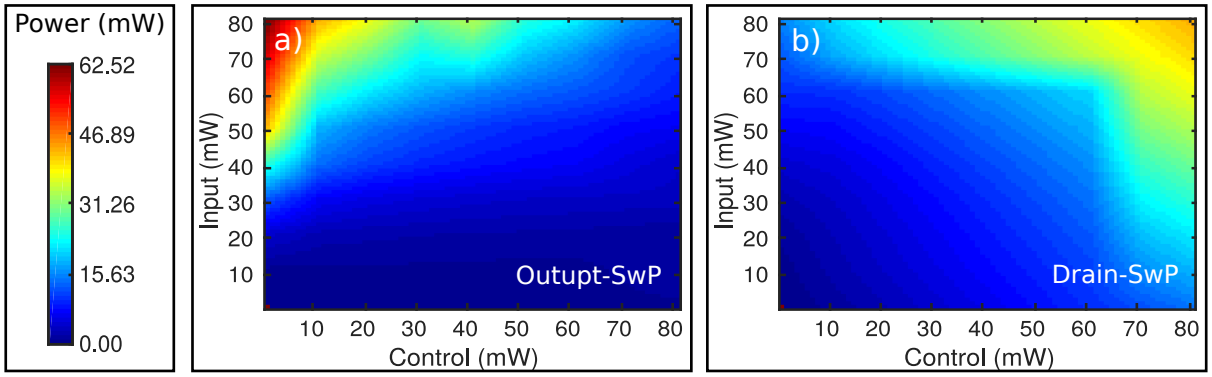


Figure 4.22: Normalized SwP power response as a function of the Input (from 0 mW to 80 mW) and Control (from 0 mW to 80 mW) for the a) Output. The lateral color bar illustrates the maximum and minimum power values obtained at the Output of SwP when the input setups SwP(80,0) and SwP(0,0) are carried out, respectively. b) Normalized power response to the maximum SwP Output value at the SwP Drain.

In the same direction, Figure 4.22a illustrates how the SwP output power changes as a function of the applied Input and Control signals. To represent the PMOS transistor, the Output is on only when the input is on, but the Control is off. Thus, for this instance, when the input setup SwP(80,0) is performed, the SwP Output achieves its maximum value, i.e., 63 mW. However, once the Control signal increases, the Output is turned off, decaying to a value of about 12 mW when the input setup SwP(80,80) is carried out. This fact demonstrates the ability of the SwP to operate as a signal reducer by applying the correct power signal at the Control source. Finally, Figure 4.22b shows the Drain power,

which is also neglected in the circuits.

4.5 Summary

We successfully proved the operation of the Switches N and P, PhC equivalents to NMOS and PMOS transistors in CMOS technology, respectively. A highly efficient clock rate, as high as 20 GHz at the same input and output wavelength (λ = 1549.75 nm) was demonstrated. For an input power of 50 mW, output power values greater than 42 mW and lower than 12 mW well-define the representation of logic 1 and 0, respectively. Furthermore, we found a ELR lower than 0.045 for our switches ensuring low energy dissipation and loss of information. These devices can support small phase delay ($\lambda/28$) at the input sources, changes in their Input power levels ($\pm$5 mW), and hole disorder effects around the cavity ($\pm$20 nm), the most sensitive region. These fluctuations, within current experimental tolerances, result in about $\pm$5 mW signal noise at the output for both switches. We also proved through a power analysis response that the SwN can operate as an optical amplifier by adjusting the Control source power. On the other hand, we demonstrated the SwP working as a signal reducer. Although our devices are larger than their electronic counterparts, they can be efficiently integrated into the network and optical fiber technologies, allowing the design of telecommunication components operating at a high speed of data processing and under a low consumption regime. Moreover, it could be possible since we can avoid the electronic-optic signal conversions. As a final consideration, we are now able to design PhC logic circuits and systems with CPCL acting as core hardware devices.

Chapter 5

Modeling of the Integrated Logic Gates and Circuits

Logic gates and circuits are essential components towards the realization of processors, sensors and multipurpose computational systems. In this chapter, we show how PhC integrated logic circuits can be designed using exclusively the switches N and P, our core hardware devices. Following, we present the AND, OR, NAND, NOR, and XOR logic gates, plus the wire split FAN-OUT and the Half Adder and Full Adder circuits.

5.1 AND

A Switch N by itself can already be used as an AND gate. However, as one of the main goals of this work is to study cascaded switches, we designed a logic circuit based on two PhC SwNs connected in series. The resulting system has three inputs and three outputs terminals, as represented in Figure 5.1a. Here, it is important to clarify that we define an Adapted Source Power (ASP), which is an adjustable reference signal to modulate the output power levels of the system. Its power value is derived empirically for each circuit, as we will explain in detail for each design. The resulting logic function for the Output (O) of AND gate can be described as follow:

$$O = SwN(A, SwN(B, ASP)), \tag{5.1}$$

where A and B are the logic inputs. Thus, the logic output terminal of this circuit will be 1 only when the outputs of the two SwNs are 1. Otherwise, it will be 0. This system is equivalent to the AND logic function, O = A·B.

Figure 5.1b shows the schematic representation of the designed PhC integrated AND circuit. It has a footprint area of 37.38 $\mu m \times 16.00\ \mu m$. At this point, we set the ASP at 30 mW, which is a suitable value to achieve the desired logic states at the output. Figure 5.2 illustrates the OS normalized intensity distribution of the optical propagating

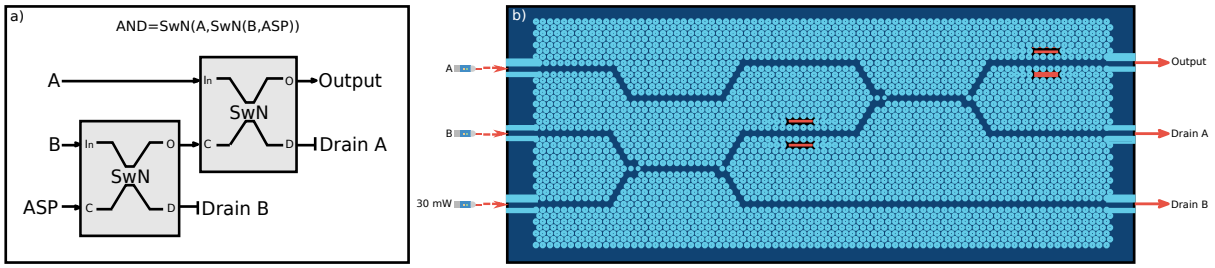
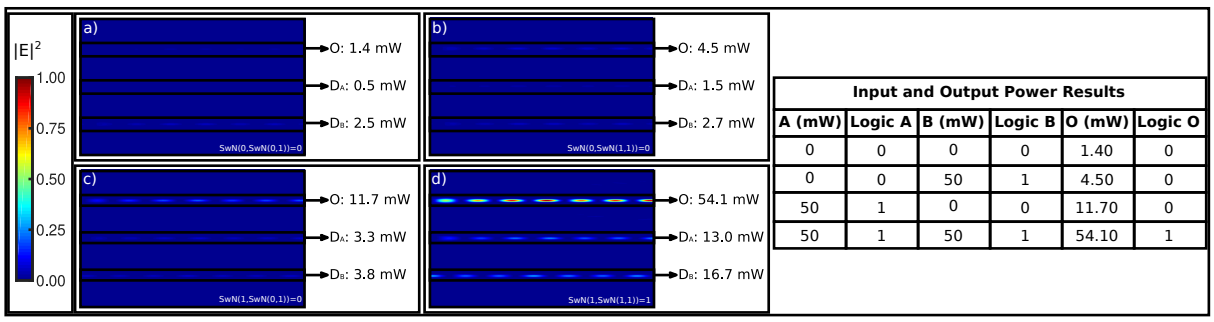


Figure 5.1: PhC integrated AND circuit. a) Diagram of the AND circuit based on CPCL. b) Simulated structure of the PhC integrated AND circuit.

mode of the PhC integrated AND circuit at the steady-state for the complete set of input combinations. The right-side table summarizes the input and output power results for this circuit. Thus, when input A and B are logic 0, we obtained 1.40 mW at the output, resulting from only launching the ASP into the structure, as illustrated in Figure 5.2a. We launched the input source B into the structure to simulate the AND(0,1) input combination. We obtain, for this case, an output value of 4.50 mW, as can be observed in Figure 5.2b. Similarly, we activated the input source A to simulate the AND(1,0) input combination. An output power of 11.70 mW is obtained, as illustrated in Figure 5.2c. Finally, inputs A and B are launched into the structure simultaneously to simulate the AND(1,1) input combination. We computed an output power value of 54.10 mW for this case, as shown in Figure 5.2d. With this information, we can set power values greater than 50 mW and lower than 12 mW as logic 1 and 0, respectively. These values mean an ON-OFF contrast ratio (CR) of 6.19 dB for this gate. It also presents a clock rate of 12.5 GHz since it reaches the steady-state at 80 ps. The ELR for this circuit was found to be 0.038. The Drain outputs are disregarded. Thus, we demonstrate the correct operation of the PhC integrated AND gate.



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
0	0	0	0	1.40	0
0	0	50	1	4.50	0
50	1	0	0	11.70	0
50	1	50	1	54.10	1

Figure 5.2: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) AND(0,0), b) AND(0,1), c) AND(1,0) and d) AND(1,1). The right-side table summarizes the input and output power results.

5.2 OR

Our OR logic gate is based on a parallel arrangement of two SwNs, as represented in Figure 5.3a. The logic output for this circuit is:

$$O = J(SwN(A, ASP), SwN(B, ASP)), \tag{5.2}$$

where A and B are logic inputs, while J represents the function of a PhC Y-junction. For this kind of PhC device, we found that the output power response is about 84% of the total input power applied. Thus, the logic output terminal (O) of the circuit will be 1 if any output of the SwNs is 1. Similarly, it will be 0 only when both of the SwNs outputs are 0. It is the equivalent circuit to the OR logic function, i.e., O=A+B.

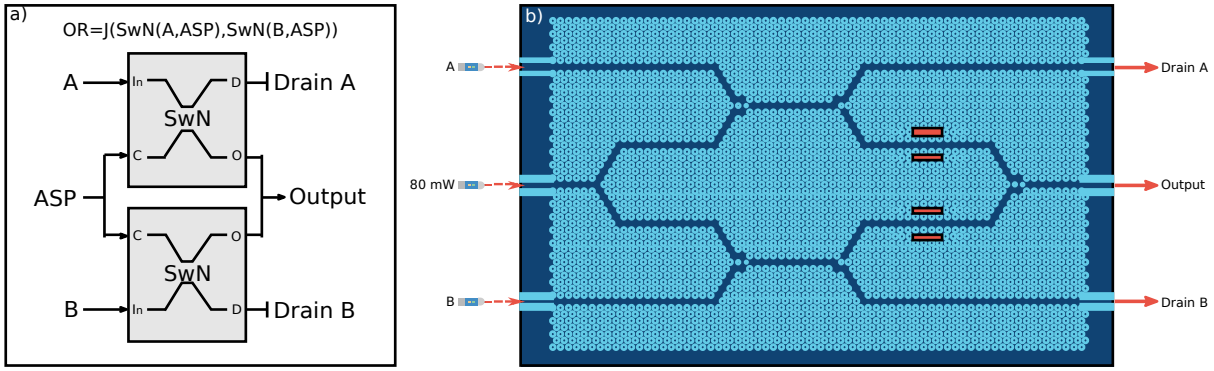
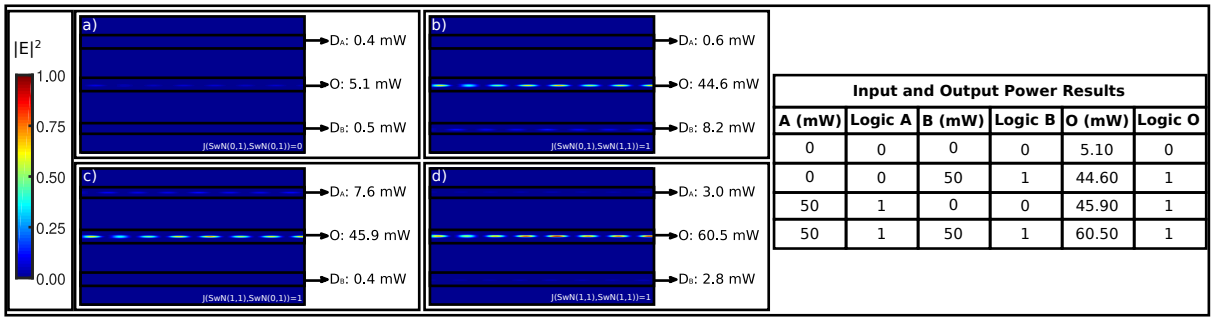


Figure 5.3: PhC integrated OR circuit. a) Diagram of the OR circuit based on CPCL. b) Simulated structure of the PhC integrated OR circuit.

Figure 5.3b illustrates the design of the PhC structure equivalent to the OR circuit, with a footprint of 31.50 $\mu m \times 20.36\ \mu m$. Since the ASP path is split to both SwNs, we set its power at 80 mW. It is important to note that our PhC splitter divides the input power into two branches with about 43% each. Figures 5.4a-d show the OS normalized intensity distribution of the optical propagating mode for our OR circuit at the steady-state for the complete set of input combinations. So, we can observe that power values greater than 44 mW and lower than 6 mW represent logic 1 and 0, respectively. These values show a CR of 8.65 dB for this circuit. We also computed a ELR of 0.05 for the OR circuit. It also exhibits a clock rate of 12.5 GHz.



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
0	0	0	0	5.10	0
0	0	50	1	44.60	1
50	1	0	0	45.90	1
50	1	50	1	60.50	1

Figure 5.4: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) OR(0,0), b) OR(0,1), c) OR(1,0) and d) OR(1,1). The right-side table summarizes the input and output power results.

5.3 NAND

Aiming to obtain an all-optical NAND logic gate, we connect a SwN to a SwP, as can be seen in Figure 5.5a, and whose logic output behavior can be described by the following expression:

$$O = SwP(ASP, SwN(A, B)). \tag{5.3}$$

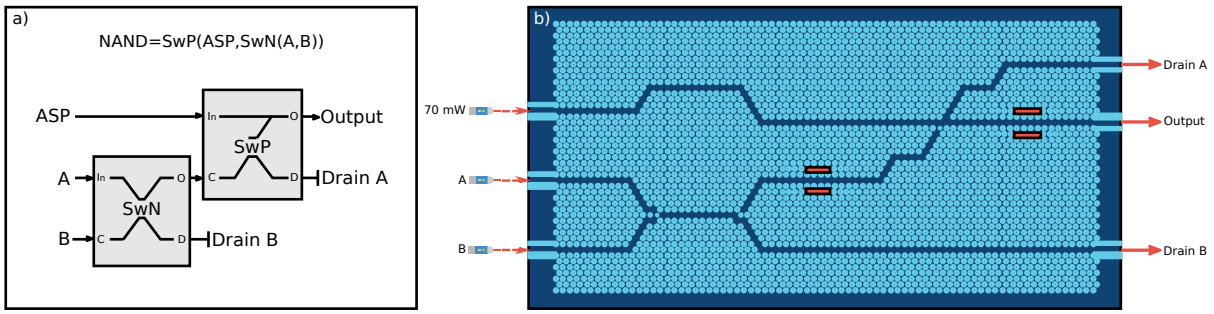
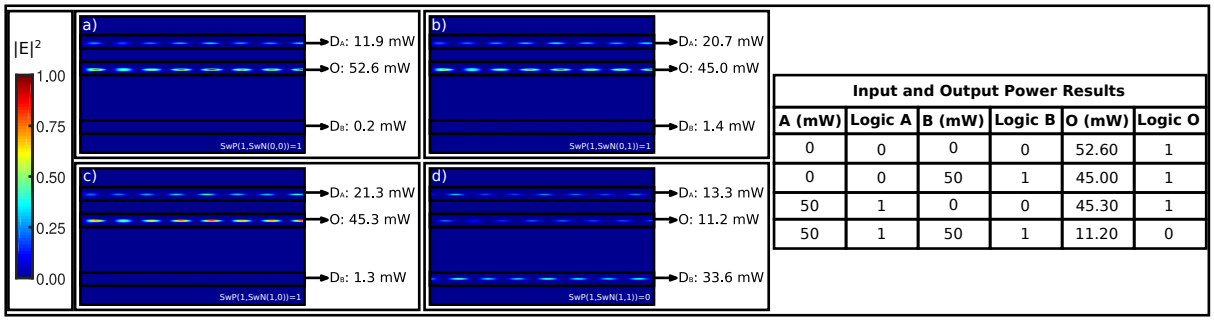


Figure 5.5: PhC integrated NAND circuit. a) Diagram of the NAND circuit based on CPCL. b) Simulated structure of the PhC integrated NAND circuit.

The output of the PhC integrated NAND gate will be 0 when the output of SwN is 1; otherwise, it will be 1. Thus, it is analogous to the NAND logic function, represented by O = ¬(A·B). The designed PhC structure for this circuit has a footprint area of 37.50 μm × 18.91 μm, and its representative scheme can be seen in Figure 5.5b. For this instance, we set the power value of the ASP at 70 mW. Figures 5.6a-d show the OS normalized intensity distribution of the optical propagating mode of the PhC integrated NAND circuit at the steady-state for the complete set of input combinations. Thus, power values greater than 45 mW and lower than 12 mW stand for logic 1 and 0, respectively. These values mean a CR of 5.74 dB for this circuit. The NAND circuit has a ELR of 0.0064. It also presents a clock rate of 12.5 GHz, reaching its steady-state at 80 ps.



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
0	0	0	0	52.60	1
0	0	50	1	45.00	1
50	1	0	0	45.30	1
50	1	50	1	11.20	0

Figure 5.6: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) NAND(0,0), b) NAND(0,1), c) NAND(1,0) and d) NAND(1,1). The right-side table summarizes the input and output power results.

5.4 NOR

Towards the realization of the PhC NOR logic gate, we connect two SwPs in series, as illustrated in Figure 5.7a. The resulting system leads to a logic output described by the following equation:

$$O = SwP(SwP(ASP, A), B). \tag{5.4}$$

Thus, we obtain an equivalent to the NOR logic function, O = ¬(A+B), since the circuit output will be 1 only if both SwPs outputs are 1. Otherwise, it will be 0.

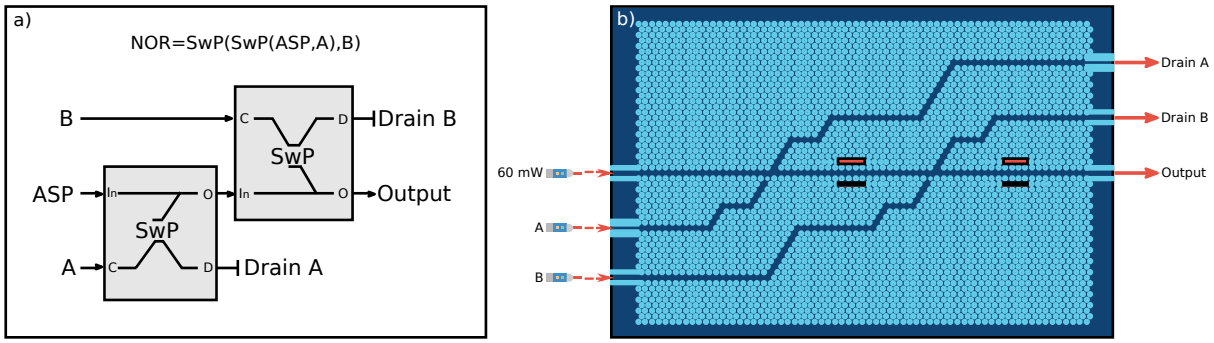
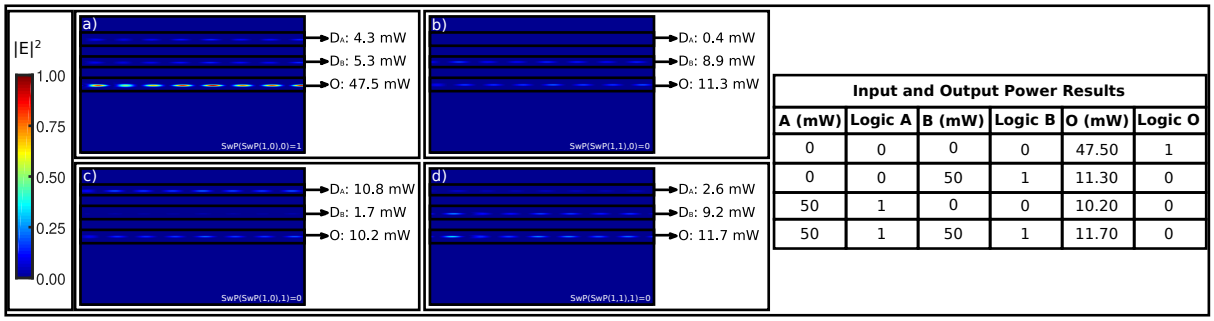


Figure 5.7: PhC integrated NOR circuit. a) Diagram of the NOR circuit based on CPCL. b) Simulated structure of the PhC integrated NOR circuit.

Figure 5.7b shows the designed structure for the PhC integrated NOR circuit, which has a footprint of 31.08 $\mu m \times 21.82\ \mu m$. In this case, we set the ASP at 60 mW. Figures 5.8a-d show the OS normalized intensity distribution of the optical propagating mode of the PhC integrated NOR circuit at the steady-state for its input combinations. Power values greater than 47 mW and lower than 12 mW indicate logic 1 and 0, respectively. These values show a CR of 5.92 dB. This circuit also exhibits a clock rate of 12.5 GHz and a ELR of 0.037.



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
0	0	0	0	47.50	1
0	0	50	1	11.30	0
50	1	0	0	10.20	0
50	1	50	1	11.70	0

Figure 5.8: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) NOR(0,0), b) NOR(0,1), c) NOR(1,0) and d) NOR(1,1). The right-side table summarizes the input and output power results.

5.5 XOR

We achieve a PhC XOR logic gate by connecting two SwPs in parallel. The description of the logic output for our XOR circuit is given by:

$$O = J(SwP(A, B), SwP(B, A)), \tag{5.5}$$

where the logic output will be 1 if any output of the SwPs is 1, otherwise it will be 0. It is the equivalent circuit to the XOR logic function, i.e., O = A⊕B. It is important to note that the inputs signals swap for each SwP. Indeed, input A serves as the Input for the first SwP and the Control for the second SwP. In the opposite direction, input B operates as the Control for the first SwP and as the Input for the second SwP. This fact implies that an intersection path occurs between the input signals generating interference between the PhC waveguides. The correct operation and the performance of the PhC XOR circuit can be affected due to the 2D nature of our structure and mainly by the absence of a cross information device that avoids the previously mentioned interference signals. Thus, we adopt a simplified dual-rail strategy consisting of replicating the input signals to prevent the undesired interference and intersection between the input sources. Figure 5.9a shows the diagram of the final setup to achieve the PhC integrated XOR circuit.

Figure 5.9b illustrates the simulated structure for the PhC integrated XOR circuit, which has a footprint of 27.30 $\mu m \times 24.73\ \mu m$. Furthermore, Figures 5.10a-d show the OS normalized intensity distribution of the optical propagating mode at the steady-state for the complete set of input combinations of this circuit. Accordingly, we set power values up to 43 mW and down to 3 mW to represent logic 1 and 0, respectively. These values mean a CR of 11.56 dB for this circuit. It also presents a clock rate of 12.5 GHz and ELR of 0.05.

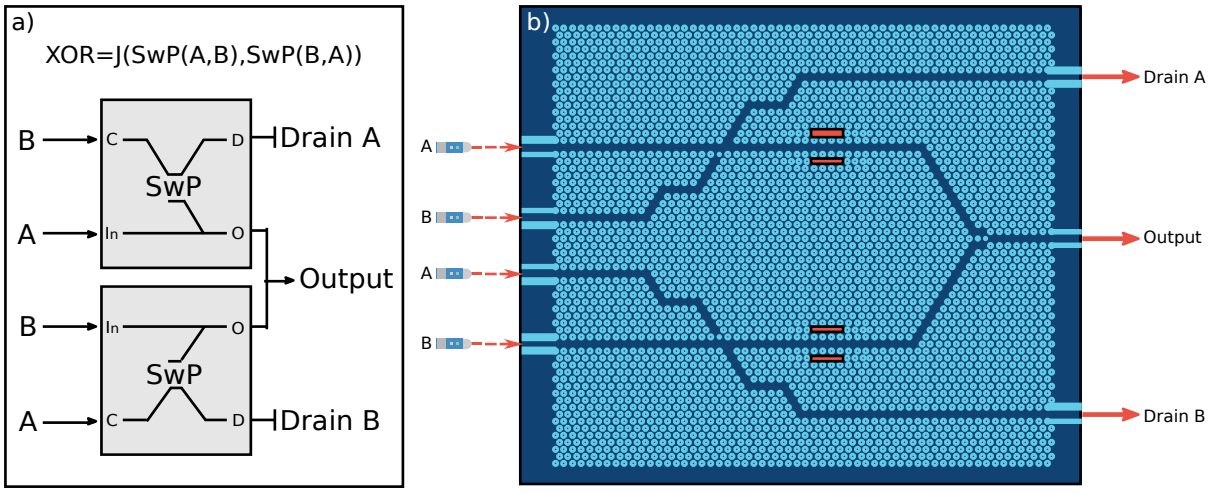
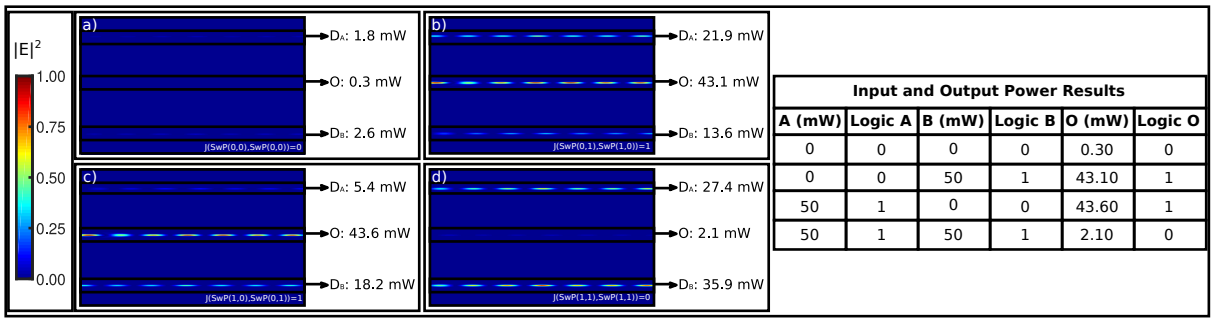


Figure 5.9: PhC integrated XOR circuit. a) Diagram of the XOR circuit based on CPCL. b) Simulated structure of the PhC integrated XOR circuit.



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
0	0	0	0	0.30	0
0	0	50	1	43.10	1
50	1	0	0	43.60	1
50	1	50	1	2.10	0

Figure 5.10: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) XOR(0,0), b) XOR(0,1), c) XOR(1,0) and d) XOR(1,1). The right-side table summarizes the input and output power results.

5.6 FAN-OUT

In this section, we implemented a circuit to split a signal in two without losing value. This is a fundamental device to drive logic gates connections in a circuit. It was designed based on two SwNs, as can be seen in Figure 5.11a, where the logic functions for each output (O1, O2) are described as follow:

$$O1 = SwN(ASP, In), \tag{5.6}$$

$$O2 = SwN(ASP, In). \tag{5.7}$$

Since the ASP will always be high, the output O1 and O2 will be 1 if the Input (In) is 1. Otherwise, they will be 0.

Our simulated structure for the PhC integrated FAN-OUT circuit is illustrated in Figure 5.11b. It has a footprint area of 26.46 $\mu m \times 20.36\ \mu m$. To achieve the desired power representations for logic 1 and 0 at the outputs, we set the ASP as 50 mW, which is

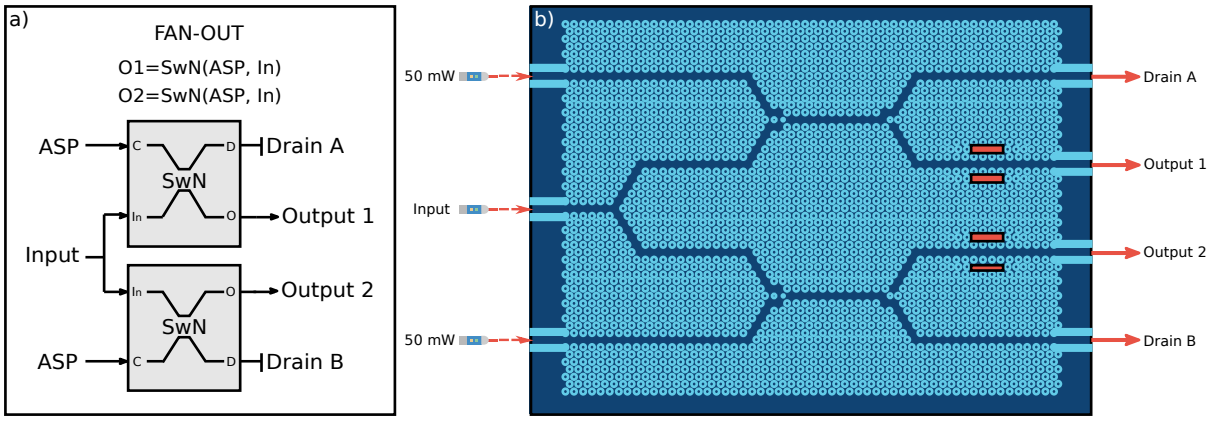
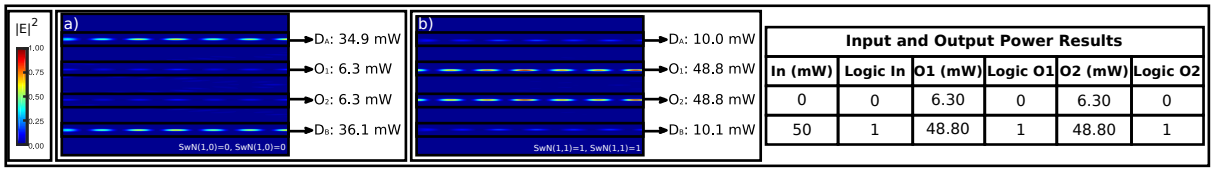


Figure 5.11: PhC integrated FAN-OUT circuit. a) Diagram of the FAN-OUT circuit based on CPCL. b) Simulated structure of the PhC integrated FAN-OUT circuit.

enough power amount. Overall, Figure 5.12a and 5.12b show the OS normalized intensity distribution of the optical propagating mode at the steady-state for the complete set of input combinations. So, we define power values greater than 48 mW and lower than 7 mW as logic values 1 and 0, respectively. These values show a CR of 8.36 dB. This circuit has a clock rate of 12.5 GHz and a ELR of 0.058.



Input and Output Power Results					
In (mW)	Logic In	O1 (mW)	Logic O1	O2 (mW)	Logic O2
0	0	6.30	0	6.30	0
50	1	48.80	1	48.80	1

Figure 5.12: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) Fan-out(0), b) Fan-out(1). The right-side table summarizes the input and output power results.

5.7 HALF ADDER

The half-adder (HA) is a circuit that adds two single binary digits (A and B) and produces two outputs (Sum and Carry), as can be observed in Figure 5.13a. The resulting Carry and Sum are generated from the AND and XOR logic operations, respectively. HAs are commonly used in computers and microprocessors in the Arithmetic Logic Unit (ALU). As mentioned before, in Section 5.5, due to the absence of a cross-information device, we replicated the input signals.

The PhC structure for the HA circuit with a footprint of 27.30 $\mu m \times 32.00\ \mu m$ is presented in Figure 5.13b. The OS normalized intensity distributions of the optical

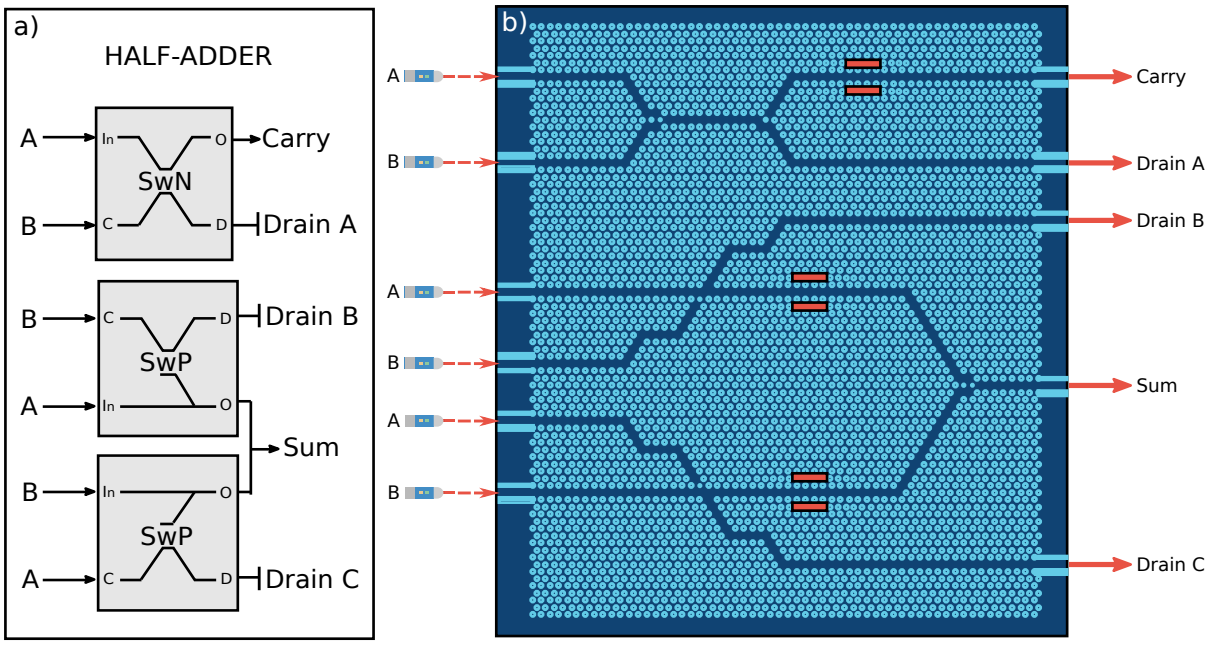
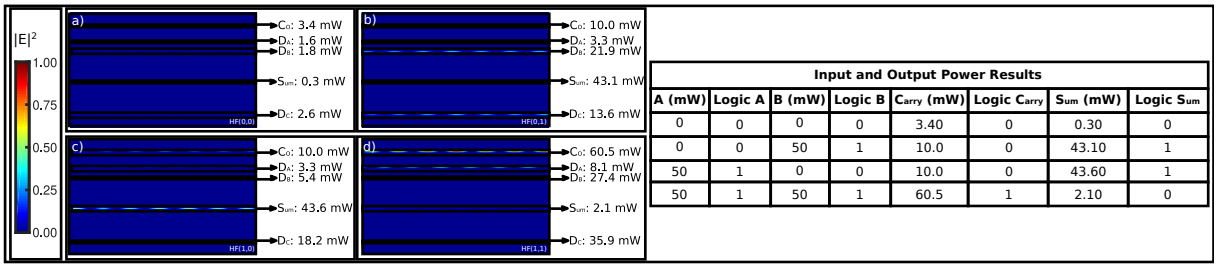


Figure 5.13: PhC integrated Half-Adder (HF) circuit. a) Diagram of the HF circuit based on CPCL. b) Simulated structure of the PhC integrated HF circuit.

propagating mode at the steady-state for all input combinations are shown in Figures 5.14a-d. Input and output power values are the same as the AND and XOR logic circuits. So, we can represent power values greater than 43 mW and lower than 12 mW as logic 1 and 0, respectively. These values indicate a CR of 5.54 dB for this circuit. The PhC integrated HA presents a clock rate of 12.5 GHz and a ELR of 0.05.



Input and Output Power Results

A (mW)	Logic A	B (mW)	Logic B	Carry (mW)	Logic Carry	Sum (mW)	Logic Sum
0	0	0	0	3.40	0	0.30	0
0	0	50	1	10.0	0	43.10	1
50	1	0	0	10.0	0	43.60	1
50	1	50	1	60.5	1	2.10	0

Figure 5.14: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) HF(0,0), b) HF(0,1), c) HF(1,0) and d) HF(1,1). The right-side table summarizes the input and output power results.

5.8 FULL ADDER

The Full-Adder (FA) is a combinational circuit based on three inputs and two outputs, which computes the binary sum of two arbitrary numbers. It solves the limitation

of the HA to handle the carry bit from the addition of two previous digits. So, we can string FAs together to create a byte-wide adder and cascade the carry bit from one FA to the next. In this work, for practical considerations and to reduce the computational cost to perform the simulations, we divided the PhC FA into two circuits, the CARRY, and the SUM, which are explained in the following sections.

5.8.1 CARRY

Our PhC-based Carry circuit for the FA has three logic inputs and one logic output (C_{out}), as follows:

$$C_{out} = J(SwN(A, SwN(ASP, C_{in})), SwN(B, SwN(ASP, C_{in}))), \tag{5.8}$$

where A, B are the two binary digits and C_{in} is the carry bit. In the Figure 5.15a, it is possible to observe the CPCL circuit equivalents to the FA Carry circuit.

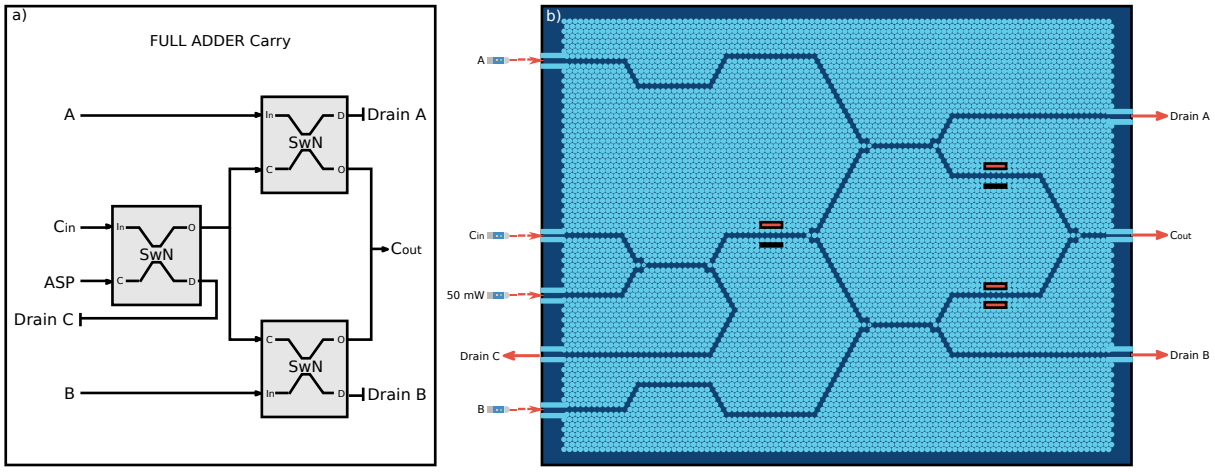
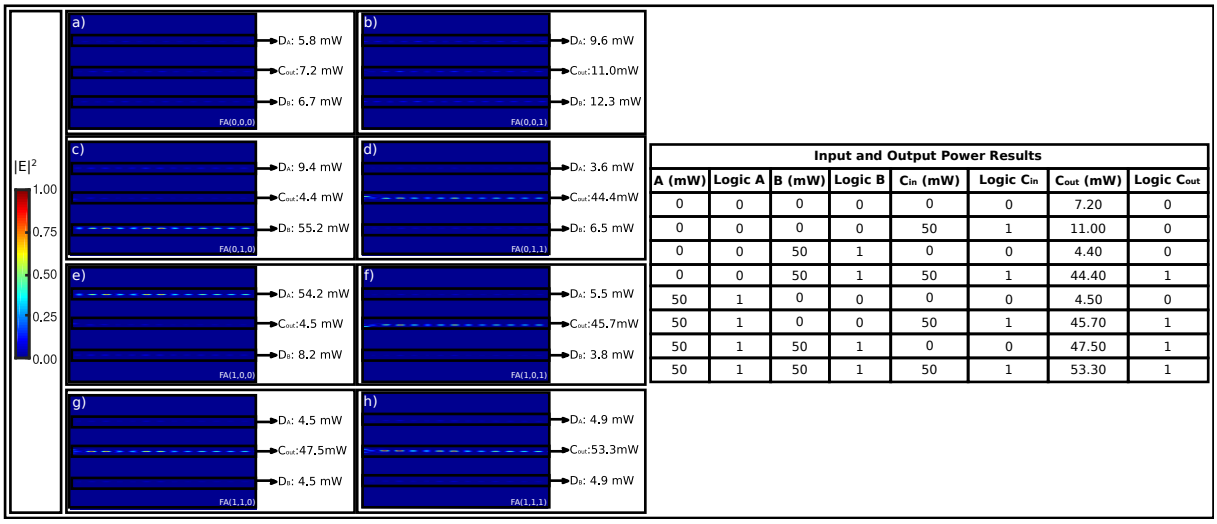


Figure 5.15: PhC integrated Full-Adder (FA) Carry circuit. a) Diagram of the FA Carry circuit based on CPCL. b) Simulated structure of the PhC integrated FA Carry circuit.

Figure 5.15b shows our designed structure for the PhC integrated FA Carry circuit, which has a footprint of 44.94 μm × 33.46 μm. For this circuit, we set the ASP as 50 mW. The OS normalized intensity distribution of the optical propagating mode for all input combinations at the steady-state of the circuit is illustrated in Figures 5.16a-h. At this point, it is important to mention that the PhC Carry circuit achieves its steady-state at 100 ps. Also, power values greater than 44 mW and lower than 12 mW stand for logic 1 and 0, respectively. These values indicate a CR of 5.64 for this circuit. The obtained clock rate for the FA Carry circuit is 10 GHz and its ELR is 0.03.



Input and Output Power Results							
A (mW)	Logic A	B (mW)	Logic B	C_{in} (mW)	Logic C_{in}	C_{out} (mW)	Logic C_{out}
0	0	0	0	0	0	7.20	0
0	0	0	0	50	1	11.00	0
0	0	50	1	0	0	4.40	0
0	0	50	1	50	1	44.40	1
50	1	0	0	0	0	4.50	0
50	1	0	0	50	1	45.70	1
50	1	50	1	0	0	47.50	1
50	1	50	1	50	1	53.30	1

Figure 5.16: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination c) FA(0,0,0), d) FA(0,0,1), e) FA(0,1,0), f) FA(0,1,1), g) FA(1,0,0), h) FA(1,0,1), i) FA(1,1,0), and j) FA(1,1,1). The right-side table summarizes the input and output power results.

5.8.2 SUM

Here, we detail the PhC Sum circuit for the FA. It consists of three inputs and one output, named S_{um}. By using the CPCL, we can calculate its logic output through the following equation:

$$S_{um} = J(SwP(SwN(ASPA, XOR(A,B)), C_{in}), SwP(C_{in}, SwN(XOR(A,B), ASPB))) \tag{5.9}$$

where A, B are the two binary digits, and C_{in} is the carry bit. Figure 5.17a represents the CPCL circuit equivalents to the FA Sum circuit.

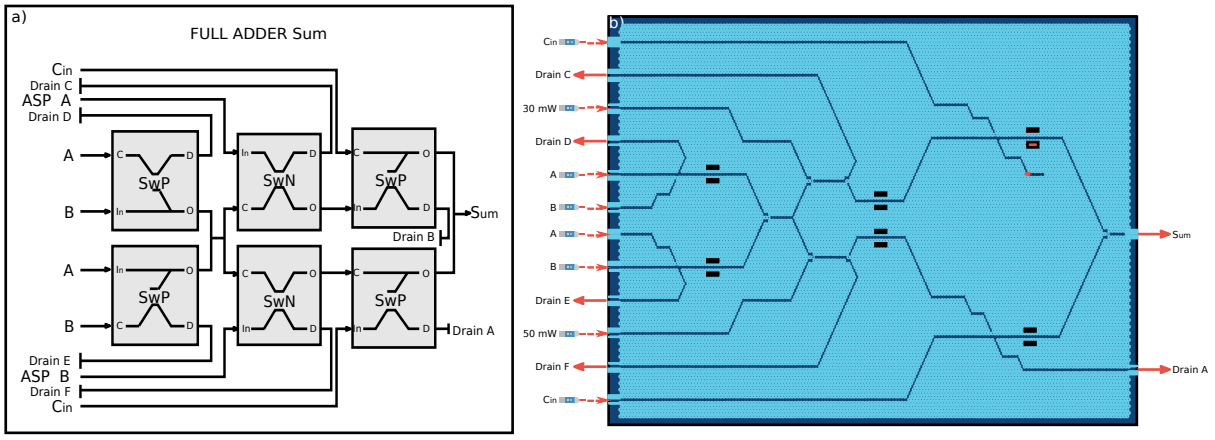
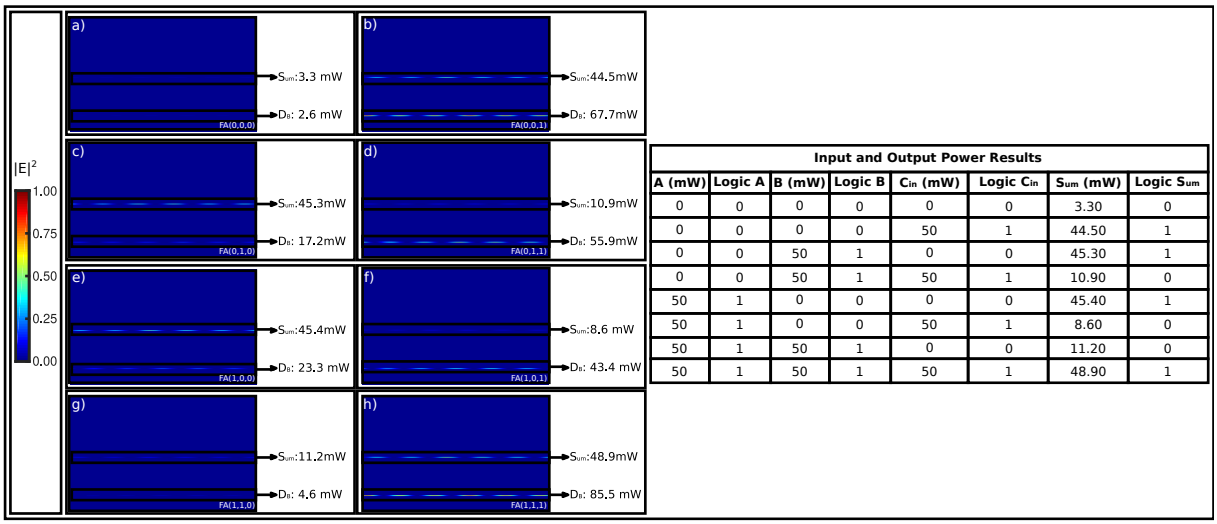


Figure 5.17: PhC integrated Full-Adder (FA) Sum circuit. a) Diagram of the FA Sum circuit based on CPCL. b) Simulated structure of the PhC integrated FA Sum circuit.

The simulated structure for the PhC integrated FA Sum circuit, which has a footprint of 74.97 μm $\times$ 45.10 μm, is illustrated in Figure 5.17b. We set ASP A and B for this circuit with 30 mW and 50 mW, respectively. So, we can see in Figures 5.18a-h the OS normalized intensity distribution of the optical propagating mode for all input combinations at the steady-state. From this information, we can define power values up to 44 mW and down to 12 mW as the logic 1 and 0, respectively. These values mean a CR of 5.64 dB for this circuit, and a clock rate of 8.3 GHz is also obtained. Its ELR is 0.042.



Input and Output Power Results

A (mW)	Logic A	B (mW)	Logic B	C_{in} (mW)	Logic C_{in}	S_{um} (mW)	Logic S_{um}
0	0	0	0	0	0	3.30	0
0	0	0	0	50	1	44.50	1
0	0	50	1	0	0	45.30	1
0	0	50	1	50	1	10.90	0
50	1	0	0	0	0	45.40	1
50	1	0	0	50	1	8.60	0
50	1	50	1	0	0	11.20	0
50	1	50	1	50	1	48.90	1

Figure 5.18: OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination c) FA(0,0,0), d) FA(0,0,1), e) FA(0,1,0), f) FA(0,1,1), g) FA(1,0,0), h) FA(1,0,1), i) FA(1,1,0), and j) FA(1,1,1). The right-side table summarizes the input and output power results.

5.9 Summary

We numerically demonstrated a complete set of PhC integrated gates and circuits, based on Complementary Photonic Crystal components, including AND, OR, NOR, NAND, XOR, FAN OUT, HALF ADDER, and FULL ADDER logic devices. The proposed systems showed excellent performance for SwN and SwP acting as core hardware devices, where a contrast ratio as high as 5.5 dB was demonstrated. We also found our PhC integrated circuits with low energy loss (≤ 0.065), meaning low energy dissipation. Furthermore, our designs were computationally guided to establish values that reliably represent logic states 1 and 0, guaranteeing an operating wavelength at $\lambda \approx 1550$ nm for input and output. Thus, we believe that this work satisfactorily contributes to address

improvements for the design of telecommunication systems, sensors, and microprocessors chips with PhC in the future.

Chapter 6

Discussion

The PhC logic devices have received great attention during the last years due to their relevance for the development of all-optical computational circuits. In this work, we successfully presented a complete set of PhC integrated logic devices, gates, and circuits with up to three levels of logic processing. Our photonic components include the switches N and P, the logic gates AND, OR, NAND, NOR, XOR plus the FANOUT, HALF-ADDER, and FULL-ADDER circuits. Table 6.1 shows the obtained parameters for each PhC integrated component.

	P_0(mW)	P_1(mW)	CR(dB)	Area(μm^2)	Response Time(ps)	ELR
SwN	10	50	6.98	22.26×11.64	50	0.03
SwP	12	42	6.23	20.58×14.55	50	0.04
AND	12	50	6.19	37.38×16.00	80	0.03
OR	6	44	8.65	31.50×20.36	80	0.05
NAND	12	45	5.74	37.50×18.91	80	0.06
NOR	12	47	5.92	31.08×21.82	80	0.037
XOR	3	43	11.56	27.30×24.73	80	0.05
FANOUT	7	48	8.36	26.46×20.36	80	0.05
HA	12	43	5.54	27.30×32.00	80	0.05
FA-Carry	12	44	5.64	44.94×33.46	100	0.03
FA-Sum	12	44	5.64	74.97×45.10	120	0.04

Avg	10.00	45.45
Std	3.19	2.84
CI - 95%	(7.85,12.15)	(43.54,47.35)

Table 6.1: PhC integrated logic circuits summary information results.

We can observe a P_0 average of 10 mW with a standard deviation (Std) of 3.19, a minimum and maximum P_0 of 3 mW and 12 mW, respectively. These values lead to a 95% confidence interval (CI) from 7.85 mW to 12.15 mW, demonstrating well representation for logic 0. On the other hand, we obtained a P_1 average of 45.45 mW with 2.84 of Std. We can observe a minimum and maximum P_1 of 42 and 50, respectively. A 95% CI from 43.54 mW to 47.35 mW is obtained, ensuring excellent achievement for logic 1. Furthermore, we can observe that our PhC integrated components present a CR higher than 5.50 dB. This information reinforces that our PhC integrated devices and circuits

are scalable components with good performance to achieve well-defined values for logic 1 and 0. Furthermore, the PhC integrated devices proposed here have dimensions less than 80 μm $\times$ 50 μm, indicating response time faster than 120 ps (clock rate up to 8 GHz). We can appreciate an ELR lower than 0.065, demonstrating low energy dissipation and loss of information of our PhC integrated circuits.

It is important to mention that our devices operate at the same input and output wavelength ($\lambda \approx 1550$ nm). Our components have great potential for fabrication since the newest technologies for manufacturing PhC devices allow us to obtain devices with an error rate below 5%, with a high rate of repeatability, and at a low production cost [67–71].

Lastly, we remark that our integrated logic gates and circuits are based exclusively on building block devices (switches N and P). This is a valuable contribution of this project compared to previously published works since we can now switch towards the pure circuit design abstraction instead of thinking on isolated components. Following, we discuss some similar works based on different PhC approaches, considering their contributions and drawbacks. Table 6.2 summarizes the information comparison of the devices proposed here with previously published works.

In Ref. [32], it is possible to appreciate all-optical OR, XOR, NOT, XNOR, and NAND logic devices, which are based on the waveguide interference paths approach. The authors reported designs for devices exhibiting a contrast ratio as high as 20 dB under a low power operation regime and a fast response time, lower than 2 ps due to the small footprint area. However, for logic gates up to three inputs, the synchronization and control of the phase difference represent a great challenge. Also, the backpropagation signal to inactive inputs and the unequal threshold values, i.e., the OR and XNOR gates, limited their fabrication and application to achieve computational circuits.

Similarly, in Ref. [37] is presented an interesting design for the NOT, AND, OR, XOR, and XNOR logic gates, where the response time is of the order of a few picoseconds (a bit rate of 0.461 Tbit/s) with a low power operation due to their linear regime nature. Nevertheless, the operation of these devices is based on input phase sensitivity, which implies a phase shift to synchronize input signals, increasing the device size. In addition, the power values representing logic 1 and 0 swap for some devices. Indeed, we can observe that Output Logic 0 for their NOT gate is approximately Output Logic 1 for the OR, XOR, XNOR gates. This fact also reflects on a high variance of the device's contrast ratios. These drawbacks limit their adjacent connection to design circuits and systems.

In Ref. [50] are demonstrated, through topological photonic crystal cavities, the OR, AND, NOT, NOR, XOR, XNOR, and NAND logic gates. They remark that the structure designs use a linear interference approach, working with low operating power and demonstrating excellent performance even when a significant amount of disorder exists. In spite of these advantages, the issues with these PhC structures include their

Ref.	Logic Gates	CR (dB)	Response Time (ps)	Output Logic 0 (mW)	Output Logic 1 (mW)
[32]	OR	-	≈2	-	$\geq 0.45P_0$
	XOR	≈20		$\leq 0.0067P_0$	$\geq 0.75P_0$
	NOT	≈20		$\leq 0.0067P_0$	$\geq 0.75P_0$
	XNOR	≈22		$\leq 0.0061P_0$	$\geq 0.85P_0$
	NAND	≈20		$\leq 0.0065P_0$	$\geq 0.75P_0$
[37]	NOT	3.74	≈2.168	$\leq 0.772P_0$	$\geq 1.326P_0$
	AND	11.47		$\leq 0.131P_0$	$\geq 1.717P_0$
	OR	12.48		$\leq 0.051P_0$	$\geq 0.717P_0$
	XOR	6.50		$\leq 0.133P_0$	$\geq 0.574P_0$
	XNOR	6.50		$\leq 0.133P_0$	$\geq 0.574P_0$
[50]	OR	54.4	-	0	$(\sqrt{2}Ee^{-i\pi/2})/2$
	AND	9.54		$(\sqrt{2}Ee^{-i\pi/2})/8$	$(3\sqrt{2}Ee^{-i\pi/2})/8$
	NOT	54.4		0	$\sqrt{2}E/2$
	NOR	9.54		$(Ee^{-i\pi/2})/4$	$(3Ee^{-i\pi/2})/4$
	XOR	54.4		0	$\sqrt{2}E/2$
	XNOR	32.6		0	$(Ee^{-i\pi/2})/2$
	NAND	31.1		0	$(Ee^{i\pi/2})/2$
[54]	NOT AND NAND	20	15.43	-	0.52A
This work	SwN	6.98	50	≤10	≥50
	SwP	6.23	50	≤12	≥42
	AND	6.19	80	≤12	≥50
	OR	8.65		≤6	≥44
	NAND	5.74		≤12	≥45
	NOR	5.92		≤12	≥47
	XOR	11.56		≤3	≥43
	FANOUT	8.36		≤7	≥48
	HA	5.54		≤12	≥43
	FA	5.64	120	≤12	≥44

Table 6.2: Information parameters such as response time, input and output power values, and contrast ratio of PhC works in the literature within the domain of logic devices and circuits.

input phase dependence and the large footprint area of the PhC structures (up to 100 μm $\times$ 45 μm), which lead to a low clock rate.

In Ref. [54] is presented an interesting and working designs for easily scalable all-optical NOT, AND and NAND logic gates using bandgap solitons in coupled PhC waveguides. The authors reported that the logic gates topologies operate with temporal bandgap solitons having stable pulse envelopes during signal processing in the different coupled PhC waveguides. In addition, the building blocks can be cascaded using the output signal from one stage as a new input signal for the subsequent stage aiming at either different logic operators or multiple input logic gate architectures. Equally important,

another advantage of this strategy is the absence of intermediate signal amplification between different coupled PhC waveguides stages or even different logic gates due to the soliton nature of the signal pulses. As an example the authors presented the NAND gate built by connecting the proposed AND and NOT gates. Nevertheless, high input power is required, increasing the energy consumption of the devices since additional source signals are necessary. For instance, three signal pulses were applied to achieve the single NOT gate. Also, the coupling between the PhC waveguides realized along the propagation direction within the device could lead to undesired interference effects when disorders or fluctuations are introduced at the holes close to the waveguides. Although authors accomplished a NAND gate by cascading the AND and NOT gates, it still lacks the design of advanced circuits such as the XOR, Half-Adder, or Full-Adder. In addition, a bridge section was proposed in order to cascade the logic gates. Its design appears to be challenging to achieve for different circuits and could increase the footprint of the devices, decreasing the desired performance. Finally, the simulated refractive index used in the PhC structure could be hard to achieve experimentally since it does not correspond to the commonly used materials in Silicon Photonics.

Chapter 7

Conclusions

This thesis explored the fundamental properties of Photonic Crystals targeting the design of photonic integrated circuits and computational systems. Indeed, our work solves some of the problems exhibited by previously proposed logic gates in PhC. We are now able to design circuits rather than isolated devices by applying our demonstrated universal logic devices switches N and P. It means that we can design any combinational circuit in a similar way that it is made with CMOS technology for digital electronics. Thus, we can design PhC integrated circuits and components for a wide range of applications for many fields of knowledge by applying a similar well-known and mature CMOS methodology. It also could simplify a possible migration from electronics to photonics.

To achieve our goals, we first presented an interesting PhC slab design that allows strong confinement of the electromagnetic TE00 mode and ensures single-mode propagation. The slab is composed of a sandwiched heterostructure of GaAs/AlGaAs with effective refractive index $n_{eff} = 2.87$. The 2D pattern is based on a triangular lattice of holes embedded in a substrate, exhibiting a PhC band-gap within the C band of the telecommunication window, i.e., 1550 nm. We expect to experimentally demonstrate our proposed devices applying fabrication techniques that were successfully applied to manufacture a similar PhC components.

We demonstrated an approach to achieve well-defined logic states representations. To accomplished it, we used a PhC side-couple system consisting of a PhC waveguide interacting with a Kerr nonlinear PhC cavity. In this, the PhC cavity works as an optical resonator and allows the system to fluctuate between high and low power states at an specific frequency. It allows us to achieve well-defined power value representations for logic 1 and 0. This approach allows us to break some of the drawbacks found in other methodologies such as self-collimation, MMI, and waveguide interference paths.

We proposed the Complementary Photonic Crystal Integrated Logic Devices, consisting of the Switches N (SwN) and P (SwP). These devices are the PhC equivalents to the NMOS and PMOS transistors, respectively. We demonstrated via extensive and reliable FDTD simulations the correct operation of these devices. As a result, we achieved a footprint area less than 25 μm $\times$ 15 μm for both switches. The devices also exhibit an ELR lower than 0.045, a clock rate of 25 GHz with a contrast ratio up to 6 dB at an

input/output operating wavelength of about 1550 nm. We also demonstrated through a power analysis that the SwN can operate as an optical amplifier and as an AND logic gate. On the other hand, the SwP can act as a signal reducer and as a logic inverter. The switches can support small phase delay ($\lambda/28$) at the input sources, changes in their Input power levels ($\pm$5 mW), and hole disorder effects around the cavity ($\pm$20 nm), the most sensitive region. These fluctuations, within current experimental tolerances, resulting in about $\pm$5 mW signal noise at the output for both switches. So, for the first time, our CPCL devices can support the development of PhC integrated circuits and systems by their adjacent connections breaking the limitations of the previous works.

Finally, we designed a complete set of logic gates by exclusively applying the CPCL acting as core hardware devices. Specifically, we presented PhC designs for the AND, OR, NAND, NOR, XOR logic gates, for the FAN-OUT component, plus the Half-Adder and Full-Adder (Carry and Sum) circuits. The logic gates and circuits presented here have CR higher than 5.5 dB deduced from power values greater than 12 and lower than 43 representing logic 1 and 0, respectively. These values indicate well-defined logic state representations with fluctuations of about $\pm$3 at 95% of confidence level. At this point, it is important to mention that our circuits work with the same input and output operating wavelength. Additionally, we found a response time of 120 ps, meaning a clock rate of 8 GHz, for our larger circuit (Full-Adder). We computed a footprint area less than 75 μm $\times$ 46 μm for all of our circuits. Additionally, the ELR for our PhC circuits was found be lower than 0.06, demonstrating low energy dissipation and low information loss. Thus, we demonstrated using CPCL exclusively their application to the development of PhC integrated logic gates and circuits. This is a significant contribution of our project to the domain of logic gates and circuits based on PhC since we can now build systems instead of isolated devices. In general, although our devices are larger than their electronic counterparts, they can be efficiently integrated into the network and optical fiber technologies, allowing the design of telecommunication components operating at a high speed of data processing and under a low consumption regime. This could be possible since we can avoid the electronic-optic signal conversions.

Future Work

The current research presented encouraging results, but many problems remain open to be addressed. Here, we discuss some possible future directions that we believe can contribute to improving the domain of development of photonic integrated logic circuits and systems.

Device Microfabrication. The fabrication process of devices is an important step to incorporate them into the industry and technology. Also, it helps to validate physical theories, which is the key idea in the modern scientific method. Although our integrated PhC SwN and SwP were designed using a practical approach for microfabrication, this thesis project focused on their theoretical demonstration through extensive, accurate, and reliable simulations and numerical analysis. At this point, we call attention to the next move to develop the fabrication methods and techniques for the experimental demonstration of our devices. We strongly believe this is a realistic step since we have evidenced technological advances for the fabrication process of III-V PhC devices. Also, there are some experimental demonstrations for similar heterostructures to the one used in this thesis [67–71].

Information Crossing Device. This PhC component will be capable of transmitting the information of two inputs (A and B) to two outputs (B' and A'), as illustrated in Figure 7.1 and detailed in Table 7.1.

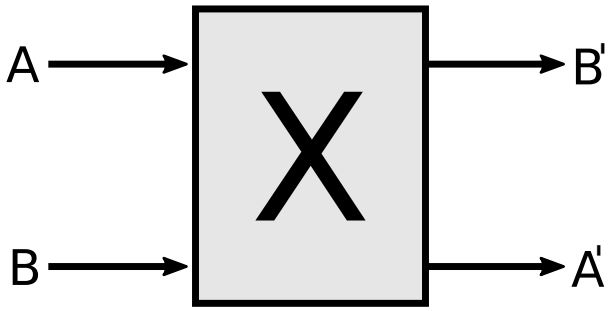


Figure 7.1: PhC information crossing device diagram.

A	B	A'	B'
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Table 7.1: Truth table for the information crossing device.

We can appreciate that an intersection between the inputs (A and B) occurs transmitting their information to the output branches. So, the main purpose of this device is to carry clean and equal power than the inputs applied to the outputs, avoiding constructive and destructive interference phenomena.

We expect that the development of this device could lead to PhC integrated circuits with lower power consumption and a smaller footprint area. In addition, we believe that research on nonlinear photonics, 3D PhC, or coupled quantum dots on microcavities could be possible solutions.

PhC Hybrid Integrated Circuits. This thesis project proposed and demonstrated

PhC circuits based on CPCL acting as core hardware devices. In addition, during the development of our research, we addressed a PhC compact and integrated design that can operate as the NAND and NOR logic gates [39].

Thus, an interesting research path towards the realization of efficient PhC sensors, systems, signal processing components and devices could be enhanced by combining the most important features of CPCL devices and circuits with the relevant behaviors of the compact and linear PhC devices. In effect, we can think of compact logic gates (presented in Section 3.3) connected to the switches as an optical amplifier or attenuator. As a result, we can achieve PhC circuits with better power responses to represent the logic states, smaller sizes, and higher clock rates. In the same direction, regarding the MMI and Self-collimation PhC devices presented in Section 3.1 and Section 3.2, frequency shifters with improved response could be designed by applying CPCL.

Modeling of High Level PhC Circuit Simulator. Despite FDTD is a well-established and accurate method, its high computational cost and the need for advanced knowledge of electromagnetic simulation intricate its application to design and analyze large integrated PhC logic circuits and systems. Considering this, it is evident the necessity of developing a PhC CAD tool to support the design of large logic circuits at a high abstraction level. Therefore, this proposal intends to provide a software package for users (circuit designers) to obtain a faster response of PhC circuits through an accurate approximation model rather than run large and expensive FDTD simulations.

CPCL on Plasmonics and Other Platforms Materials. Plasmonics studies the optical phenomena at the surfaces and interfaces of nanostructured metals with dielectrics and semiconductors. These phenomena are due to elementary excitations called surface plasmons, which are coherent collective oscillations of electrons with respect to the lattices [106]. In a similar way of PhC, Plasmonic microstructures can confine light into subwavelength-scale regions and exhibit strong plasmonic enhancement, which provides an approach to scale down photonic devices further and to realize direct integration with solid-state chips [107]. Logic gates based on Plasmonic microstructures have been successfully accomplished [107, 108].

With this in mind, we believe that CPCL can be implemented on Plasmonics using the same approach than for PhC. This implementation can lead to the realization of photonic devices and circuits in a nanometric scale and suitable for applications on light-matter interactions. On the other hand, we can take advantage of the capabilities and mature stage of Silicon technology and replicate CPCL under this material. In this way, SiN or other nonlinear effects such as Two-Photon absorption can be exploited [109, 110].

Photonics for Artificial Intelligent and Vice versa. In recent years we have witnessed rapid growth and development of Machine Learning (ML) algorithms applied to accelerate technology. Specifically, ML offers an efficient means to design photonic struc-

tures, spawning data-driven approaches complementary to conventional physics- and rule-based methods [111, 112]. At the same time, photonic integrated circuits have enabled ultrafast artificial neural networks, providing a framework for a new class of information processing machines. Algorithms running on such hardware can address the growing demand for machine learning and artificial intelligence in areas such as medical diagnosis, telecommunications, and high-performance and scientific computing [6].

Taking the above into consideration, we expect ML conducting to optimized PhC integrated circuits based on CPCL. The main challenge here is to build the datasets which are generally collected from electromagnetic simulations. This can be covered with the high abstraction level PhC circuit simulator previously discussed. On the other hand, we can take advantage of the main capabilities of CPCL in order to design suitable hardware to accelerate ML algorithms.

Neuromorphic Computing. Neuromorphic engineering is partly an attempt to move elements of machine learning and artificial intelligence algorithms to hardware that reflects their massively distributed nature [6]. A Numerical demonstration of neuromorphic computing with photonic crystal cavities was recently presented [113]. In this context, we think that using CPCL coupled to integrated PhC components can address next stages on the field of Neuromorphic Computing.

Publications

The results obtained during our research on PhC logic circuits and systems have been published in recognized conferences and journals dedicated to the field of optics, photonics, microelectronics and computing [36, 39, 103, 114–117]

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