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Modeling and design of a power thyristor-based industrial arc-flash quenching device

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MODELING AND DESIGN OF A POWER THYRISTOR-BASED INDUSTRIAL ARC-FLASH QUENCHING DEVICE

Fernando Venancio Amaral

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FOLHA DE APROVAÇÃO

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To Jesus Christ, our lord and savior, for blessing me with faith and strength.
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"*Low expectations, high hopes.*"

Foreword

This scientific research and development work was born out of the increasing industry demand for safety in workplace, which has been intensified after arc flash risk was recognized around the world as a danger no less important than electric shock. In oil & gas sector, this concern is intensified by the fact that an arc flash occurrence is capable of triggering part of the facility into fire, leading to a disaster. The research group that the author of this dissertation is involved with started to investigate a power electronics-based solution to this problem around the year 2015, when the masters thesis entitled *Estudo e Projeto de um Sistema Rápido de Supressão de Arco baseado em Tiristores de Potência* (Study and Design of a Fast Arc-flash Suppression System Based on Power Thyristors) was presented by Claudio Alvares Conceição within the Graduate Program in Electrical Engineering, Universidade Federal de Minas Gerais. The results were so promising that since then, two Ph.D. works were set forward: (i) a continuity of the study on the thyristor behavior when applied as an arc flash suppression switch, which is centered on its physics of failure; and (ii) the present work, which is focused on design and operational reliability aspects of the proposed solution. These works are complementary in their nature and compose, together, part of a research project funded by Petrobras / ANEEL.

Resumo

Desde que as faltas a arco em sistemas elétricos começaram a ser reconhecidas como um importante perigo em ambiente industrial, soluções têm sido propostas para mitigação dos seus efeitos a pessoas e equipamentos. A mais recente é baseada em uma chave eletrônica, composta essencialmente por dois tirisores conectados em antiparalelo entre si e em série com um uma impedância limitadora de corrente. Esse arranjo é imediatamente acionado quando uma falta a arco é detectada no barramento de um painel de distribuição ou centro de controle de motores, suprimindo essa falta em um intervalo de tempo da ordem de microssegundos e praticamente anulando a energia incidente. O projeto e / ou especificação desses elementos não é tarefa simples, sendo dependente de muitas variáveis, como a razão de curto-circuito e o arranjo dos dispositivos de proteção a montante. A principal contribuição desta tese de doutorado é a proposição, desenvolvimento e validação de uma solução que trata com profundidade do ponto acima apresentado, em níveis plenos de tensão e corrente. Destacam-se: (i) um estudo para predição da suportabilidade de tiristores de potência a surtos de elevada corrente de um e de vários ciclos c.a. na frequência fundamental, com diferentes amplitudes entre ciclos consecutivos, sendo esta uma condição diversa dos testes apresentados nas folhas de dados desses dispositivos; e (ii) a análise e proposição de diretrizes para o dimensionamento da impedância limitadora de corrente, de forma que a corrente no supressor e no sistema elétrico a montante seja reduzida, mas ainda assim garantido a eliminação da falta. Tanto (i) quanto (ii) são validados computacional e experimentalmente. Contribuições sobre a modelagem em tempo discreto de faltas a arco internas também são apresentadas.

Palavras-chave: Sistemas elétricos industriais; Proteção de subestações; Segurança elétrica; Arco elétrico; Tiristores

Abstract

Since arcing faults in power systems started being recognized as a hazard in the industry, solutions have been proposed to the mitigation of its effects on equipment and personnel. The most recent rely on a power electronics-based switch, composed by two antiparallel thyristors connected in series with a current-limiting impedance, that is immediately operated when an arcing fault is detected by a relay in a busbar of a switchgear or motor control center, quenching the arcing path in a time interval of the order of microseconds and practically annulling the incident energy. The design and / or specification of these elements is not a simple task, being dependent on many variables like the short-circuit power and ratio and the existing upstream protective devices. The main contribution of this dissertation is the proposal, development and test of a solution that handles this concern, in full voltage and current levels. Two specific points can be highlighted: (i) a theoretical study useful for the prediction of the ride through capability of power thyristors submitted to high single- and multi-cycle ac, power frequency current surges with different amplitudes among consecutive cycles, which is not a standard data sheet test condition that can be readily used; and (ii) the analysis and proposition of fundamental guidelines to the design of a current-limiting impedance so that the surge current through the electronic switch and the upstream power system is reduced still guaranteeing that the arcing fault is safely eliminated. Both (i) and (ii) are validated by simulation and experimentally. Contributions on the discrete-time modeling of an internal arcing fault are also given.

Keywords: Industrial power systems; Substation protection; Electrical safety; Arc-flash; Thyristors

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Nomenclature

Roman Symbols

C	Capacitance
c	Capability
d	Diameter
Δt	Time step
E	Energy
ℓ	Lenght
F	Magnetic force
f	Frequency
G	Stationaty arc conductance
g	Instantaneous arc conductance
h	Impulsive response of a linear system
I	Current level
i	Instantaneous current
j	Unit imaginary number $\sqrt{-1}$
L	Inductance
N	Number of
P	Power

p Recursive convolution constant

q Recursive convolution constant

R Resistance

r Instantaneous resistance

s Laplace's variable

T Temperature

t Time

u Unit step function

V Voltage level

v Instantaneous voltage

X Reactance

x Input signal of a system

Y Admittance

y Output signal of a system

Z Impedance

Greek Symbols

α Horizontal axis on Clarke transformation

β Vertical axis on Clarke transformation

κ Asymmetry factor

ω Angular frequency

π $\simeq 3.14\ldots$

ϕ Angular phase

τ Time constant

θ Geometric angle in deg or rad

Subscripts

0	Zero-sequence
1	Positive-sequence
A	Phase A
a	Arc
ac	Alternating current
ak	Anode-to-cathode
B	Phase B
b	Bus
bl	Blocking
C	Phase C
c	Case
cbl	Cable
cd	Conduction
cr	Critical
cyc	Cycles
D	Direct
d	Dissipated
dc	Direct current
ℓ	Low
Fk	Phase k fault
Fn	Fault n
G	Ground
GT	Gate trigger

h	High
hc	Half-cycle
htc	Heat chamber
i	Generic index i = 1, 2, 3, ...
$j-c$	Junction-to-case
k	Phase k
ka	Cathode-to-anode
kN	Phase k-to-neutral
L	Line
l	Load
Lk	Phase k load
M	Motor
m	m^{th}
max	Maximum
min	Minimum
μ	μ^{th}
N	Neutral
n	Generic index n = 1, 2, 3, ...
O	Constant, per-length
oc	Open-circuit
OV	Overload
p	Pulse
pk	Peak
q	Generic initial time stamp

R Reverse

r Rated

RM Repetitive maximum

S Source

s ac tests

sc Short-circuit

scp Stray capacitance

Sk Phase k shunt branch

sw Switching

sym Symmetrical

T Thyristor

t Time-related

th Thermal

Th Thévenin equivalent

TSM Transient surge maximum

v Voltage drop-related

vj Virtual junction

w Generic final time stamp

x Node x

z Recursive convolution-related

Acronyms / Abbreviations

ac Alternating Current

AF Arc-Flash

AFR Arc-Flash Relay

$ATPV$ Arc Thermal Performance Value

BCT Bi-directional Control Thyristor

CB Circuit Breaker

$CLCB$ Current-Limiting Circuit Breaker

$CONT$ Contactor

dc Direct Current

DPG Double phase-to-ground

DSP Digital Signal Processor

$DTRC$ Discrete-time Recursive Convolution

DUT Device Under Test

dvc Device

EMC Electromagnetic Compatibility

$EMTP$ Electromagnetic Transients Program

EPP Equivalent Power Pulse

$ERMS$ Energy-Reducing Maintenance Switch

ESR Equivalent Series Resistance

FCT Fault Clearing Time

FDR Feeder

GTO Gate Turn-off Thyristor

HRC Hazard Risk Category

HRG High Resistance Grounded

IE Incident Energy

IEC International Electrotechnical Commission

IED Intelligent Electronic Device

$IEEE$ Institute of Electrical and Electronic Engineers

$IGBT$ Insulated-Gate Bipolar Transistor

$IGCT$ Integrated Gate-Commutated Thyristor

IR Infrared

LV Low-voltage

$LVPCB$ Low-Voltage Power Circuit Breaker

MCC Motor Control Center

$MCCB$ Molded Case Circuit Breaker

MCP Motor Circuit Protector

$MSAE$ Multi-sectional Arc Eliminator

MTR Motor

MV Medium-voltage

NA Not applicable

NEC National Electrical Code

$NFPA$ National Fire Protection Association

NTC Negative Temperature Coefficient

$OCPD$ Overcurrent Protective Device

OCR Overcurrent Relay

OL Overload

$OSHA$ Occupational Safety and Health Administration

PCB Printed Circuit Board

PCT Phase Control Thyristor

PF Power Factor

PFD Probability of Failure on Demand

PLL Phase-Locked Loop

POW Point-on-Wave

PPE Personal Protective Equipment

PPT Pulse Power Thyristor

PTC Positive Temperature Coefficient

$p.u.$ Per-unit

$R\&D$ Research and Development

RMS Root Mean Square

SCR Silicon-Controlled Rectifier

SPG Single phase-to-ground

$SSCB$ Solid-State Circuit Breaker

Std Standard

$SWGR$ Switchgear

$TACS$ Transient Analysis Control Systems

TCC Time-Current Characteristic

TR Technical Report

UL Underwriters Laboratories

UV Ultraviolet

ZSI Zone Selective Interlocking

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Chapter 1

Introduction

"Society needs visionaries of means, not dreamers of ends."
Power vs. Force - David R. Hawkins, Ph.D.

This chapter presents the basic structure of the dissertation, providing the reader with an overall view of its context, its scope and the driving line established to ensure the proper development of the work from the problem delimitation to the proposition and development of an appropriate solution through a convenient methodology.

1.1 Context and Relevance

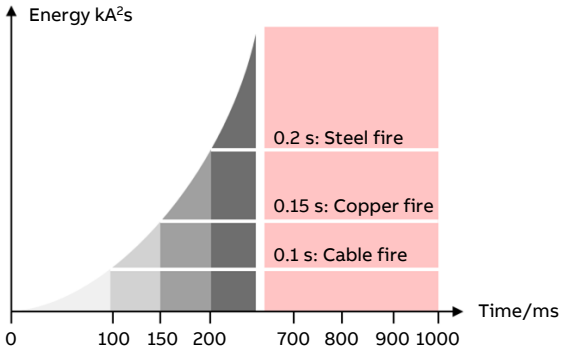
While the ideal solution is to deenergize[1] the electrical system during maintenance, this may not be possible in mission critical facilities such as commercial buildings, hospitals and data centers (Latzo, 2011; Arefi and Abur, 2015). This demand has created the need for electrical workers to operate and perform maintenance work on exposed live parts of electrical equipment like *switchgears* (SWGRs) and *motor control centers* (MCCs) (Simms and Johnson, 2013), which is a condition prone to incidents due to human error - a wrench left behind in the equipment (Littelfuse, 2017a; Rajvanshi and Hawkins, 2017) or an improper working procedure (El-Mahayni et al., 2017; Haluik, 2017; Roberts et al., 2017), for example -, bad cable terminations and loose busbar joints (which cause degradation due to the associated temperature rise) (Hussain et al.,

[1]Even the task of checking if a power system is in fact deenergized poses safety issues to the operators.

2016; Faried et al., 2017), broken insulation between live conductors and between energized conductors and ground due to aging, accumulation of moisture and dust, contamination and corrosion (GE, 2015; Littelfuse, 2017a), transient voltage surges (Rajvanshi and Hawkins, 2017), presence of animals (Parikh et al., 2014; SEL, 2017) or mechanical faults (ABB, 2017).

The aforementioned events can lead to internal arcing faults, which are mainly characterized by high temperature (up to 20,000 °C) plasma release and pressure shock waves (rise between 0.3 and 0.7 kgf/cm^2 in less than 10-15 ms) (Gammon et al., 2015). Employee is exposed to hazards like blast fragments, hot toxic gases, intense light and high noise level during the execution of energized work around the faulty compartment of the concerned panel, resulting in potential injury or death (Faried et al., 2017; Rau et al., 2017; Valdes et al., 2017b). Downtime, production outage, equipment replacement and reputational damage can also occur (Divinnie et al., 2015; Faried et al., 2017; Rajvanshi and Hawkins, 2017). These consequences can be particularly catastrophic in flammable areas, for example oil & gas industry (Hodgson et al., 2013; Littelfuse, 2016a; SEL, 2017).

Figure 1.1 shows a graph illustrating how the released electrical energy[2] increase along the time during an *arc-flash* (AF), and a picture of a test for the assessment of the damage to a manikin wearing a flame resistant clothing during such condition.



(a) Released energy vs. fault duration.

(b) A manikin subjected to an event.

Figure 1.1 Arc-flash released energy and its power of destruction (ABB, 2018).

[2]A phase-to-phase fault on a 480 V system with 20 kA of fault current lasting for 200 ms provides 2 MJ of energy, which corresponds roughly to two sticks of dynamite (Littelfuse, 2016a).

Industrial AF events are the cause of approximately 80% of electrically-related accidents and fatalities among qualified electrical workers, according to the *Occupational Safety and Health Administration* (OSHA)[3] (Littelfuse, 2015; Seedorff, 2015). References (Krause et al., 2014; Safety and News, 2014; Salisbury, 2014; Campbell and Dini, 2015; LaFlair et al., 2017; Ferro, 2018; James Lagree and DeFloria, 2018; Safety and Health Administration, 2018; Safety, 2020) present more statistics on AF incidents.

1.1.1 Incident Energy

Incident energy (IE) is defined as the amount of thermal energy impressed on a surface, a certain distance from the source, generated during an electrical arc event. It is typically measured in cal/cm^2 (Simms and Johnson, 2013; Safety and Health Administration, 2018; Association, 2021). The increase of the bolted-fault current level, the duration and / or voltage level have been found to impact the level of IE, while the distance from the fault point has an inverse exponential effect on it (Hughes et al., 2011; Lee et al., 2013; IEEE, 2018). Higher fault current will cause higher IE for fixed clearing times. Lower arcing currents can result in slower protection operation, also resulting in higher IE due to the increased protective device operating time (Hodgson et al., 2013). Electrode and enclosure configuration have smaller impact on the IE level. System X/R ratio[4], frequency, electrode material, and other variables were found to have little or no effect on arc current and IE, and so they are neglected (IEEE, 2018).

After a system has been designed and constructed[5], reduction of the clearing time is the most feasible strategy (Simms and Johnson, 2013; El-Mahayni et al., 2017). All of the existing methods for reducing AF hazard in existing systems without a complete replacement of equipment are limited in one extent or another and can incur significant costs in terms of material or operational risk (Roscoe et al., 2011). For new installations, the selection of lower nominal voltages and the reduction bolted fault current level must be taken into account, as well as new technologies that have been designed to address the issue (Durocher, 2015; Burnette et al., 2017).

IE calculation is based on an empirical, inexact method[6], making arcing fault elimination even more important, preferably in its early phase, in which electrical

[3]OSHA is equivalent to the Ministério do Trabalho e Previdência in Brazil, which keeps the NR-10.

[4]This is true for non-extinguished arcing faults. The lower the AF duration, the higher the impact of dc level component on the IE.

[5]This is the predominant scenario of the R&D project that this dissertation is involved.

[6]The Annex D of NFPA 70E presents various methodologies for the calculation of the IE. IEEE Std 1584-2018 is also frequently used. It is based on empirical equations obtained from the results of 1800 experimental tests, which may not represent actual real-world conditions (Association, 2020a).

energy is not yet converted to mechanical / thermal forms (Gordon et al., 2018). Available fault current may vary during the day due to different topologies used for various reasons, either by the serving utility or by the end user. Additional sources of variation in arcing current calculation are: (i) incorrect assumptions regarding conductor impedances; (ii) incorrect assumptions about regenerating sources; (iii) variance in source voltage due to system loading; and (iv) motor contribution (Koutoula et al., 2016; Valdes et al., 2017b). Moreover, phase-to-ground faults can escalate into three-phase faults within two cycles[7] (Dunki-Jacobs, 1972; Stokes and Sweeting, 2006; Mohajeryami et al., 2017), with a considerable increase in the fault current level. Therefore, the additional energy released by single-phase-to-ground faults before becoming three-phase faults can be substantial.

In 1982, Ralph Lee established the curable burn threshold for the human body as 1.2 cal/cm^2 (5 J/cm^2) (Lee, 1982), which is currently used to define[8] the AF boundary (Das, 2012; Laboratory, 2017). To obtain IE levels lower than 8 cal/cm^2 over a broad range of possible fault currents, the protection must clear the fault at 50 ms or less. To be at or below the energy level of 4 cal/cm^2, the system must clear in 25 ms or less. Typical LV *circuit breaker* (CB) operating times are 25 ms (molded case) and 50 ms (power CB) (Kay and Kumpulainen, 2013; Simms and Johnson, 2013). However, when the time required for fault detection and trip signaling is taken into account, total opening time of 50 ms or more is verified (Luna et al., 2011). On the other hand, to achieve less than 1.2 cal/cm^2, clearing should occur within 10 ms (Roscoe et al., 2011).

1.1.2 Arc-Flash Mitigation Techniques

Many companies have been establishing methods to ensure AF mitigation is in place (Pragale et al., 2018). Arc protection can be classified according to the hierarchy of risk control methods presented in Figure 1.2 or divided into two basic groups (Faried et al., 2017):

[7]Therefore, single-phase-to-ground faults do not have the chance to escalate to three-phase if the elimination is completed fast enough. Still, it is possible that the arc initiates including the three phases of the busbar. Practically all faults originating as a three-phase fault were the result of maintenance errors where safety grounds were found to have been left on the equipment when the system was reenergized (Nelson et al., 2014).

[8]NFPA 70E defines as "flash protection boundary" the approach limit at a distance from live parts that are insulated or exposed within which a person could receive a second-degree burn. The IE at this boundary is calculated to be 1.2 cal/cm^2, which results in a curable burn on unprotected skin (Krause et al., 2012; Association, 2021).

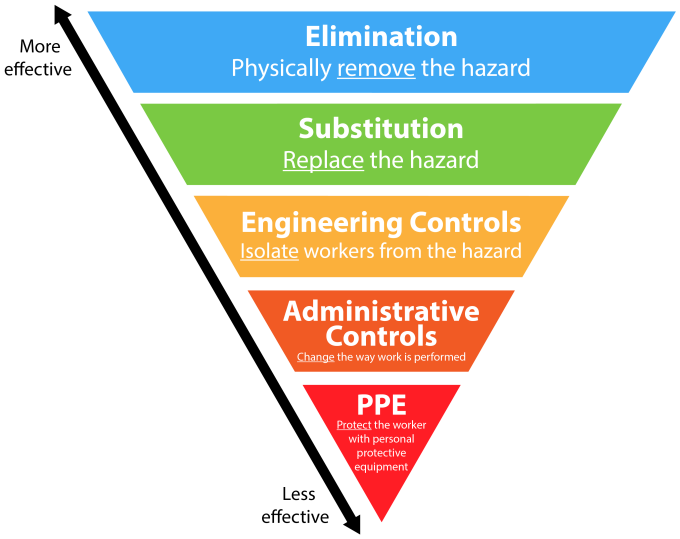


Figure 1.2 Hierarchy of risk control methods (Association, 2021).

1. Pre ignition: to avoid arc faults by appropriate prediction technologies covering analysis of typical pre-arc conditions as well as prevention methods which are more focused on switchgear / MCC design, skilled personnel and maintenance.

2. Post ignition: to mitigate impacts after arc fault ignition with a constructively safe switchgear design as well as active protection systems.

Cost, maintainability, reliability, safety, simplicity and logistical factors (for example, equipment size) affect the suitability of any solution in a given situation (D'Mello et al., 2016; GE, 2017b; Sevov and Valdes, 2017).

Prediction technologies have emerged in the last years, like online monitoring of partial discharges, *infrared* (IR) and *ultraviolet* (UV) systems for detection of incipient faults due to bad connections in LV switchgear, for example (Kumpulainen et al., 2013; Hussain et al., 2014, 2015). These techniques have not been widely implemented, and they cannot avoid AF incidents caused by human errors or by animals (Kay et al., 2011; Kumpulainen et al., 2014).

Regarding prevention methods, both the design of new equipment, retrofit of existing one as well as the design of the feeding power system are very important (Sauve et al., 2017; Valdes et al., 2017a; Parise et al., 2018). The "safety by design" philosophy has been taken into account so seriously that documents specifying fundamental considerations were recently proposed, like IEEE Std 1683 (IEEE, 2014). The main strategies are locating protection, control and testing equipment remote from the primary equipment to increase the "distance to arc" (Liang et al., 2016; Cheng et al.,

2017; El-Mahayni et al., 2017; Valdes et al., 2017a; IEEE, 2018), increase in-line impedance (Simms and Johnson, 2013; Arefi and Abur, 2015; Faried et al., 2017; Bottaro et al., 2019) and application of *high resistance grounded* (HRG) scheme[9] to decrease the arcing current (Floyd et al., 2003; IEEE, 2007; Das, 2011, 2012; Nelson, 2015) and to avoid fault escalation[10] (IEEE, 1994; Littelfuse, 2017a; Association, 2021), full compartmentalization to prevent the spread of arc effluent at high pressure across sections or compartments (Bugaris and Doan, 2014; GE, 2015; D'Mello et al., 2016), and insulation to reduce the arc duration and the chance that a falling object shorts the bus creating a fault (Rajvanshi and Hawkins, 2017). Besides their respective drawbacks, all of these solutions are better accommodated during the facility design phase.

Traditional post-ignition methods rely on a reactive principle, i.e. minimizing the extent of damage after the initiation of an AF (Hussain et al., 2016). The main technique is the application of an arc-resistant switchgear, which diverts the AF explosion effluents to the exterior of the building (Bugaris and Rollay, 2011) - see Figure 1.3. Though ensuring personnel protection under normal operating conditions, it does not during repair work[11]. Arc-resistant SWGR cost is increased since it must be designed and tested according to recognized industry standards, besides the limitation on where the equipment can be installed, since it may be larger and heavier than the standard SWGR. Moreover, its effectiveness rely on the integrity of the enclosure, since an improperly secured panel, door, or cover can compromise its ability to contain the explosion. Finally, it must be noticed that equipment inside an arc-resistant SWGR is damaged, incurring in replacement costs and production interruption after the occurrence of an arcing fault. Furthermore, equipment not designed for arc resistance can not be readily modified to be arc resistant (Roscoe et al., 2011; Sauve et al., 2017).

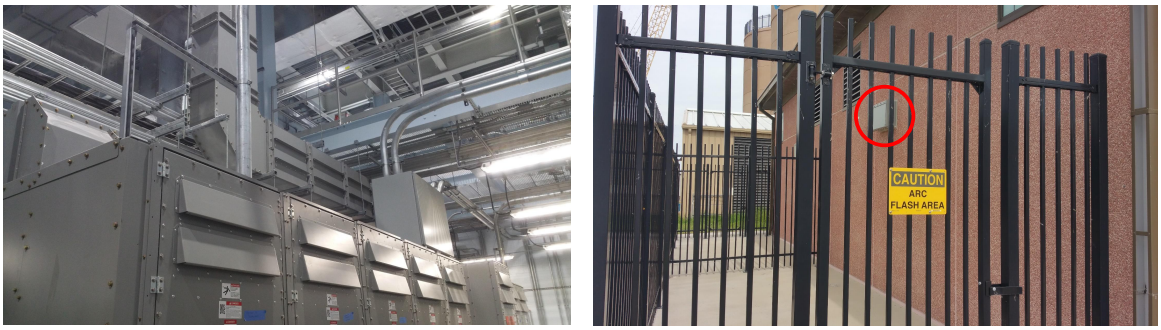
Another conventional post-ignition method is the *personal protective equipment* (PPE), which is currently limited to thermal and acoustic hazards and may only reduce severity of injury to a curable level[12] as opposed to completely protecting the individual

[9]It is a known fact that more than 95% of faults in a power system start as a single-line-to-ground (Nelson et al., 2014). Single-phase can even exceed three-phase fault current levels (IEEE, 1998), propagating into three-phase faults within 5 ms (Nelson et al., 2015).

[10]For this reason article 230.95 of NEC requires ground-fault protection of equipment for solidly grounded electric services of more than 150 V to ground but not exceeding 600 V phase-phase for each service disconnect rated 1000 A or more (Das, 2005; Paul and Chavdarian, 2015).

[11]It has been estimated that 65% of internal arc faults occur with operator working in the switchgear, 25% without operator, and 10% with operator in front of a closed door (ABB, 2017).

[12]NFPA 70E defines 5 *hazard risk categories* (HRC) of PPE, also called *arc thermal performance value* (ATPV). Each of them protects an individual up to a certain IE level: Category 0 (up to 1.2 cal/cm^2); 1 (5.0); 2 (8.0); 3 (25); and 4 (40). When IE exceeds 40 cal/cm^2, the equipment should only be maintained in the de-energized condition. There is no PPE outfits specified for IE release greater than this threshold (Das, 2012).

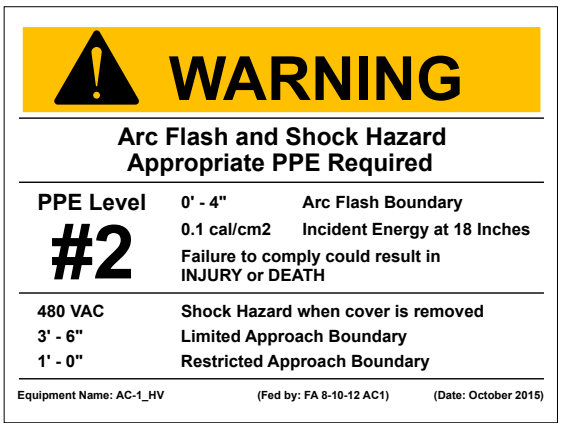


(a) Switchgear zone inside the facility. (b) Escape area.

Figure 1.3 Arc-resistant switchgear (Bukovitz, 2020).

(Crnko and Dyrnes, 2001; Das, 2012; Krause et al., 2012; Rau et al., 2017). Furthermore, end users typically prefer not to wear PPE since it is bulky, hot, restrictive and leads to loss of dexterity (Divinnie et al., 2015; Safety, 2020) - see Figure 1.4. The time required to put it on is typically much longer than the maintenance activity for which it is worn, and training is required to use it effectively (Rajvanshi and Hawkins, 2017). PPE can also lead to a false sense of security. A person may conclude that it is sufficient to mitigate the hazard, when other measures, such as isolation or physical barriers, would be more appropriate under the circumstances by further reducing the risk (Haluik, 2017). Ergo, PPE must be utilized as the last line of defense (Liang et al., 2016), as it is defined in NFPA 70E (Association, 2021). Another drawback of PPE is that equipment and environment are not prevented from damage (Roscoe et al., 2011; Krause et al., 2012; Faried et al., 2017).

Third and last, detection of an arcing fault can be used to trigger an upstream protective device. The early an event is detected, the early a mitigation strategy can be put into work and the less severe are the consequences. In classical protective functions like time-overcurrent and instantaneous overcurrent, the coordination intervals between the *time-current characteristic* (TCC) of adjacent *overcurrent protective devices* (OCPDs) can be reduced to detect arcing faults, but trip times are still likely to be high (from 200 ms to 2 s) since these classical protection schemes are configured to react best to bolted faults, taking longer to isolate arcing faults from a system because of their lower current magnitudes (Simms and Johnson, 2013; Sevov and Valdes, 2017). For arcing faults, the OCPD should operate as quickly as possible at the lowest arcing current levels (Fox, 2015; Sauve et al., 2017), which is a concept opposite to that adopted for bolted faults (Luna et al., 2011; Hodgson et al., 2013; Mardegan and Rifaat, 2015). Other classical protective functions like bus differential do not add coordination intervals or desensitizing pickups, but although having fast operating



(a) Arc-flash label indicating the required PPE level, AF boundary and IE at a distance of 18" (Laboratory, 2017).

(b) PPE (Safety, 2020).

Figure 1.4 Arc-flash label and personal protective equipment.

times (from 20 ms to 60 ms), they are commonly applied in MV systems, where the cost of the relays, instrument transformers and space required for the devices is more easily accommodated (Das, 2012; Valdes and Dougherty, 2014). Finally, it does not provide protection against faults in the feeder cable compartments, which has been documented as the most probable location for an arcing fault in normal operating condition (Kay et al., 2011; Zeller et al., 2011).

Other strategies like *energy-reducing maintenance switch* (ERMS)[13] (Valdes and Dougherty, 2014; Fox, 2015; Sauve et al., 2017) and *zone selective interlocking* (ZSI) implement alternative ways to accelerate the detection of an arcing fault by eliminating intentional coordination delays. Typical clearing time with ERMS is 25-50 ms (GE, 2017b; Eaton, 2018), but it is effective exclusively when personnel are performing energized work in the switchgear or MCC (Kay et al., 2011; El-Mahayni et al., 2017; Walsh and Price, 2017), besides requiring operator intervention, which in turn increases the risk of human error. ZSI utilizes fast communication signals between the upstream main or ties and downstream outgoing feeder trip units of a switchgear (Simms and Johnson, 2013). Typical operation times of the algorithm can range from 4 ms to 30 ms (D'Mello et al., 2013; Smith et al., 2016). The main limitation of ZSI is that it inherently takes time to operate (GE, 2017a; Siemens, 2017). Despite allowing CBs at the 2nd and higher tier to operate faster than if they did not implement ZSI, the lowest tier devices will not operate any faster than they could have without this scheme.

[13]Also called "energy reduction maintenance setting".

Additionally, it is complicated to implement blocking schemes in complex systems with two or more incomers, tie breakers, and varying topology (Sevov and Valdes, 2017).

Arc-flash relays (AFRs) rely on detecting a sudden increase of light intensity instead of an increase of RMS current, which allows for the quickest feasible reaction time (Littelfuse, 2017a; Sauve et al., 2017). Since they are stand-alone protection systems, there is no concern related to coordination with other devices (Faried et al., 2017). A light-based AFR protects a volume[14] instead of a bus, and only from arcing faults, not bolted faults. Optical sensors are divided into point sensor and unclad fiber optic sensor. Point sensor protects a single zone / compartment, while the fiber sensor can cover a wide protection zone since it absorbs light throughout the cylindrical surface over its entire length[15] (Zhou et al., 2014; Littelfuse, 2016a; Faried et al., 2017) - see Figure 1.5. Therefore, selective protection can be achieved (Kay et al., 2011; Kumpulainen et al., 2014). Light sensor inputs are sampled every 125 μs. The relay counts the number of consecutive samples (in general, 3) above the trip level and activates the output[16] when a sufficient number has been achieved. Typical operational time of an AFR is as low as 1 ms (Drewiske, 2014; Zhou et al., 2014). The main concern related to AFRs is that in LV applications within enclosures, where there are multiple air CBs, AFRs can improperly operate due to light caused by a CB interrupting a remote fault (D'Mello et al., 2016). With application of current supervision, the AF event can occur without causing sufficiently high current due to high arcing resistance and weak system source. In addition, current sensing slows down AF detection because current measurement is slower than that of light (Parikh et al., 2014; Seedorff, 2015; Abboud et al., 2016).

Arc detection strategies alone purport improved abatement of thermal effects, but support no degree of pressure minimization (Krause et al., 2012) since an AFR does not clear the fault itself, i.e., it only sends a trip signal to another device, normally a CB, that effectively eliminates the fault. Since an AFR detects an AF in 1 ms and a LV CB has a typical clearing time of 3 to 5 cycles (50-83 ms at 60 Hz) (Seedorff, 2015), it is noticeable that there is inconsistency between the speeds of arc detection, which is done by electronic means, and arc elimination, which is based on an electromechanical device. This is the protective system "bottleneck" (Faried et al., 2017; GE, 2017a). In other words, time required to operate the upstream protective device is not accelerated beyond its electrical / mechanical capability, no matter what is the detection technique

[14] i.e., the protection zone is a definite space.

[15] Fiber can be configured in a loop, providing a continuous self-supervision functionality.

[16] Redundant *insulated-gate bipolar transistor* (IGBT) outputs operate trip signal within 200 μs (Seedorff, 2015).

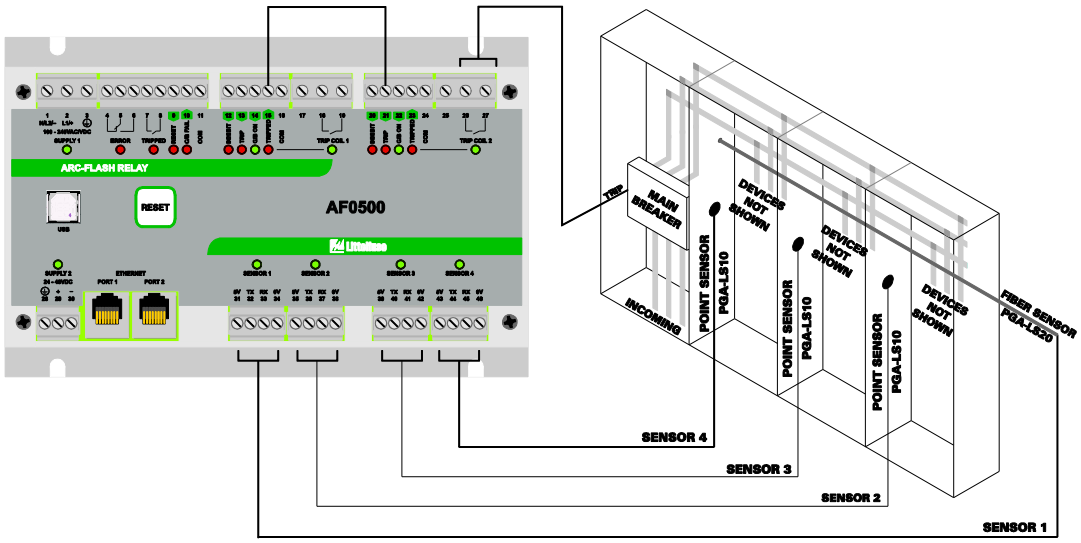


Figure 1.5 Application of arc-flash relays on a typical switchgear (Littelfuse, 2017b).

(Roscoe et al., 2011; Gu et al., 2017). For this reason, even the best detection technique may be not good enough to reduce the IE below the threshold of 1.2 cal/cm^2.

In LV industrial power systems, which is the focus of this work, two types of CBs are mainly encountered: *low-voltage power circuit breakers* (LVPCBs) and *molded case circuit breakers* (MCCBs). LVPCBs are generally characterized by physically large frame sizes, drawout construction, and the highest short-time withstand ratings of all the types of *low-voltage* (LV) CBs. Their clearing times are typically less than 60 ms (IEEE, 2015; NEMA, 2016). MCCBs are devices which current-carrying parts, mechanisms, and trip devices are completely contained within a molded case of insulating material. The arc in a MCCB serves the additional function of suddenly injecting a resistive element into the circuit to limit the fault current. Then virtually all[17] MCCBs interrupt fast enough to limit the amount of prospective fault current let-through, and some limit enough current and operate fast enough - within one half-cycle (Gregory and Lippert, 2012; Valdes et al., 2012; Larsen et al., 2017) - to be identified as *current-limiting circuit breakers* (CLCBs) - see Figure 1.6. Typical clearing times are less than 30 ms (Das, 2012; IEEE, 2015; Wu et al., 2015; NEMA, 2016). However, the arcing current may be a small fraction of the calculated bolted-fault current and, as a result, when CLCBs are used for protection, the available fault current is likely to be below the current-limiting threshold of these devices, causing them to take longer to

[17] A special category of MCCB specifically designed to MCCs is called *motor circuit protector* (MCP) (Das, 2012).

trip and increasing the IE (Walker, 2013). Moreover, CLCBs have limited availability and may require replacement after limited number of operations (Bukovitz, 2020).

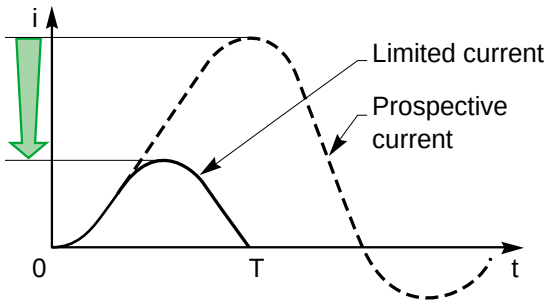


Figure 1.6 Effect of a current-limiting circuit breaker on the fault current waveform (Schueller, 1998).

Other solutions have been proposed for the fast elimination of an arcing fault, like *solid-state circuit breakers* (SSCBs) and controllable fuses. A SSCB offers tripping speeds of up to hundreds of microseconds (Kapoor et al., 2012; Ghanbari et al., 2016; Radmanesh et al., 2016). As there is no mechanical components or parts, neither contact erosion, electric arc, nor strong mechanical shake exists (Alsalemi et al., 2017; Gu et al., 2017). However, a practical, efficient, reliable and economically feasible SSCB, until now, has remained elusive. The main challenges are minimizing on-state losses and off-state leakage current, as well as increasing power density (Meyer and Doncker, 2006; Nasereddine et al., 2013; Shukla and Demetriades, 2015; Hasan et al., 2018; Radmanesh and Fathi, 2018; Song et al., 2018). By applying wide bandgap devices, e.g., SiC or GaN, the performance of SSCBs may be improved so that it becomes suited to industrial and commercial power systems needs (Gu et al., 2017; Peng et al., 2017). In a controllable fuse, the protective relaying senses the arc fault and signals the controllable fuse to change to a faster acting time-current response (Walsh and Price, 2017; Mersen, 2020). Fuse current goes through the main fuse elements and then trough the normally closed contact out to the base of the fuse. In this normal state, the fuse TCC is similar to the original fuse. When an arc fault is detected, the trip signal is sent to the fuse to open its contact. The contact opening routes the current from the output of the main fuse element to the input of a small fuse current. That electrically places the small fuse element in series with the normal fuse element, changing the TCC, and then the short-circuit current is extinguished before its peak is

reached, like in a CLCB. However, commercially available devices are intended for MV applications[18], operating in 5-10 ms (ABB, 2014).

1.1.3 Arc Elimination: Quenching Devices

Since series CBs do not eliminate the arcing path adequately, the other option is to deploy a parallel, normally open, active arc elimination[19] system to extinguish an internal arc by redirecting the uncontrolled energy release into a defined and controlled connection of all 3 phases to earth potential. The voltage at the point of the fault is collapsed to a low value so that arc is no longer sustainable. Arc elimination devices are designed to quench a burning internal arc in less than $1/3^{rd}$ of a cycle ($\approx$ 5 ms at 60 Hz)[20], despite several cycles of high fault current flow through the system until clearing by an upstream device (Zhang et al., 2015; Faried et al., 2017; Siemens, 2017; Katsiris and Scheuerman, 2018). These devices manage the fault, not the flash.

Along with tripping the arc quencher, the arc detection system sends a trip command to the upstream CB, which eliminates the short-circuit current within a few cycles. Thus, the elimination of the fault is carried out in two phases: in the first phase, the arc is quenched by the arc eliminator, and then, the short-circuit current is eliminated by the CB (Kay and Kumpulainen, 2013) - see Figure 1.7.

The effectiveness of a quenching device in comparison with other methods is noticeable since it is the only capable of extinguishing the fault before the peak pressure wave is achieved inside the switchgear, which would occur around 6 ms after the initiation of the event. The technology is listed in IEC standards as an option to provide highest possible level of protection to persons in case of an internal arc in a SWGR, besides procedural simplicity, power system reliability and improved system availability (Kumpulainen et al., 2014). Troubleshooting, repair, testing, and return to service are simplified and relatively quick. In addition, it is desirable that quenching devices can be added after normal equipment installation, as well as the ability to be easily tested without the need for cumbersome high-current and / or high-voltage test equipment (Roscoe et al., 2011).

[18] Besides the limited availability, one has to bear in mind that fuses must be replaced after operation.

[19] Also called crowbar unit, arc quencher, high-speed earthing device or arc-flash suppressor. Standard EN 50110-1 (for Electrotechnical Standardization, 2013) defines "arc quenching" as "A fast-acting low-impedance arc-flash mitigation system which has a total clearing time from arc-flash initiation to complete extinguishing of the arc-flash event in less than 6 ms." NFPA 70E Annex O.2.3(4) gives a similar definition, but does not define a maximum time. However, it requires that "the energy-reducing active arc-flash mitigation system works without compromising existing selective coordination in the electrical distribution system."

[20] Notice how this is compatible with the operating time of the detection system ($\approx$ 1 ms).

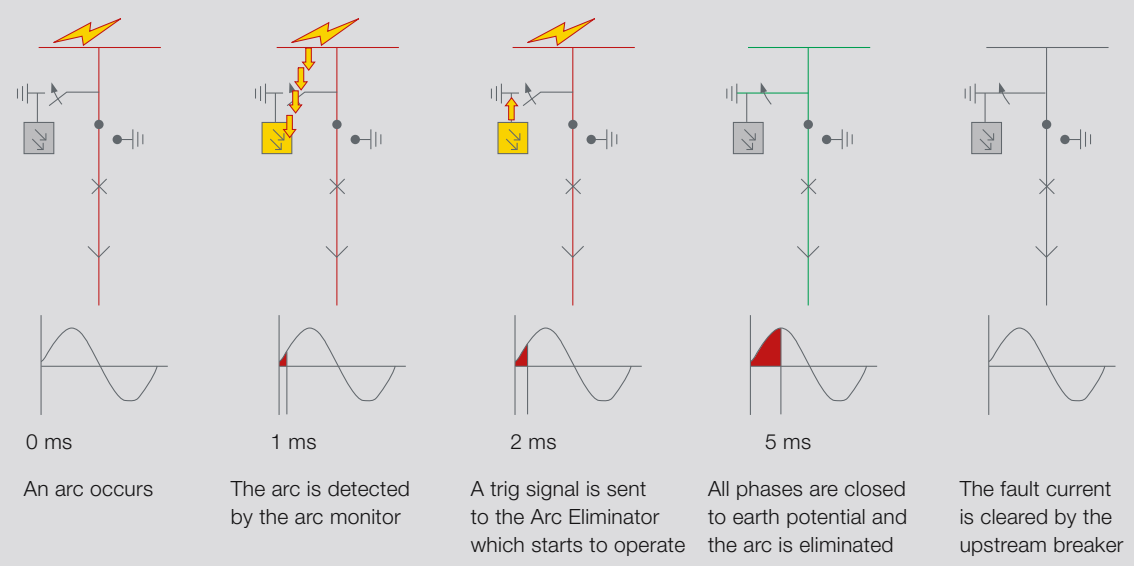


Figure 1.7 Operation steps of an arc eliminator (Gemme et al., 2008).

Quenching devices have been criticized because a bolted fault remains on the system until cleared by the source overcurrent device. However, a bolted fault is not a new concern for equipment ratings, since a power system shall be designed to withstand the electromagnetic forces and thermal stresses produced during the flow of short-circuit currents, regardless of quenching device installation or not. Despite the fact that the bolted fault peak current due to arc eliminator operation is larger than the peak current due to an arcing fault alone, phase-to-ground arcing faults on solidly grounded systems are expected to escalate to three-phase faults (Roscoe et al., 2011; Divinnie et al., 2015). Finally, when an arc eliminator operates, it creates an intentional, controlled short-circuit with balanced current, which is less detrimental than some asymmetrical currents - a phase-to-phase-to-ground fault leads to a current 173% higher than a three-phase fault, for example. In conclusion, the risk level is acceptable and the benefits of using arc eliminators clearly overweight the negative consequences of the potentially increased current level (Kay and Kumpulainen, 2013).

Various manufacturers have different technologies related to the shorting of the circuit (Kay and Kumpulainen, 2013; Kumpulainen et al., 2014; Divinnie et al., 2015).

Mechanical Quenching Devices

In the group of mechanical quenching devices, the main technologies available are pyrotechnical pressure elements and micro gas cartridges. In the first case, a pyrotechnically initiated actuator, as used in airbag systems, fires a copper bolt that penetrates

an insulation plate to establish electrical contact (one per phase). This is currently available for LV switchgear assemblies up to 690 V. Rated short-time withstand current of the quenching device depends on the time duration: 85 kA / 1 s, 105 kA / 500 ms, and 150 kA / 200 ms.

In the second case, a vaccum interrupter specially developed for this application in conjunction with a phase-independent micro gas generator mechanism for energy storage ensures that the switching operation is completed within 1.5 ms. When tripped, the micro gas generator causes a rapid pressure rise in the piston chamber surrounding it. Propelled in this way, the piston penetrates the lid of the vaccum interrupter at the prepared rupture point, and drives the moving contact, which is at earth potential in its initial position, into the fixed contact socket which is at busbar potential. A firmly latched, undetachable connection is established - see Figure 1.8. As this proccess is irreversible, the tripped primary switching element is to be replaced with a new one after a switching operation. The replacement of the micro gas generator should be executed each 15 years, and this work is to be performed by the manufacturer. Total extinguishing time is less than 4 ms after detection. The system can be used in any new or existing short-circuit proof switchgear system. Test results indicate the IE level peak was 0.5 cal/cm^2, which is well below the AF threshold of 1.2 cal/cm^2, where PPE is required. It is available for voltages from 1.4 kV to 40.5 kV, which does not prevent it from being used at LV. Rated short-time withstand currents are 130 kA / 3 s, 165 kA / 2 s, and 220 kA / 500 ms (ABB, 2015).

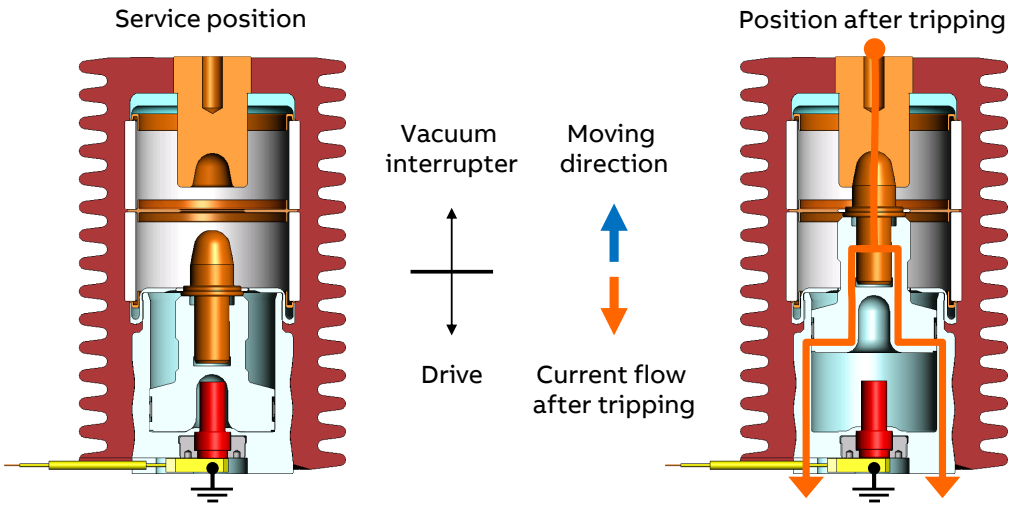


Figure 1.8 Principle of operation of a vaccum interrupter-based eliminator (ABB, 2018).

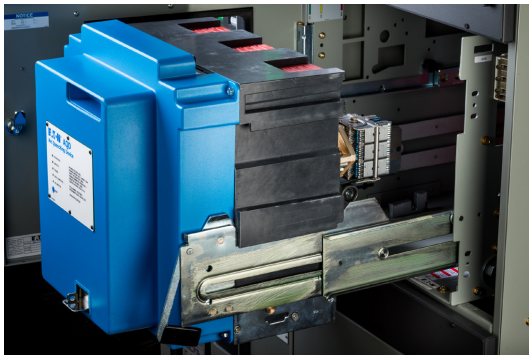
Electromechanical Quenching Devices

The main technologies available in this group are arcing chambers and Thomson coil elements. Chamber-based eliminators have no moving parts. When activated, a plasma gun is triggered to break down the dielectric in the air gap within the absorption chamber. The arc from the plasma gun derives its power from a capacitor array. The resulting arc creates a lower impedance between the three phase electrodes compared to the open air or "in equipment" arcing fault. This low impedance path is not a bolted fault and in turn re-directs fault current originally flowing towards the arcing fault within the controlled environment of the containment chamber, where the "in equipment" arc is then safely cooled and vented, being extinguished as the bus voltage decreases due to the low impedance path within the absorber. The time required to quench the open-air arc is 8 ms. Since this system works at arcing fault current levels, as opposed to bolted fault levels, there is a significant energy reduction. The commercially available containment dome of the product is about the size of a 800 A frame breaker - see Figure 1.9a - and is rated for applications of 65 kA at 480 V. It requires service and / or replacement after 1 arc incident event if it lasts longer than 6 cycles (Clapper, 2015; GE, 2015).

More recently, a new technology, also based on producing a controlled arc inside a containment dome, has been developed and is currently available as shown in Figure 1.9b. Its operation mechanism is represented in Figure 1.10. In this case, the operation is on a per-phase basis (Burns et al., 2019; Eaton, 2019, 2021). When a trip signal is received from the AFR, an actuator produces subtle current circulation through an arc trigger wire, which was previously physically arranged so that it is subjected to a Lorentz force that results in repulse between its parallel segments. Once the repelled segment touches the upper pole of the eliminator, an AF is formed inside the chamber and the elimination process takes place.

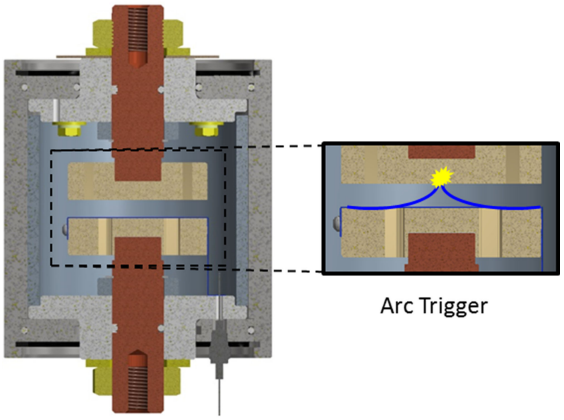
Thomson coil - see Figure 1.11a - is a fast mechanical switch based on repulsion coil, which can achieve faster mechanical operation (3.5 ms) compared to a conventional magnetic mechanism. When the trip signal is applied to a control switch, it turns on and allows a pre-charged capacitor bank ('C' in the figure) to discharge through the opening coil ('B' in the figure). The fast rising discharge current in the coil induces current in the copper disk ('D' in the figure), located between the opening and closing coils, which results in a strong repulsive force F between the coil and copper disk. As the coil is held firmly by its container on a stationary frame, the copper disk will be repulsed to move downward and close the switch. This movement is stopped by a disc spring with a hold and latch mechanism. The device should be tested after each

(a) (Clapper, 2015).

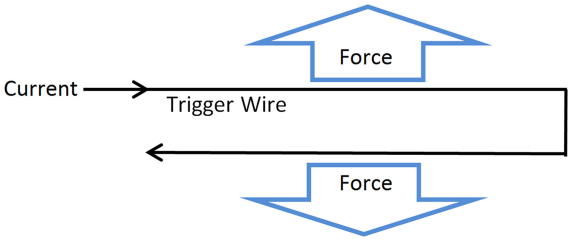


(b) (Eaton, 2021).

Figure 1.9 Arcing chamber eliminators.



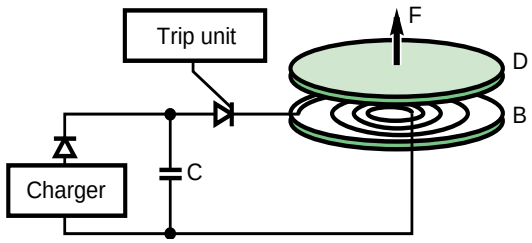
(a) Cross sectional view.



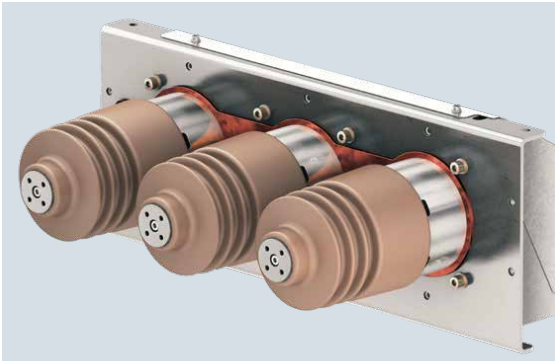
(b) Operating mechanism of the trigger wire.

Figure 1.10 Containment dome and its associated trigger wire (Burns et al., 2019).

operation before being put in operation again, and its operation would be guaranteed only up to 2 times (Ahn et al., 2015). There are commercially available Thomson coil-based devices both for low- and *medium-voltage* (MV) levels. For MV level - see Figure 1.11b, the equipment operates no more than 5 times (Siemens, 2021). For LV level, no more than twice (Arcteq, 2021).



(a) Schematic diagram of the Thomson coil element (Schueller, 1998).



(b) A commercially available three-phase, MV equipment.

Figure 1.11 Electromechanical arc-flash quenching device (Siemens, 2019).

Electronic Quenching Devices

In arc protection applications which utilize an arc eliminator device, while aiming at mitigation of the pressure impact along with the thermal impacts of the fault arc, every millisecond counts (Valdes et al., 2012; Kumpulainen et al., 2017; Valdes et al., 2017b). However, mechanical and electromechanical quenching devices have some technological limitations like mandatory replacement after one or a few operations and the impossibility of being tested in normal operation - they have to be trusted (Divinnie et al., 2015).

Some proposals on the application of power electronics devices to arc elimination have been made in the last years. Alsalemi et al. in (Alsalemi et al., 2017), for example, presents the application of a series voltage compensator, which is primarily designed for power quality purposes, to synthesize phase-opposite voltages in relation to the grid voltages, resulting in zero voltage at the faulted bus. The main drawback of this solution is that the series converter has to stay constantly operational, regardless the existence of a power quality problem or an arcing fault. It leads to increased system losses and lower reliability. Moreover, the design of a series converter including its application as an arc eliminator impacts the selection of power components, leading to increased cost, weight and volume.

Other references have proposed the application of power thyristors in AF elimination (Zhang et al., 2015). The main reason for choosing the thyristor is its fast turn-on speed - which is crucial -, high thermal endurance, compact size and lower price compared to other solid state candidates of similar rating. Figure 1.12 presents a schematic diagram of the solution that will be studied in this work, which has been previously presented in (Conceição, 2015). In this figure, V_{kN}, $k \in$ {A,B,C}, is the phase k-to-neutral

open-circuit voltage at the secondary of the MV-LV transformer[21], Z_k is the phase equivalent impedance, Z_N is the transformer neutral-to-ground impedance (if any), S_k is the eliminator switch, Z_{Sk} is the phase k switch-to-ground impedance, and Y_{FA} is the arcing admittance supposing a single phase A-to-ground fault. Once the switch S_A is closed, fault current I_{FA} commutes from the arcing path (Y_{FA}) to the quenching device path (Z_{SA}). The shunt impedance Z_{Sk} limits the short-circuit current to a lower value compared to bolted-fault current. Another benefit is that thyristors can be monitored / diagnosed during normal operation (online).

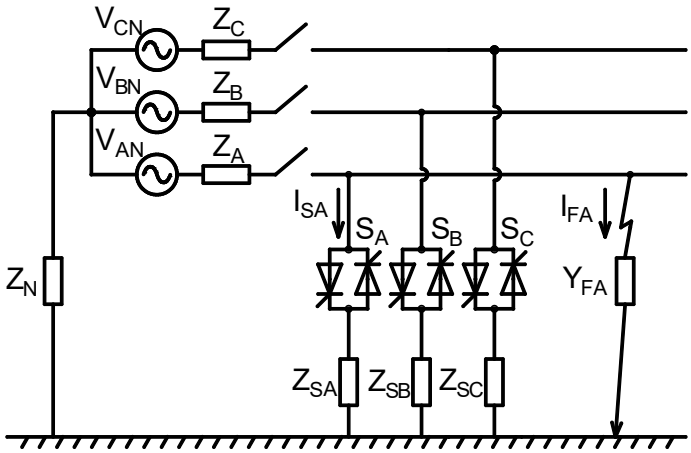


Figure 1.12 Electronic arc-flash eliminator.

More recently, Nowak et al. (Nowak et al., 2019, 2020, 2021) proposed that multiple branches of thyristors can be associated in parallel to perform the task of arc elimination. These branches have different number of thyristors - see Figure 1.13, which are fired according to the specific angle of measured voltage waveform. The higher is the number of thyristors of the active branch, the higher is the voltage drop across the eliminator, assigning some redundancy level to the equipment as well. The main disadvantage of this approach is the component count and the associated triggering and phase-control circuitry, which in turn reduces the reliability of the solution. Moreover, the thyristors are not used at their full capability, and the result is more weight, volume, cost, and complexity of operation and maintenance.

Both aforementioned works discussed their respective ideas and presented results only in the field of single-phase tests with extremely reduced current and voltage levels,

[21] See Figure 2.1 again.

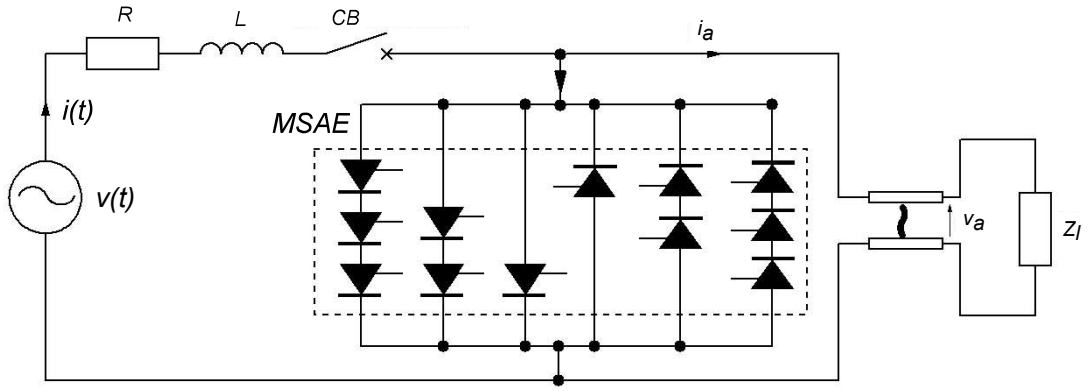


Figure 1.13 Multi-sectional arc-flash eliminator (MSAE) (Nowak et al., 2021).

with few considerations on the design of the elements[22]. When compared against other strategies, only arc quenching systems are capable of eliminating the NFPA 70E requirement for AF-rated PPE clothing, guaranteeing at the same time improved asset life and power system continuity. Moreover, as well as the consolidation of CB represented a huge improvement over fuses along the course of the last decades, the development of an AF quenching device that supports a high number of operations is a natural requirement in the field of AF elimination. Even though the development of a normally-closed, series-connected electronic switch capable of eliminating the arcing fault as fast as needed has not became feasible up to the present time, the same cannot be said about the development of a normally-open, shunt-connected electronic switch. This work presents a contribution in this direction.

1.2 Problem Statement

Recent proposition of a fast AF quenching device brought the possibility of an innovative solution to a severe problem that leads to injured and dead people besides huge profit reduction every day around the world. However, since the AF quenching device is a short-term operating equipment, the design and specification of its elements cannot be readily done based only on the information provided by their data sheets. Moreover, since this application demands high reliability - that is, the AF quenching device is a mission critical device that must operate properly whenever requested - the whole

[22]This and all the other arc quenching techniques do not rely necessarily upon detection by means of an AFR. Any diverse means can be used to generate the trip signal to the arc eliminator. In this sense, any advance in detection technology can be readily applied to the electronic AF eliminator.

study has to be done under this perspective. This is the question in which this work is inserted.

1.3 Motivation

The main motivation for this work is to fill the gap between the proposal of power thyristor application for the solution of arcing faults in industrial systems, which has been recently presented in the literature, and the current demand of the industry for electrical safety in the workplace. Traditional approaches are based on the solution of the effects of an arcing fault event, which are mostly thermal, instead of its causes, which are electrical. In this scenario, the calculation of the so-called IE, which is empirically done based on fitting of experimental data, is an indication that the industry lacks of a solution that is capable of eliminating the problem in its initial stage. Another evidence is the recent inclusion, in the *National Electrical Code* (NEC)[23] of articles 240.87 and 240.67, which intend to reduce the AF hazard by decreasing clearing time for circuits rated 1200 A or greater whether protected by CBs or fuses, respectively (Siemens, 2017). According to the article 240.87, additional protection methods must be included in the circuit, among which is an "energy-reducing active arc-flash mitigation system" (GE, 2017b; Katsiris and Scheuerman, 2018). In the article 240.67, additional protection is described for fusible switches 1200 A or larger where the fuse does not clear the available arcing current in 70 ms or less (GE, 2017b). The requirements are similar to those found in 240.87. The state-of-the-art in AF mitigation is the application of electromechanical apparatus like Thomson coil principle, which main limitation is the need of replacement after one or a few operations. Finally, the development of a new solution for AF elimination should be made under the strict condition that it is advantageous over those existing, both in technical and economic aspects.

1.4 Objectives

The main objective of this work is to provide an approach for the design of an electronic AF eliminator which serves initially for LV and can be extended to MV industrial and commercial power systems. In order to achieve this, the following specific objectives may be stated:

[23] NEC is the standard for the safe installation of electrical wiring and equipment in the United States (Association, 2020b).

- To present a state-of-the art scientific review in the field of arcing fault elimination, that serves as a solid basis for the work, especially in terms of guidance on the integration of the proposed solution to LV industrial power systems.

- To present and validate a computational time-domain model that allows the simulation of arcing faults in industrial power systems with the thyristor-based AF mitigation solution.

- To perform the evaluation of the solution effectiveness and investigate the design and / or specification of its components - power thyristors and reactors, both in computational and experimental environments. Regarding the thyristors, the objective is to assess the ride through capability of a given device when subjected to the current profile that circulates through it during the operation of the AF quenching device, so that it works in its safe limit without being overrated. Moreover, it is desired to know whether there is a device with lower size, weight and cost among a set of commercially available options with approximately the same electrical ratings.

- To realize and test a full-scale 480 V, 25 kA prototype, including a reliable electronic triggering and measurement hardware capable of providing the safe operation of the proposed AF quenching device.

The following points are out of the scope of this work:

- IE studies: Ralph-Lee's equations, *National Fire Protection Association* (NFPA) 70E-2021[24] (Association, 2021) or *Institute of Electrical and Electronics Engineers* (IEEE) Std 1584-2018[25] (IEEE, 2018). There are many references and computational tools already available for this purpose.

- High-voltage systems. This work is centered on LV levels, since it is where arcing faults cause more severe problem. MV systems up to 6.9 kV are included in the scope. The application of the proposed solution to higher voltage levels would demand series association of power semiconductor devices, which would deviate this work from its focus.

[24]First published in 1979, NFPA 70E - *Standard for Electrical Safety Requirements for Employee Workplaces* serves as the foundation for electrical safety practices in the United States (Lee et al., 2013). It identifies specific methods for working on or near live parts in industrial and commercial electrical systems (utilities are not included) (Sperl et al., 2009; Simms and Johnson, 2013).

[25]First published in 2002, IEEE Std 1584 - *Guide for Performing Arc-Flash Calculations* has become the predominant method in the industry for performing AF calculation studies.

- Peculiarities of specific topologies of industrial or commercial electric power systems. The bottom line for all the studies presented in this dissertation consider the simplest possible electrical equivalent for the entire upstream power system, i.e. a voltage source behind an impedance (Thévenin equivalent) and a protective device (CB).

- Investigation on failure mechanisms of thyristors. This work treats the avoidance of catastrophic failure, not accumulated damage and fatigue - which manifest themselves through measurable variables, for example leakage current. Existing references on this subject are considered, but it is not intended that this work results in more knowledge on this field.

1.5 Methodology

This research has primarily a scientific characteristic but, at the same time, a technical approach. In this sense, an extensive literature review is presented to give the proper support for the proposition of a suitable methodology.

Experimental results registered in the IEEE-NFPA Collaborative Research Project are used in this work to validate the applicability of an AF model reported in the literature that was primarily developed for free-air phenomena. The main advantage of this model is that its equations are based on a set of variables that have physical meaning, which is desirable since this work is focused on the electrical variables of the arc (essentially its conductance) - not the IE, which is often the variable that one desires to calculate.

A detailed evaluation on the electrothermal behavior of power thyristors under high amplitude, short duration (up to dozens of ms) current surges is presented, including both simulation (using MATLAB® and Microsoft® Excel) and experimental results. *Phase control thyristors* (PCT), *pulse power thyristors* (PPT) and *bi-directional control thyristors* (BCT) are taken into account. This investigation is solely based on data sheet information.

The discrete-time simulation models of some real records of LV arcing faults in switchgears, as well as the models of the elements of the quenching device (current-limiting reactors and power thyristors), are solved in MATLAB to evaluate the interation between them, and then they are implemented in *Electromagnetic Transients Program* (EMTP), using the ATPDraw™ graphical interface. The model has been developed so that the combination of any type (single-phase-to-ground, phase-to-phase, etc.)

of shunt arcing fault, any type of thyristor, and any supplying power system can be simulated provided that their parameters are properly inserted. Generic current sources have been added to incorporate the possible impact of other elements (motors, capacitor banks, distributed generation, etc.) to the effectiveness of the AF quenching device. The effect of neutral earthing is also evaluated. Sensitivity analysis technique is applied to evaluate the results, since a transient, nonlinear problem cannot be readily solved analytically by algebraic equations. The worst case is searched for by comparing the simulation results with each other.

The developed experimental setup, including the prototype as well as the bunch of tests performed to validate the aforementioned studies, are presented. The design of the power elements of the prototype has been done based on the results individually obtained during the studies of the power thyristors, of the arcing faults and also with the support of the complete computational simulation model in ATPDraw. Since the selection of the components of the quenching device is inherent to a given set of parameters of the power system, the design has been performed taking into account the Thévenin equivalent at the point of connection of the prototype in the laboratory. Tests have been done in two different voltage levels: 220/127 V and 440/254 V.

It is important to disclaim that in the beggining of this work reference IEC 60947-9-1:2019 (Commission, 2019) was not taken into account, which limits the maximum voltage drop across an arc quenching device to 34 V peak. At the time the reference has been released, the work presented in this dissertation was already in considerable advance. However, the aforementioned condition can be easily incorporated in the design phase. No modification is necessary since only a limiting value should be observed. Still, additional experiments have been executed to show that the requirement can be easily accomplished should the quenching device comply with the standard.

The tests consisted of arcing faults provoked in the busbar of the prototype, according to described in *International Electrotechnical Commission* (IEC) TR 61641:2014 (Commission, 2014) and IEEE Std C37.20.7-2017 (IEE, 2018). A thin copper wire is inserted into the switchgear at previously selected ignition points. Once the busbar is energized, an arcing fault starts right after the sublimation of the wire, triggering the AFR, that signals a trip condition simultaneously to the upstream CB and to the electronic system embedded into the quenching device, which fires the thyristors.

1.6 Contributions

The main contribution of this dissertation is the proposition and validation of means for the evaluation of the operation of power thyristors out of the standard conditions presented by the manufacturer in their data sheets. It consists of the prediction of the catastrophic failure limit for a given model of power thyristor subjected to a given industrial frequency ac current surge profile. It allows the application of the device up to its limiting capability, resulting in a optimized specification. Philosophically, it is a new sight on the specification of power thyristors, extensible to other bipolar power devices, for example diodes, subjected to short-term, high current profiles that include dc level, which is the case of the AF quenching device, but also of other applications like in bypass switches of series power converters undergoing a short-circuit at the load side, for example.

Moreover, this work presents the development of an original proposition, based on the recursive convolution method, that allows the discrete-time domain calculation of the virtual junction temperature rise of the device. This has created a clear way to the incorporation of the power thyristor terminal behavior into a computational simulation, in a unified platform, allowing the analysis the interaction between the electronic quenching device, the arcing fault and the power system. This is a valuable contribution since the power thyristor is the key element of the device. A minor contribution on the discrete-time modeling of internal arcing faults is also provided.

The aforementioned contributions were imperative for the achievement of the specification of the shunt impedances and the thyristors for the AF quenching device, which by their turn supported the design, building and testing of a full-scale prototype. Exhaustive experimental investigation has been done to prove the effectiveness of the equipment.

1.7 Structure of the Dissertation

The text is composed by four chapters in addition to this introductory one. Chapter 2 is focused on the electronic AF quenching device: mathematical models of arc conductance, power thyristor and power system are presented. In Chapter 3, a complete computational model that allows the evaluation of system behavior is developed. Finally, Chapter 4 presents and discusses the results, both simulation and experimental, and Chapter 5 reinforces the main conclusions and states continuity proposals for future opportunities.

Chapter 2

System Analysis

"Keep It Simple Stupid."
Kelly Johnson (1910*-1990†), Aircraft Engineer - Lockheed Skunk Works

A detailed discussion as well as an analytical evaluation is necessary before any modelling or simulation / experimental validation of the thyristor-based AF quenching device can be properly made. Such analysis is presented in this chapter. To do so, the behavior of each part of the system must be understood before it can be mathematically modelled, which is necessary for an holistic analysis and proper design of the elements of the quenching device. Therefore, taking into account Figure 1.12, the system can be divided essentially into the power circuit, the arcing fault and electronic AF quenching device itself, both at system level and component level.

In this work, it is expected that the power elements of the electronic AF quenching device are designed so that the elimination of the fault is guaranteed still preserving the equipment. Therefore, the conditions for the design must be properly defined, considering both technical and technological aspects and possible associated constraints and limitations. In this sense, the essential questions listed below have to be answered:

1. *What are the effects of operation of the quenching device on the energy delivery power circuit and are there negative unintended consequences?* Main items to be considered:

   (a) Electrodynamic forces on busbars.

   (b) Suportability of the upstream CBs.

2. *What is the maximum voltage drop across the AF quenching device that is still low enough to extinguish the arcing fault?* Points to be examined:

   (a) Voltage drop across a thyristor when submitted to a high-amplitude, industrial-frequency current surge profile.

   (b) The maximum magnitude of the shunt impedance and what should be its phase angle.

3. *How to guarantee that the electronic switch will not be damaged?* This has to do with the fact that the thyristors will be operating at a condition that differs a lot from those declared in the manufacturer's data sheets and how to take advantage of the presented information.

4. *What are the possible failure modes and do they have any impact on the safety / reliability of the protection?* The main aspects to evaluate regarding this topic have to do simultaneously with keeping personal safety and asset life but at the same time the operational continuity of the power system. This concern is applicable both for the power semiconductor devices and the associated snubbers.

Additionally, any normative constraint must be properly taken into account before working on the aforementioned points. Besides all of these questions, this chapter paves the way to the mathematical / computational model that best suits the investigation that will be carried in this work.

2.1 Power System

An electrical power system is often composed of a wide range of equipment, including distributed generation, power quality dedicated equipment, nonlinear loads and other, which often have dynamic behavior that changes over time[1]. This intrinsic complexity makes it reasonably complex and subjected to failures, besides making it difficult to consider all the variables in a study that is not centered on the power system itself. In general, the LV section of a distribution scheme (Figure 2.1) is powered by an upstream feeder to supply small LV motors and other static loads through a step-down transformer (T4), 0.48 kV metal enclosed switchgear (LV SWGR), and

[1]The topology of the power system and the type of the protective device of a specific bus is extremely variable among different facilities (due to operational risk management strategies, required reliability, etc.) and even among different plants inside the same place due to specific and technological advances in electrical devices and standards (for example: automatic reclosing and circuit breaker failure). Therefore, the worst case scenario must be particularly evaluated.

0.48 kV MCC (LV MCC 1) (Lee et al., 2013; El-Mahayni et al., 2017). The available short-circuit current is determined mainly from the impedance of T4. For typical LV electrical systems, the nominal current normally does not exceed 4 kA, and the related maximum short-circuit current is generally kept below 80 kA[2] (Hazel et al., 2017). For multiple-section bus arrangements, the fault current nearly double when both sections are in service and the tie breaker is closed (LV SWGR TIE in Figure 2.1), assuming the transformer impedance is large compared to the upstream source impedance - which is often the case (Rifaat et al., 2007).

The analysis of the power system should be made according to the specific type of study that is of interest, preferably using the simplest model that is still suitable for the required computational simulations. In a LV section with insulated cables, for example, the configuration of the cables is not uniform over their entire length, besides being subjected to modification during maintenance service. There are industry applications in which equipment are occasionally moved, which turns the parametrization of the model even more complicated (Kumpulainen et al., 2014; Nelson et al., 2014; Durocher, 2015). Besides the uncertainties on the parameters, incorrect assumptions contribute also to inexact results. Hence, to improve the accuracy of fault current calculations, the system studies have to be as detailed as possible (Nepveux, 2007).

On the other hand, AF voltage comprises elevated odd harmonics, but they are of low-order (often negligible beyond the 13^{th}) (Gammon and Matthews, 2001). Therefore, it is not necessary to adopt high-frequency models for the elements of the system. Moreover, the operation of the AF quenching device leads to purely 60 Hz voltages and currents (including dc levels) in the system. Litovski et al. in (Litovski et al., 2017) adopts a simple RL equivalent for a study of arcing faults taking place in isolated cables. The same approach will be adopted in this work. The capacitance of the switchgear busbar can be neglected[3] since it produce insignificant effects in the results at the frequency range of the arcing fault. Moreover, the AF quenching device proposed in this work includes an inductive turn-on as well as a capacitive turn-off snubber for the thyristors, as will be demonstrated later in this dissertation. They are concentrated elements that dominate the distributed parasitic inductances and capacitances of the switchgear. Moreover, both snubbers have damping resistances that contribute positively to the elimination of any resonance that could lead to arc-flash reignition.

[2]There are isolated power plants with embedded power generation systems (oil platforms, for example), which have exotic characteristics like short-circuit currents in the order of 100 kA.

[3]Its value ranges from 1 to 3 pF/ft for a bus gap in the range of 2 to 12 in (Greenwood and Selzer, 1971; Bonatto, 2001). 1 ft $\approx$ 30 cm.

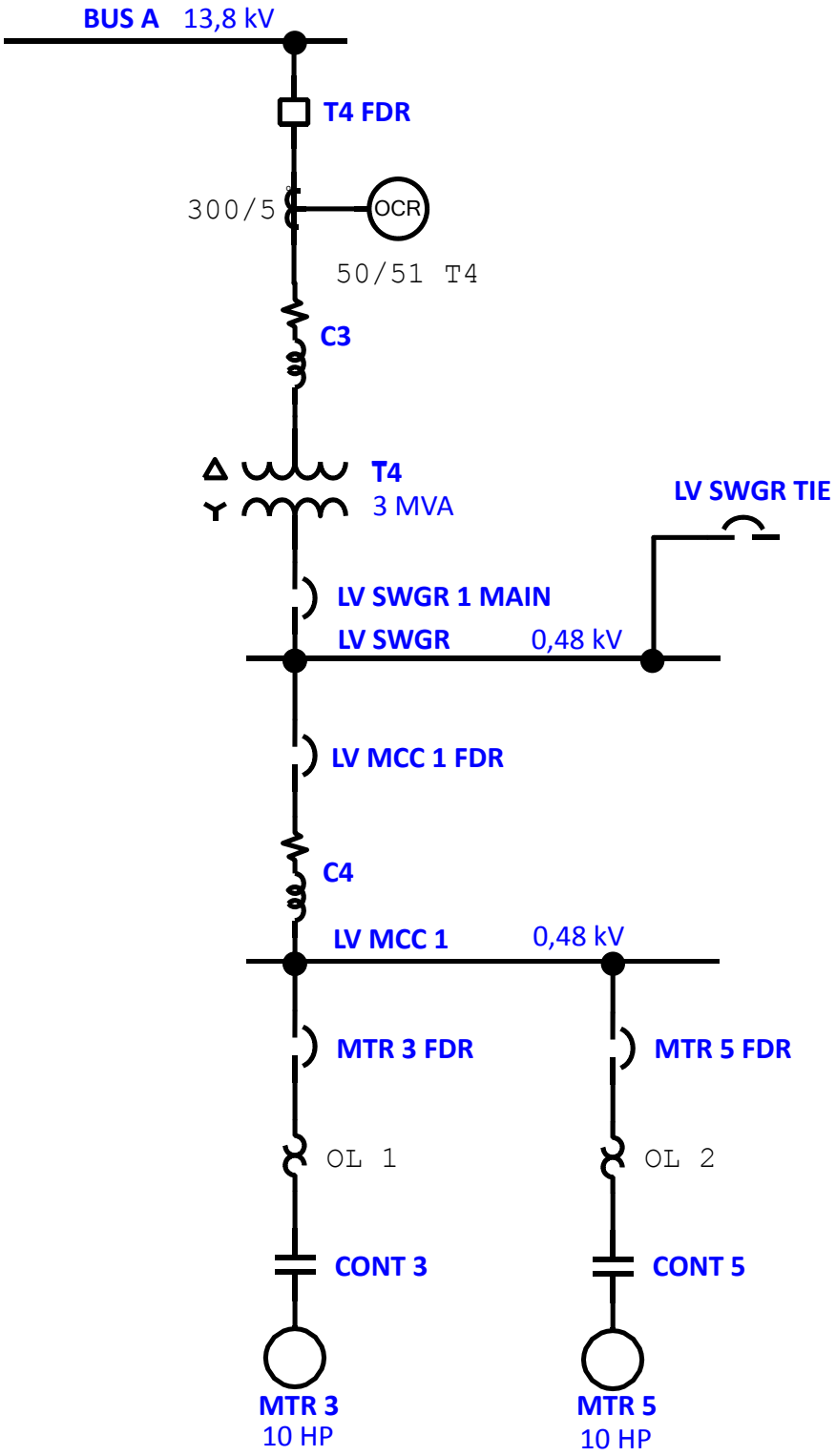


Figure 2.1 Typical industrial power distribution scheme - LV section.

2.1.1 Neutral Grounding

A grounding resistor R_N forms a RLC circuit with equivalent series resistance and inductance and the shunt capacitance of the power system. To avoid resonance and possible consequent overvoltages and restriking ground faults, the resistance R_N must be calculated according to (2.1), where I_{scp} is the stray capacitance current and V_{LN} is the line-to-neutral voltage (Das, 2012):

$$R_N = \frac{V_{LN}}{3 \cdot I_{scp}}. \tag{2.1}$$

Besides this, (2.2) and (2.3) must be satisfied simultaneously by a system in order to be considered effectively grounded (Das, 2012; IEE, 2017). Reactances X_0 and X_1 are the zero- and the positive-sequence, respectively, and R_0 is the zero-sequence resistance calculated by the Fortescue transformation.

$$0 < \frac{X_0}{X_1} < 3; \tag{2.2}$$

$$\frac{R_0}{X_0} < 1; \tag{2.3}$$

$$0 < \frac{R_0}{X_1} < 1. \tag{2.4}$$

2.1.2 Motor Contribution to Fault Current

When a fault occurs at the bus with induction motors, the rotating magnetic field in the rotor will attempt to support the reduced voltage condition by acting as a power source. The motor now provides additional current into the faulted electrical system. Its ac amplitude depends on the impedance of the motor, its mechanical frequency is initially different from the system frequency because of motor slip, and the dc component rate of decay is dependent on the motor and load inertia and electrical system X/R ratio (Broussard, 2013). Typically, the effect of short-circuit current from induction machines can be ignored in a couple of cycles depending upon the rating of the motor. For small motors less than 100 hp, this decay may be one to two cycles, and even for very large motors, it rarely exceeds seven to eight cycles (de Metz-Noblat et al., 2005; Tinsley et al., 2007; Dixon et al., 2014; Siemens, 2016).

In short-circuit calculations, the worst case arcing fault for a bus could be obtained with motor fully running or turned off (Ayoub and Valdes, 2015; Fox, 2015). The motor short-circuit current contribution will have a degree of asymmetry similar to that of

the locked-rotor current, which is customarily assumed to be a factor ranging from 1.60 to 1.76 (Fox, 2016). The IEEE Std C37.010 (IEEE, 2017) offers guidance when calculating motor contribution for a group of motors if detailed data is not available. Assuming a motor contribution of four times rated full load current is acceptable. For large motors or groups of large motors, lock rotor current, typically five to seven times full load current, is used instead of the motor (Broussard, 2013).

2.1.3 Switchgear Configuration

Typical switchgear of medium-size industrial building is fed at 480/277 V level[4], with equivalent upstream impedance around 6.5 mΩ at the main LV bus of the panel and $X/R \approx 9.3$. These values lead to a three-phase symmetrical RMS short-circuit current in the order of 42 kA. The gap width of the panel busbar is about 3" (≈ 76 mm). At the panel feeder, the gap width is roughly 2" (≈ 51 mm). The equivalent impedance increases to 21 mΩ and the X/R ratio decreases to approximately 0.81. The short-circuit current also reduces to a level of 13 kA (Gammon and Matthews, 2001). The IEEE Std 1584-2018 (IEEE, 2018) adopts default bus gaps of 32 mm for LV switchgears and 25 mm for LV MCCs and panelboards.

Typical bus arrangements are in a flat horizontal or vertical configurations. The impedance of the arcing fault is not expected to be balanced, being higher between the two phases that are more distant from each other (Nelson et al., 2014).

2.2 Arc Conductance

In addition to the issues described above, which are inherent to any power system, there is a concern related to the AF model, which consists of a nonlinear conductance that depends on many parameters of the SWGR or the MCC (Ventruella, 2019).

Bolted fault studies are the first to be taken into account when a power system is being analyzed, despite the fact that arcing fault is the type that occurs the most (D'Mello et al., 2013). In fact, arcing fault analysis is much harder to be accomplished than bolted fault, especially due to the fact that the modeling has proven to be very difficult. Moreover, the probability of two identical arcing faults in the real world is a physical impossibility because of the random nature of the arcing in a plasma cloud (Nelson et al., 2014). The plasma cloud is started when there is a flashover in a gap between energized conductors with sufficient potential difference or between

[4]In Brazil, 440/254 V and 380/220 V are also common.

one energized conductor and earth potential (Faried et al., 2017; IEEE, 2018). The insulation medium - normally air - becomes ionized, which constitutes a low - but substantially higher than solid material - impedance path that is superheated by the passage of current (Das, 2012; ABB, 2017).

Voltage drop in an arc in open air is of the order of 5-10 V/cm (Das, 2012; ABB, 2017). Longer arcs result in larger voltage drop, leading to not only lower arcing current but also directly impacting the ability of the arc to self-sustain. Three-phase arcing is more likely to sustain because multiple arcs coexistence and higher voltages (480 V vs. 277 V). With multiple arcs, when one arc extinguishes temporarily at a voltage zero, there are still adjacent arcs generating heat and ionized gas (Crnko and Dyrnes, 2001; Eblen and Short, 2017).

On LV systems with appropriate bus spacing, the arc voltage has been estimated in the range of[5] 140–150 V. Therefore, for LV, the arc length consumes a substantial portion of the available voltage (Das, 2012; ABB, 2017), resulting in a fault current substantially lower than bolted fault current (Fox, 2015). For MV systems, arcing voltage is practically an insignificant portion of the available voltage, and arcing fault current is considered equal to the bolted fault current (Tinsley et al., 2007).

The arcing path can be modeled as a resistance with a nonlinear time-varying component (Saleh et al., 2015), which represents a fast, irregular change in arcing geometry due to convection, plasma jet, electromagnetic forces, among other effects like transient recovery voltage between conductors of a busbar (Queiroz, 2011). Since the current path is resistive in nature, unity power factor is yelded. Arc resistance remains the same when the system voltage varies between 208 V and 600 V, given a busbar configuration and bolted fault current (IEEE, 2018).

Since the exact values for an arc resistance cannot be given (Kay et al., 2011), resultant current level cannot either. Moreover, arc fault current is not a pure sine wave at the fundamental frequency, because the arc resistance is not constant (Abboud et al., 2016). Arcs for ground fault can be sustained even at low values of ground fault currents of the order of 800 A, which may not be any more than the load current

[5]With an arc voltage of approximately 150 V, it is obvious that an arc cannot be maintained on a 120 V system since the driving voltage of an arcing fault needs to be in excess of approximately 150 V. This explains why an arcing fault on a 208/120 V (220/127 V in Brazil) system tends to self-extinguish, being rarely experienced (IEEE, 2001; Loucks, 2013; Nelson et al., 2014). Arc-flash events are generally limited to systems where the bus voltage exceed 240 V (Durocher, 2015; Zhang et al., 2015; Liang et al., 2016). More than 90% of LV burn-related injuries and fatalities correspond to 480 V power systems (Nelson et al., 2014).

(Das, 2012). At 600 V, arcing current can be as small as 50% of bolted-fault current, reaching levels even as lower as 30% at lower voltages[6] (Nelson et al., 2014).

Current and Voltage Waveforms

An arc discharge behaves like a variable resistor, having the voltage–current characteristic of the magnetic hysteresis shape. This means that, for the same current value, the arc voltage is higher when the current is increasing compared with the case when the current is decreasing. This is due to the increase of the temperature of the arc (higher stored energy), which increases its conductivity. Hence, the arc resistance becomes smaller. A decay of the electric arc conductivity near the zero current is an important parameter impacting the interruption and reignition of the arc. The current interruption takes place near the zero current because at this point the ions and electrons available for conduction in the arc column are also at minimum and the temperature is decreased due to the loss of energy (Marszalek and Trzaska, 2017).

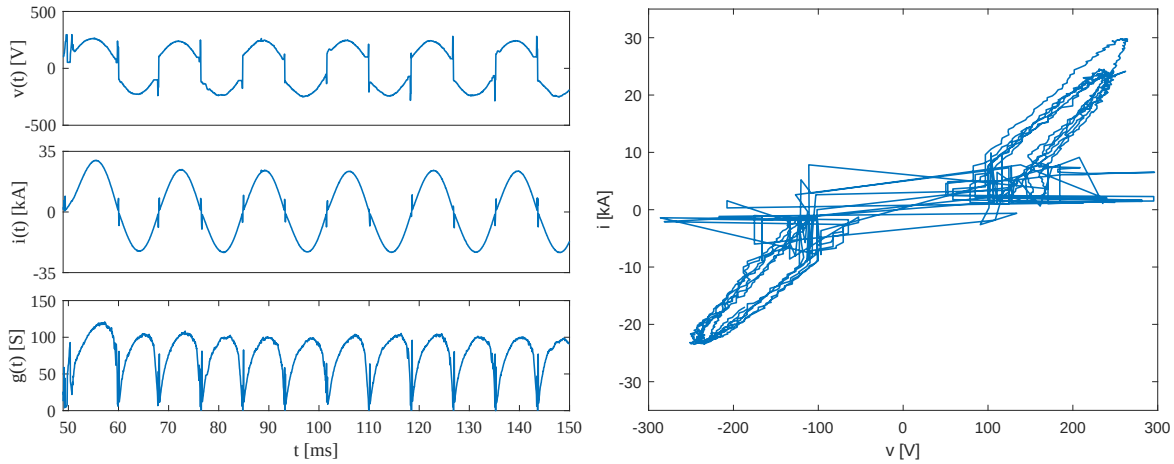
The arcing current is discontinuous and its variation rate depends on the inductances of the system where it is occurring. The current increases and decreases gradually due to the stored inductive energy in the circuit. Moreover, the discontinuity causes the equivalent RMS value to be depressed in comparison with a pure sinusoidal waveform (Dunki-Jacobs, 1986; Parise et al., 2013).

Figure 2.2a presents the waveforms of voltage and current captured during a real arcing fault test performed on a 25 mm gap fed by a 480 V system. Notice how the voltage has a nonlinear behavior due to the time-variable conductance, which manifests itself as a change on the voltage vs. current locus represented in Figure 2.2b.

Conductance

There are arc models that provide a physical investigation of the phenomena, which is not among the objectives of this dissertation, and black box models, which describe only the external relation between current and voltage, being suitable for the study of the interaction between the arc and the electrical system during the fault (Darwish and Elkalashy, 2005; Andrea et al., 2010; Yuan et al., 2013). These macroscopical models will be adopted in this work, as far as investigation of the quenching device performance in an industrial / commercial power system is concerned, i.e., arcs between electrical conductors. The basis of black box models is the energy balance between

[6]For 480/277 V systems, typical factors were derived for arcing fault current value in relation to the bolted-fault value: 0.89 (three-phase), 0.74 (phase-to-phase) and 0.38 (phase-to-ground) (Dunki-Jacobs, 1986; IEEE, 1994).



(a) Instantaneous voltage and current (measured) and conductance (calculated).

(b) Current vs. voltage locus.

Figure 2.2 Arcing fault waveforms.

heat production inside the arc and heat losses to the surroundings. Black box models depend on fitting experimental results, which is not an easy task (Andrea et al., 2015).

Between the simplest LV arc-flash models available in the literature, rectangular voltage waveform across the path (Mattews model) and empirically derived current-dependent instantaneous arc voltage (Stokes and Oppenlander model[7] and Fisher model) are the most known[8]. Although the arc voltages have been shown to be flat-topped[9], a larger voltage transient is sometimes visible at the moment of zero-crossing (Gammon and Matthews, 2001). Other models, including the most traditional like Cassie's, Mayr's and their variations (for example, the hybrid model), were originally developed for studying how the arc extinguishes in high-voltage CBs[10] (Idarraga Ospina et al., 2008; Yuan et al., 2013; Katare et al., 2017). In the course of time, these models have been adapted for other applications, for example welding (currents of hundreds of ampere) (King-Jet Tseng et al., 1997; Sawicki et al., 2011) and electric arc furnaces (currents in the order of kiloampere) (Mokhtari and Hejri, 2002; Teklić et al., 2017), where differently from CBs, it is desired that the arcing path is ignited and kept active. Many of these models are not ready for simulation as a circuit element. Additionally,

[7]Originally developed for electric arcs in open air (Ammerman and Sen, 2007).

[8]There are other less known models reported in the literature, like Paukert's, Wilkins' and Hickery's.

[9]The restrike voltage is assumed to be 375 V and the flat-topped arc voltage is assumed to be 140 V. Voltages less than about 350 V are not capable of initiating arcs at room temperature and atmospheric pressure (Gammon and Matthews, 2001).

[10]Which does not apply in this work, since here we do not try to force the interruption of the arc. There is no transient recovery voltage, no extinction chamber or moving mechanical parts. Instead, the arc-flash quenching device creates an alternative path that deviates the current from the fault.

each one of these models has its own particularities, some of them with a lot of parameters, which makes the tuning process difficult (Khakpour et al., 2016), besides having variables without any physical meaning. For these models, many techniques have been already proposed for parameter estimation, like trial and error, genetic algorithms (Pessoa et al., 2021), multiobjective optimization (Illahi et al., 2018) and even filming the arc (Khakpour et al., 2017). Moreover, some of these models are not capable of representing both the ignition and the extintion of an arcing fault.

2.2.1 Kizilcay's Arcing Fault Model

On the other hand, the model presented by references (Kizilcay and Pniok, 1991; Kizilcay and Seta, 2005; Kizilcay and Koch, 2007) was specifically developed for the study of free-air arcing faults, as well as for integration in computational simulation as an electrical circuit element. This is the model mostly used for arcing fault studies in bulk-power systems, being widely applied to arcing fault analysis (Yin and Ding, 2016). Besides, it has good representation of the arc properties (Idarraga Ospina et al., 2008). It is based on the energy balance of arc column:

$$\frac{dg(t)}{dt} = \frac{1}{\tau} \cdot [G(t) - g(t)], \tag{2.5}$$

where t is the time, g is the time-varying arc conductance[11], τ is the time constant, and G is the stationary arc conductance given by:

$$G(t) = \frac{|i(t)|}{(V_O + R_O \cdot |i(t)|) \cdot \ell(t)}, \tag{2.6}$$

where i is the instantaneous arc current, V_O is a constant voltage per arc length, R_O is a resistive component per arc length, and ℓ is the time-dependent arc length[12].

Although this model has been developed for arcs in high voltage overhead lines (Katare et al., 2017; Litovski et al., 2017), circuit simulations will be presented later in this work to evaluate its suitability for LV arcing faults in SWGRs and MCCs. The arcing voltage does not depend on the power system voltage, but only on the physical characteristics of the fault. In addition, the time-dependency of the arcing path length is significant only if it is long as is characteristically observed in overhead

[11] Convergence problems are frequently encountered whenever the value of resistance of any circuit element tends to a very small value during any of the iterations. Therefore, the arc conductance is used instead of its resistance (King-Jet Tseng et al., 1997).

[12] Both the arc length and the arc resistance increase with the gap width. A larger distance requires a large arc voltage and arc resistance to sustain the fault (Gammon and Matthews, 2001; Nelson et al., 2014).

power distribution networks. Therefore, the arc length can be considered constant and equal to the distance between the busbar conductors of the switchgear. Another reason that supports this assumption is the duration of the fault, which is mitigated to a few milliseconds due to the fast operation of the quenching device. Furthermore, there is actually no arcing fault current interruption, but rather deviation to a more conductive electrical path.

Determination of the Parameters

The determination of the arc parameters is based on the computation of the time-varying arc conductance using the measured arc voltage v and current i:

$$g(t) = \frac{i(t)}{v(t)}. \tag{2.7}$$

The procedure can be divided into two steps. First, V_O and R_O can be determined using (2.5) and (2.6) at generic time points t_q and t_w where $dg/dt = 0$, so $g = G$. A two-equation, two-variable (V_O and R_O) linear system is obtained. The second step is the computation of the time constant τ, which is conducted by inserting (2.6) and (2.7) into (2.5) and integrating the result from t_q to t_w:

$$\tau = ln\left(\frac{g(t_w)}{g(t_q)}\right) \cdot \left[\int_{t_q}^{t_w} \frac{|v(t)|}{(V_O + R_O \cdot |i(t)|) \cdot \ell}\, dt - (t_w - t_q)\right]. \tag{2.8}$$

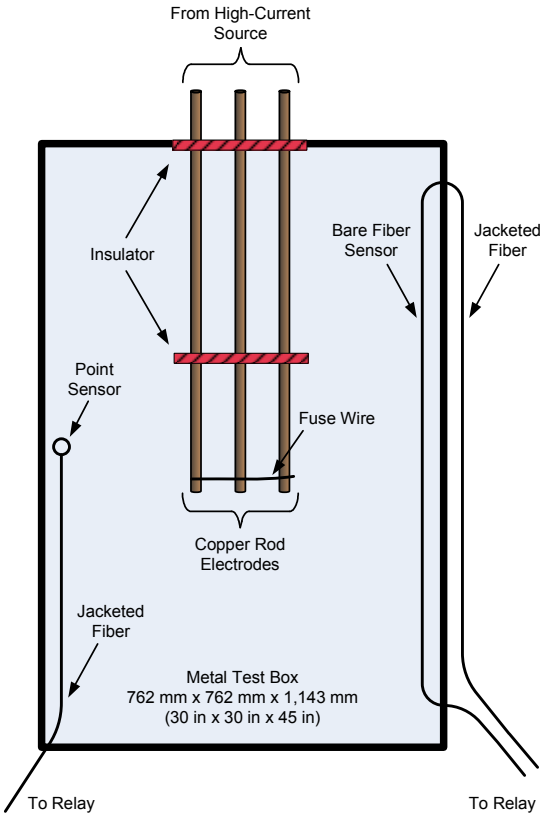
The values of V_O, R_O, and ℓ determine the voltage at which the arc is extinguished. Increasing values of τ produce increasing overvoltage in the arcing voltage during zero crossing (King-Jet Tseng et al., 1997).

2.2.2 Arc-Flash Tests by the IEEE-NFPA Project

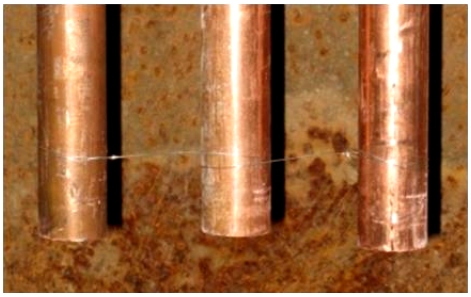
The updated equations for IE calculation documented in the IEEE Std 1584-2018 guide was developed from testing organized by the IEEE-NFPA Collaborative Arc-Flash Research Project (IEEE, 2018). All tests were conducted at high power laboratories for the purpose of developing an understanding of the electrical characteristics of AFs. Such test results are stored in the IEEE DataPort tool (Association and Association, 2019) and can be used to verify physical model-based equations.

Figure 2.3 illustrates the test setup typically used for this kind of test. A total of 932 experiments with voltages ranging from 208 V to 600 V have been performed, including single- and three-phase trials. Arcs were initiated by applying bolted fault current through a solid 20 AWG copper wire that is connected between the ends of

the electrodes. In this dissertation, 4 of these test results will be considered. Their main parameters[13] are detailed in Table 2.1. All of them are single-phase and have open-circuit voltage equal to 480 V. Arcing voltage and current have been registered for each test using a sample time of 50 μs. The waveforms previously shown in Figure 2.2 are relative to test #67.



(a) AF test box.



(b) Bare copper fuse wire.

Figure 2.3 Typical AF test setup (Hughes et al., 2011).

2.3 The Electronic Arc-Flash Quenching Device

The electronic AF quenching device[14] studied in this work is composed basically of two components: current-limiting shunt impedances and power thyristors. This section provides a preliminary analysis on the behavior of these two components during the operation of the quenching device, so that well founded guidelines can be properly given in Chapter 3 for the design of these elements.

[13] The tests have been named here exactly as they appear in the data set.
[14] See Figure 1.12 again.

Table 2.1 Basic parameters of selected single-phase arcing-fault tests

Parameter	***Test***			
	#67	**#68**	**#65**	**#63**
Available symmetrical current [kA]	21.7		5.03	
Power factor	0.075		0.034	
Bus gap [mm]	25	10	25	10
Peak current [kA]	27.3	29.8	9.69	10.8

2.3.1 Shunt Impedance

Once the proposed solution is shunt-connected, it is natural to think of a current-limiting impedance included in the same branch of the fast switch (Z_{Sk}). Higher shunt impedance reduces the current that circulates through the quenching device branches due to the operation of the thyristors. This way, the thyristors are subjected to a lower peak current, leading to the specification of low-rated, low-priced, lower size and smaller weight power semiconductor devices. Besides, the impedance reduces the short-circuit current produced by operation of the switches of the AF quenching device, which in turn leads to less thermal and mechanical stresses to the switchgear. On the other hand, higher shunt impedance leads to higher busbar voltage, which should not exceed a limiting value below which the arcing fault is safely extinguished. Therefore, there is a compromise to be accomplished.

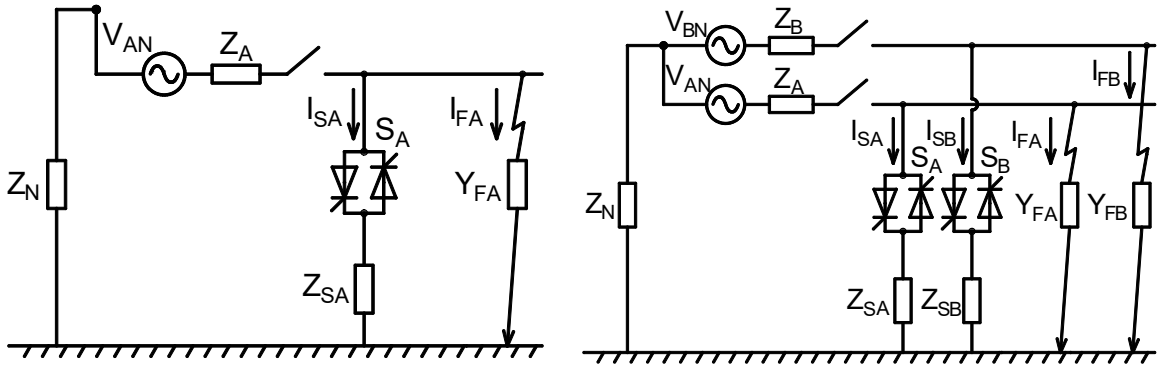
Moreover, the shunt impedance adds one more element to the AF quenching device, which could compromise its fail-safe characteristic, specially in case of passive parts like reactors or resistors, which usually fail as an open-circuit. Since it is a protective device that must guarantee a reliable operative condition for people working on energized equipment, new components represent additional spots of design, assembly, and burn-down failures, then care must be taken in this sense.

Finally, the most suitable characteristic (resistive or reactive) for this impedance should be evaluated. Together with the positioning of the quenching device in the busbar and the operation strategy of the three switches, this attribute has a direct impact on the effectiveness of the equipment as will be discussed below.

Location and Operation of the Quenching Device

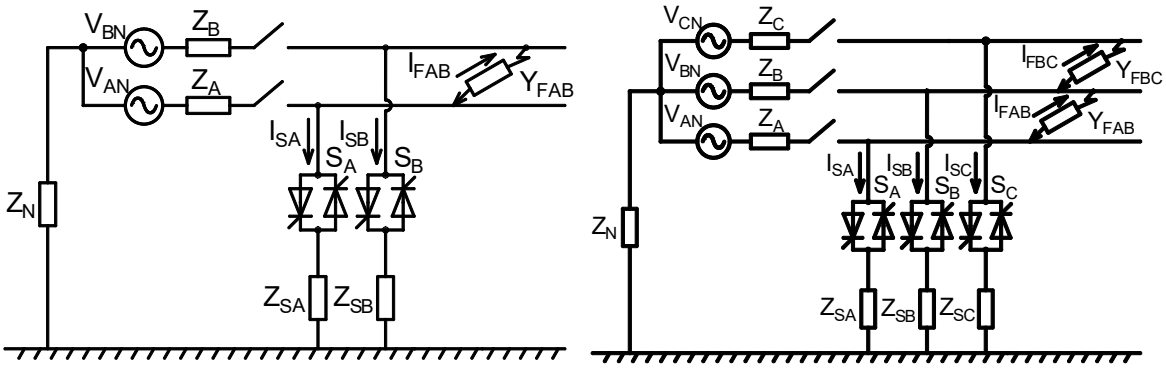
Figure 2.4 presents the operation of the AF quenching device for phase A-to-ground and AB-to-ground arcing faults. In both cases, the operation of a switch S_C connected between phase C and ground would not be necessary. For three-phase-to-ground faults,

though, the operation of switch S_C is imperative. Figure 2.5 shows phase-to-phase cases. Figure 2.4b could be also modeled as a combination of the cases presented in figures 2.4a and 2.5a.



(a) Single-phase-to-ground. (b) Double-phase-to-ground.

Figure 2.4 Elimination of different types of arcing faults.



(a) Phase-to-phase. (b) Three-phase.

Figure 2.5 Phase-to-phase arcing fault elimination.

The operation of the specific switches necessary to eliminate the arcing fault would increase the protective system complexity and lead to the deterioration of its main characteristic, which is fast speed of fault elimination. Safety would be compromised as well since the identification of the affected phase(s) before turning on the ac switches would be necessary. Moreover, single-phase operation of the quenching device can lead to increased phase-to-ground voltages on the unaffected phases of non-effectively grounded systems, which in turn results in stress to the components and equipment. Additionally, it can be demonstrated by the symmetrical component method that a bolted fault in a solidly-grounded neutral system has respectively 173% and 150% higher amplitude for phase-to-phase-to-ground and phase-to-ground faults relatively

to a three-phase fault (including ground or not)[15] (Grainger and Stevenson, 1994). Finally, the strict operation of the involved phases would incur in a scenario where the elimination of an arcing fault between phases is critical, since in this case there are two impedances (Z_{SA} and Z_{SB} in Figure 2.5a) across the arcing path.

Therefore, three-phase-to-ground operation guarantees AF elimination for all of the possibilities without leading to additional tasks, besides resulting in balanced three-phase currents[16] and increased safety. It is adopted in this work.

The position of the quenching device on the busbar is also a critical factor. Figure 2.6 shows two possible series arcing faults which could result from main breaker rack out (phase C fault, Y_{F1}) or from a loose load cable (phase A fault, Y_{F2}), for example. In the first case, three-phase operation of the quenching device does not quench the arcing path, but can result in a worse scenario where the arcing path current is increased and so does the IE. In the second case, the path formed by switches S_A and S_B quenches the fault[17]. Then, it is recommended that the quenching device is installed as close as possible to the main breaker in order to reduce the length of the path in which an arcing fault would not be eliminated, but the lack of effectiveness for main breaker rack out must be solved through the correct equipment handling.

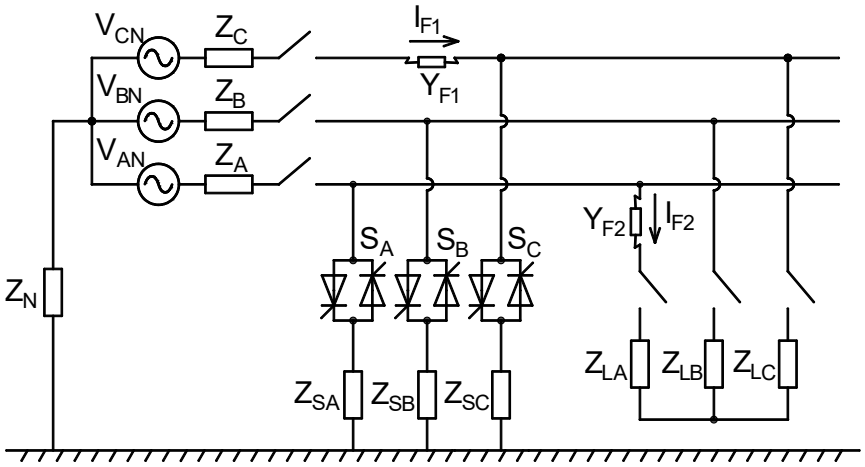


Figure 2.6 Series arcing fault quenching device.

Any impedance between Y_{F2} and Z_{Sk} may have an impact on quenching device effectiveness as well. This is because as the inductance between the arc and the

[15] Only a phase-to-phase fault would result in a lower current amplitude (87%), but it is impossible with the topology considered in this work since the three phases are connected simultaneously to the ground potential.

[16] At least if it reaches the steady-state, which is more likely to happen for slow CBs and power systems with small X/R ratios.

[17] Considering that the feeder CB is closed.

quenching device becomes large, high current increasing rate di_T/dt over it can generate high reverse voltage (Zhang et al., 2015), increasing fault current commutation time (Das, 2012). In other words, the time to reduce arcing voltage to a safe value is influenced by the position of the device with respect to the supply side, and the parallel impedance introduced by the new circuit when it closes (Gemme et al., 2008). This suggests that the quenching device should be integrated to the busbar that is meant to be protected, resulting in minimum transfer circuit inductance. A positive side effect of this is that the equivalent impedance of the upstream power system is also reduced, making it possible to decrease the value of the impedances Z_{Sk} of the electronic AF quenching device. Notice that each branch impedance of the quenching device (Z_{Sk}) forms a voltage divider with its respective equivalent phase impedance (Z_k).

Another relevant consideration for the design of the shunt impedances of the AF quenching device is that the power system equivalent impedance can change over the time. In power system harmonic studies, for example, this variation is generally considered by defining a wide zone over the R-X plane so that the possible expected effects can be taken into account (Arrillaga and Watson, 2003). Such consideration is very important for the AF quenching device, both if the power system impedance reduces, which could make the device ineffective, or increases, which would enable that the impedance of the device is increased if desired.

Constraints

There are specific standards regarding the construction and operation of AF quenching devices:

- UL 2748-2017 (Standards, 2016) defines performance tests including maximum current withstand, internal arcing faults and arc transfer.
- IEC 60947-9-1:2019 (Commission, 2019) defines that the peak voltage drop across an arc quenching device is up to 34 V.
- IEC TR 61641:2014 (Commission, 2014) defines test procedures for a switchgear under internal arcing fault, stating that, for a 440 V switchgear fed by a power system with RMS symmetrical three-phase bolted short-circuit current between 20 kA and 50 kA, the power factor[18] of the upstream impedance must be 0.25, which leads to an asymmetry factor of 2.1. It means that a switchgear rated for 25 kA would be subjected to a peak current I_{pk} of:

[18] Actually, the report references IEC 61439-1 (Commission, 2020), which is the standard that in fact brings these values.

$$I_{pk} = 25 \cdot \sqrt{2} \cdot 2.1 = 74.2\ kA \tag{2.9}$$

during a bolted fault. Moreover, the voltage applied to the switchgear is 5% higher than its nominal value.

Since the AF quenching device does not produce a bolted connection between phases and ground, then bolted fault current level will not be reached. The higher is the value of the shunt impedance, the lower is the current. However, these three references include additional constraints to the design of the shunt impedances, and what they have in common is that all point out to the reduction of the impedance value, leading to higher electrodynamic effects to the AF quenching device and to the switchgear busbar as well.

Characteristic of the Impedance

As an initial guideline, it has been suggested that quenching device current should be limited between the values of bolted and arcing short-circuit (Conceição, 2015). According to Krause et al. (Krause et al., 2012), an alternative impedance only 5% lower than the arcing path resistance is sufficient to extinguish the arc.

Due to the resistive nature of the arcing fault path and the intent of commuting the current from the fault to the quenching device branch without any time delay, the first proposition would be that the nature of the shunt impedance is chosen to be resistive. Another reason why resistive would be more suitable is to avoid resonance with stray busbar capacitance[19]. On the other hand, a resistive element would lead to power dissipation and heating, and consequently reduced reliability due to the possibility of an eventual burn. Moreover, stray inductance is not negligible especially if the resistor is wire wound, which is typically true for power resistors. Finally, the thyristors already include a resistive portion into the quenching device branches, as will be detailed in Subsection 2.3.2.

Nonetheless, thyristors have an intrinsic limitation regarding the rate of rise of the current during the turn on process. In general this information is explicit in the manufacturer's data sheet as the *critical rate of rise of on-state current* (di/dt_{cr}), which requires that a minimal inductance is connected in series with the semiconductor so that this threshold is not transcended. This is normally called the "turn-on snubber". The busbar of a switchgear have a stray inductance, but its value is in the order of 0.1

[19]This is why transformer grounding impedance Z_N, which is effective to reduce phase-to-ground fault currents, is resistive.

to 0.2 μH/ft (Greenwood and Selzer, 1971), which is generally not enough[20] to fulfill the role of a snubber, specially if the quenching device is to be compact as previously shown in Figure 1.9. Conversely, the main drawback of inserting a reactance in the busbar is exactly the current inertia that it represents, increasing the time necessary for the completion of the fault current switching. Moreover, the X/R ratio of the AF quenching device increases, favoring the dc level[21] in the currents, which contribute negatively to the specification of the thyristors. In this sense, however, the stray resistance of the reactor can be of interest.

For all the reasons presented above, it is clear that the impedance should be low with a more inductive than resistive characteristic. Air-core, dry type reactors will be the choice in this work due to their high operating availability, very low failure rate and low operation and maintenance costs (GE, 2017c).

2.3.2 Electrothermal Behavior of a Thyristor

The *silicon-controlled rectifier* (SCR), or thyristor, has been one of the most powerful semiconductor switches ever produced due to the clear advantages in fabricating a high-power device in a single wafer and the highly reliable press-pack[22] packaging technology (Huang, 2017). At the time this dissertation was being written, typical press-pack thyristor was commercially available up to 7.6 kA and 8.5 kV (Semi, 2019). Part number FT1500AU-240 from Mitsubishi is rated 1.5 kA, 12 kV and is commercially available as well (Corporation, 2020).

Thyristors have been frequently used in crowbar circuits in which a capacitor bank is discharged into a load, like army applications (Boenig et al., 1997), electric guns (Pastore et al., 1993; Podlesak et al., 2001), and electromagnetic launchers and flash lamps (Liu et al., 2019). By forming a very low-impedance short-circuit they provide a freewheel path for the load current (Pawar and Patil, 2016). In the field of industrial applications, these devices are often used in pulsed power tools intended for removal of surface layers and drilling (Akiyama et al., 2007). Another application of power thyristors is as bypass switch for series-connected power conditioners, for example dynamic voltage restorers (Amaral et al., 2015). In this case, a bidirectional ac switch, composed by two antiparallel-connected thyristors, remains closed until a voltage sag is detected on the supply side – when the ac switch then opens leading to the operation

[20] 1 ft $\approx$ 30 cm.

[21] The initial dc level is precisely the instantaneous symmetrical current that would be circulating in the reactor at that instant if it was not initially inactive.

[22] Also called capsule.

of the series power converter to the load side voltage restoration. However, should a short-circuit take place at the protected load side, the bypass switch would be subjected to a high current surge until the operation of an upstream OCPD – often a CB.

Since thyristors have been designed for steady operating mode, typical of power supplies, motor drives or power conversion systems, their application in pulsed switching is out of the ordinary and therefore requires special considerations. The best choice of power semiconductor devices is dependent on the specific pulse switching application. In pulsed applications the switched current waveform goes beyond the continuous ratings in data sheets (Vitins et al., 1989). Even though the operation of the ac switch under such circumstances is relatively rare, the large current surge that arises when it does occur may lead to the catastrophic failure of the thyristors that compose the ac switch. In this sense, these components must be designed considering their anticipated withstanding to the expected short-circuit current that may be clearly part of their mission profile. This scenario is worsened by the fact that short-circuit currents may include a dc-level component, leading to time-varying current amplitude through the ac switch and consequently in asymmetry between the current waveforms that each of the two thyristors is subjected to.

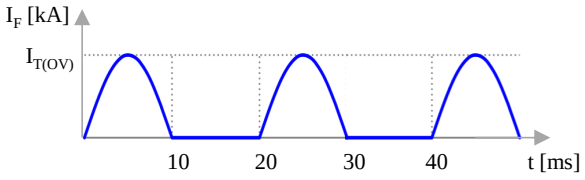
The ratings of power semiconductor devices are extremely important because of the high probability of catastrophic device failure if they are exceeded (Read and Dyer, 1967; Chamund and Rout, 2009b). Almost all thyristors ratings are based on their virtual junction temperature (T_{vj}), which maximum calculated value is limited by the blocking capability of the device. This is normally set at 125 °C. If this limit is exceeded, then the subsequent reliability of the device operation cannot be guaranteed.

Main Ratings

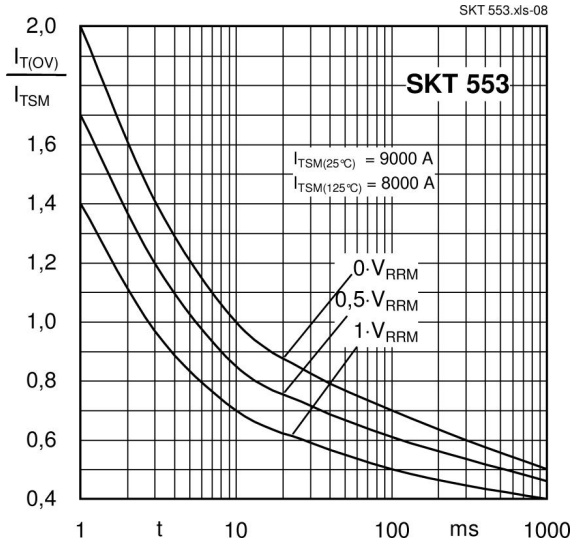
Parameter I_{TSM} (*peak non-repetitive surge current*) is the maximum allowable non-repetitive surge current the device will withstand at a specified pulse width. Manufacturers often specify this parameter in the data sheets as the maximum 10 ms half-sine wave of current, following maximum load current (case temperature $T_c = 125$ °C) that the thyristor can conduct without the device experiencing thermal runaway and the silicon melting. Yet the temperature may temporarily increase to as much as 400 °C (Somos et al., 1995; Wintrich et al., 2015). I_{TSM} is empirically determined by the manufacturer by viewing the forward voltage characteristic of the thyristor at high currents and observing the onset of thermal runaway. Exceeding this limit will damage the device. In other words, the surge current rating is determined to be the maximum peak surge current at which none of a significant sample of devices failed or degraded in

voltage classification (Motto, 1971). Because the device is so hot following the surge current pulse it loses its ability to block voltage, this rating is for zero reverse re-applied voltage. Also the temperature excursion is so high that the device will fail due to temperature cycling wear out if this level of current is repeated several (over 100) times along its life (Motto, 1971).

Manufacturers commonly present a curve relating permissible on-state current surge peak $I_{T(OV)}$ normalized[23] to I_{TSM} shown as a function of the duration[24] t. For events lasting longer than 10 ms, the graph assumes the current waveform to be a series of half-sine waves of 10 ms duration[25] occurring at a rate of one every[26] 20 ms (Semikron, 2015), as shown in Figure 2.7a. Figure 2.7b shows permissible overload on-state currents, $I_{T(OV)}$, in relation to surge on-state current, I_{TSM}, for semicycles of 10 ms as a function of time t and various reverse voltage conditions directly following the last sinusoidal half-sine wave. It was taken from Semikron part number SKT-553/18E (41 mm, 1.8 kV, 553 A) data sheet (Semikron, 2018). The values presented in the curves of Figure 2.7b are derived by calculating the current that gives the same peak temperature as the 10 ms half-sine wave from the physical rating of the device.



(a) Standard current profile considered for definition of the surge capability of the thyristor (Wintrich et al., 2015).

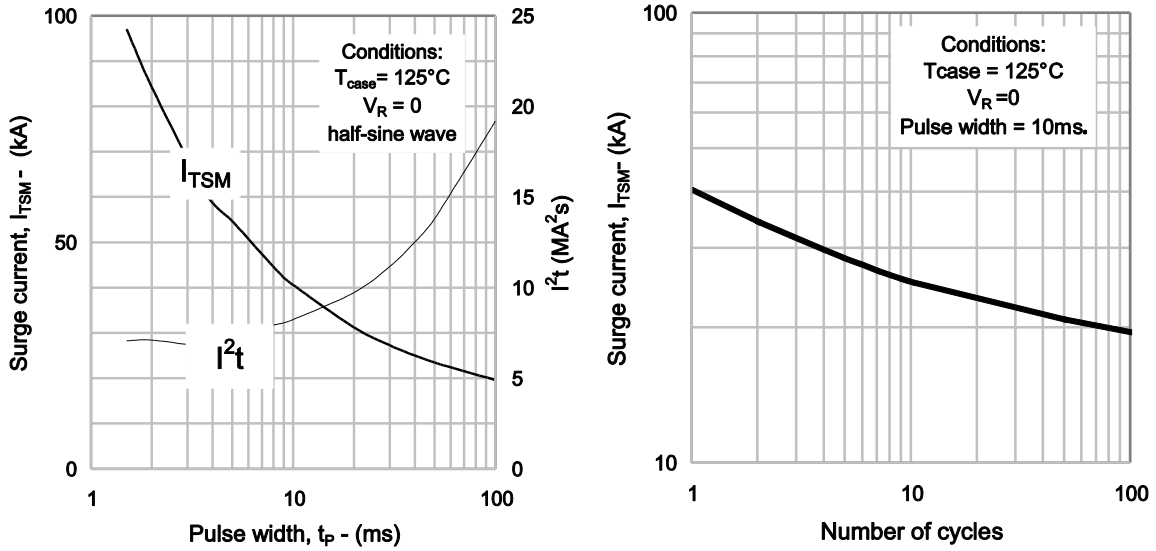


(b) Surge current capability of part number SKT-553/18E (Semikron, 2018).

Figure 2.7 Standard current profile and surge capability of a commercial thyristor.

[23]This parameter is also called "limiting overload characteristics".
[24]Or the number of cycles.
[25]Sequential 50 Hz sinusoidal semicycles.
[26]At 60 Hz, each semicycle has a duration of 8.3 ms, ocurring one every 16.7 ms. In this case, I_{TSM} is about 10% higher (Wintrich et al., 2015).

The I^2t has been applied[27] in the selection of protective devices, especially fuses, for power semiconductors (Rout, 2014a). Therefore, it has to do essentially with avoiding that excessive heating effect due to thermal energy dissipated in the device during a fault in the equipment. Some manufacturers present a curve showing I^2t ratings for shorter and longer pulses of current, as shown in Figure 2.8, which was taken from Dynex part number DCR3030V42 (100 mm, 4.2 kV, 3030 A) data sheet (Semi, 2014). Although the peak current increases with decreasing time, as expected, the I^2t actually decreases (Crnko, 1979; Semiconductor, 2006). The main reason is that, the longer the time interval, the more heat is dissipated from the device to the heatsink. This is particularly true for double sided cooling and high current ratings (Pearse and Newberry, 1970; Newell, 1976a). At 60 Hz, I^2t has almost the same value as at 50 Hz, since I_{TSM}, which is 10% higher at 60 Hz, is offset by the shorter time pulse, i.e.: $1.1^2 \cdot 8.3 = 10$ (Wintrich et al., 2015).



(a) As a function of the pulse width.

(b) As a function of the number of cycles.

Figure 2.8 Thyristor surge current (Semi, 2014).

In the bypass switch application mentioned before in this section, for example, as well as for the AF quenching device, the electronic switch must conduct a high ac current when a short-circuit happens, but this surge lasts for no more than 3 to 5 power-frequency cycles, which is the typical time period that the upstream CB takes to complete its clearing process (Kay and Kumpulainen, 2013). In this scenario, the selection of the devices based only on their non-repetitive ratings available in

[27] Joule integral, or "circuit fusing considerations".

the data sheets, like I_{TSM}, is not good enough to the optimum realization of the solution. I_{TSM} is not readily applicable because the expected current profile has variable amplitudes along the time. I^2t is not readily applicable because the conditions for I^2t to be a constant in the thyristor would be that the forward voltage drop be directly proportional to forward on state current, like in pure copper, and that the forward drop is independent of junction temperature. Both conditions are not true.

Ratings V_{DRM} and V_{RRM} are the voltages that the device reaches when the leakage currents I_{DRM} and I_{RRM} attain their test limits as given in the data sheet, or the maximum rated voltage whichever is reached first. The device may well be capable of reaching a higher voltage but excessively large leakage currents will make temperature control difficult and failure through thermal runaway may occur (ABB, 2007).

Parameter $(di/dt)_{cr}$ (*critical rate of rise of on-state current*) is the maximum rate of rise of load current under the conditions of forward blocking voltage of $67\% \cdot V_{DRM}$, peak forward current of twice the rated average current, $T_{vj} = 125$ °C and the gate conditions for each device type. When a thyristor is triggered on the initial conduction area is small and hence the current carrying capacity is limited. If the $(di/dt)_{cr}$ rating is exceeded then damage to the thyristor may occur.

The parameter $(dv/dt)_{cr}$ (*critical linear rate of rise of off-state voltage*) is the maximum value for the linear rate of rise of forward voltage (from 0 V to $67\% \cdot V_{DRM}$) that can be applied without initiating turn-on in the thyristor with the gate open circuit. The value of $(dv/dt)_{cr}$ is specified at case temperature $T_c = 125$ °C.

Transient Thermal Impedance

The thermal properties of a thyristor are described by its transient thermal impedance characteristic curve - see Figure 2.9 (Semi, 2014). This curve takes into account both transient and steady state behavior. It is obtained by thermal modelling of the device using finite element method and is verified by measurements (Wintrich et al., 2015). Because of heat storage effects due to thermal capacity, the transient thermal impedance for short pulse time durations is much lower than that for steady-state or long pulse times. The steady-state value, which is the flat upper right-hand portion of the curve, is defined as *thermal resistance*, $R_{th(j-c)}$. In other words, the transient thermal impedance curve gives the temperature response to a unit power step. For a dissipated power of 1 kW and an imposed case temperature of 0 °C, the junction temperature is equal to the *transient thermal impedance*, $Z_{th(j-c)}$ (Volle et al., 2010).

The use of the transient thermal impedance curve in rating calculations allows the consideration of cyclic junction temperature excursions. At power frequencies, these

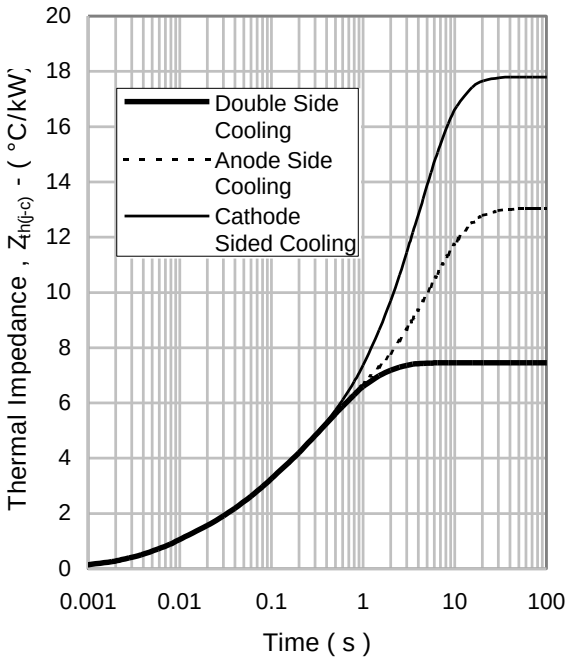


Figure 2.9 Transient thermal impedance curves of device DCR3030V42 (Semi, 2014).

cyclic excursions are appreciable because the current pulse widths that occur in phase controlled circuits are of the same order of magnitude as the thermal response time of the semiconductor crystal.

A complete expression for time-dependent transient thermal impedance is commonly presented by device data sheet as the sum of n terms[28] (Semiconductor, 2006):

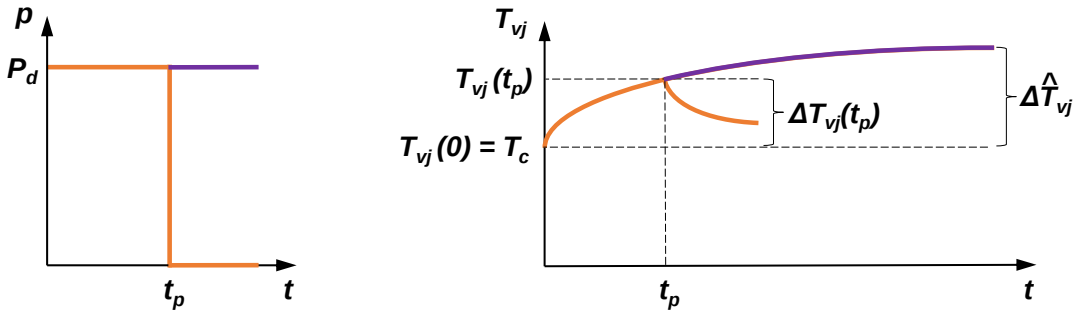
$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_{th(j-c),i} \cdot \left(1 - e^{\frac{-t}{\tau_{th(j-c),i}}}\right). \tag{2.10}$$

The parameters $R_{th(j-c),i}$ and $\tau_{th(j-c),i}$ (*thermal time constant*) are given in a table in the data sheet. If not, they can be easily estimated using curve fitting techniques. $Z_{th(j-c)}(t)$ is used to calculate the device junction temperature for time dependent power dissipation (Allard et al., 2001; Semikron, 2015).

When a junction dissipates power associated with a single pulse of length t_p and amplitude P_d (see Figure 2.10a), its temperature increases during the pulse and decays towards the original temperature after the energy pulse ceases. The junction temperature varies from case temperature[29] (T_c) to a level above the normal maximum

[28] In general, $n = 4$ or $n = 5$.

[29] Assuming that the device stayed previously turned off for a long time, i.e., thermal equilibrium before the application of the current surge. For pulses up to 100 ms, no stationary temperature difference develops between junction and case and therefore T_c may be appropriately considered



(a) Power pulse. (b) Virtual junction temperature.

Figure 2.10 Virtual junction temperature variation after a single power pulse.

operating limit (see Figure 2.10b), according to (2.11). The upper temperature due to the power pulse, $T_{vj}(t_p)$, can[30] cause silicon damage if the maximum allowable limit is exceeded too often or by a large amount on just a single occasion (Williams, 2006).

$$\Delta T_{vj}(t_p) = P_d \cdot Z_{th(j-c)} = P_d \cdot \sum_{i=1}^{n} R_{th(j-c),i} \cdot \left(1 - e^{\frac{-t_p}{\tau_{th(j-c),i}}}\right), \tag{2.11}$$

where the maximum temperature variation attained if the power pulse were kept is:

$$\Delta \hat{T}_{vj} = \Delta T_{vj}(t_p)|_{t_p \to \infty} = P_d \cdot \sum_{i=1}^{n} R_{th(j-c),i}. \tag{2.12}$$

Virtual Junction Temperature Calculation

From (2.11) and Figure 2.10b, the instantaneous virtual junction temperature of the device, $T_{vj}(t)$, submitted to a single rectangular power pulse P_d can be expressed as:

$$T_{vj}(t) = T_{vj}(0) + \Delta T_{vj}(t) = T_{vj}(0) + P_d \cdot \sum_{i=1}^{n} R_{th(j-c),i} \cdot \left(1 - e^{\frac{-t}{\tau_{th(j-c),i}}}\right) \tag{2.13}$$

during the heating period ($t \leq t_p$), and as:

constant during this interval (Wintrich et al., 2015), i.e., the process can be considered adiabatic (Sperow, 1973). In practice, the temperature of the case starts increasing later and rises at a slow pace than the junction temperature. Assuming an adiabatic process for design purposes is a conservative measure, since heat (even if only slightly) will be transferred from the junction to the case.

[30]The subscript 'v' stands for "virtual". It comes from the fact that the junction temperature of a power semiconductor is not measurable.

$$T_{vj}(t) = T_{vj}(0) + \Delta T_{vj}(t) = T_{vj}(0) + P_d \cdot \sum_{i=1}^{n} R_{th(j-c),i} \cdot \left(1 - e^{\frac{-t}{\tau_{th(j-c),i}}}\right) + \\ -P_d \cdot \sum_{i=1}^{n} R_{th(j-c),i} \cdot \left(1 - e^{\frac{-(t-t_p)}{\tau_{th(j-c),i}}}\right) \tag{2.14}$$

during the cooling period ($t > t_p$).

For a non-rectangular power pulse and for a complex power waveform, which is often the case, it has to be approximated by a number of sequential step waves[31] of 1 ms (Schonholzer, 1972; Dynex, 2002; Wintrich et al., 2015), each one representing the average power at that interval. This approach takes advantage of the linear properties of the thermal system, for which the superposition principle is valid. This is the method that has been historically used for virtual junction temperature calculation. For m sequential power pulses, (2.15) can be directly applied:

$$T_{vj}(t_m) = T_c + \sum_{\mu=1}^{m} \left\{ (P_\mu - P_{\mu-1}) \cdot \sum_{i=1}^{n} \left[R_{th(j-c),i} \cdot \left(1 - e^{\frac{-(t_m - t_{\mu-1})}{\tau_{th(j-c),i}}}\right) \right] \right\}, \tag{2.15}$$

where P_μ is the equivalent rectangular pulse power at instant t_μ. The calculation of the equivalent power pulses depend on the instantaneous power, which in turn depends on the calculation of the voltage drop across the device.

Voltage Drop Under Current Surge

In the application covered in this work, the correct calculation of the voltage drop across the device is extremely important both for the correct computation of the power dissipation and for the proper calculation of the thyristor contribution to the voltage across the AF quenching device. There are many references for curve fitting-based models of thyristor voltage drop (Schonholzer, 1972; Newell, 1976a,b; Motto et al., 1997, 1998; Profumo et al., 1999). The most known are *MNOP* (Somos et al., 1995), *KNHM* (Walker and Weldon, 1999) and *ABCD* models. *ABCD* model is commonly used by the manufacturers (Chamund et al., 2009):

$$v(i) = A + B \cdot ln(i) + C \cdot i + D \cdot \sqrt{i}. \tag{2.16}$$

[31] Also called "equivalent power pulses".

This relation is valid for a fixed temperature (isothermal) and a specified current range (often up to I_{TSM}). The parameters A, B, C, and D are either given for $T_{vj} = 125$ °C. These are usually obtained by curve fitting the measured on-state characteristics using regression method. The first constant term is related to the threshold voltage of a diode which is about 0.5 V for silicon. The next term is the classical log relationship of a PN junction at low injection levels. Next, the linear or ohmic drop in a thyristor. The last term is the space charge limited emission characteristic (Motto et al., 1996).

This relation gives reasonable accuracy if self-heating is minimal, which is not the case in this work since the peak currents reached by the devices are much higher than the average current rating. Figure 2.11, which was taken from Dynex DCR3030V42 data sheet, shows how the instantaneous i vs. v curve changes for different values of junction temperature.

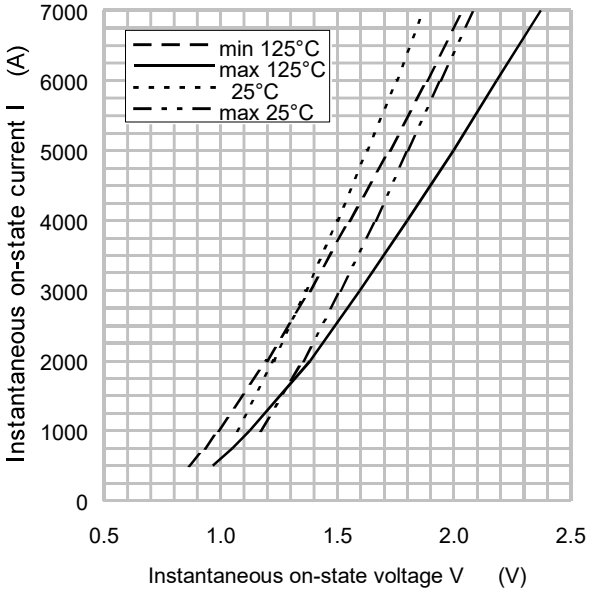


Figure 2.11 Thyristor instantaneous on-state forward current as a function of voltage and temperature of device DCR3030V42 (Semi, 2014).

At current densities of interest for operation, on-state voltage increases with increasing temperature[32]. It is beneficial because when the device is to ride through a fault current and reach high temperature due to self heating, a positive temperature dependence makes uneven temperatures on the silicon pellet tend to even out as the local current distribution favors the cooler regions (Rodrigues et al., 1998). The transi-

[32]Silicon thermal conductivity at -193 °C is 53 times the value at 927 °C, and specific heat of silicon at 927 °C is 5 times the value at -193 °C (Walker and Weldon, 1999).

tion from *negative temperature coefficient* (NTC) to *positive temperature coefficient* (PTC) can be observed on the voltage curves shown in Figure 2.11.

Equation (2.16) should be then modified into a temperature dependant relationship by assigning a separate temperature coefficient element to the constants A, C, and D. The logarithmic term is eliminated without loss of accuracy, and the exponent k_v is introduced to reflect the fact that the on-state voltage grows faster with temperature at elevated temperatures (Cepek, 1999):

$$v(i, T_{vj}) = [A + a_v \cdot T_{vj}] + [C + c_v \cdot T_{vj}^{k_v}] \cdot i + [D + d_v \cdot T_{vj}] \cdot \sqrt{i}, \tag{2.17}$$

where the coefficients A, a_v, C, c_v, k_v, D, and d_v can be obtained using a regression method on the values of the on-state voltage obtained from the data sheet, i.e. $v(i,25°\text{C})$, $v(i,125°\text{C})$. The constraints $a_v > 0$ and $k_v < 1.3$ are generally adopted (Cepek, 1999).

Catastrophic Failure

The junction temperature of a power semiconductor in any particular situation profoundly affects its performance and reliability. High junction temperature will change device features and may cause failure (Read and Dyer, 1967; Westcode, 2012a; Rout, 2014b; Wintrich et al., 2015; Dai et al., 2016). If a thyristor is subjected to surge on-state current load, the junction temperature may temporarily increase[33] to as much as 400 °C, as long as the magnitude and rate of rise of current (di/dt) is restricted to tolerable levels (Eriksson et al., 1996; Semiconductor, 2006; Chamund et al., 2009). For the reader's reference, at 600 °C the metal of the surface contacts starts to penetrate into the silicon causing eventual short-circuit. At 1100 °C, non-repetitive di/dt limits are reached (Sankaran et al., 1991, 1993). The high local thermal stress causes cracking of the silicon. The melting point of silicon is 1415 °C.

The normal failure mode for a ceramic press-pack thyristor is on a short-circuit. Since there are no bonded wires or flexible leads that can be ruptured or break as in the case of the soldered modules, it is extremely unlikely that these device types will fail open circuit. Whist it is impossible to guarantee these statements, press-pack devices will fail to a stable short-circuit condition with a resistance comparable to that of a normal device in forward conduction (Westcode, 2012b). This condition is essential to the fail-safe operation of the electronic AF quenching device, once a low-impedance path is guaranteed in parallel with the arcing fault even under a failure condition[34].

[33] Peak temperature lags peak current by typically 2 or 3 ms (Dynex, 2002).

[34] The failure of the power thyristor does not lead to loss of protection, but this is not valid for the gate-driver.

By increasing the magnitude of the gate trigger pulse to several times the minimum required, and applying it with a very fast rise time, one may considerably increase the size of the spot in which conduction starts, improving the di/dt capabilities and reducing the stress on the device (Semiconductor, 2006). The RC element connected in parallel for overvoltage protection can contribute to a fast-rising discharge current through the thyristor at every trigger (Wintrich et al., 2015). On the other hand, the limiting value of the di/dt before damage occurs is related to the size of the initial turn-on area and the spreading velocity[35]. The larger the device, the smaller the relative initial area, and more appreciable is this effect. Under high di/dt conditions the junction temperatures can vary rapidly in high-power devices (1 °C/μs) (Rohwein et al., 1995; Rodrigues et al., 1998).

Figure 2.12a shows typical hysteresis-type[36] curves of a thyristor under a single pulse of half-sine surge wave for three values of peak current I_{max}: (a) 1.15 kA; (b) 1.24 kA; and (c) 1.30 kA. The initial junction temperature is T_{vj} = 125 °C. Curve 'c' has a peculiar shape: after the current has almost reached its maximum value of 1.30 kA, a strong increase of voltage occurs - leading to exceedingly high power dissipation, followed by the crossing of the curves 'a' and 'b' in their falling part, which leads subsequently to the electrothermal failure of the device (dashed line) (Silard, 1984).

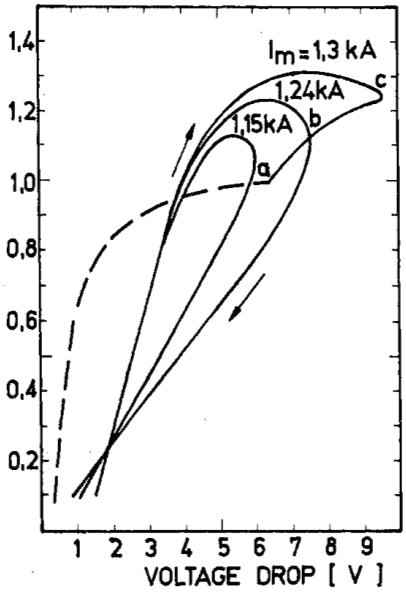
Besides catastrophic failure, wearout failures due to thermal stress induced defects[37] make more likely that any localized rise of temperature might eventually lead to electrothermal runaway and subsequent failure of devices even under a single pulse surge with peak current well below the destructive threshold. Figure 2.12b shows measured dynamic voltage drop for a thyristor under a single pulse of 50 Hz half-sine surge wave for five characteristic values of peak current and initial junction temperature T_{vj} = 125 °C. The device failed at the beginning of the surge cycle with peak current of I_{max} = 1.3 kA, most likely due to thermal stress-induced defects occured during their testing at I_{max} = 1.2 kA (Silard, 1984).

This work is focused on the specification of the device so that it is guaranteed that it will not undergo a catastrophic failure during the operation of the AF quenching device. In this sense, the mission profile must be understood and the information contained in the data sheets of the devices applied so that the best result is achieved.

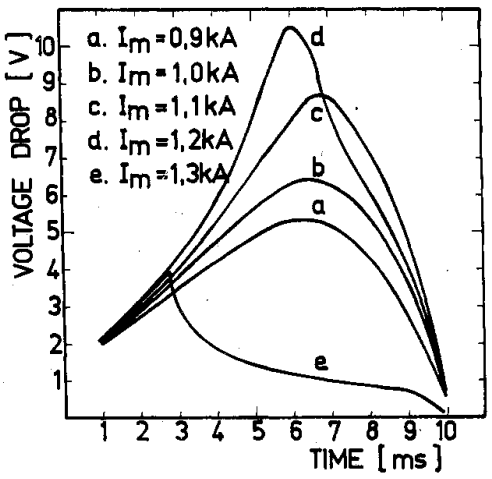
[35]Because of the lateral base resistance the portion of the gate closest to the gate contact is the first to be turned on because it is the first to be forward biased. The spread of conduction takes place at typically 1 mm/μs (Dunlop, 2000; Smith and Rout, 2014; Rout, 2017).

[36]Notice that the voltage is greater during current decrease. This is the PTC behavior previously shown in Figure 2.11.

[37]The most important failure process is mechanical wear out due to expansion and contraction caused by cyclic power loading (Chamund and Rout, 2009a; Liang et al., 2018).



(a) i vs. v.



(b) v vs. t.

Figure 2.12 Thyristor behavior under a half-sine surge wave (Rodrigues et al., 1998).

2.3.3 Mission Profile

If the shunt impedances and the thyristors are not properly selected, the current surge will produce internal structure melting and subsequent device failure. On the other hand, overrating is equally a concern, leading to increase in the volume, weight and cost of the equipment. Therefore, the specification of the components should take into account both the operational effectiveness of the equipment and its reliability / safety.

It has been reported that the lifetime of an industrial switchgear is about 50 years. During this time interval, it is estimated that not more than three arcing faults take place in the equipment (Conceição, 2015). Therefore, both the shunt impedances and the thyristors have null "steady state" current[38]. Once in operation, though, these elements experience a large current surge that lasts from three to five power-frequency cycles, depending on the time the upstream CB takes to complete its opening process. The higher the number of cycles, the higher is the number of half-sine waves (plus dc components) that the shunt impedances and the thyristors will be subjected to. This is the mission profile that will be considered for design purposes in this work.

There is the possibility that the CB fails to open. In this case, the surge current produced by the operation of the quenching device lasts until the complete opening of the immediately near upstream protective device. The quenching device will remain

[38] So called "hot stand by" state.

effective only if it was previously designed to withstand such condition, since the electronic switch will be subjected to a longer current surge, which will certainly result in higher thyristor junction temperature and more severe commitment of device supportability. The backup CB should not be directly activated by the AFR, since it would lead to loss of selectivity. Hence, fast selectivity / coordination schemes contribute to electronic quenching device preservation, i.e., it is desirable that the operation of the device trips the upstream *overcurrent relay* (OCR) after a certain coordination interval. This is a backup procedure.

It should be noticed that the thyristors operate normally open in the AF elimination, being triggered only if an arcing fault is detected. Therefore, the surge does not start with $T_c = 125$ °C as is the case during manufacturer test condition. Since the device stays out of operation for a long time interval, junction temperature is equal to case temperature, which is conservatively considered to be from 40 to 50 °C in a switchgear or MCC (Jacks, 1969; Sperow, 1973). In this case, a higher surge rating than that declared by the data sheet can be applied (Pearse and Newberry, 1970).

Finally, since the breaker isolates the busbar after the operation of the AF quenching device, the ability of the thyristors of blocking voltage after the event is not required. However, this capability must return following a sufficient cooling interval after the surge, which demands that breaker reclosing is allowed only after a preset time period. This can be programmed as a lockout in the protective system (Smith et al., 2016).

2.4 Summary

In this chapter it has been presented a general view of the system treated in this work. An analytical evaluation comprising the power system, arc conductance, shunt impedances and the electrothermal behavior of thyristors has been given. Though being a traditional device, the specific application of thyristors to an AF quenching device presents new difficulties associated to the short-time, high current surges that the component will be subjected to. In this sense, the ratings presented by manufacturers can not be readily applied for the specification of these components. These exotic characteristics must be also considered for the specification of the shunt impedances. For both elements, there are effectiveness, reliability and trade-off aspects to be taken into account. These questions have been carefully clarified in this chapter, opening the way for the proposal that will be presented in the following one.

Chapter 3

Modeling and Proposal

"Failure is not an option."
Apollo 13 - Imagine Entertainment

This chapter is centered on the specification of the power components of the AF quenching device so that it operates reliably, but also have a low cost, is compact and fully reusable. As it was made clear in the previous chapter, the particularities of the application dictate the demand for an original proposal, which is the central contribution of this chapter. For design purposes, the discrete-time modeling of the overall system, including the arcing path conductance, is presented, so that it can be lately implemented in Chapter 4 to obtain simulation results.

3.1 Discrete-time Arcing Path Conductance

In this section, single- and three-phase discrete-time domain AF equations will be derived for later implementation in MATLAB and ATPDraw.

3.1.1 Single-Phase Model

Equation (2.6) can be directly inserted into (2.5), which is solved for $g(t)$ in discrete-time domain:

$$g(t) = \frac{\Delta t}{\tau + \Delta t} \cdot \left[\frac{\tau}{\Delta t} \cdot g(t - \Delta t) + G_{min} + \frac{|i(t)|}{(V_O + R_O \cdot |i(t)|) \cdot \ell} \right], \tag{3.1}$$

where Δt is the time step. Constant G_{min} was previously added to $G(t)$ in order to avoid numerical overflow, since the arcing fault path will be implemented within the power system in the form of a controlled resistance $r(t) = 1/g(t)$, which would have an infinite value if $g(t - \Delta t) = 0$ and $i(t) = 0$ simultaneously in (3.1). More than avoiding numerical overflow, the parameter G_{min} has electrical significance since it can be interpreted as the air conductance that previously exists between the busbar conductors before the fault starts. It dictates the arc striking voltage in normal conditions. Moreover, the arcing faults stablished in the laboratory for testing purposes are triggered by inserting a thin bare copper wire that melts at the initial instants of the experiment, then the arcing fault starts through a hot, extremely ionized plasma channel. Therefore, G_{min} is too high during the initial instants of the arcing fault. In this work, this behavior will be considered in the model by splitting G_{min} into two portions:

$$G_{min}(t) = G_{min,\ell} \cdot u(t) + G_{min,h} \cdot [1 - u(t - t_{min,h})], \tag{3.2}$$

where u is the unit step function, $G_{min,\ell}$ is the free air conductance, $G_{min,h}$ is the plasma channel conductance and $t_{min,h}$ is the time at which the copper wire melting process ends.

3.1.2 Three-Phase Model

The AF tests performed in the IEEE-NFPA Collaborative Research Project include three-phase trials, which will be then considered in this dissertation. Phase voltages and line currents have been recorded during the experiments. Figure 3.1 presents the model of a three-phase arcing fault that will be adopted in this work, where g_{AB}, g_{BC}, and g_{CA} are phase-to-phase conductances, v_{AB}, v_{BC}, and v_{CA} are phase-to-phase fault voltages, i_{AB}, i_{BC}, and i_{CA} are fault currents, and i_A, i_B, and i_C are line currents.

The line voltages v_{AB}, v_{BC} and v_{CA} can be obtained from measured phase voltages according to:

$$\begin{cases} v_{AB} = v_{AN} - v_{BN} \\ v_{BC} = v_{BN} - v_{CN} \\ v_{CA} = v_{CN} - v_{AN} \end{cases}. \tag{3.3}$$

Moreover, the relation between phase and line currents can be stated as in:

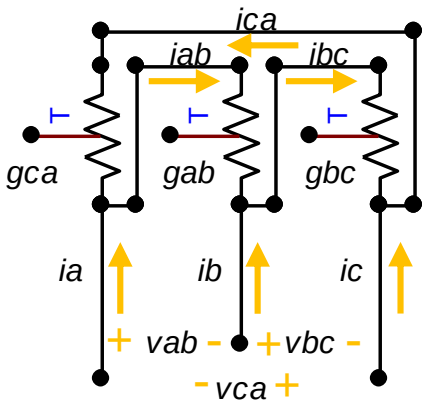


Figure 3.1 Three-phase arcing fault model.

$$\begin{cases} i_{AB} - i_{CA} = i_A \\ i_{BC} - i_{AB} = i_B \\ i_{CA} - i_{BC} = i_C \end{cases} . \tag{3.4}$$

Also, (3.5) relates the phase conductances g_{AB}, g_{BC}, and g_{CA} to their respective voltages and currents:

$$\begin{cases} i_{AB} = v_{AB} \cdot g_{AB} \\ i_{BC} = v_{BC} \cdot g_{BC} \\ i_{CA} = v_{CA} \cdot g_{CA} \end{cases} . \tag{3.5}$$

From the combination of (3.3), (3.4), and (3.5), one can obtain the equation below, which allows for the calculation of the instantaneous arc conductances from the measured values:

$$\begin{bmatrix} g_{AB} \\ g_{BC} \\ g_{CA} \end{bmatrix} = \begin{bmatrix} v_{AB} & 0 & -v_{CA} \\ -v_{AB} & v_{BC} & 0 \\ 0 & -v_{BC} & v_{CA} \end{bmatrix}^{-1} \cdot \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} . \tag{3.6}$$

Once the calculation presented above is accomplished, the conductances can be individually modelled according to the development previously given in Section 3.1.1.

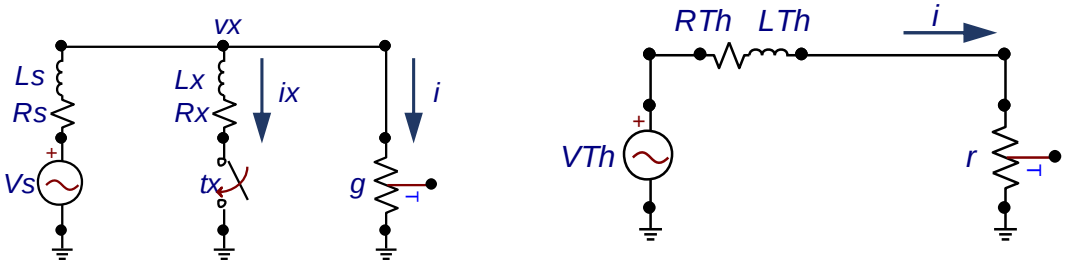
3.2 Electronic Arc-Flash Quenching Device Design

3.2.1 Shunt Impedance Design

The objective of this section is to present a detailed analysis, modeling and solution for the design of the shunt impedances of the AF quenching device.

Simplified Formulation and Solution

Figure 3.2a presents the diagram of an electric circuit that represents a simplified single-phase version of the working principle behind the idea of AF elimination. The arc, represented by its dynamic conductance $g(t)$, is fed by a power system that is represented by its equivalent at the point of interest[1], i.e., a voltage source V_S behind an equivalent resistance R_S and inductance L_S. Once the arcing fault is detected, the switch t_x is closed so that the current i_x starts flowing and the current at node x is decreased to a value low enough to extinguish the AF current i.



(a) Simplified circuit.

(b) Linear portion replaced by its Thévenin equivalent.

Figure 3.2 Application of the compensation method for the calculation of the shunt impedance.

Notice that the impedance $\dot{Z}_x = R_x + j\omega L_x$ forms a voltage divider with $\dot{Z}_S = R_S + j\omega L_S$ in steady state conditions. Let us consider that the switch t_x is closed and the branch that contains the arc is disconnected from the circuit. In this situation, the magnitude of the steady-state voltage at the node x can be calculated as:

$$|\dot{V}_x| = \left| \frac{\dot{Z}_x}{\dot{Z}_x + \dot{Z}_S} \cdot \dot{V}_S \right|. \tag{3.7}$$

From the equation above, one can conclude that the lower is the value of $\dot{Z}_S$, the lower must be the value of $\dot{Z}_x$, given $\dot{V}_x$ and $\dot{V}_S$. Therefore, it is interesting that the

[1]The node x, which represents the busbar of a switchgear, for example.

design starts by calculating $\dot{Z}_x$. At this point, the voltage drop across the thyristor can be neglected since the device is not selected yet. Then, the design can advance by considering the maximum dc-level that can take place in the studied system. The higher the equivalent X/R factor[2], the higher the asymmetry factor κ - see Figure 3.3.

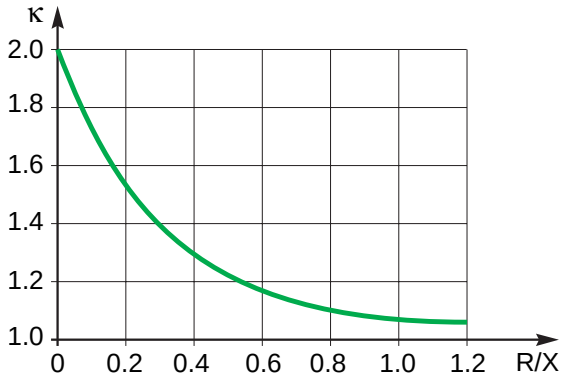


Figure 3.3 Asymmetry coefficient κ vs. R/X ratio (de Metz-Noblat et al., 2005).

Next, the thyristors can be pre selected initially by taking into account the value of I_{TSM}, so that their voltage drop (at least the resistive portion, which is declared in the data sheet as r_T) can be included in the model. Moreover, there is a minimum value for the inductance L_x, which has to be incorporated in series with the thyristor so that $(di/dt)_{cr}$ described in Subsection 2.3.2 is not exceeded at the beginning of the operation of the AF quenching device. For press pack thyristors with I_{TSM} in range of kA, 100 A/μs $< (di/dt)_{cr} <$ 300 A/μs. For a 440 V system:

$$v_{L_x,max} = 1.1 \cdot 440 \cdot \frac{\sqrt{2}}{\sqrt{3}} = L_{x,min} \cdot \frac{di}{dt}_{cr} \Rightarrow L_{x,min} = \frac{1.1 \cdot 440 \cdot \frac{\sqrt{2}}{\sqrt{3}}}{\frac{di}{dt}_{cr}}, \tag{3.8}$$

where the factor 1.1 has been conservatively adopted due to possible sustained over-voltages in the power system. For $(di/dt)_{cr} = 200$ A/μs, one will obtain $L_{x,min} \approx 2$ μH.

Finally, the time-domain simulation can be performed, initially for single- and then for three-phase cases. The time-domain solution of the circuit illustrated by Figure 3.2a can be achieved by the application of the compensation method, where the linear portion is replaced by its Thévenin equivalent, as shown in Figure 3.2b.

$g(t)$ is calculated according to (3.1) and:

$$v_S(t) = V_{max} \cdot sin(\omega t + \phi), \tag{3.9}$$

[2]Or, conversely, lower R/X values.

$$r(t) = \frac{1}{g(t)} = \frac{v_x(t)}{i(t)} \Rightarrow g(t) = \frac{i(t)}{v_x(t)} \Rightarrow i(t) = g(t) \cdot v_x(t). \tag{3.10}$$

Considering that for an inductor and for a capacitor:

$$\begin{aligned} v &= L \cdot \frac{\Delta i}{\Delta t}; \\ i &= C \cdot \frac{\Delta v}{\Delta t}, \end{aligned} \tag{3.11}$$

then:

$$v_S(\Delta t) - (R_S + R_x) \cdot i_x(\Delta t) - (L_S + L_x) \cdot \frac{i_x(\Delta t) - i_x(0)}{\Delta t} = 0. \tag{3.12}$$

Solving for $i_x(\Delta t)$, one will obtain:

$$i_x(\Delta t) = \frac{v_S(\Delta t) + i_x(0) \cdot \frac{L_S + L_x}{\Delta t}}{R_S + R_x + \frac{L_S + L_x}{\Delta t}}. \tag{3.13}$$

And solving for $v_x(\Delta t)$ on the central branch of Figure 3.2a:

$$v_x(\Delta t) = i_x(\Delta t) \cdot R_x + L_x \cdot \frac{i_x(\Delta t) - i_x(0)}{\Delta t}. \tag{3.14}$$

By disconnecting the nonlinear conductance $g(t)$ from the circuit shown in Figure 3.2a, $i(t) = 0$ and:

$$v_{Th} = v_x. \tag{3.15}$$

The Thevenin's equivalent resistance (R_{Th}) and inductance (L_{Th}) can be calculated by taking the parallel between the source ($\dot{Z}_S$) and the quenching device ($\dot{Z}_x$) branches:

$$\begin{aligned} R_{Th} &= \frac{R_S \cdot R_x \cdot (R_S + R_x) + \omega^2 \cdot \left[R_S \cdot L_x \cdot (R_x + L_S) + R_x \cdot L_S \cdot (L_S + R_x) \right]}{R_S^2 + R_x^2 + 2 \cdot (R_S \cdot R_x + L_S \cdot L_x) + L_S^2 + L_x^2} \\ L_{Th} &= \frac{R_S^2 \cdot L_x + R_x^2 \cdot L_S + \omega^2 \cdot L_S \cdot L_x \cdot (L_S + L_x)}{R_S^2 + R_x^2 + 2 \cdot (R_S \cdot R_x + L_S \cdot L_x) + L_S^2 + L_x^2}. \end{aligned} \tag{3.16}$$

Applying the Kirchhoff's voltage law to the circuit shown in Figure 3.2b:

$$v_{Th}(\Delta t) - [R_{Th}(\Delta t) + r(\Delta t)] \cdot i(\Delta t) - \frac{L_{Th}}{\Delta t} \cdot [i(\Delta t) - i(0)] = 0. \tag{3.17}$$

Since:

$$g(\Delta t) = \frac{\Delta t}{\tau + \Delta t} \cdot \left[\frac{\tau}{\Delta t} \cdot g(0) + G_{min} + \frac{|i(\Delta t)|}{(V_O + R \cdot |i(\Delta t)|) \cdot \ell} \right], \tag{3.18}$$

and:

$$r(\Delta t) = \frac{1}{g(\Delta t)} = \frac{1}{\frac{\Delta t}{\tau+\Delta t} \cdot \left[\frac{\tau}{\Delta t} \cdot g(0) + G_{min} + \frac{|i(\Delta t)|}{(V_O+R\cdot|i(\Delta t)|)\cdot\ell} \right]}, \tag{3.19}$$

then inserting (3.19) into (3.17) leads to:

$$v_{Th}(\Delta t) - \left[R_{Th}(\Delta t) + \frac{1}{\frac{\Delta t}{\tau+\Delta t} \cdot \left[\frac{\tau}{\Delta t} \cdot g(0) + G_{min} + \frac{|i(\Delta t)|}{(V_O+R\cdot|i(\Delta t)|)\cdot\ell} \right]} \right] \cdot i(\Delta t) + \\ - \frac{L_{Th}}{\Delta t} \cdot [i(\Delta t) - i(0)] = 0. \tag{3.20}$$

Since this is a transcendental equation, the solution for $i(\Delta t)$ must be obtained numerically, with the application of Newton-Raphson's method, for example. Once the solution is found, $v_x(\Delta t)$ can be calculated by:

$$v_x(\Delta t) = \frac{i(\Delta t)}{g(\Delta t)}, \tag{3.21}$$

where $g(\Delta t)$ can be obtained by inserting $i(\Delta t)$ into (3.18).

Finally, $i_x(\Delta t)$ can be obtained by applying the Kirchhoff's current law to the quenching device branch in Figure 3.2a:

$$R_x \cdot i_x(\Delta t) + \frac{L_x}{\Delta t} \cdot [i_x(\Delta t) - i_x(0)] = v_x(\Delta t). \tag{3.22}$$

Solving for $i_x(\Delta t)$,

$$i_x(\Delta t) = \frac{v_x(\Delta t) + i_x(0) \cdot \frac{L_x}{\Delta t}}{R_x + \frac{L_x}{\Delta t}}. \tag{3.23}$$

Complete Formulation and Solution

The single-phase system shown in Figure 3.4, which is more realistic[3], will be analyzed in this subsection. It is composed by the power system equivalent (V_S and Z_S), arcing

[3]The most important limitation is that the voltage drop due to the potential barrier of the thyristors was not considered.

fault conductance (g_a), quenching device branch (Z_x) along with thyristor conduction and blocking resistances (R_{cd} and R_{bl}, respectively), a current source (I_M) that emulates a generic load, motor backfeeding or even a generator, depending on the adjusted displacement angle. It could include harmonic content as well.

The solution of the circuit shown by Figure 3.4 will be implemented in MATLAB first. Both results from simulation in MATLAB and in ATPDraw will be treated later in Subsection 4.1.2. The rest of this section is devoted to the development of the numeric formulation necessary for the execution in MATLAB.

For organization purposes and to avoid any confusion, from now on in this work, the conductance of a single-phase arcing fault will be called[4] g_a and the conductances of a three-phase one will be called g_{AB}, g_{BC} and g_{CA}, as they were in Figure 3.1.2.

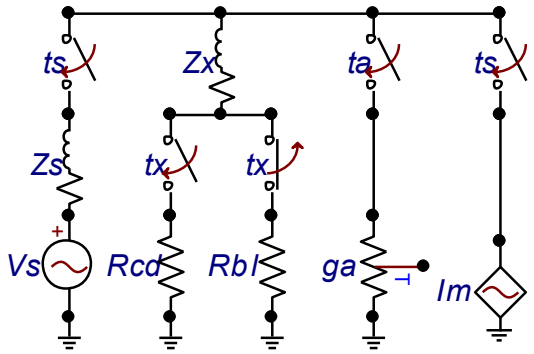


Figure 3.4 Single-phase simplified system including arcing fault, electronic quenching device and a generic current source. t_S, t_x and t_a are the commutation time stamps.

The superposition theorem and the compensation method (Martinez-Velasco, 2020) will be applied to solve the circuit by using discrete-form implementation in MATLAB along with Newton-Raphson method. The simulation will be divided into the three steps specified below.

1. Normal operation ($t_S \leq t < t_a$): This is the pre-fault circuit. The supply branch is feeding the load branch, establishing a one-mesh circuit. The quenching device branch, which is composed by Z_x and R_{bl}, is connected to the bus, but the current through it is remarkably low since the value of thyristor blocking resistance is extremely high. This circuit establishes the initial conditions to the next state.

2. Arcing fault ($t_a \leq t < t_x$): This is the fault circuit. The arc fault branch is added in parallel with the previous circuit. Its solution is useful to the determination

[4]The main reason is that the single-phase model will be considered for a per-phase analysis of three-phase cases.

of the minimum bus voltage required to trigger and keep the arc active. This voltage is the upper limit value that will be allowed in the bus during the next step. Notice that there are two ways for the initiation of the arcing fault:

(a) Operation mode: This case is verified if $t_a > t_S$. It means that the arcing fault starts while the system is in normal operation. The fault is not looked-for in this case. It is characteristic of arcing faults caused by animals or by circuit breaker rack out under load, for example.

(b) Test mode: It is the case if $t_S > t_a$. This is characteristic of the tests described by IEC and IEEE in (Commission, 2014; IEE, 2018) since the arc is pre-established even before the application of voltage to the system. The fault is intended in this case. However, a similar situation can be found in practice if a tool is left at the busbar after the execution of a maintenance work, for example.

In both cases, the impact of t_S and t_a is to drive the circuit to a given state at t_x, immediately before the arc-flash quenching device is inserted. This state will define the dc level at the quenching device current, which impacts the design of the shunt impedance and in the specification of the thyristors.

3. Fault elimination ($t \geq t_x$): This is the post fault circuit. R_{cd} replaces R_{bl} in the quenching device branch. The impedance Z_x must be designed in order to keep the bus voltage below the threshold observed in Step 2.

The implementation of the discrete-time algorithm associated with this formulation was developed in the same mode as described in the previous subsection. Its parametrization and the obtained results will be shown in Chapter 4.

The study presented here will be focused on the single-phase system. Since the operation of the electronic AF quenching device is three-phase (balanced), then the deep study of the single-phase case is helpful to the understanding of the system and design of its components. Still, the three-phase case will be modeled and simulated directly in ATPDraw later in Chapter 4.

Practical Aspects

At first, the wiring inductances and resistances should be considered (Semiconductor, 2006). However, since the LV eliminators have been built to be installed in a switchgear cell, as shown in Figure 1.9, there is not plenty length for this impedance to become

significant. Only in a scenario where the value of the equivalent upstream impedance of the power system is extraordinarily low is that the wiring impedance could become sufficiently high. For the sake of comparison, 1 m of a flat wire has approximately 1 μH of self inductance (Electronics, 2019).

Conversely, a single-layer air-core circular coil with a diameter of 20 cm made of 4 turns has an inductance around 5 μH (66pacific, 2021). The cross section area of the wire will determine the resistance of the coil. Flexible isolated power cables ranging from 6 AWG (16 mm^2) to 1 AWG (50 mm^2) can be applied for easiness of construction. Besides this benefit, low cost, absence of magnetic saturation and high reliability - same as the conventional cable, can be cited as the main advantages of this approach. The cable gauge can be low since the duration of the event is short, i.e., the heat produced is low and is distributed along the overall cable length. However, it cannot result in excessive temperature rise during the operation of the AF quenching device, which could compromise the insulation quality. If a high quality factor is desired, then a larger gauge should be chosen. Nonetheless, it could make it difficult the assembly of the coil into the space available inside the compartment of the equipment.

It will be shown also in Chapter 4 that a commercial inductor with these same characteristics is expensive, heavy and large. The main reason is that it is an element that operates out of conventional conditions, which in turn makes it a not commercially available off-the-shelf item since it is rarely requested.

3.2.2 Thyristor Specification

The selection of thyristors for the application discussed in this work will be based on two criteria: voltage drop and supportability.

The calculation of the voltage drop across a power thyristor undergoing high current conditions has been discussed in Subsection 2.3.2, where a suitable technique has been pointed out. The higher the current through the device, the higher is the voltage drop. Higher voltage drop can be interesting provided that it does not overcome the threshold value established for the safe extinction of the arcing fault. It contributes positively against the need of a shunt impedance, since the current across the AF quenching device becomes naturally lower as the voltage drop across the device raises. In other words, not always the device with higher I_{TSM} is the more suitable.

Moreover, the calculation of the voltage drop is useful for the determination of the power dissipated in the device, which in turn is necessary to predict its capacity of surviving the event safely. In this application, the thyristors are subjected to conditions

out of those that they have been tested for[5], as previously seen in Subsection 2.3.2: the initial junction temperature, the current waveform, and the frequency are different. Among these three concerns, only the last one is easily treated. An overrated device leads to improper oversizing, overweight and increased cost for the solution. On the other hand, the specification of underrated devices certainly leads to loss of reliability due to the high probability of catastrophic failures. In this sense, a device with lower I_{TSM} may not be applicable.

The method proposed in this dissertation for a precise evaluation of the supportability of the power thyristor to a given surge current waveform is composed by two stages, which are described below.

Stage 1: Discrete-time Virtual Junction Temperature Calculation

Convolution integral is the approach considered the reference method for junction temperature calculation. The instantaneous power is calculated for discrete increments throughout the conduction angle, and the temperature rise due to each increment is summed to arrive at the total temperature rise. This is the standard method for providing sine wave ratings for thyristors (Newell, 1976b; Motto, 1993; ABB, 2012):

$$\begin{aligned} T_{vj}(t) &= T_c + \Delta T_{vj}(t) = T_c + P(t) * Z_{th(j-c)}(t) = \\ &= T_c + \int_0^t i(\tau_t) \cdot v(\tau_t) \cdot \frac{d}{dt} Z_{th(j-c)}(t - \tau_t) \cdot d\tau_t, \end{aligned} \tag{3.24}$$

where τ_t is the variable of integration, i and v are respectively the device current and voltage.

However, the integral of (3.24) is not easily applicable to discrete-time simulation results or experimental data recorded. It is proposed in this work that *discrete-time recursive convolution* (DTRC) is applied in this case.

For a signal $x(t)$ applied to a system which impulsive response is $h(t)$, the output $y(t)$ is given by:

$$y(t) = x(t) * h(t). \tag{3.25}$$

If k_z and a_z are constants and:

$$H(s) = \frac{k_z}{s + a_z}, \tag{3.26}$$

[5]The information presented in the data sheet comes from standardized experimental test procedures.

then:

$$h(t) = k_z \cdot e^{-a_z \cdot t} \cdot u(t), \tag{3.27}$$

$$Y(s) = \frac{k_z}{s + a_z} \cdot X(s); \tag{3.28}$$

$$s \cdot Y(s) + a_z \cdot Y(s) = k_z \cdot X(s); \tag{3.29}$$

$$\frac{dy(t)}{dt} + a_z \cdot y(t) = k_z \cdot x(t); \tag{3.30}$$

$$\int_{y(t-\Delta t)}^{y(t)} dy(t) + a_z \cdot \int_{t-\Delta t}^{t} y(t) \cdot dt = k_z \cdot \int_{t-\Delta t}^{t} x(t) \cdot dt. \tag{3.31}$$

Applying trapezoidal integration rule with time step Δt:

$$y(t) - y(t - \Delta t) + a_z \cdot \frac{\Delta t}{2} \cdot [y(t) + y(t - \Delta t)] = k_z \cdot \frac{\Delta t}{2} \cdot [x(t) + x(t - \Delta t))], \tag{3.32}$$

from which one can obtain:

$$y(t) = p_z \cdot y(t - \Delta t) + q_z \cdot x(t) + q_z \cdot x(t - \Delta t), \tag{3.33}$$

where:

$$p_z = \frac{2 - a_z \cdot \Delta t}{2 + a_z \cdot \Delta t}; \qquad q_z = \frac{k_z \cdot \Delta t}{2 + a_z \cdot \Delta t}. \tag{3.34}$$

If the impulsive response $h(t)$ is a sum of n exponential terms, i.e.:

$$h(t) = \sum_{i=1}^{n} k_{z,i} \cdot e^{-a_{z,i} \cdot t}, \tag{3.35}$$

the superposition theorem may be applied:

$$y(t) = x(t) * k_{z,1} \cdot e^{-a_{z,1} \cdot t} + x(t) * k_{z,2} \cdot e^{-a_{z,2} \cdot t} + ... + x(t) * k_{z,n} \cdot e^{-a_{z,n} \cdot t}. \tag{3.36}$$

From (2.10):

$$\frac{d}{dt}Z_{th(j-c)}(t) = \sum_{i=1}^{n} \frac{R_{th(j-c),i}}{\tau_{th(j-c),i}} \cdot e^{\frac{-t}{\tau_{th(j-c),i}}}, \tag{3.37}$$

which has the same form of (3.35). Then from (3.24):

$$k_{c,i} = \frac{R_{th(j-c),i}}{\tau_{th(j-c),i}}; \quad a_{z,i} = \frac{1}{\tau_{th(j-c),i}}; \quad p_i = \frac{2 - a_{z,i} \cdot \Delta t}{2 + a_{z,i} \cdot \Delta t}; \quad q_i = \frac{k_{z,i} \cdot \Delta t}{2 + a_{z,i} \cdot \Delta t}, \tag{3.38}$$

and:

$$\begin{aligned} T_{vj}(t) = T_c + \sum_{i=1}^{n} p_i \cdot [T_{vj}(t - \Delta t) - T_c] + \\ + q_i \cdot i(t) \cdot v[i(t), T_{vj}(t)] + q_i \cdot i(t - \Delta t) \cdot v[i(t - \Delta t), T_{vj}(t - \Delta t)], \end{aligned} \tag{3.39}$$

where i and v are respectively the current through and the voltage drop across the thyristor, and $v[i(t), T_{vj}(t)] \approx v[i(t), T_{vj}(t - \Delta t)]$ can be assumed if Δt is made sufficiently small. The initial conditions are $T_c = 40$ °C and $i(0) = 0$. Case temperature T_c can be assumed constant for events in the range of milliseconds (Wintrich et al., 2015) and considering thermal equilibrium ($T_{vj}(0) = T_c$) before current surge, as previously discussed in Subsection 2.3.2.

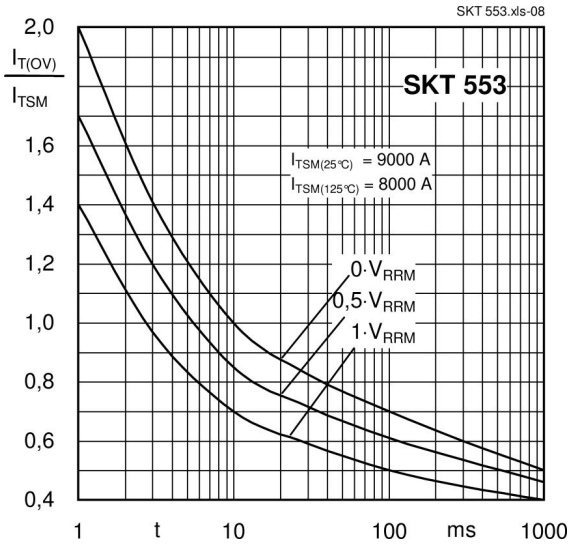
A comparison between (2.15) and (3.39) demonstrates that, in the first case, all the past terms must be accounted for the calculation at any instant, whereas in the second case only the immediately previous term is needed. This reduces the computational cost. The voltage drop across the device can be calculated using (2.17).

For any surge current waveform, (3.39) can be compared to the limiting threshold above which the device reliability is not guaranteed by the manufacturer. This threshold is the *maximum virtual junction temperature* ($T_{vj,max}$) reached for the standard test reported in the data sheet, i.e., a single 50 Hz half-sine wave surge of amplitude I_{TSM} starting at $T_{vj}(0) = 125$ °C.

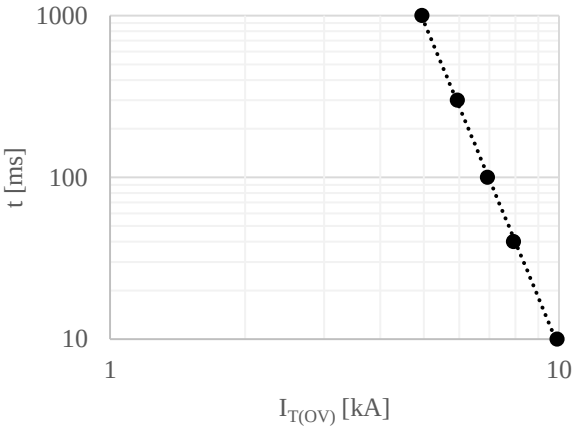
Stage 2: Catastrophic Failure Prediction

The curve previously shown in Figure 2.7b, repeated below for convenience (Figure 3.5a), can be splitted into two parts: subcycle (half-sine wave under 8.33 ms) and multi-cycle (one or more consecutive half-sine waves) events. By reading some points from the curve (see Table 3.1) and plotting them on a chart with both axes in logarithm

scales, one will notice that a linear curve is obtained, as shown[6] in Figure 3.5b. The relative values were read from the curve $0 \cdot V_{RRM}$ and multiplied by 1.1 since the frequency of 60 Hz is of interest in this work instead of 50 Hz. In this case, the values of the abscissa are multiplied by $8.33/10 = 0.833$, since one power-frequency cycle does not correspond to 10 ms (1 half-sine wave at 50 Hz), but 8.33 ms (1 half-sine wave at 60 Hz) instead, i.e., $I_{T(OV)}/I_{TSM} = 1$ for 8.33 ms, not 10 ms.



(a) Original plot (Semikron, 2018).



(b) Log vs. log plot, for $t > 10$ ms.

Figure 3.5 Peak non-repetitive surge current chart for multi-cycle events for part number SKT-553/18E.

Table 3.1 Points selected from Figure 3.5a

t [ms]	10	40	100	300	1000
$I_{T(OV)}$ [kA]	9.9	7.9	6.9	5.9	4.9

Notice that the axes have been swapped from Figure 3.5a to Figure 3.5b. The points in Figure 3.5b can be approximated by a straight line described by:

$$log(t) = -a_r \cdot log(I_{T(OV)}) + b_r. \tag{3.40}$$

The application of the least square regression method leads to:

[6] In this specific case, it was considered the value of I_{TSM} at 25 °C, which is closer of the operational conditions of a thyristor in the AF quenching device than at 125 °C. However, manufacturers usually provide only the value at 125 °C.

$$\begin{bmatrix} -log(9.9) & 1 \\ -log(7.9) & 1 \\ -log(6.9) & 1 \\ -log(5.9) & 1 \\ -log(4.9) & 1 \end{bmatrix} \cdot \begin{bmatrix} a_r & b_r \end{bmatrix} = \begin{bmatrix} log(10) \\ log(40) \\ log(100) \\ log(300) \\ log(1000) \end{bmatrix}. \tag{3.41}$$

Applying the pseudo-inverse, one can easily find the following result:

$$\begin{cases} a_r = 6.693 \\ b_r = 7.643 \end{cases}.$$

Now, (3.40) may be rewritten applying basic logarithm properties as:

$$I_{T(OV)}^{a_r} \cdot t = c_{max}, \tag{3.42}$$

where $c_{max} = 10^{b_r} = 4.39{\cdot}10^7$ is the *maximum dissipation capability* of the device. For a given current waveform composed by half-sine waves of different amplitudes, one can account for the effect of each one as will be demonstrated below.

For a current waveform containing only a half-sine wave of amplitude I_1, the inequation presented in (3.43) must be satisfied so that this waveform can be safely applied without incurring in thyristor catastrophic failure:

$$I_1^{a_r} \cdot 10 \leq c_{max}. \tag{3.43}$$

In other words, any half-sine wave with amplitude not greater than $I_{T(OV)}$ is acceptable.

For a current waveform containing two half-sine waves of amplitudes I_1 and I_2, (3.44) must be satisfied:

$$I_1^{a_r} \cdot 20 + I_2^{a_r} \cdot 10 \leq c_{max}. \tag{3.44}$$

For N half-sine waves[7] of amplitudes I_1, I_2, I_3, ..., I_N:

$$(I_1^{a_r} + I_2^{a_r} + I_3^{a_r} + \cdots + I_{N-1}^{a_r}) \cdot 20 + I_N^{a_r} \cdot 10 \leq c_{max}. \tag{3.45}$$

Based on the description given above, the impact of each current half-sine wave on the device's *dynamic energy dissipation* $c_d(t)$ is calculated according to:

[7] See Figure 2.7a again.

$$c_d(t) = \sum_{i=1}^{n} I_i^{a_r} \cdot 1, \tag{3.46}$$

where I_i is the peak value of the i^{th} current half-sine wave, n is the number of current half-sine waves that will circulate through the device during the surge and a_r is a constant obtained from the application of mathematical manipulation to the multi-cycle current surge capability curve given by the manufacturer in the data sheet, as explained earlier in this section. The constant '1' means that one half-sine wave is considered at a time. If the frequency of the current surge is 50 Hz, then '1' corresponds to one half-sine wave of 10 ms. If the current surge is at 60 Hz, then the '1' is related to one half-sine wave of 8.33 ms[8]. For any surge current waveform, the result of (3.46) can be compared to the limiting threshold above which the device reliability is not guaranteed by the manufacturer. This threshold is given by $c_{max} = 10^{b_r}$, where b_r is a constant obtained from the data sheet as demonstrated above in this section. Notice that c_d calculated in (3.46) has the unit of $[\mathrm{A}]^{a_r}\cdot[\mathrm{s}]$, which can be interpreted as:

$$[A]^{a_r} \cdot [s] = [A]^{2+a_r-2} \cdot [s] = ([A]^2 \cdot [A]^{a_r-2}) \cdot [s] = ([A]^2 \cdot [s]) \cdot [A]^{a_r-2}. \tag{3.47}$$

The first term of the right-side of (3.47) is the energy per unit resistance (Joule integral) that the device will be subjected to during one half-sine wave, while the second one can be considered as a factor that depends on the value of the constant a_r. The greater the value of a_r, the higher the value of the factor and consequently the higher the contribution of the Joule integral to $c_d(t)$. This is physically in accordance with reference (Motto, 1971), which suggested that since peak current I_{TSM} versus time curves are nonlinear functions, the dissipation capability of a device varies as to the $\sqrt{t}$ for the first tens of milliseconds of the thermal response and, in effect, the measure of a device's energy capability would be closer to $I_{TSM}^2 \cdot \sqrt{t}$ instead of $I_{TSM}^2 \cdot t$.

The technique of Stage 2 is based exclusively on information contained in the data sheet and is applicable to waveforms composed by a combination of ac surges not necessarily with the same amplitudes. Additionally, this procedure does not depend on the calculation of the virtual junction temperature, which is not even measurable, but rather estimated. This is an advantage over the technique proposed for the Stage 1.

[8]Up to (3.45), the method treated here has been developed using time as the independent variable, as it is often presented in the data sheets. However, this can cause confusion because one half-sine wave at 50 Hz corresponds to a time interval different than at 60 Hz. Therefore, it is better to represent the number of half-sine waves instead of the time. This will be done hereinafter.

However, Stage 2 has the disadvantage that it has assumed that the current surge is composed by perfectly sinusoidal half-cycles. This is not true especially for current profiles containing high-amplitude dc components. Figure 3.6 illustrates the difference between a pure 60 Hz sinusoidal waveform and a characteristic 60 Hz bolted short-circuit current waveform composed by ac and dc components. The waveforms have the same amplitudes over time.

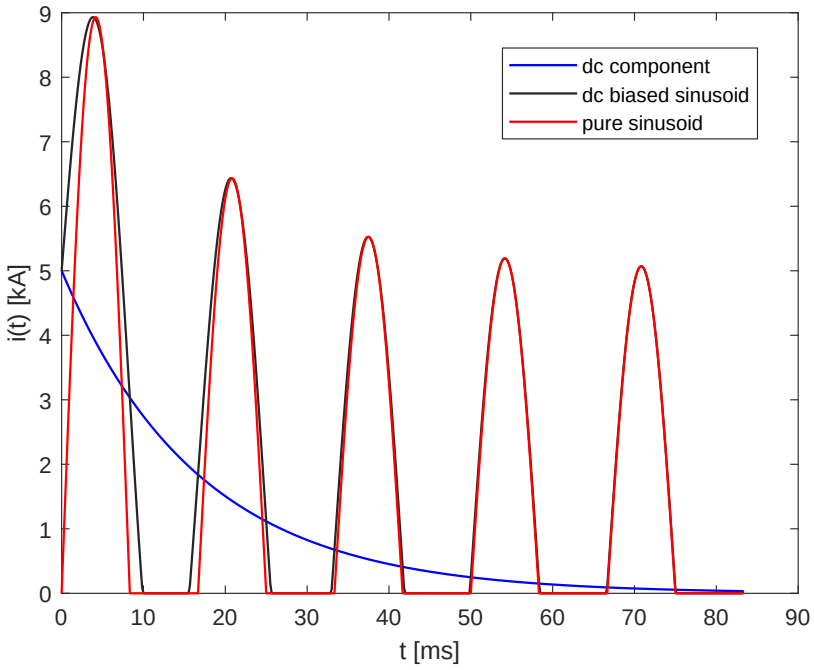


Figure 3.6 Comparison between same amplitude, same frequency pure sinusoid and sinusoid with dc level.

Application of the Method

The two-stage method described above is advantageous over other techniques because:

- Stage 1 inherently considers any dc level present in the current waveform since it is an instantaneous calculation. Moreover, it allows the computation of the real initial junction temperature.
- Stage 2 yields to a conservative result since it implicitly considers that the current waveform is purely sinusoidal and the initial junction temperature is 125 °C.
- Stages 1 and 2 can be applied in a cooperatively way for the selection of thyristors for a given application whenever the data sheet provide enough information.

However, some manufacturers do not provide the multi-cycle current surge capability curve, turning the calculation of Stage 2 unfeasible. In contrast, other manufacturers do not provide the device voltage drop curve at 25 °C. Unless the user is prone to test the device in such conditions, which is hard to accomplish due to the need of a high current source and temperature control, the application of Stage 1 is impracticable since the strong dependence of the device voltage drop on the value of T_{vj} cannot be accounted for. In these cases, only Stage 1 or Stage 2 can be employed. In this work, both stages will be used whenever possible.

Additional Considerations for the Specification of the Device

Since there are a great number of thyristor manufacturers worldwide, which offer a vast range of products[9] for a given class of power device, the designer must take into account variables like cost and lead time besides the technical concerns that are being discussed in this work. Moreover, there are other types of power thyristors other than PCT[10] that can be considered for the AF quenching device application, namely PPT and BCT. PPT has been specially designed for increased rate of change and peak current capability, as well as reduced forward voltage drop (Semi, 2019; Hoffman et al., 2003), which is achieved due to its high interdigitated gate structure. These devices have been used as crowbars to protect high power circuitry in railway propulsion units for many years (Semi, 2019). BCT has two anti-parallel monolithically integrated onto one single silicon wafer and assembled into one housing, enabling compactness and increased reliability. Each half thyristor performs like the corresponding full-wafer thyristor in respect to its static and dynamic properties. BCTs are designed with a focus on avoiding harmful cross coupling effects under all relevant operating conditions (Thomas et al., 1998; ABB, 2013; Vobecky, 2020). These options will be compared to each other in the next chapter, in light of the method proposed in this section.

Regardless of the device type, fast transient circuit conditions can cause thyristors to turn on in the absence of the trigger signal. Due to the nature of thyristor construction, a small capacitor is formed across each PN junction. When voltage is impressed suddenly across a PN junction, a charge current flow. If this current becomes greater than gate trigger current (I_{GT}), the thyristor switches on. Normally, this type of

[9] In general, the manufacturers update their catalogs on an annual basis.

[10] The acronyms PCT, PPT and BCT have already been defined in Subsection 1.5. They stand for phase-control, pulse-power and bi-directional control thyristors, respectively.

turn-on does not damage the device. To avoid such false triggering[11] from a high rate of rise of the voltage across the device (dv/dt) or eventual transient overvoltages (e.g., provoked by lightning), a snubber circuit (normally a passive, series RC) is inserted across the switch. Since the RC branch is connected in parallel with the thyristors, then it does not constitute a critical path to the quenching device operation. Both an open-circuit resultant from resistor failure and a capacitor short-circuit failure would lead to no commitment of thyristor fail-safe mode, although the quenching device becomes susceptible to spurious triggering in this case. The monitoring of the current in this RC branch, as it is done in transformer neutral grounding resistor applications, for example, consists on a simple, safe solution that can be incorporated to the measurement and control system of the AF quenching device in the future.

The RC snubber makes up a resonant circuit with the inductive RL shunt impedance. At turn-off, the snubber circuit limits the slope of the reapplied voltage but generates an overvoltage. Such overvoltage must be low enough not to lead to the reignition of the arcing fault during commutation from one thyristor to its anti-parallel counterpart. There is an unintentional dead time between the natural commutation of one thyristor and the turn-on of the other. The lower the gate-driver triggering frequency, the larger is this interval. Therefore, there is a design trade-off to be considered: low $(dv/dt)_{off}$ requires high C and low R, while low $(di/dt)_{on}$ requires low C and high R. In addition, low R and high C leads to higher current through the snubber during steady-state operation. The combination of values having highest resistance and lowest capacitance that provides satisfactory operation is generally preferred (Semiconductor, 2006; Microelectronics, 2007; Littelfuse, 2013).

3.3 Summary

In this chapter, a proposition for the design of the main elements of the AF quenching device has been developed. It has been shown that the design has to be done by means of a multi-task procedure, which starts by choosing the model of arcing fault register that best represents the switchgear (or MCC) considered (the busbar clearances play an important role in this sense), the detailed modeling of the feeding power system (the maximum voltage, including overvoltage conditions, and the minimum equivalent impedance and possible variations over the time), the complete electrical model of the

[11] In the AF quenching device, avoiding a false positive operation due to a spurious turn-on is important to prevent undesired operational consequences, including the depreciation of the device itself.

thyristors (including the dependence of its terminal behavior on the virtual junction temperature) and the shunt impedance (including its X/R ratio), besides the arcing fault starting angle and other active and nonlinear loads that may be connected to the system. Simulation and experimental results will be provided in the next chapter to validate the proposals.

Chapter 4

Results

"Big changes, big headaches."
Ken Box, Protection Engineer - Schneider Electric

The main goal to be achieved in this chapter is the validation of the propositions presented in this dissertation for the design / specification of the elements of the electronic AF quenching device. Innovative contributions are achieved on the arcing fault elimination process. Both simulation and experimental results will be presented, as well as the methods used to implement and execute them. The chapter is divided into 4 parts:

1. Preliminary simulation results: it covers separate analysis on each one of the essential parts of the system, i.e., the arcing fault, the shunt impedance and the power thyristors.

2. Simulation focused on the power thyristors: some part numbers from different manufacturers, ratings and types were grouped and their behavior under high-current surges have been evaluated and compared.

3. Complete simulation results: the different parts previously studied were joined together to allow the evaluation of the interaction between them and the effectiveness of the quenching device under various operational circumstances.

4. Experimental results: the first half of the section presents results particular of the thyristor behavior, while the second half treats the tests of a full-scale prototype with the elimination of real internal arcing fault events.

The discrete-time modeling previously presented in Chapter 3 is fully explored for obtaining the simulation results using essentially charts from Microsoft Excel spreadsheets, scripts prepared in MATLAB and simulations executed in ATPDraw, which were developed using the *Transient Analysis Control Systems* (TACS) package of the software.

4.1 Preliminary Simulation Results

The main objective of this section is to perform a separate, simulation-level evaluation of the elements studied in this dissertation: the arcing fault, the shunt impedance and the power thyristors. This evaluation give support for the subsequent integration of these elements, which will be given in a following section of this chapter.

4.1.1 Arcing Fault

This subsection demonstrates the modeling of an arcing fault register from IEEE-NFPA data set.

IEEE-NFPA Arc-Flash Data Set Modeling

The group of four tests listed in Table 2.1 have been modeled into ATPDraw. First, the parameters of the electrical power system have been derived from the available symmetrical current and *power factor* (PF), according to:

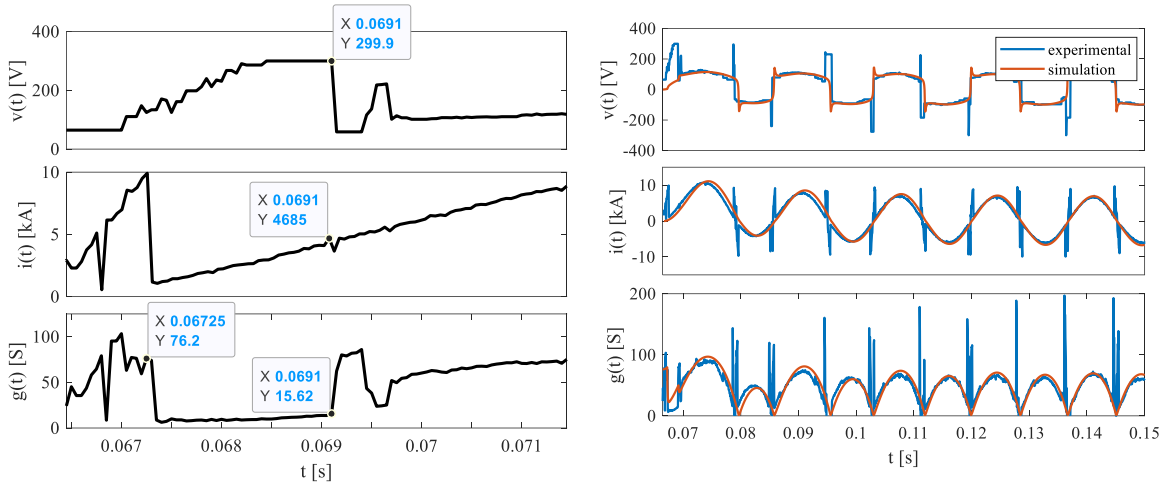
$$\frac{V_{oc}}{I_{sc}} = |\dot{Z}_S| = \sqrt{R_S^2 + X_S^2}; \tag{4.1}$$

$$PF = \frac{R_S}{|\dot{Z}_S|}, \tag{4.2}$$

where V_{oc} is the open-circuit voltage (480 V), I_{sc} is the available symmetrical current, $\dot{Z}_S$ is the equivalent impedance of the electric power system and PF is its power factor.

The second step was the calculation of the parameters of each arcing fault according to Section 2.2. The value of ℓ is equal to the gap length, while the values of V_O and R_O have been calculated according to (2.5) and the value of τ has been obtained according to (2.8). The value of $G_{min,\ell}$ of (3.2) was considered to be the free-air conductance between the conductors. A reference value of 10 nS/m at 20 °C has been adopted according to (Kamsali et al., 2011). For a gap length of 25 mm, $G_{min} = 250$ pS.

The value of $G_{min,h}$ has to do with the increase in the fault path conductance due to the conditions produced by the melting of the thin copper wire inserted between the conductors before the beginning of the experiment. Figure 4.1a shows the voltage and current waveforms registered during the beginning of test #63 and calculated conductance. The interval can be divided into 3 parts: (i) solid copper (up to 67.25 ms) – low voltage, high current and high conductance; (ii) melted copper and forming plasma (from 67.25 ms to 69.10 ms) – increasing voltage, low current and low conductance; and (iii) established arcing path (from 69.10 ms on). As one can notice, the strike voltage was 299.9 V. Based on these considerations, $G_{min,h}$ and $t_{min,h}$ have been adjusted so that the voltage at which the arcing fault starts in the simulation matches the experimental waveform. For the case shown in Figure 4.1a, a good approximation is given by $G_{min,h} = 15.6$ S and $t_{min,h} = 69.1$ ms.



(a) Values registered at the beginning.

(b) Experimental vs. simulation.

Figure 4.1 Arc-flash voltage, current and conductance - experimental and simulation results - test #63.

Table 4.1 summarizes the values calculated for the parameters of the experiments considered in this section. The procedure previously described in Subsection 2.2.1 has been used. Variable t_t represents the time at which the recording has been started in the experiment. It has been directly read from test data and reproduced into the simulation.

Figure 4.1b shows the comparison between simulation and experimentally obtained waveforms for arc voltage, current and conductance of test #63. To preserve the originality of the experimentally obtained signals and to avoid any undesired attenuation or time delay effect, the curves obtained by measurement were not filtered. For this

Table 4.1 Parameters calculated from the waveforms of the arcing tests adopted in this work

Parameter	***Test***			
	#67	**#68**	**#65**	**#63**
$\dot{Z}_S$ [mΩ]	1.66 + j22.1		3.24+j95.4	
ℓ [mm]	25	10	25	10
V_O [V/mm]	4.189	11.65	4.462	7.476
R_O [$\mu\Omega$/mm]	187.0	391.5	132.1	357.8
τ [μs]	236.0	340.6	161.2	39.67
$G_{min,\ell}$ [pS]	25	10	25	10
$G_{min,h}$ [S]	7.77	7.77	12.3	15.6
$t_{min,h}$ [ms]	49.7	49.7	60.6	69.1
t_t [ms]	48.9	48.9	57.8	66.5

reason, noise is observed in it. The transient peak observed at the zero crossing of the measured signals has to do with the reignition voltage of the arc. Once the current becomes null during voltage zero-crossing, the arc voltage starts increasing and its conductance during this short interval is very small. When it reaches the reignition voltage, the current and the conductance increase and rapidly decrease to the burning voltage value, as reported in (Ammerman and Sen, 2007).

Appendix B presents a parametric analysis on the model of test #67.

4.1.2 Shunt Impedance

This subsection presents a preliminary investigation on the effects of inserting a shunt impedance (called here Z_x) in series with the ac switch, as previously shown in Figure 3.4. The impact will be evaluated initially by simulation in ATPDraw and then a calculation procedure will be explored by means of a code developed in MATLAB.

Impact Evaluation

Single-phase-to-ground fault #67 has been simulated again, but now including an impedance as the current-limiting element. The feeding power system is 220 / 127 V and its series equivalent Thévenin impedance is formed by a resistance of 9.9 mΩ and an inductance of 30.7 μH per phase[1]. The thyristor that was considered in the AF quenching device is the part number SKT-553/18E from Semikron, using simply the

[1]These values represent the equivalent impedance at the point of connection available in the laboratory, which will be detailed in Subsection 4.4.1.

fixed parameters $r_T = 450\ \mu\Omega$ at $T_{vj} = 125\ ^\circ\text{C}$ and $V_T = 1.65$ V at $T_{vj} = 25\ ^\circ\text{C}$ / $I_T = 1.5$ kA from the data sheet. The discrete-time model of the arcing fault, represented by (3.1), has been added to the system shown in Figure 3.4 in the form of a TACS-controlled variable - see Figure 4.2, and the simulation has been performed directly in ATPDraw considering a phase-to-phase arcing fault since it is the worst scenario for the effectiveness of the quenching device. Figures 4.3 and 4.4 show bus voltage and quenching device current for four cases: 10% (Figure 4.3a), 20% (Figure 4.3b), 40% (Figure 4.4a) and 80% (Figure 4.4b) of the equivalent power system reactance[2]. The impedance is assumed to be a reactor with an equivalent series resistance of 1 mΩ. For all cases, the operation of the quenching device has been intentionally delayed so that the arcing fault period can be better visualized. Notice that in the three first cases the bus voltage is not high enough to the reignition of the arcing path. In the fourth case, though, the fault restarts when the ac switch current reaches zero.

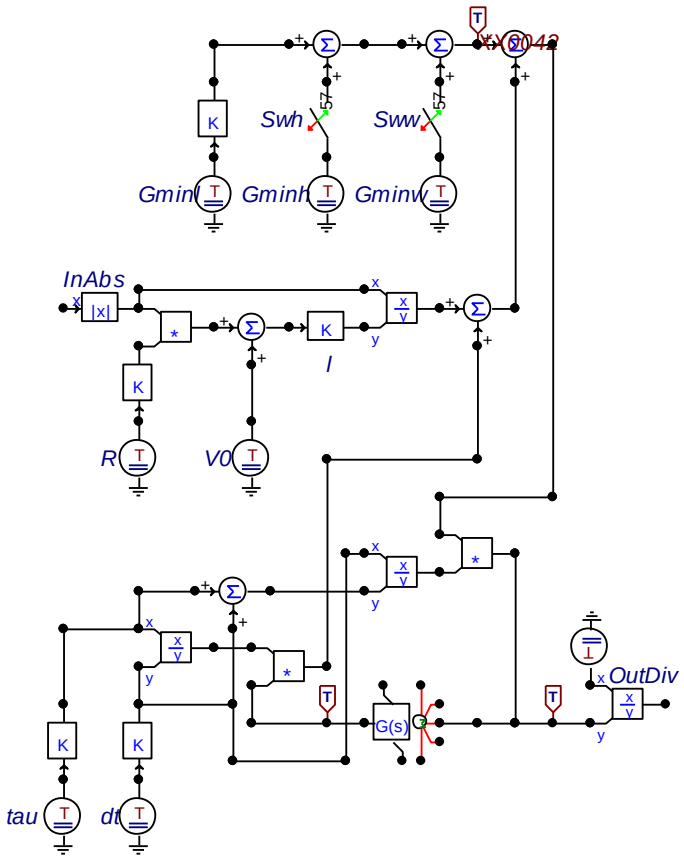
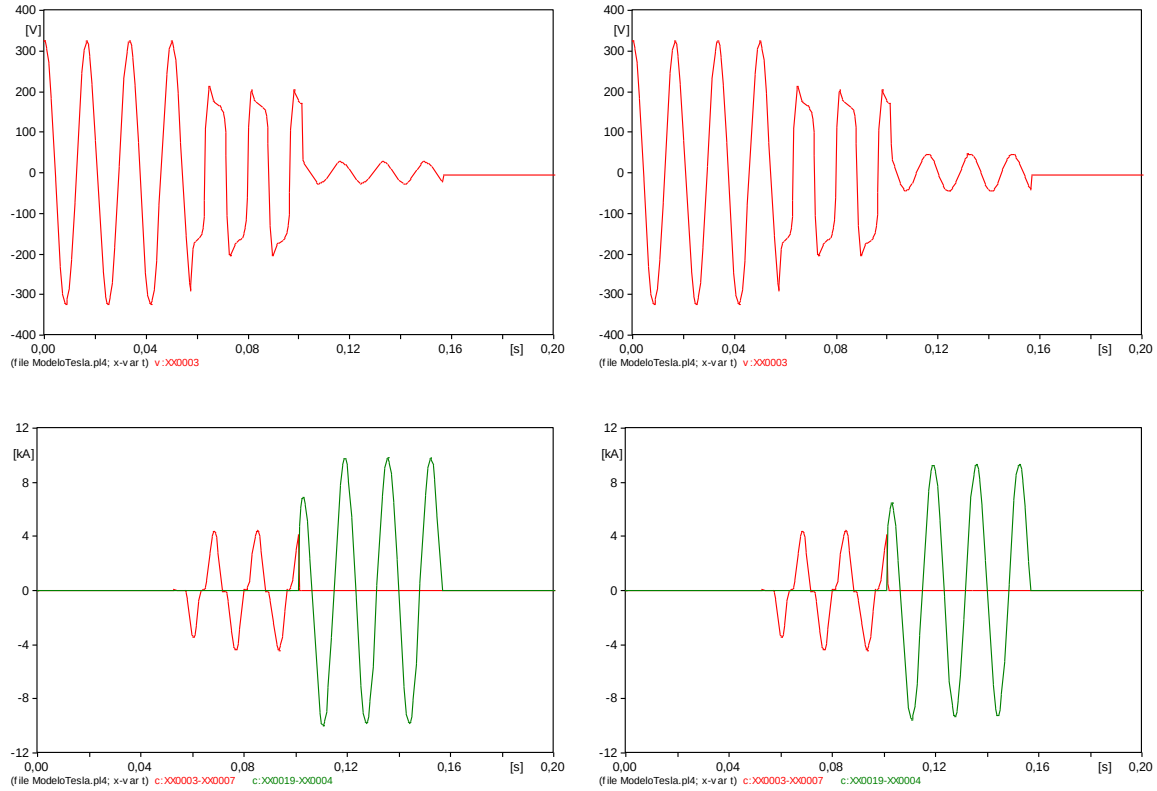


Figure 4.2 Discrete-time implementation of the arcing fault model in ATPDraw.

[2]Which is considered to be equal to $2 \cdot 30.7\ \mu\text{H} = 61.4\ \mu\text{H}$ in this case, since there are two phases involved.



(a) For Z_S with 6.14 μH and 1 mΩ.

(b) For Z_S with 12.3 μH and 1 mΩ.

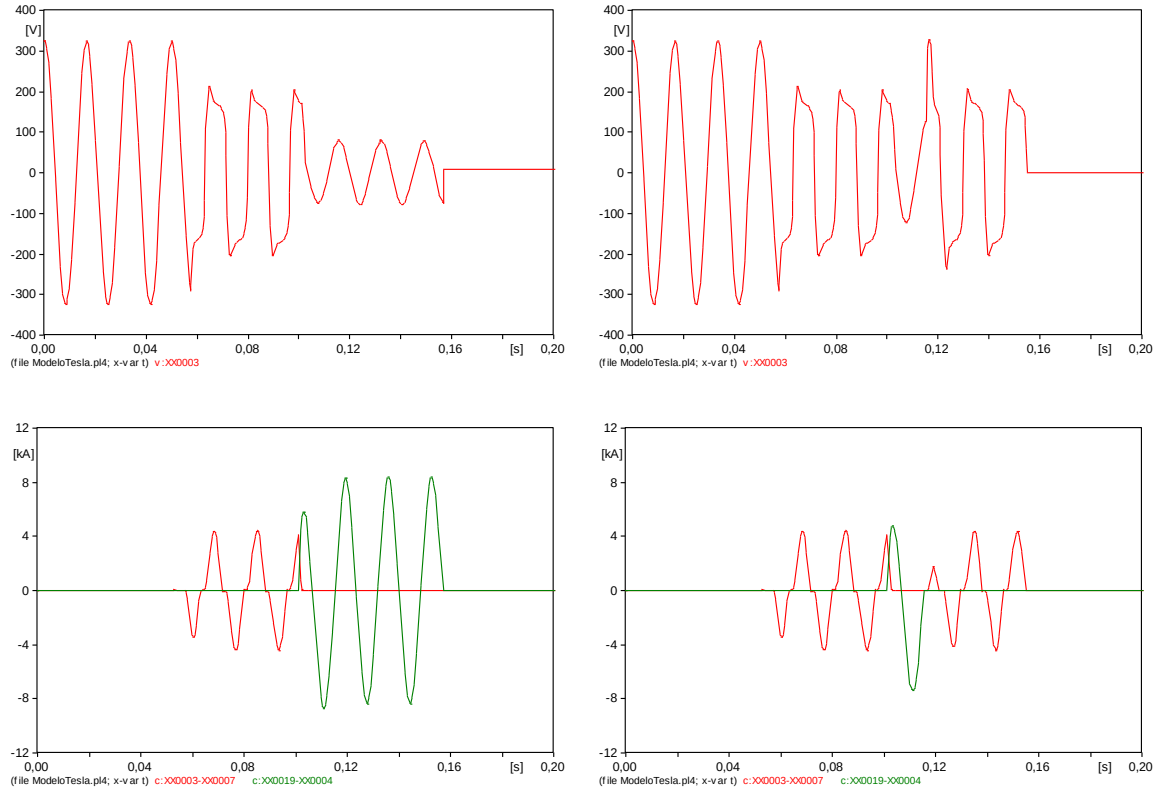
Figure 4.3 Voltage across the arc (top chart) and currents through the arc (bottom chart, red) and through the quenching device (bottom, green).

The calculation of the maximum admissible impedance will depend on the specific system parameters, the worst instant for fault starting, etc.

Practical Example

The arc-flash trial #67 will be used along with the original electric power system used for the test (see Table 2.1 again). The X/R ratio is 13.3, which is much higher than the ratio of 1.17 of the system formerly assumed in this section. The nominal voltage is 480 V and the symmetrical, RMS short-circuit current is 20 kA.

Before proceeding to the study that will be presented in this subsection, it is important to point out that a MATLAB code has been developed to calculate and plot the instantaneous values of current, power, energy and joule integral on the AF quenching device given the parameters of a generic single-phase power system, of the resistive (with constant resistance) fault (resistance and starting angle) and of the quenching device - essentially the resistance of the thyristors and the reactance and the



(a) For Z_S with 24.6 μH and 1 mΩ.

(b) For Z_S with 49.2 μH and 1 mΩ.

Figure 4.4 Voltage across the arc (top chart) and currents through the arc (bottom chart, red) and through the quenching device (bottom, green).

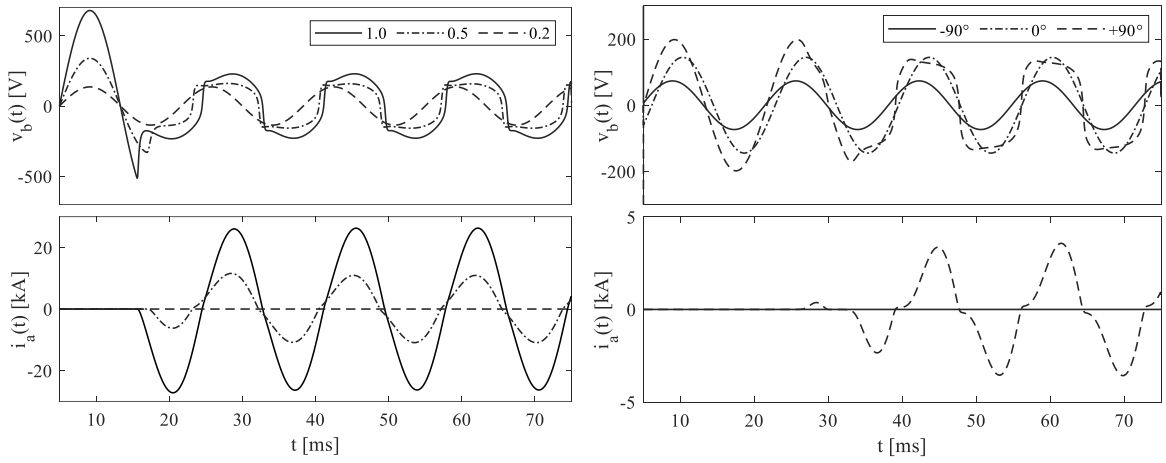
equivalent series resistance (ESR) of the shunt impedance. Such simulation has been executed to reproduce the effects of the current commutation, dc-level peak current and other important effects before proceeding to the analysis including the model of the arcing fault. Since the results achieved by this simplified analysis do not involve any novelty beyond simple electrical circuit analysis, they will not be discussed here.

Relevant results on the simulation of the system illustrated by Figure 3.4 are presented below. Only operation mode will be considered in this section, with $t_S = 5$ ms, $R_{bl} = 12$ kΩ and $R_{cd} = 110$ $\mu\Omega$. The sampling time of 50 μs has been adopted for the simulations, to preserve the compatibility with the arc-flash measurement[3]. Figure 4.5a presents bus voltage v_b and arc current i_a for intervals 1 and 2 described in Subsection 3.2.1, for $t_a = 15$ ms, $I_M = 0$ and progressively increasing values of supply voltage amplitude V_S (1.0 p.u., 0.5 p.u., and 0.2 p.u.).

[3]ATPDraw has an intrinsic time delay between variables calculated by TACS and the power system, but this is not a concern since the sampling time is low enough for the frequency range being studied (Kizilcay and Pniok, 1991).

It was noticed that there is no arcing fault only if V_S is equal to or below 0.2 p.u. of rated value (480 V), which results in peak bus voltage of 135 V. It is important to observe that when the arcing fault starts, the X/R ratio of the mesh composed by Z_S and g_a is low due to the resistive characteristic of the fault, but still enough to result in dc level at i_a. This produces proportionally higher bus voltage. Fortunately, this is not a concern from the quenching device design point of view, since it will be calculated to guarantee[4] $v_b < 135$ V.

Figure 4.5b presents v_b and i_a for $V_S = 0.2$ p.u. and $I_M = 2$ kA RMS with notable displacement angles with respect to V_S: -90°, 0, and +90°. The verified peak bus voltage is 73.5 V, 144 V, and 198 V respectively. For +90°, the arc occurs. It means that a load, especially with capacitive characteristic, may contribute to increase the bus voltage. The effect of I_M can be better understood by observing that[5] during Step 2, the current I_M has a preferential route throughout the power supply branch instead of the arc branch, since $Y_S = 1/Z_S$ is substantially higher than g_a. Hence, the contribution of I_M to the bus voltage can be calculated by applying the superposition theorem to the mesh composed by I_M and Z_S when the voltage source V_S is deactivated, i.e., the contribution is equal to $\dot{Z}_S \cdot \dot{I}_M$.



(a) $I_M = 0$ and various amplitudes for V_S. (b) $V_S = 0.2$ p.u. and various angles for I_M.

Figure 4.5 Single-phase bus voltage v_b and arc current i_a for intervals 1 and 2, with t_a = 15 ms.

These results show that keeping the bus voltage below 135 V during Step 3 is enough to guarantee no arcing fault (at least for the specific fault adopted in this

[4]Up to the date these results have been achieved, IEC 60947-9-1:2019 (Commission, 2019), which requires $v_b < 34$ V, was not published yet.

[5]See Subsection 3.2.1 again.

study), even if it starts with dc level at current and / or under influence of any type of load. To keep the bus voltage below 135 V, it is necessary that the voltage divider constituted by Z_S and $Z_x + R_{cd}$ comply with (4.3):

$$\left| \frac{Z_x + R_{cd}}{Z_S + Z_x + R_{cd}} \right| \cdot V_S < 135, \tag{4.3}$$

where $V_S = 1.1 \cdot 480 \cdot \sqrt{2} \approx 747$ V. Assuming $X_x/R_x = 5$ and solving for L_x, one will obtain $L_x < 12.6$ μH and $R_x < 950$ $\mu\Omega$. Notice that this result makes the impedance of the branch Z_x much lower than Z_S, turning the quenching device branch into the preferential path for the current I_M. Now, the application of the superposition theorem must be done to find the bus voltage increase due to the current source I_M. The product $(\dot{Z}_x // \dot{Z}_S) \cdot \dot{I}_M$ is calculated. If this contribution does not result in $v_b > 135$ V, then the design of the current-limiting impedance is finished. Else, Z_x must be decreased. The effect of a linear load Z_l in parallel with I_M would turn the calculation into $(\dot{Z}_x // \dot{Z}_S // \dot{Z}_l) \cdot \dot{I}_M \approx (\dot{Z}_x // \dot{Z}_S) \cdot \dot{I}_M$ since $Z_l >> Z_S$.

Right before the instant t_x at which the quenching device starts operating, the current through Z_S is equal to $i_a(t_x^-) - i_M(t_x^-)$. Since the current $i_x(t_x^+)$ throughout the device is equal to $i_x(t_x^-)$, the highest dc component $i_{x,dc,max}$ that can take place in the quenching device current occurs at t_x^+ and its initial amplitude $i_{x,dc,max}$ is given by:

$$i_{x,dc,max} = |i_{x,sym}(t_x^-) - [i_a(t_x^-) - i_M(t_x^-)]|, \tag{4.4}$$

where $i_{x,sym}(t_x^-)$ is the instantaneous symmetrical current that would circulate through the mesh formed by V_S, Z_S and Z_x, which can be calculated by:

$$i_{x,sym}(t_x^-) \approx \frac{V_S}{|\dot{Z}_S + \dot{Z}_x| \cdot sin(\omega \cdot t_x^- - \phi_{\dot{Z}_S + \dot{Z}_x})}, \tag{4.5}$$

where ω is the angular frequency of the power supply, V_S is its amplitude and ϕ is the angle of $Z_S + Z_x$. The value of $i_a(t_x^-) - i_M(t_x^-)$ depends on the exact parameters of g_a and I_M and the exact time instant t_x at which the quenching device is triggered. One of the greatest advantages of the electronic arc-flash quenching device is its fast operation after the fault detection (≈ 2 ms). It means that the arcing fault current starts from zero and does not reach its peak value. For a stiff power system, i.e., high short-circuit ratio (> 20), and since $|i_M(t_x^-)|$ is a normal load current, it is reasonable to consider therefore $i_{x,sym}(t_x^-) >> [i_a(t_x^-) - i_M(t_x^-)]$. This simplification makes the calculation feasible. In this condition, the worst case scenario happens for the time instant t_x, where $i_{x,sym}(t_x^-)$ is maximum, i.e.:

$$t_x^- = \frac{\phi_{\dot{Z}_S+\dot{Z}_x} + \pi/2}{\omega}. \tag{4.6}$$

For the system considered in this work, $\phi_{\dot{Z}_S+\dot{Z}_x}$ = 1.47 rad, ω = 377 rad/s and t_x^- = 8.1 ms. It means that the operation of the quenching device exactly 8.1 ms after the zero crossing of the supply voltage leads to the worst dc level in the quenching device current if $i_a(t_x^-) - i_M(t_x^-) \to 0$. For L_x = 12.6 μH, R_x = 950 $\mu\Omega$, $V_S = 1.1 \cdot 480 \cdot \sqrt{2}$ V, I_M = 0 and $i_a(t_x^-) = 0$, $i_{x,dc,max} = i_{x,sym}(t_x^-)$ = 27.7 kA. The peak current through the quenching device would be given by:

$$i_{x,max} = i_{x,dc,max} \cdot [1 + e^{-[(1/60)/2]/(L_t/R_t)}], \tag{4.7}$$

where $L_t = L_S + L_x$ and $R_t = R_S + R_x$, resulting $i_{x,max}$ = 48.1 kA.

Figure 4.6 presents the solution of the system for I_M = 0 and for I_M = 2 kA RMS (short-circuit ratio = 10) with the following displacement angles with respect to V_S: -90°, 0°, +90° and +180°. Since V_S starts from zero at 5 ms, t_x = 5.0 + 8.1 = 13.1 ms was selected. To make the result accurate, it was considered that the arcing fault has started at 13.1 – 2.0 = 11.1 ms. It can be concluded from the results that $i_a(t_x^-) - i_M(t_x^-) \neq 0$ has a marginal impact on the peak current through the quenching device. The worst case is i_S = -48.5 kA, for +90°. Both contributions from arc and motor did not produce any impact on the effectiveness of the quenching device.

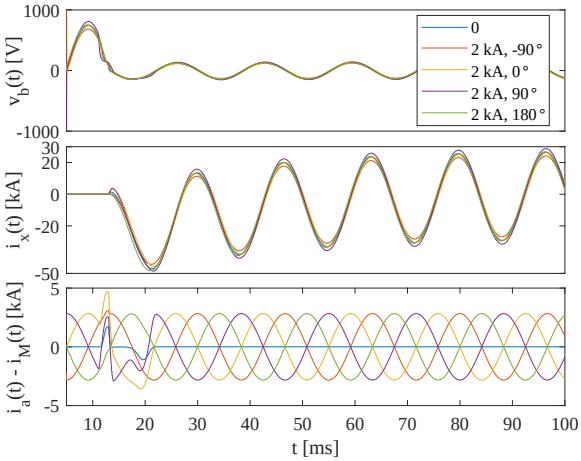


Figure 4.6 Bus voltage v_b, quenching device current i_x and difference between arc and motor currents ($i_a - i_M$) for various values of I_M.

Two comments are very important to be made at this point: first, it is expected that the fault current has not significant dc level since the arcing path is essentially resistive. It was verified in all the simulation results presented in this subsection. This

is important since a dc level at fault current could increase the bus voltage, hampering the quenching procedure. Second, the current through the quenching device presents dc level, and therefore the shunt impedance must be designed to support the corresponding electrodynamic forces, and the thyristors must be selected taking this current profile into account as well.

4.1.3 Power Thyristors

In this subsection, it is presented the determination of the coefficients for the transient thermal impedance and voltage drop of a commercially available thyristor part number and then some results on the calculation of its virtual junction temperature and catastrophic failure prediction.

Commercially Available Thyristor Modeling

Semikron's part number SKT-553/18E (Semikron, 2018) has been modeled according to (2.10) and (2.17). The parameters were determined using the curve fitting tool of MATLAB (cftool). Table 4.2 and Table 4.3 show the obtained constants[6]. Figures 4.7b and 4.8a present the comparison between the original and the adjusted curves.

Table 4.2 Numeric coefficients for the transient thermal impedance curve of thyristor SKT-553/18E

i	1	2	3	4
$R_{th(j-c),i}$ [mΩ]	1.75	5.07	28.0	110
$\tau_{th(j-c),i}$ [ms]	0.708	11.8	378	2360

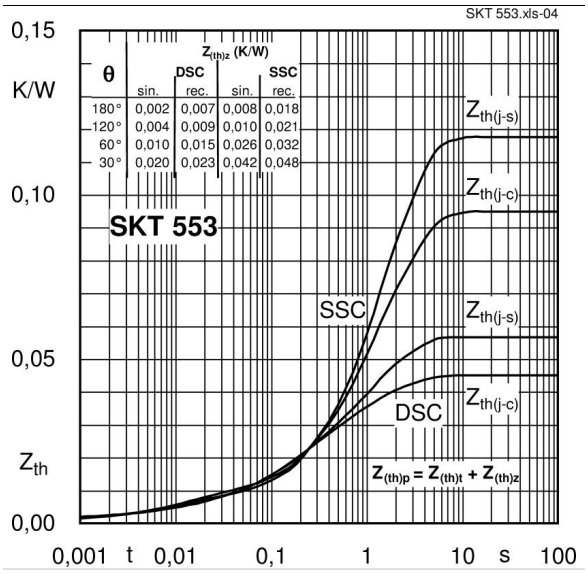
Table 4.3 Coefficients for current- and temperature-dependent voltage drop calculation of the thyristor SKT-553/18E

A	a_v	C	c_v	k_v	D	d_v
0.96	-2.21 $\cdot 10^{-3}$	1.08 $\cdot 10^{-4}$	-7.99 $\cdot 10^{-5}$	-9.35	1.38 $\cdot 10^{-2}$	4.95 $\cdot 10^{-5}$

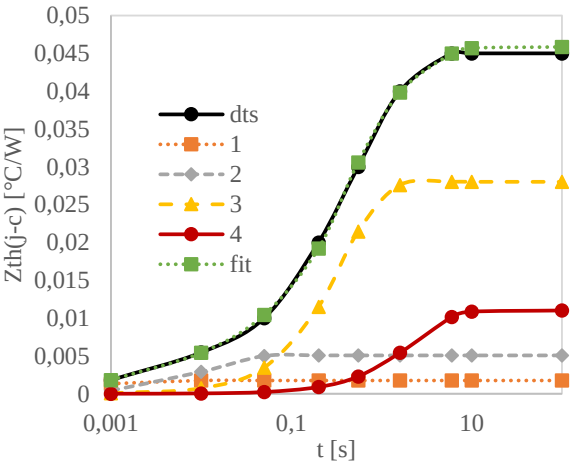
Thyristor Virtual Junction Temperature Calculation

The results produced by the application of the discrete-time recursive convolution method will be compared to the ones given by the *equivalent power pulse* (EPP) method.

[6] Coefficient of determination $R^2 = 0.9981$.

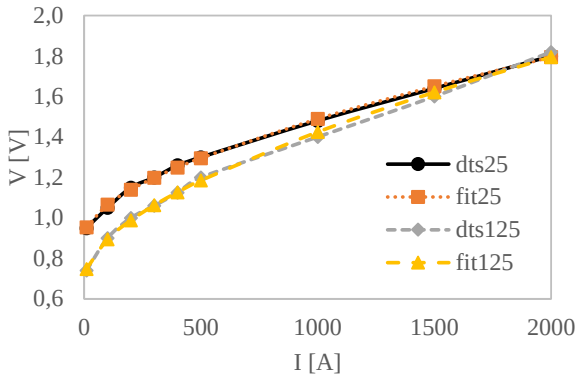


(a) Original.

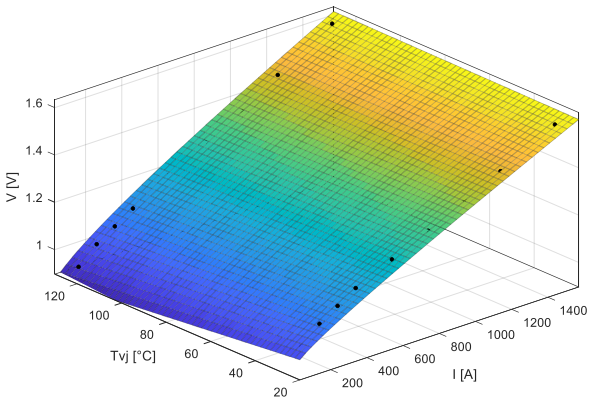


(b) Plotted from points read from the data sheet (dts) and from (2.10) (fit) using coefficients (from $i = 1$ to $i = 4$) shown in Table 4.2.

Figure 4.7 Transient thermal impedance curve of thyristor SKT-553/18E.



(a) Points directly read from data sheet (dts25 and dts125) and points obtained by using (2.17) with coefficients of Table 4.3 (fit25 and fit125), at 25 °C and at 125 °C.



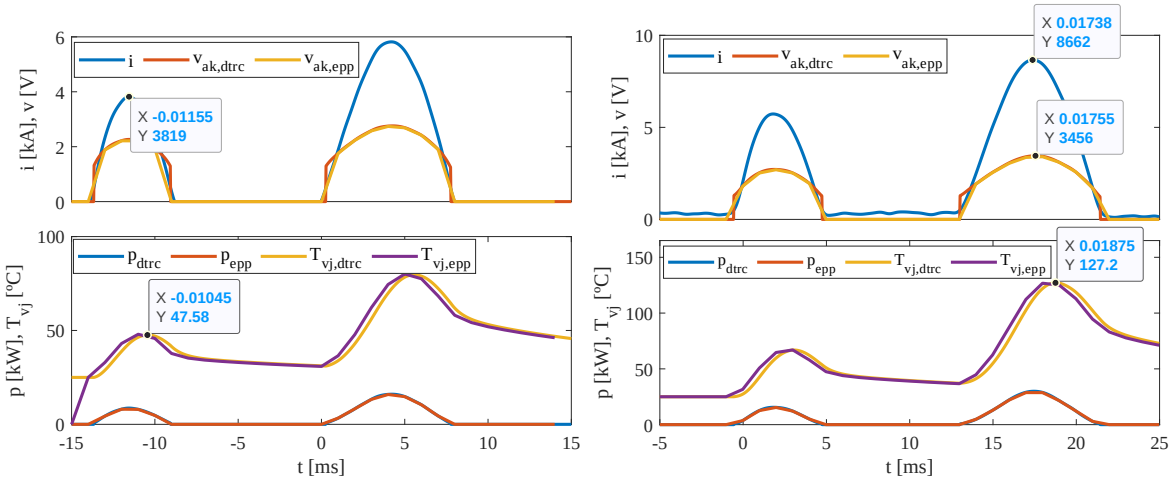
(b) Curve fitting obtained with cftool.

Figure 4.8 Voltage drop of thyristor SKT-553/18E.

A code has been implemented in MATLAB to execute this task. Two double-cycle 60 Hz current waveforms will be considered for the simulations: one with amplitudes of 4.0 kA and 6.0 kA and the other with amplitudes of 5.7 kA and 8.7 kA. These two current profiles will be called respectively surge #3 and surge #4.

Figure 4.9a presents the comparison between calculated voltage drop, power and virtual junction temperature for surge #3. The sample time is 25 μs. Discrete-time

recursive convolution was computed using this time interval. For the equivalent power pulse calculation, the simulation was performed considering rectangular power pulses with duration of 1 ms. The initial virtual junction temperature is $T_{vj}(0) = T_c = 25$ °C. As one can notice, the difference between the results is practically negligible. Figure 4.9b shows the results obtained for surge #4. Again, no significant difference can be noticed between the results.



(a) Surge #3. (b) Surge #4.

Figure 4.9 Voltage drop, power and virtual junction temperature calculated for a thyristor SKT-553/18E submitted to multi-cycle current surges, using DTRC and EPP methods. Voltage data tips are in mV.

Catastrophic Failure Prediction

The results presented in this section are based on the surge current waveforms characterized by the amplitudes given in Table 4.4. It includes single and multiple half-sine wave events.

For the single half-sine wave surges, #1 and #2, the following results are obtained by using (3.43):

$$\begin{cases} 13^{6.693} \cdot 10 = 2.85 \cdot 10^8 > 10^{7.643} = 4.39 \cdot 10^7 \\ 15^{6.693} \cdot 10 = 7.44 \cdot 10^8 > 10^{7.643} = 4.39 \cdot 10^7 \end{cases}.$$

Then a thyristor SKT-553/18E submitted to surge #1 or surge #2 is not expected to survive. For multi half-sine wave surges, the direct application of (3.45) results in the curves shown in Figure 4.10. The vertical axis is presented as a percentage of $10^{b_r} = 4.39 \cdot 10^7$.

Table 4.4 Amplitude [kA] of each 60 Hz current half-sine wave of the surge

Surge	***Half-sine***				
	1	**2**	**3**	**4**	**5**
#1	13	-	-	-	-
#2	15	-	-	-	-
#3	4.0	6.0	-	-	-
#4	5.7	8.7	-	-	-
#5	7.0	7.0	7.0	-	-
#6	7.0	7.5	9.0	-	-
#7	7.3	7.3	7.3	7.3	-
#8	7.3	7.5	7.8	8.0	-
#9	6.7	6.7	6.7	6.7	6.7
#10	6.7	6.8	7.0	7.5	8.0

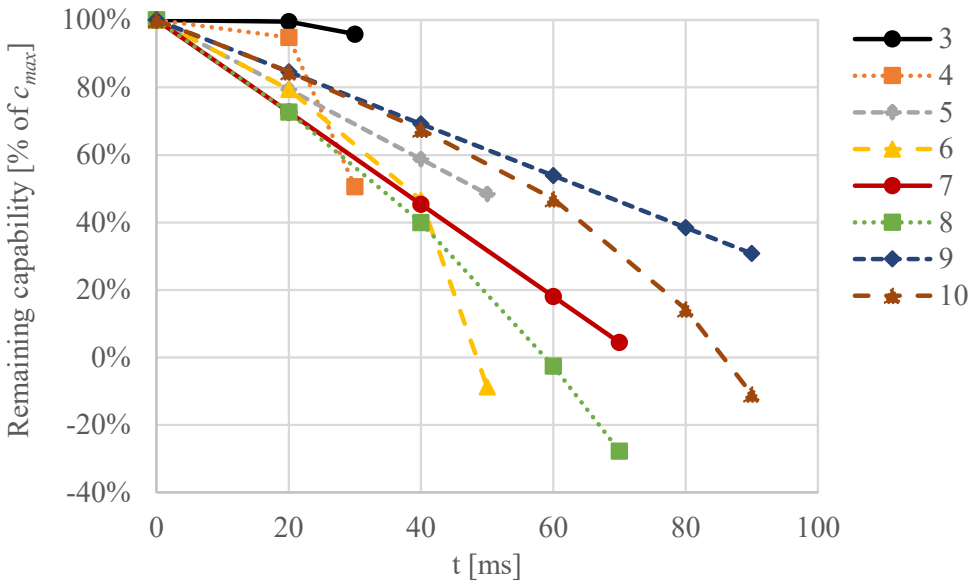


Figure 4.10 Theoretical percentage supportability commitment for part number SKT-553/18E submitted to multi half-sine wave surges (from #3 to #10) of Table 4.4.

For surges #3 and #4, no catastrophic failure is expected since the numeric result is greater than 0 at the end of the interval. For surge #5, the result is well greater than 0, which indicates the ride through surge survival condition for this thyristor for the corresponding waveform. This result is in accordance with Figure 3.5a: for $0 \cdot V_{RRM}$ and 50 ms, the curve leads to a value around $0.77 \cdot 9$ kA $\cdot\ 1.1 = 7.6$ kA[7]. It means that this thyristor survives to a current surge of three consecutive 60 Hz half-sine waves of

[7]Remember: the factor 1.1 is adopted for 60 Hz half-sine waves.

7.6 kA. Since the amplitude of surge #5 is 7.0 kA, then it can be anticipated that the thyristor will not be damaged. For surge #6, though, it is predicted that the device would not survive. The reader can perform similar analysis for surges #7 and #8 as well as for #9 and #10.

4.2 More Simulation on Power Thyristors

Since thyristors are the key elements of the proposed AF quenching device, they deserve to be deeply studied so that the design techniques presented in this work can be safely ensured. This section is devoted to the application of the techniques proposed in Subsection 3.2.2 to 11 preselected thyristors divided into three sets, each one containing devices with approximately the same I_{TSM}, which will be exposed to predetermined current surge profiles. Each group of devices include different types of thyristors - phase control, pulse power and bi-directional control thyristors (PCT, PPT and BCT, respectively) - from different manufacturers (A, B, C, and D). Devices rated for medium-voltage level were considered too. The current surges have been specified by predefined data sets of the random variables listed below:

- RMS symmetrical current (I_{sym}) and equivalent X/R ratio: normal distribution. Mean and standard deviation values were defined based on Table 4.5 (Roybal, 2001).
- Starting angle on the voltage waveform ($0 \leq \theta_{hc} \leq 90°$) and event duration in number of power-frequency cycles ($3 \leq N_{cyc} \leq 5$): uniform distribution.

Table 4.5 X/R ratios at which low-voltage protective devices are tested

I_{sym} [kA]	X/R ratio
≤ 10	1.73
> 10 and ≤ 20	3.18 to 3.87
> 20	4.90 to 6.60

The results of $T_{vj}(t)$ and $c_d(t)$ will be computed for each of the devices of a predefined group and compared. Because the ac switch of the electronic AF quenching device is formed by two antiparallel-associated thyristors, both will be included in the analysis, being named T_1 and T_2.

4.2.1 Overview

In order to clarify the procedure that was adopted in this section, an example that represent a simplified overview of the simulations will be shown. Specifically in this subsection, the virtual junction temperature of three different devices operating under varied current surge profiles will be evaluated. For all the tests, $T_{vj}(0) = 40$ °C and $f = 60$ Hz was considered. Table 4.6 illustrates the other conditions, where N_{cyc} is the number of power-frequency cycles, X/R and $I_{sym,pk}$ are respectively the characteristic of the equivalent impedance and the peak symmetrical, bolted-fault short-circuit current of the feeding power system, and θ_{hc} is the angle of the voltage waveform at which the short-circuit event through the ac switch starts.

Table 4.6 Test conditions

Test	N_{cyc}	X/R	$I_{sym,pk}$ $[kA]$			θ_{hc} [°]
AC_19	1	2	30	35	I_{sym,pk,max,AC_19}	0.1
AC_20	N_{cyc,max,AC_20}	2	30			0.1
AC_21	5	5	25			90

The variable I_{sym,pk,max,AC_19} denotes the maximum amplitude of the power-frequency symmetrical current waveform that can be applied to the device submitted to test AC_19 so that its maximum virtual junction temperature is not exceeded. The maximum virtual junction temperature ($T_{vj,max}$) is the value reached when the device initially at $T_{vj} = 125$ °C is submitted to one 50 Hz half-sine wave with amplitude I_{TSM}, as it can be seen in Figure 4.11 for devices #8, #9 and #11.

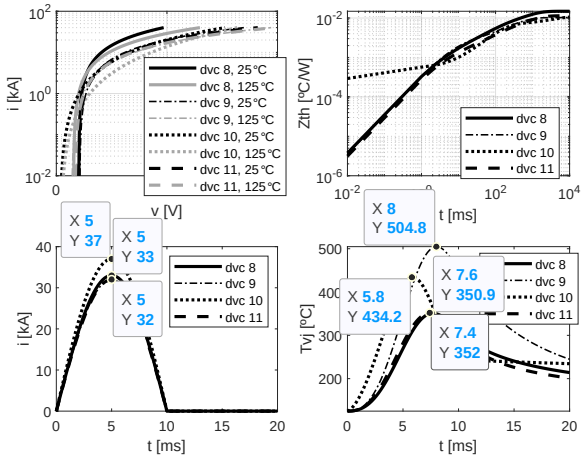


Figure 4.11 Voltage drop v, transient thermal impedance $Z_{th(j-c)}$, current i, and virtual junction temperature T_{vj} for devices #8, #9 and #11.

The variable N_{cyc,max,AC_20} denotes the maximum number of cycles that lead a device submitted to test AC_20 to reach a value not greater than $T_{vj,max}$.

Table 4.7 presents the main characteristics[8] of the three devices that will be evaluated in this introductory subsection.

Table 4.7 Basic characteristics of the devices

Device	***Type***	***Manufacturer***	I_{TSM} [kA]	V_{RRM} [kV]
#8	PCT	D	33.0	1.8
#9	PCT	B	32.0	4.2
#11	BCT	B	32.0	4.2

Figures 4.12 and 4.13 present the results obtained by the application of test AC_19 to the three devices. Their respective values of $I_{sym,pk}$ are 43.25 kA, 39.50 kA and 40.75 kA. Notice how these values are greater than those presented by Table 4.7. This result was expected due to the fact that the test started at a lower temperature. In all cases, $T_{vj,max}$ reached by T_1 and T_2 are the same. It was also a foreseen result since X/R is low and $\theta_{hc} \approx 0$.

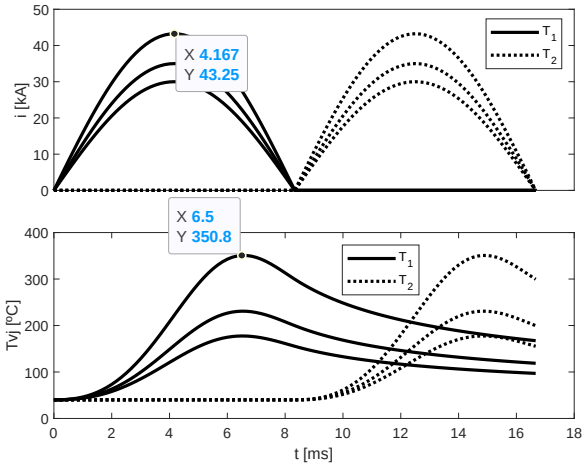
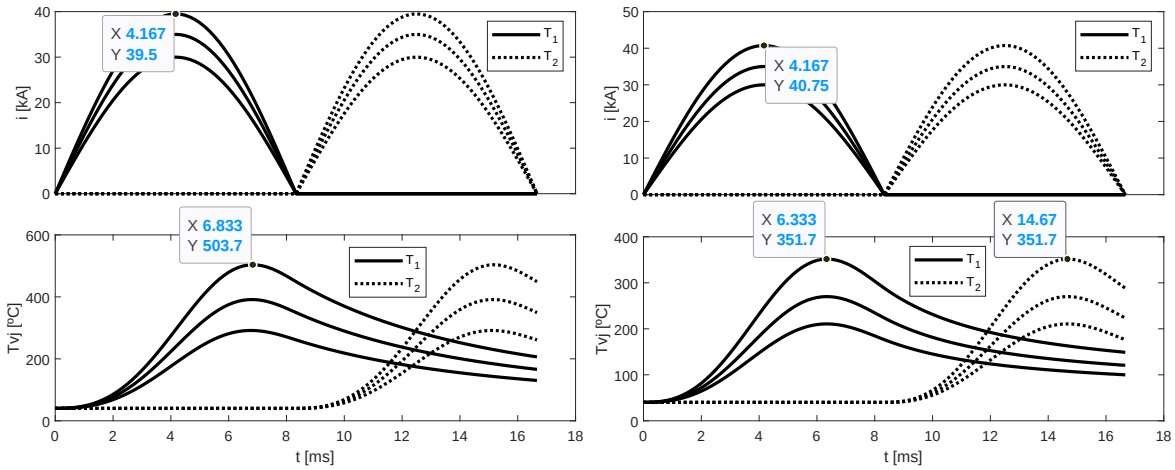


Figure 4.12 Current profile i and virtual junction temperature T_{vj} for test AC_19 applied to device #8.

Figures 4.14 and 4.15 show the results obtained by the application of test AC_20 to the three devices. Their respective values of N_{cyc,max,AC_20} are 4, 4 and 5. The data tips in the curves demonstrate that the respective $T_{vj,max}$ of the three devices are exceeded in the subsequent cycle. Again, $T_{vj,max}$ reached by T_1 and T_2 are practically the same.

[8] for $T_{vj}(0) = 125$ °C, $f = 50$ Hz, no direct or reverse voltage applied after surge.



(a) Device #9. (b) Device #11.

Figure 4.13 Current profile i and virtual junction temperature T_{vj} for test AC_19 applied to devices #9 and #11.

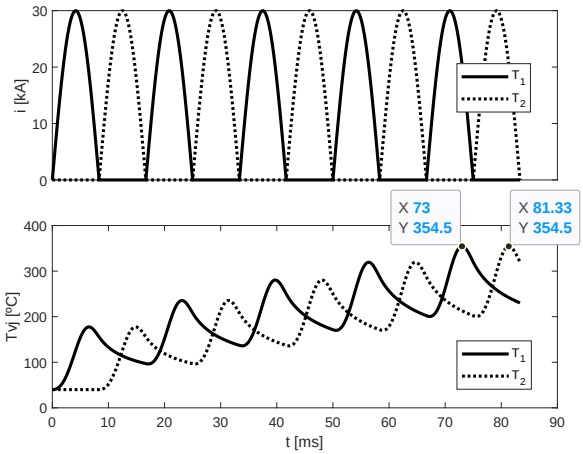
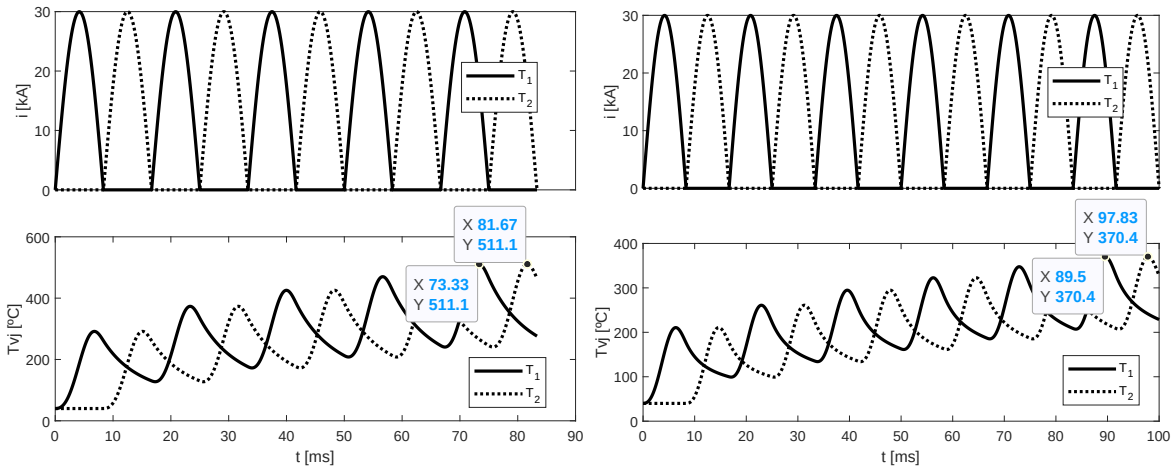


Figure 4.14 Current profile i and virtual junction temperature T_{vj} for test AC_20 applied to device #8.

Finally, figures 4.16 and 4.17 demonstrate the results gathered by the application of test AC_21 to the three devices. In this case, the objective was to evaluate if T_{vj} would overcome $T_{vj,max}$ at any instant during the 5-cycle interval, which was verified just at the 1st cycle for devices #9 and #11. Notice the huge effect that the dc level existing in the current waveform has in the thermal unbalance. In fact, in both cases only device T_2 has reached the critical condition.



(a) Device #9. (b) Device #11.

Figure 4.15 Current profile i and virtual junction temperature T_{vj} for test AC_20 applied to devices #9 and #11.

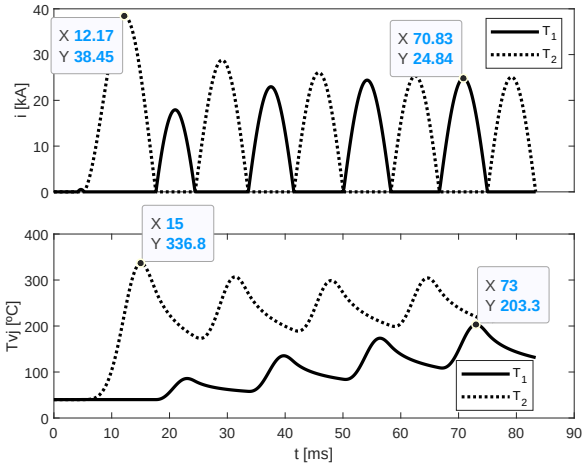
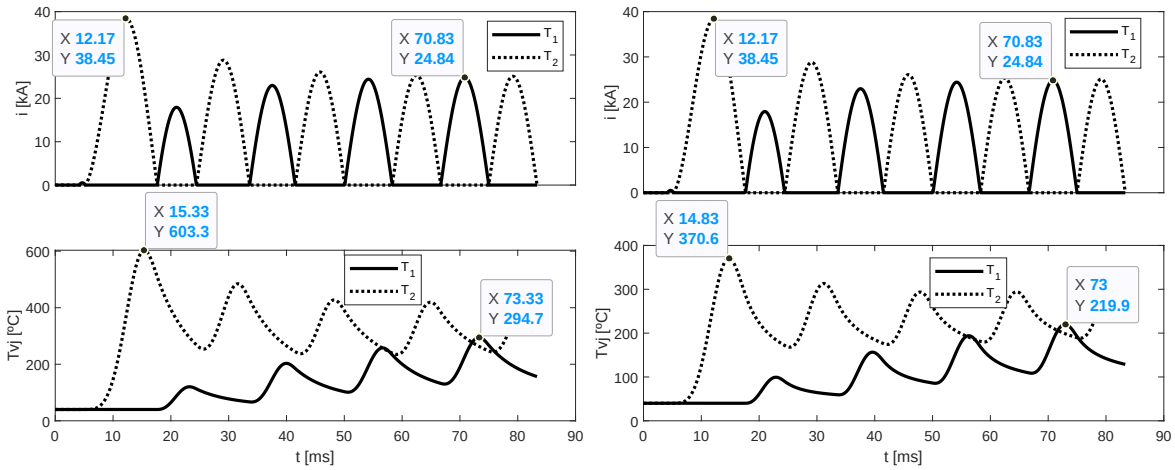


Figure 4.16 Current profile i and virtual junction temperature T_{vj} for test AC_21 applied to device #8.

4.2.2 Set 1 – Devices with I_{TSM} in the range of 10 kA

Set 1 is composed by three devices from different manufacturers. Up to the date that this dissertation was written, it was not found any commercial model of PPT or BCT with rated surge current below 10 kA. Still, for the sake of clarification of the results that will be presented in this section, three PCTs from different manufacturers and similar ratings will be evaluated. Their main attributes[9] are shown in Table 4.8.

[9]For $T_{vj}(0) = 125$ °C, $f = 50$ Hz, no direct or reverse voltage applied after surge.



(a) Device #9. (b) Device #11.

Figure 4.17 Current profile i and virtual junction temperature T_{vj} for test AC_21 applied to devices #9 and #11.

Table 4.8 Basic characteristics of the devices of Set 1

Device	***Type***	***Manufacturer***	I_{TSM} [kA]	V_{RRM} [kV]	a_r	b_r
#1	PCT	A	8.0	1.8	5.829	5.431
#2	PCT	B	9.0	1.8	N/D	N/D
#3	PCT	C	9.1	1.4	5.049	5.044

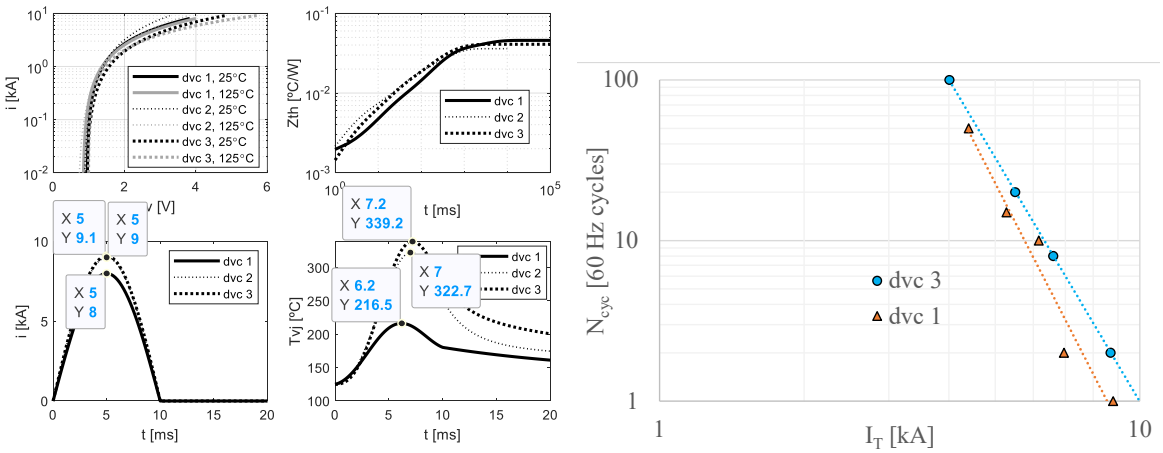
Preliminary Information from the Data Sheets

Figure 4.18 presents[10] the curves obtained by the application of the methodology previously described in Subsection 3.2.2. Notice that the Stage 2 of the methodology is also considered.

For each one of the devices listed in Table 4.8, Stage 1 of the methodology was applied to obtain the curves of current- and temperature-dependent voltage drop, transient thermal impedance, and virtual junction temperature for the standard single-cycle current surge defined in their respective data sheet. As it can be seen in the figure, device #1 achieves $T_{vj} = 216.5$ °C, while devices #2 and #3 reach $T_{vj} = 322.7$ °C and $T_{vj} = 339.2$ °C, respectively.

For devices #1 and #3, the respective values of c_{max} can be calculated from Table 4.8 as $c_{max} = 2.697 \cdot 10^5$ and $c_{max} = 1.107 \cdot 10^5$. This value cannot be calculated for device #2 since the data sheet does not provide information for the computation of

[10] In (a), $N_{cyc} = 1$; $T_{vj}(0) = 125$ °C; $f = 50$ Hz; $X/R = 0.1$; $I_{sym,pk}$ according device; $\theta_{hc} = 0.1$.



(a) Voltage drop v, transient thermal impedance $Z_{th(j-c)}$, current i, and virtual junction temperature T_{vj}.

(b) Supportability N_{cyc} vs. surge current I_T.

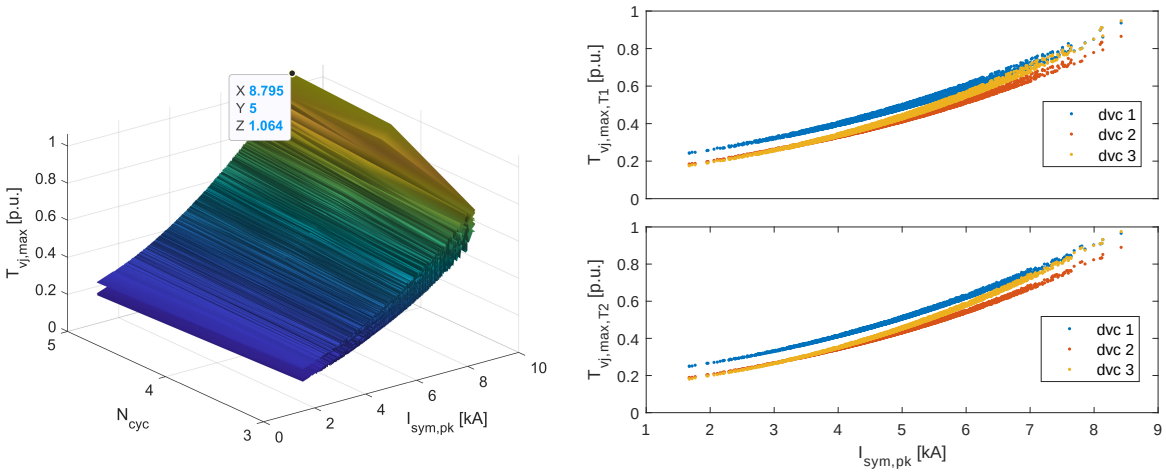
Figure 4.18 Preliminary evaluation of the devices of Set 1.

constants a_r and b_r. Therefore, Stage 2 of the proposed methodology can be applied only for devices #1 and #3 of Set 1.

Performance for Other Surge Profiles

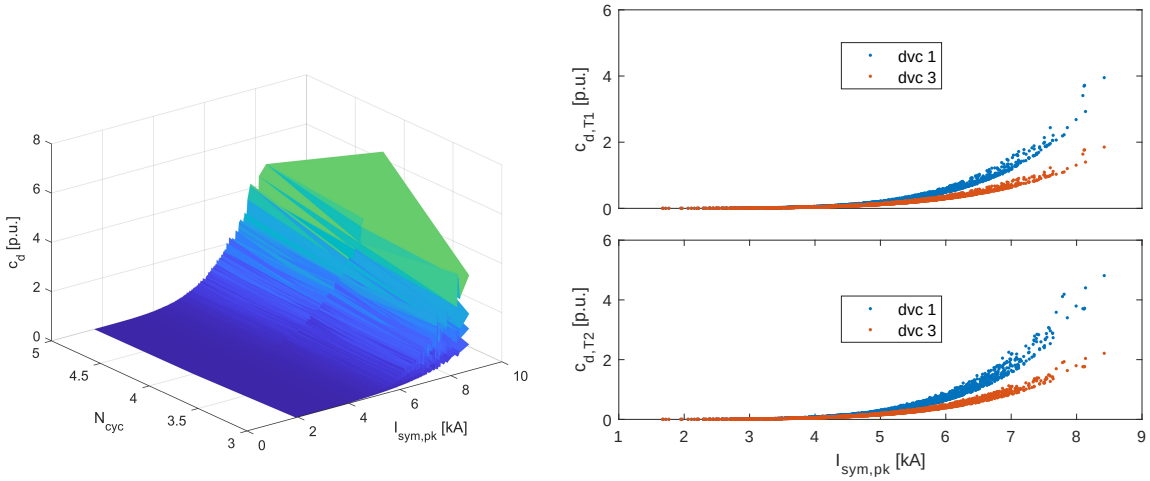
Figures 4.19 and 4.20 show graphs relating the per-unit (a) peak virtual junction temperature $T_{vj,max}$ and (b) compromised capability c_d as functions of the peak symmetrical current ($I_{sym,pk}$) and the number of cycles N_{cyc}, for $T_{vj}(0) = 40$ °C and $f = 60$ Hz, for a number of 10,000 cases where $\mu = 5$ kA and $\sigma = 1$ kA for $I_{sym,pk}$, $\mu = 1.855$ and $\sigma = 0.125$ for X/R, $0 \leq \theta_{hc} \leq 90°$ and $3 \leq N_{cyc} \leq 5$. The figure includes one plot for each thyristor of the ac switch for each one of the devices of the Set 1 (total of 6 surfaces for (a) and total of 4 surfaces for (b), since Stage 2 involves only devices #1 and #3). The base value for $T_{vj,max}$ is the respective peak virtual junction temperature obtained for the data sheet conditions – see Figure 4.18a, while the base value for c_d is the respective maximum capability $c_{max} = 10^{b_r}$ – see Table 4.8. The effects of X/R and θ_{hc} over $T_{vj,max}$ and c_d were almost insignificant in this case, which was expected for such a low asymmetry factor that results in a minor asymmetry in the current waveform. Figures 4.19b and 4.20b show the respective results from 4.19a and 4.20a for $N_{cyc} = 5$.

The performance of the three devices using Stage 1 of the methodology is similar, but device #2 has been shown to be slightly superior in comparison to device #3, even though device #2 has a lower I_{TSM} rating. The comparison between devices #3 and



(a) Overlayed surfaces. (b) Superimposed curves for $N_{cyc} = 5$.

Figure 4.19 Per-unit $T_{vj,max}$.



(a) Overlayed surfaces. (b) Superimposed curves for $N_{cyc} = 5$.

Figure 4.20 Per-unit c_d.

#1 shows that #3 is superior, which is confirmed by the results obtained by Stage 2 of the methodology. Despite this agreement, Stage 2 is much more conservative than Stage 1, as it was expected. For $I_{sym,pk} = 8$ kA, for example, Stage 2 leads to $c_{d,T_1} >> 1$ p.u., while Stage 1 leads to $T_{vj,max,T_1} < 1$ p.u. The same is true for thyristor T_2.

4.2.3 Set 2 – Devices with I_{TSM} in the range of 20 kA

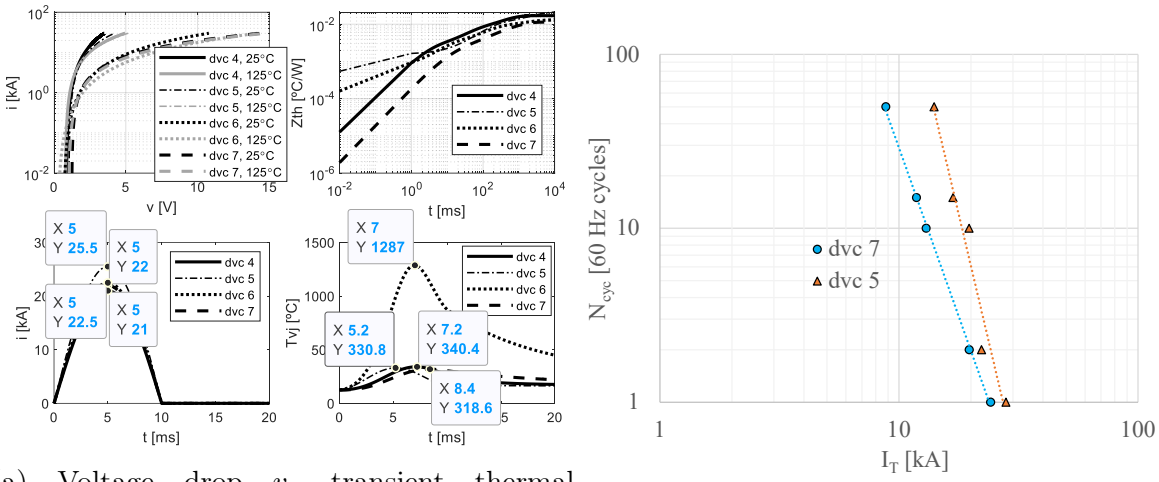
Set 2 is composed by four devices from different manufacturers. Their attributes[11] are shown in Table 4.9.

Table 4.9 Basic characteristics of the devices of Set 2

Device	***Type***	***Manufacturer***	I_{TSM} [kA]	V_{RRM} [kV]	a_r	b_r
#4	PCT	B	21.0	1.8	N/D	N/D
#5	PCT	A	25.5	1.6	5.829	8.366
#6	PPT	C	22.5	4.5	N/D	N/D
#7	BCT	B	22.0	6.5	3.879	5.341

Preliminary Information from the Data Sheets

Figure 4.21 presents[12] curves achieved by the application of the methodology described in the previous section. For devices #5 and #7, the respective values of c_{max} can be calculated from Table 4.9 as $c_{max} = 2.323 \cdot 10^8$ and $c_{max} = 2.193 \cdot 10^5$.



(a) Voltage drop v, transient thermal impedance $Z_{th(j-c)}$, current i, and virtual junction temperature T_{vj}.

(b) Supportability N_{cyc} vs. surge current I_T.

Figure 4.21 Preliminary evaluation of the devices of Set 2.

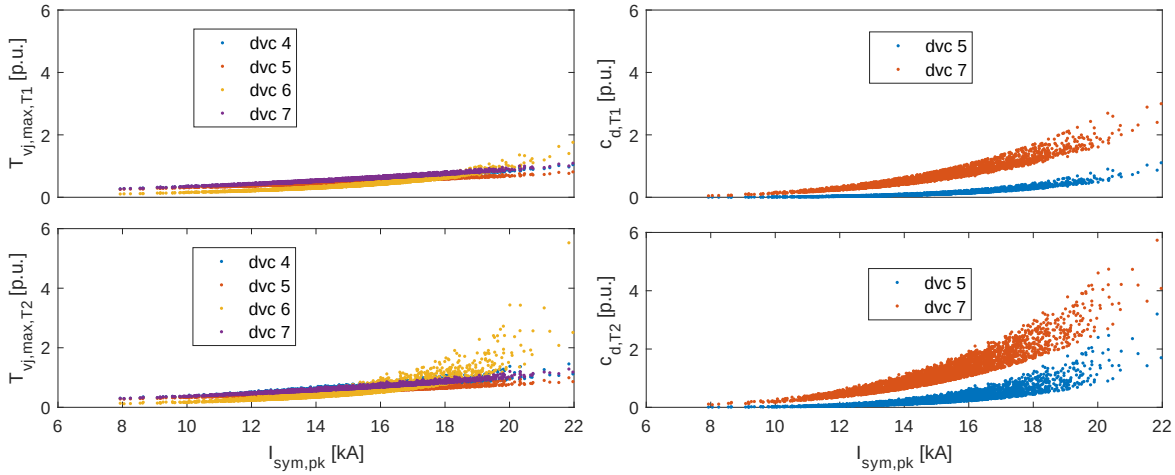
Notice in Figure 4.21a that device #6, which is a PPT type, has a peak virtual junction temperature $T_{vj,max} = 1287$ °C - much higher than of the other three devices.

[11] for $T_{vj}(0) = 125$ °C, $f = 50$ Hz, no direct or reverse voltage applied after surge.
[12] In (a), $N_{cyc} = 1$; $T_{vj}(0) = 125$ °C; $f = 50$ Hz; $X/R = 0.1$; $I_{sym,pk}$ according device; $\theta_{hc} = 0.1°$.

According to reference (Dynex, 2002), 1100 to 1300°C is the temperature range reached at non-repetitive di/dt limits. The melting point of silicon is 1415 °C.

Performance for Other Surge Profiles

Figure 4.22 shows curves relating the per-unit (a) peak virtual junction temperature $T_{vj,max}$ and (b) compromised capability c_d as functions of the peak symmetrical current ($I_{sym,pk}$) for $T_{vj}(0) = 40$ °C, $f = 60$ Hz and $N_{cyc} = 5$. These results were taken from a group of 10,000 cases where $\mu = 15$ kA and $\sigma = 2$ kA for $I_{sym,pk}$, $\mu = 3.525$ and $\sigma = 0.345$ for X/R, $0 \leq \theta_{hc} \leq 90°$ and $3 \leq N_{cyc} \leq 5$. There is one subplot for each thyristor of the ac switch for each one of the devices of the Set 2 (total of 8 curves for (a) and total of 4 curves for (b), since Stage 2 involves only the devices #5 and #7). The base value for $T_{vj,max}$ is the respective peak virtual junction temperature obtained for the data sheet conditions – see Figure 4.22a, while the base value for c_d is the respective maximum capability $c_{max} = 10^{b_r}$ – see Table 4.9.



(a) $T_{vj,max}$. (b) c_d.

Figure 4.22 Per-unit values for $N_{cyc} = 5$.

The effects of X/R and θ_{hc} over $T_{vj,max}$ were considerable in this case, which can be verified by the increased dispersion of the points, especially for high values of $I_{sym,pk}$ and the significative difference between the results for T_1 and for T_2. Moreover, it can be seen from Figure 4.22 that device #5 (PCT) is the one that has the best performance among the devices of Set 2, followed by devices #7 (BCT) and #4 (PCT). On the other hand, device #6 (PPT) is the one that performs better for low-peak current profiles, but it is also the worse for high-peak current profiles. This surely has to do with the fact that it reaches a much higher value of T_{vj} at the first current

half-sine wave, as it can be verified in Figure 4.21a. Therefore, it can be concluded that it is not advantageous over PCT and BCT for $N_{cyc} > 1$. Device #7 (BCT) has a performance like that of device #4 (PCT).

4.2.4 Set 3 – Devices with I_{TSM} in the range of 30 kA

Set 3 is composed by four devices from different manufacturers[13]. Their attributes[14] are shown in Table 4.10.

Table 4.10 Basic characteristics of the devices of Set 3

Device	***Type***	***Manufacturer***	I_{TSM} [kA]	V_{RRM} [kV]	a_r	b_r
#8	PCT	D	33.0	1.8	3.219	5.051
#9	PCT	B	32.0	4.2	4.267	6.549
#10	PPT	C	37.0	4.5	N/D	N/D
#11	BCT	B	32.0	4.2	4.267	6.549

Preliminary Information from the Data Sheets

Figure 4.23 presents[15] curves obtained by the application of the methodology described in the previous section. For the devices #8 and #9 and #11, the respective values of c_{max} can be calculated from Table 4.10 as $c_{max} = 1.125 \cdot 10^5$ and $c_{max} = 3.540 \cdot 10^6$.

Performance for Other Surge Profiles

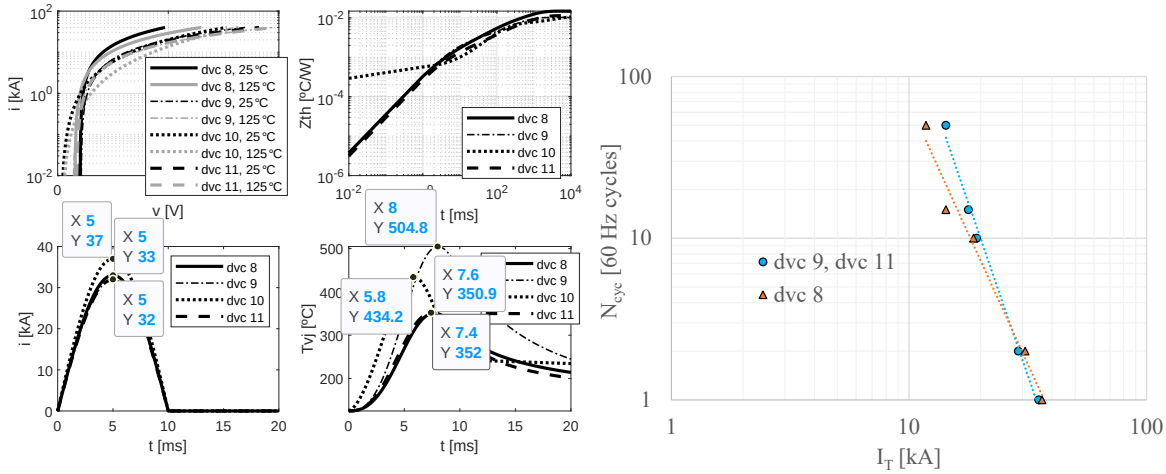
Figure 4.24 shows that devices #8 and #10 perform better than #9 and #11, especially for high values of $I_{sym,pk}$. Moreover, device #8 is slightly better than device #10 for the group of surges tested (10,000 cases where $\mu = 25$ kA and $\sigma = 2$ kA for $I_{sym,pk}$, $\mu = 5.750$ and $\sigma = 0.850$ for X/R, $0 \leq \theta_{hc} \leq 90°$).

According to the results achieved in Subsection 4.2.1, the dc level at surge current contributes to the preservation of one thyristor of the ac switch, at the cost of imposing harsher conditions to the other thyristor. The device that does not fail can be reused, while the other cannot. This situation is a strong indicator against the application of BCT in the AF quenching device, since both thyristors are encapsulated in the same package, making reuse unviable. Moreover, the performance of BCTs has been shown

[13] Devices #9 and #11 appear to be identical, but their transient thermal impedance are different, as it can be seen in Figure 4.23a.

[14] For $T_{vj} = 125$ °C, $f = 50$ Hz, no direct or reverse voltage applied after surge.

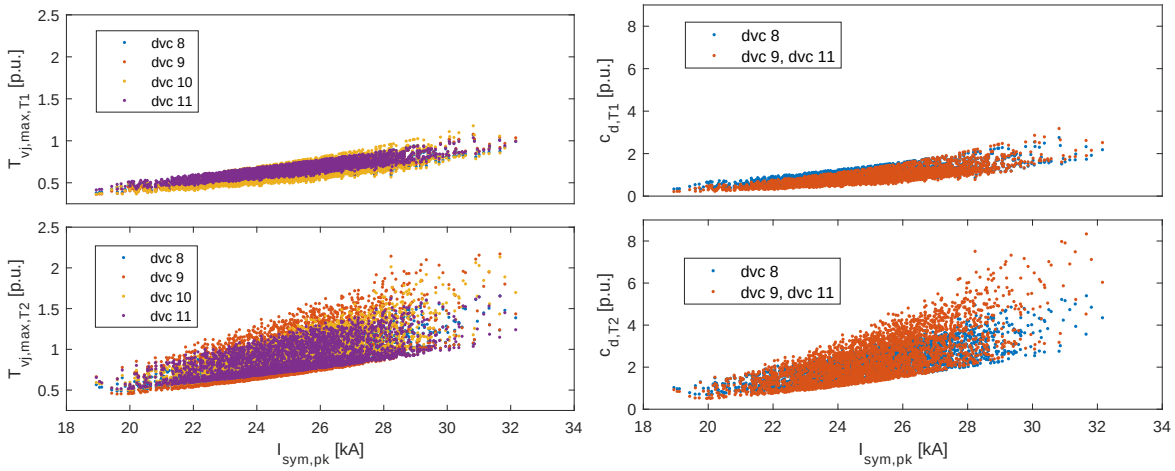
[15] In (a), $N_{cyc} = 1$; $T_{vj}(0) = 125$ °C; $f = 50$ Hz; $X/R = 0.1$; $I_{sym,pk}$ = according device; $\theta_{hc} = 0.1°$.



(a) Voltage drop v, transient thermal impedance $Z_{th(j-c)}$, current i, and virtual junction temperature T_{vj}.

(b) Supportability N_{cyc} vs. surge current I_T.

Figure 4.23 Preliminary evaluation of the devices of Set 3.



(a) $T_{vj,max}$.

(b) c_d.

Figure 4.24 Per-unit values for $N_{cyc} = 5$.

to be not superior in comparison to the performance of the other kinds of devices analysed. Finally, heat transfer from one device to the other in a BCT may be verified during the surge, since a perfect thermal insulation between the two parts is impossible and given that they share the same housing.

Regarding PPTs, no advantage is verified as well, both from performance and commercial availability point of view. Besides having restrict availability at low current ratings, some of the devices found on the market do not block reverse voltage, being apparently useful only in short-term, dc applications. Finally, among the PPT part

numbers that could be relevant for the AF quenching device, the data sheets do not provide all the information necessary for the utilization of the methodology proposed in this work.

4.3 Complete Simulation Results

Despite being representative of most arcing fault events that do happen in practice, the analyses presented in Section 4.1 are not enough for the fully understanding and reliable design of the quenching device. The main reason is that other types of arcing faults (phase-to-phase-to-ground, three-phase, and three-phase-to-ground) are a real possibility, even if these are an intermediate stage of an evolving fault. This will be considered in this section.

Moreover, one should bear in mind that since the arc-flash quenching device is intended to substitute any other solution suitable for that purpose, then it should be verified according to standard acceptance tests. IEEE C37.20.7-2017 (IEE, 2018) and IEC/TR 61641-2014 (Commission, 2014) are the usual references for testing switchgear and controlgear assemblies under conditions of arcing due to internal fault. The purpose is to assess the ability of the assembly to limit the risk of personal injury and damage of assemblies resulting from an internal arcing fault. Both require the execution of three-phase test for three-phase equipment. It is recommended that the applied voltage is 105% of rated operational voltage, the prospective short-circuit current is calibrated according to the switchgear design, and the duration of the test is 10 power-frequency cycles after the operation of the quenching device. The arc is initiated between phases without connection to earth by means of a bare copper ignition wire. For metal-enclosed LV switchgear, the X/R ratio of the test circuit shall be 6.6 or greater. This value is suitable for switchboards and LV MCCs as well.

Single phase-to-phase faults have already been examined in Section 4.1.1. Phase-to-phase-to-ground is only an intermediate stage between phase-to-phase fault and three-phase-to-ground fault, and this may be the main reason why it is not tested. According to references (Dunki-Jacobs, 1972; Stokes and Sweeting, 2006) the escalation times are in the order of two cycles, with a considerable increase in fault current level. This is another fact that supports the direct application of three-phase faults to the busbar.

Based on the above, the objectives of this section are:

1. To present complementary analyses for the case of single-phase arcing fault, so as to give support to the development of the item 2 below.

2. To present the mathematical modeling, discrete-time computational implementation and simulation results for three-phase arcing fault cases, once they have to be necessarily performed to the validation of the proposed AF quenching device.

3. To provide a practical analysis on the impact of a failure on a thyristor on the effectiveness of the quenching device in eliminating an arcing fault.

4.3.1 Single-Phase Complete Modeling and Solution

This subsection details the implementation of the model of a complete single-phase system, including the dynamic models of the arcing fault and of the power thyristors, as well as the snubbers and other particularities that would turn the algebraic solution very difficult.

Voltage Drop and Virtual Junction Temperature

The simplified circuit of Figure 3.4, which was previously explored in Subsection 4.1.2, is useful for the calculation of the shunt impedance Z_x. However, a more detailed model that comprises the complete behavior of the ac switch, including the representation of the dynamic thyristor voltage drop as a function of the instantaneous current and virtual junction temperature, is a must for the design validation. Figure 4.25 shows the implementation of (3.39) in ATPDraw by means of the TACS tool.

Turn-off Snubbers

Part number N3175HE160 (Westcode, 2014) from Westcode will be considered as an example. For this device, the limiting values for dv/dt_{off} and di/dt_{on} are respectively $dv/dt_c = 1$ kV/μs and $di/dt_c = 150$ A/μs. However, the design should not be restricted only to satisfy these ratings, but also to limit the overvoltage in the switch and consequently in the bus. The procedure detailed in (Microelectronics, 2007) was adopted to obtain the result presented in Figure 4.26, which shows the transient voltage in the ac switch for five conditions: without snubber and with snubber designed for dv/dt equal to 10%, 5%, 2% and 1.25% of dv/dt_c. The higher the damping is, the higher the required capacitance. For 1.25%, $C = 4.6$ μF and $R = 1.25$ Ω. The power P_r in the resistor is given by (Dubilier):

$$P_r = C \cdot V_b^2 \cdot f_{sw}, \tag{4.8}$$

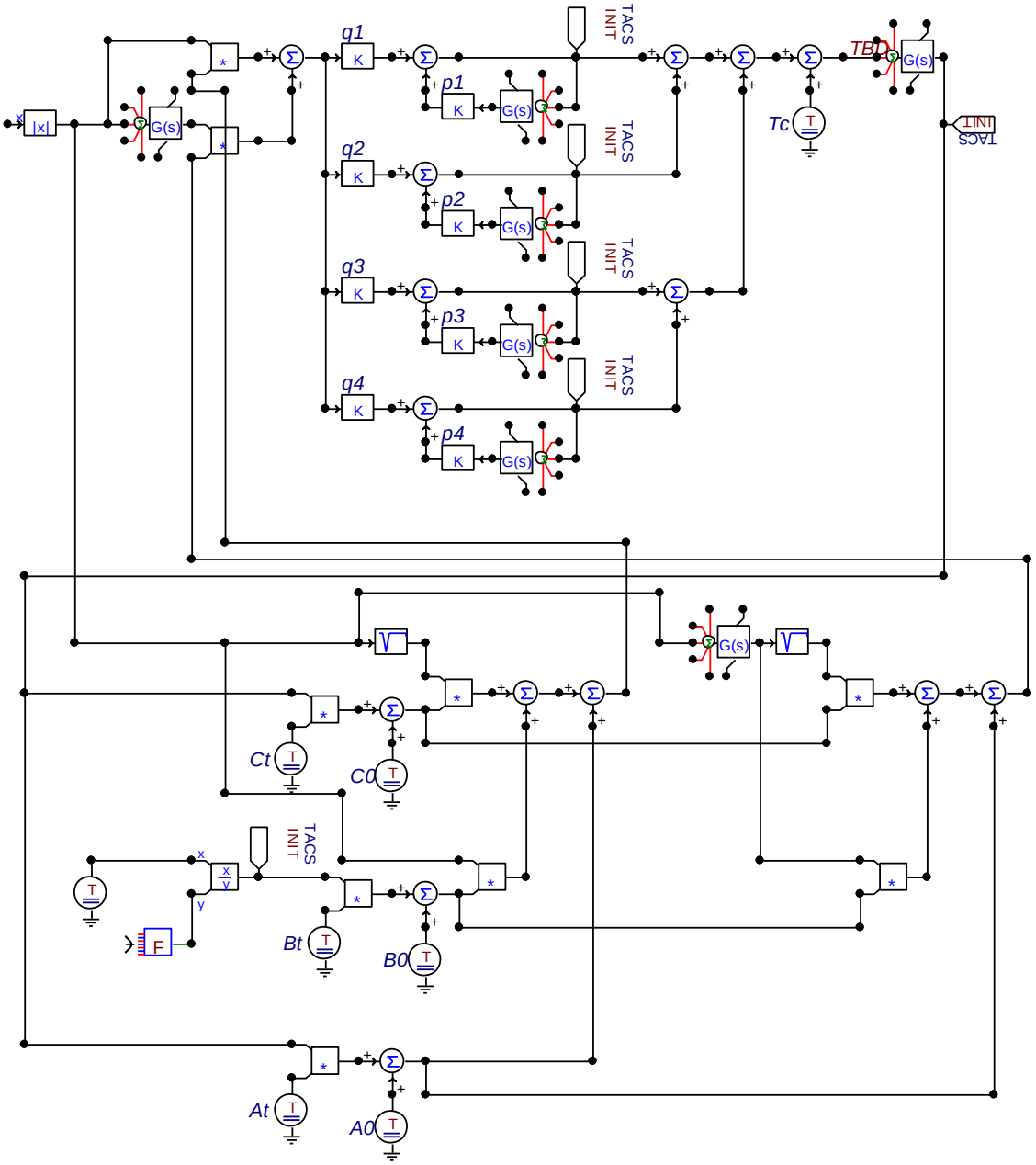


Figure 4.25 Implementation of the recursive convolution-based calculation of T_{vj} in ATPDraw / TACS.

where $V_b = 135$ V is the voltage after the transient and f_{sw} is the frequency of snubber operation, which is $2 \cdot 60$ Hz $= 120$ Hz in this case. Therefore, $P_r = 10$ W. A non-inductive resistor, as the carbon-film one, is the ideal option for the present application. This is a highly conservative calculation since the electronic switch of the AF quenching device operates for a short time interval. The power dissipated by the resistor during

normal operation (hot stand-by state) is way below the value calculated by (4.8), since the reactance of the capacitor is $1/(\omega \cdot C) \approx 576\ \Omega$, leading to truly low current ($\approx$ 530 mA RMS) through the quenching device.

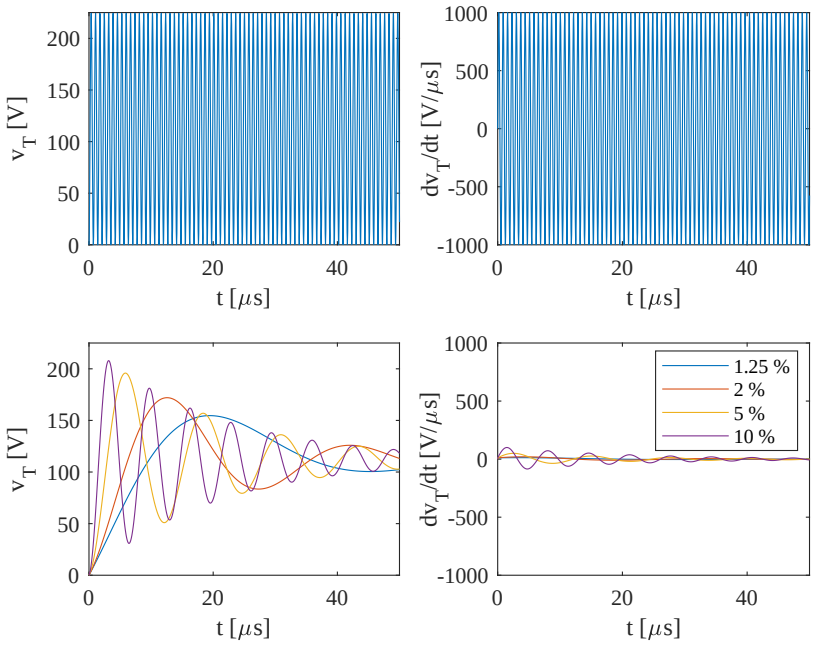


Figure 4.26 Voltage across the electronic switch (v_T), and rate of variation (dv_T/dt), without (top) and with (bottom) voltage snubber for 1.25%, 2%, 5% and 10% of dv/dt_c.

For the capacitor, it is desired a polypropylene or film / foil component due to its increased supportability to transient current. The peak current I_{pk} to the capacitor is given by (Dubilier):

$$I_{pk} \leq \frac{V_S}{R}, \tag{4.9}$$

which results in $I_{pk} \leq 597.6$ A at 120 Hz. To optimize the snubber efficiency, it must be located very close to the switch.

Results - Part 1

The enhanced model has been implemented in ATPDraw as shown in Figure 4.27, where Z_d is the RC snubber (with the parameters calculated above). The subsystem "kiz" contains the block diagram previously shown in Figure 4.2 (whith the parameters of test #67), while the subsystem "scr" encloses the block diagram of Figure 4.25 (with the parameters of thyristor SKT-553/18E). Both thyristors are fired from t_x on. Figures 4.28a and 4.28b show simulation results for the operation of the quenching

device with exactly the same power system and shunt impedance parameters and sampling time used in Subsection 4.1.2 and $I_M = 0$. As it can be clearly seen in Figure 4.28a, arc current i_a is quickly eliminated, while quenching device current i_x reaches approximately 48 kA peak, as previously calculated[16]. The maximum virtual junction temperature reached by the thyristors during the operation of the device is 225 °C.

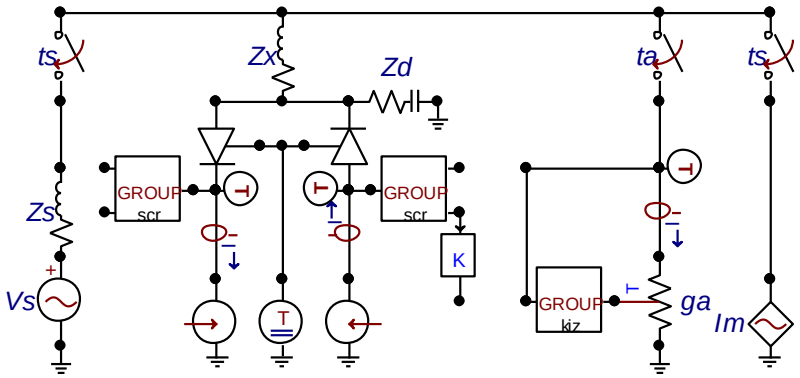
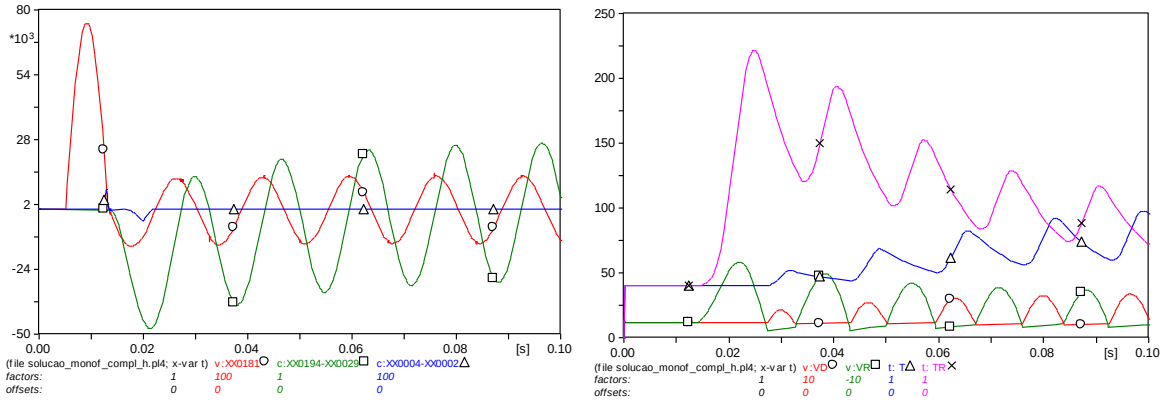


Figure 4.27 Complete single-phase system implemented in ATPDraw.



(a) Red (circular mark): v_b ($x100$); green (square): i_x ($x1$); blue (triangle): i_a ($x100$).

(b) Red (circular mark): v_{T_1} ($x10$); green (square): v_{T_2} (x -10); blue (triangular): $T_{vj,T1}$ ($x1$); magenta (cross): $T_{vj,T2}$ ($x1$).

Figure 4.28 Single-phase simulation results for the complete single-phase system implemented in ATPDraw.

Results - Part 2

Given the three-phase operation of the quenching device regardless the type of fault, the single-phase model has been extended and realized into ATPDraw. As yet, only

[16] See Figure 4.6 again.

single-phase arcing faults will be considered - three-phase faults will be treated in the next subsection.

The models of the real arcing fault register of test #67, the thyristor SKT-553/18E and the calculated RC snubber were considered again for the simulations. The sampling time of 50 μs has been kept as well. The feeding power system, though, is the Thévenin equivalent of the real laboratory system at the point where the AF quenching device would be connected to perform the experimental tests, which will be presented in Section 4.4. The parameters of the equivalent itself have been obtained by means of an experiment. The no-load voltage is 440 V and the impedance has 33 mΩ plus 100 μH. The neutral is solidly grounded (the resistor inserted in the model represents the grounding resistance, considered to be 33 mΩ). To make the model more realistic, a linear RL, three-phase, Y, balanced load has been included ($R = 10\ \Omega$, $L = 1\ \mu$H) as well as a generic three-phase, Y, balanced sinusoidal current source with amplitude of 500 A. The current source is connected to the bus through a balanced impedance with $R = 1$ mΩ, $L = 1\ \mu$H per phase.

The results presented in this subsection will be given for different systematically organized conditions, so the impact of each one to the effectiveness of the AF quenching device can be evaluated. The main objective here is to perform a sensitivity analysis about the insertion of the shunt impedance to the branch of the ac switch. A time interval of 1 ms from the beginning of the arcing fault is required for the detection by the protective relay (Seedorff, 2015; SEL, 2017), and an additional interval of 1 ms will be conservatively considered for the effective operation of the gate-drivers of the quenching device. Then, a total of 2 ms will be allowed from the initiation of the arcing phenomena (which is $t = t_{min,h} = 69.1$ ms in Figure 4.1a, for example) to the thyristor firing. It is worth emphasizing that independently of the fault type, the three electronic ac switches are simultaneously turned on. The main reason for that is operational reliability, as it was concluded in Subsection 2.3.1.

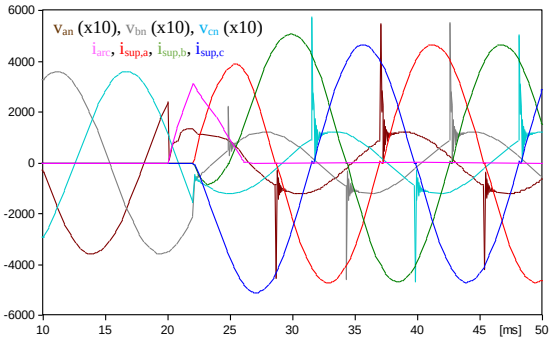
The analysis performed in this subsection will be centered on the evaluation of the effects produced by the variation of two parameters: (i) the shunt impedance; and (ii) the point-on-wave at which the arcing fault starts. Moreover, two fault types will be examined: phase A-to-ground and phase A-to-phase B. Solid-neutral grounding will be initially assumed for the power system. Since the typical bus gap of LV MCCs and panelboards is 25 mm (IEEE, 2018), the arc-flash model of test #67 will be adopted. Despite real faults do not start from a bonding copper wire, this condition will be kept in the simulations presented in this paper, since it is a good representation of events like circuit breaker rack out under load. Reference (Gammon and Matthews, 2001)

reports values of about 350 V for the initiation of an arcing fault at room temperature and atmospheric pressure.

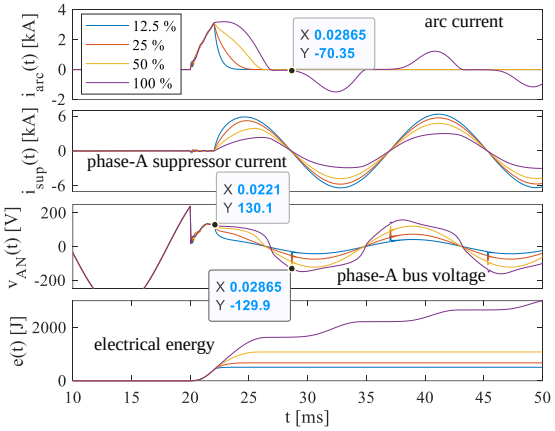
For simplicity, the current-limiting impedance $\dot{Z}_x$ will be calculated in this initial analysis as a percentage of $|\dot{Z}_S|$. The following values will be tested: 100%, 50%, 25% and 12.5%, with PF angles of 0, 22.5°, 45°, 67.5° and 90° lagging. The following *point-on-wave* (POW) angles were chosen for the arcing fault starting (with respect to phase-A voltage): 0, 45°, 90° and 135°. The coverage of the overall half-sine wave eliminates any need for simulating the fault in the other phases, i.e., similar results would be obtained for phase B-to-ground, phase C-to-ground or phase B-to-C, phase C-to-A faults, except for the fact that they would be displaced in time from those found for phase A-to-ground and phase A-to-B, respectively.

Figure 4.29a presents line-to-neutral bus voltages, arcing path current, and quenching device currents for phase-to-ground fault, $50\% \cdot |\dot{Z}_S|$, PF = 45° and POW = 45°. The current through the arcing path starts decaying immediately after the operation of the quenching device and then become extinct within 6 ms. Specifically for this simulation, the RC snubbers have been deactivated so that one can see they play a fundamental role in avoiding AF restrike.

Figures 4.29b, 4.30a and 4.30b present phase-A bus voltage, phase-A quenching device current, arcing fault current and electrical energy for the set of previously defined values for $|\dot{Z}_x|$, $\angle\dot{Z}_x$ and POW, respectively.



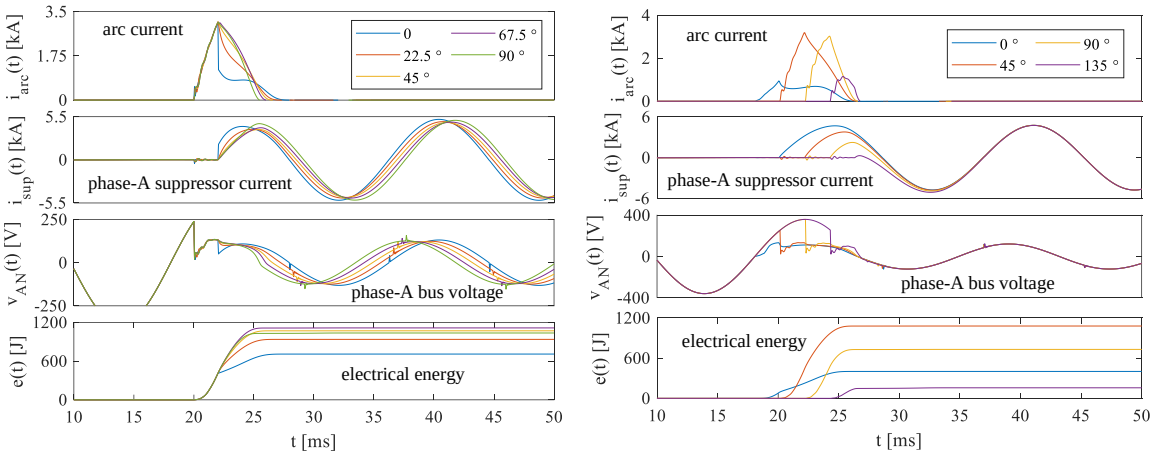
(a) $50\% \cdot |\dot{Z}_S|$, PF = 45° and POW = 45°, no RC snubber.



(b) Variation of $|\dot{Z}_x|$, RC snubber active.

Figure 4.29 Waveforms obtained by the simulation of phase A-to-ground fault and various $|\dot{Z}_x|$.

Notice in Figure 4.29b that for 12.5%, 25% and 50%, there is no fault restrike. It can be explained observing that for $|\dot{Z}_x| = 100\%$, the voltage becomes greater than



(a) For various values of $\angle \dot{Z}_x$.

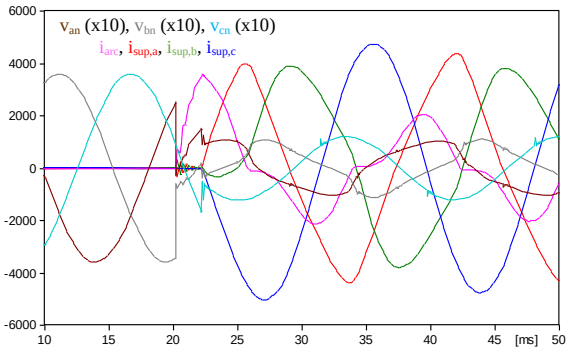
(b) For various values of POW.

Figure 4.30 Waveforms obtained by the simulation of phase A-to-ground fault.

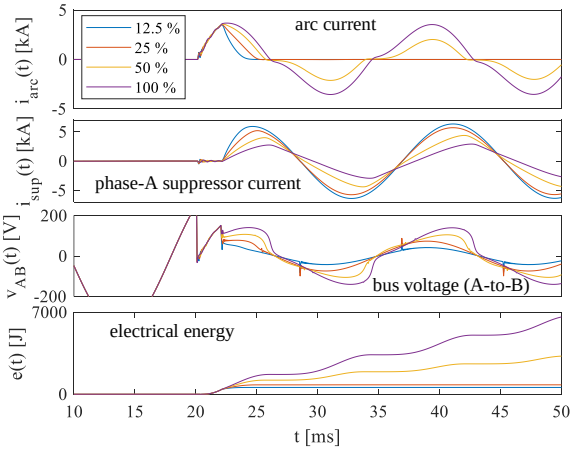
130 V after $t = 28.65$ ms, which was not achieved in any other case. Figure 4.30a shows that peak bus voltage depends little on the shunt impedance power factor, but the more resistive is the impedance the lower is the resultant energy. This is easily explained by the fact that the arcing fault has a purely resistive characteristic, then the current commutation to an inductive path takes some amount of time depending on the X/R ratio of the shunt impedance. Finally, Figure 4.30b demonstrates that the point-on-wave where the fault starts has a huge impact on the value of the peak current at the quenching device and arc energy. The worst case happens for POW = 45°. This is because for a PF angle of 45°, POW = 45° leads to the highest possible di/dt at the fault initiation.

Figure 4.31a displays line-to-neutral bus voltages, arcing path current, and quenching device current waveforms for phase A-to-phase B fault, $50\% \cdot |\dot{Z}_S|$, PF = 45° and POW = 45°. Notice that the arc fault current is not eliminated in this case. When the quenching device operates, the voltage across the arcing path is formed by the series combination of phase-A and phase-B branches, meaning that the current-limiting impedance is now effectively twice the value it was for phase A-to-ground fault. Another difference is that the AF is submitted to phase-to-phase voltage, which is greater than phase-to-ground voltage.

Figures 4.31b, 4.32a, and 4.32b present A-to-B bus voltage, phase-A quenching device current, arcing fault current and electrical energy waveforms for the set of previously defined values for $|\dot{Z}_x|$, $\angle \dot{Z}_x$ and POW, respectively. In Figure 4.31b, the arcing fault is extinguished only for $|\dot{Z}_x| = 12.5\%$ and 25%. Since 50% is not effective in this case, the analysis on the effect of PF and POW was done for $|\dot{Z}_x| = 25\%$.



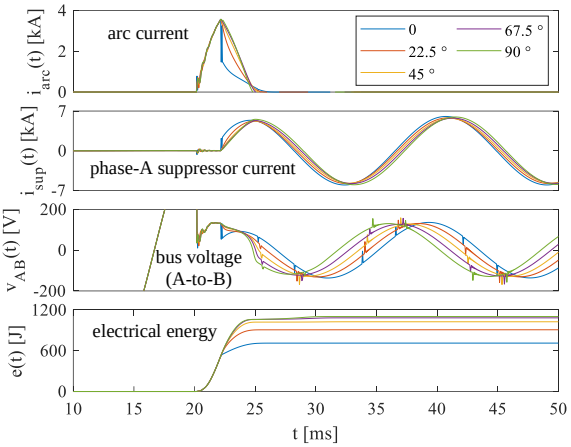
(a) For $50\% \cdot |\dot{Z}_S|$, PF = 45° and POW = 45° (ATPDraw).



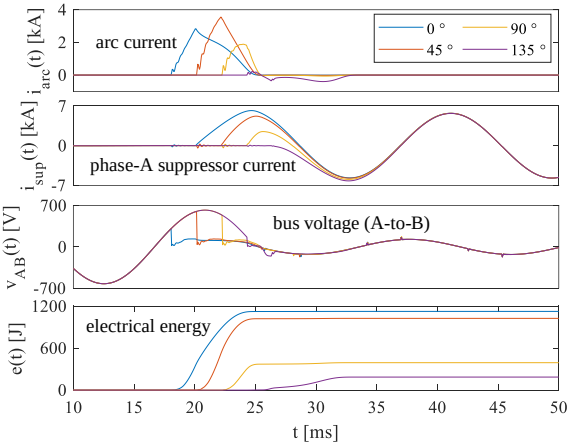
(b) For several values of $|\dot{Z}_x|$ (MATLAB).

Figure 4.31 Waveforms obtained by the simulation of phase A-to-B fault.

Figure 4.32a shows the same result that was verified for phase-to-ground fault: the more resistive the shunt impedance is, the faster the arc current is eliminated and the lower is the arc electrical energy. Last, Figure 4.32b shows that the behavior of phase-to-ground fault is true for phase-to-phase, i.e., the more the value of POW is close to the point where di/dt would be maximum for a bolted fault (48.6° for the system studied in this subsection), the higher is the peak current through the quenching device.



(a) For several values of $\angle\dot{Z}_x$.



(b) For several values of POW.

Figure 4.32 Waveforms obtained by the simulation of phase A-to-B fault.

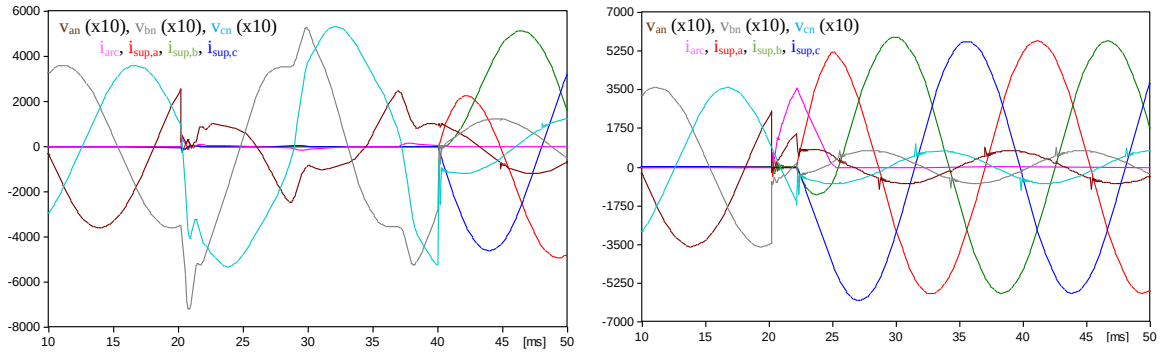
In addition to the original solidly grounded system, it will be included in this work an analysis of the impact of resistance-grounded neutral, which is commonly found

in industrial facilities (IEEE, 2007). In general, the value of the resistance R_N is calculated so that bolted single-phase to ground fault has RMS current limited to 5 A. Then (4.10) must be satisfied. Solving for R_N, one will obtain 50.8 Ω.

$$\left| \frac{440/\sqrt{3}}{\dot{Z}_S + R_N} \right| = 5. \tag{4.10}$$

Figure 4.33a presents the waveforms observed for phase A-to-ground fault under the base-scenario adopted throughout this subsection: $|\dot{Z}_x| = 50\%$, PF = 45° and POW = 45°. The time at which the quenching device is activated was changed to 40 ms so that the reader can see that the arcing fault does not even start. Phase-to-neutral voltages are distorted, though.

Phase-to-phase fault has been also simulated under the base-scenario which parameters are $|\dot{Z}_x| = 25\%$, PF = 45° and POW = 45°. As it is shown in Figure 4.33b, nothing changes in comparison with the case where the neutral is solidly grounded.



(a) Phase A-to-ground fault.

(b) Phase A-to-B fault.

Figure 4.33 Waveforms obtained by the simulation of a fault in a resistance-grounded neutral system.

A null power factor leads to the maximum time for current commutation from the fault to the quenching device, resulting in the highest possible released electrical energy, while PF = 1 results in lower energy. However, the lowest voltage at the busbar is obtained when the power factor of the shunt impedance is equal to the power factor of the system equivalent impedance, as shown in Figure 4.34 for the power system analyzed in this subsection. This is the best for avoiding fault restrike and should be adopted. Since the X/R ratio of industrial power systems are often high, the resistive part of the shunt impedance tends to be small. Having an inductive shunt impedance is advantageous as a turn-on snubber for the thyristors. Moreover, since POW = PF

leads to the maximum peak current through the quenching device, this should be agreed as the reference situation for the design.

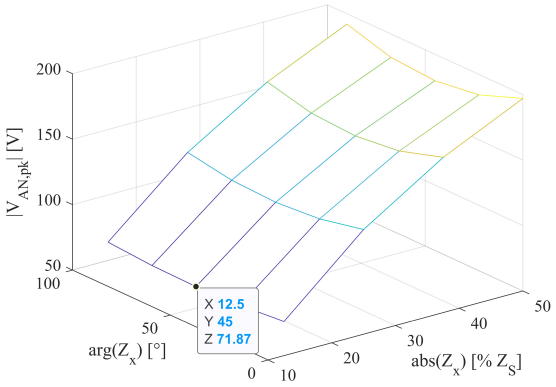


Figure 4.34 Peak phase voltage as a function of angle and module of $\dot{Z}_x$.

Figure 4.35 shows the waveforms for one of the thyristors of phase A branch during event of Figure 4.33b.

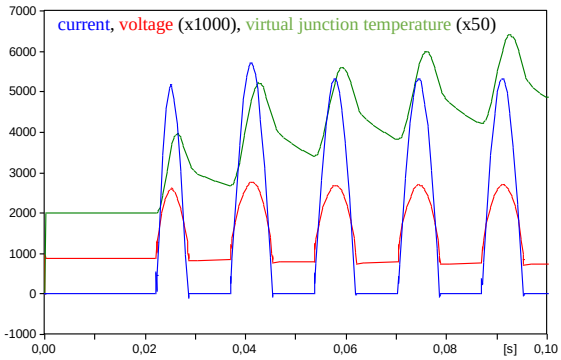


Figure 4.35 Waveforms representative of thyristor behavior during the event of Figure 4.33b.

4.3.2 Three-Phase Complete Modeling and Solution

The analytical solution of a three-phase arcing fault in a deep level like the presented in Subsection 4.1.2 is more complex to achieve. Therefore, the execution of extensive simulation and sensitivity analysis will be done again in this subsection. The objective is to take advantage of the concepts fully explored before in this section and contribute to the safe design of the components of the three-phase solution.

The AF models currently adopted by the industry focus on the calculation of the incident energy levels, being based on equations empirically developed through test data from the laboratory (Nelson et al., 2014). These tests are performed according to procedures described in references (Commission, 2014; IEE, 2018), where the initiating mechanism is a three-phase fault. However, it is experimentally demonstrated in reference (Zhang et al., 2007) that a three-phase arc fault consists of two possible existing partial fault arcs in parallel. Among three possible partial arcs, two must regularly be commutated into a single-phase fault arc when one line current goes through zero. Despite the fact that more than 98% of faults originate as phase-to-ground in industrial systems (Nelson et al., 2014), typically through a catastrophic failure of the insulation, both phase-to-ground and phase-to-phase faults quickly evolves into a three-phase fault within 5 ms (Nelson et al., 2015), for both solidly grounded and HRG neutral. This is the cause of destruction of most LV equipment that operate on solidly grounded 480 V systems.

Fault Modeling

The IEEE Std 1584-2018 (IEEE, 2018) states that there is no difference between the incident energy calculated from tests with bonded and unbonded enclosure. In fact, a comparative evaluation reveals no variation between measured voltages and currents. Therefore, the study presented here will be centered on the analysis of IEEE-NFPA trial #46, which was made with 25 mm gap horizontal busbar fed by a 480 V power system with 20 kA of symmetrical available short-circuit current, power factor of 0.091, surrounded by an unbounded box.

Figure 4.36 shows the waveforms of instantaneous phase voltages (v_{AN}, v_{BN}, and v_{CN}) and line currents (i_A, i_B, and i_C) recorded during the experiment, line voltages (v_{AB}, v_{BC}, and v_{CA}) calculated according to (3.3), conductances (g_{AB}, g_{BC}, g_{CA}) calculated by (3.6), and phase currents (i_{AB}, i_{BC}, i_{CA}) calculated according to (3.5). The measurement data is shown without any filtering.

Since a three-phase arc can be divided into three single-phase alternating arcs, it is possible then to calculate the parameters of their conductances according to (3.1). Table 4.11 presents the obtained values. Phase B is the central one in the horizontal arrangement. The equivalent impedance of the power system used in the test is $\dot{Z}_S = (1.20 + j13.3)$ mΩ and the open circuit line-to-line voltage is 480 V RMS.

Figure 4.37a shows simulation results of this event in ATPDraw. Since the AF quenching device discussed in this work takes no more than 2 ms from the detection of the fault to operate, the modelling and simulation of the arcing fault was performed

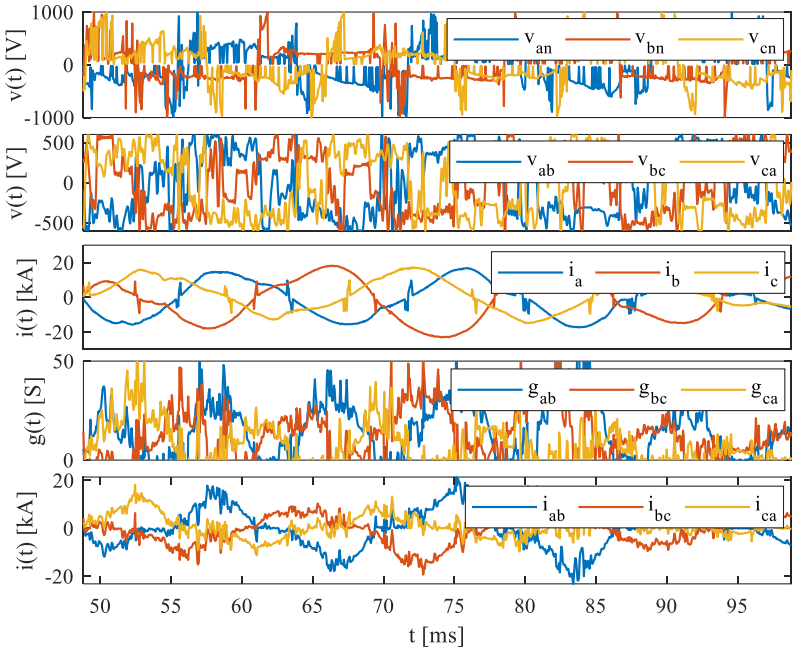


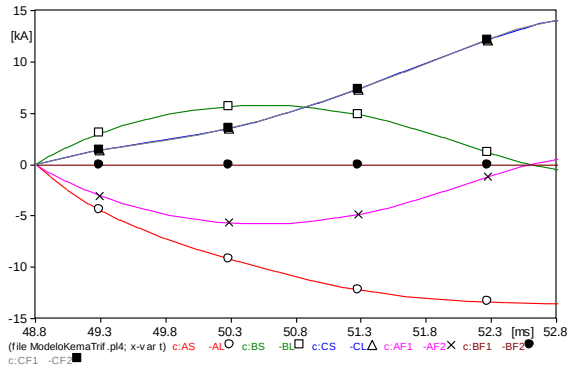
Figure 4.36 Three-phase arcing fault quantities measured during an experiment (phase voltages and line voltages) and derived by calculation (line currents, phase conductances and phase currents).

Table 4.11 Parameters derived for IEEE-NFPA test #46

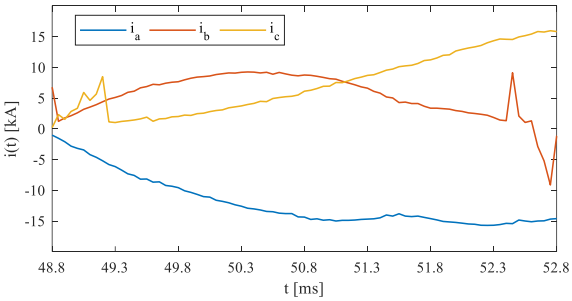
Path	ℓ [mm]	V_O [V/mm]	R_O [$\mu\Omega$/mm]	τ [μs]
AB	25	8.90	384	316
BC	25	9.22	96.5	2400
CA	50	7.00	17.3	341

from 48.8 ms (start of the event in Figure 4.36) to 52.8 ms. During this interval, the current i_{BC} is practically null, which means that only the partial arcs AB and CA are active in the bus. Still regarding the fault model, it was assumed $G_{min,h} = 10$ S for arc AB and $G_{min,h} = 5$ S for arc CA, with $t_{min,h} = 49.2$ ms. For the sake of comparison, Figure 4.37b displays a close view of line current waveforms from Figure 4.36 during the analyzed time interval.

Figure 4.38 shows line and phase fault voltage waveforms from the simulation. For a single-phase fault, it is known that with a 277 V RMS driving voltage - which equates to 390 V peak for a sinusoid - the restrike voltage is about 375 V, followed by a flat-topped voltage of about 140 V (Dunki-Jacobs, 1986; Nelson et al., 2014). It has been shown before in this dissertation that the arc is extinguished if the bus voltage



(a) Line currents (A: red / circle; B: green / square; C: blue / filled square) from the simulation.



(b) Close view from Figure 4.36.

Figure 4.37 Arcing fault current waveforms - simulation vs. measurement.

is quenched to 135 V or less. This results in peak voltage equal to $135 \cdot \sqrt{3} \approx 235$ V between phases. A three-phase fault composed by two partial arcs between phases would be properly eliminated only if this voltage is low enough. The rest of this section is devoted to the analysis of the quenching device effectiveness in this case.

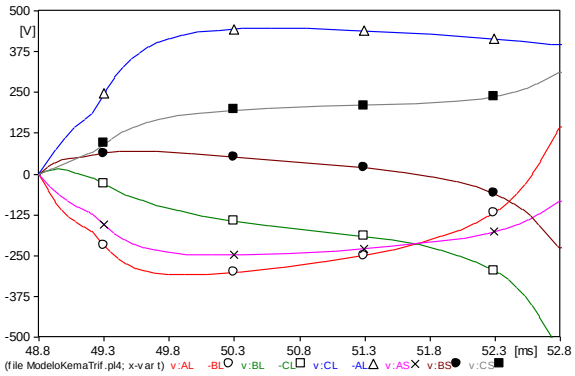


Figure 4.38 Line (A-B, B-C, C-A: red, green, blue) and phase (A-N, B-N, C-N: magenta, brown, gray) arcing fault voltage waveforms from the simulation.

Effectiveness of the Quenching Device for Three-phase Faults

Since the AF quenching device performs a three-phase-to-ground short-circuit once it is operated, then it must be designed for this condition. Considering initially the steady-state operation and balanced grid voltage condition, there is only positive-sequence current through it, according to the Fortescue theorem. Therefore, the three-phase

system can be reduced to a single-phase equivalent for which (4.3) can be applied if the variables are accordingly altered from phase-domain to symmetrical components:

$$\left| \frac{Z_{x,1} + R_{cd,1}}{Z_{S,1} + Z_{x,1} + R_{cd,1}} \right| \cdot V_{S,1} < V_{m,1}, \tag{4.11}$$

where the subscript '1' designates positive-sequence and $V_{m,1}$ is the maximum peak voltage in the busbar. Solving for $Z_{x,1}$ such that $V_{m,1}$ results in phase-to-neutral peak voltage not greater than 135 V, one will obtain $|Z_{x,1} + R_{cd,1}| < 6.1$ mΩ. Considering $X_x/R_x = 5$ and $R_{cd,1} = 110$ $\mu\Omega$, $L_x = 15.9$ μH and $R_x = 1.08$ mΩ. The three-phase short-circuit current of this system is 20.4 kA RMS symmetrical. With the insertion of the shunt impedance Z_x, it turns out that the current through the AF quenching device becomes 14.3 kA. The overall X/R ratio decays from 11.1 to 8.4, which contributes to reduce the dc level in the quenching device current. From (4.5), $t_x^- = 8.0$ ms, and from (4.4) with $V_S = 1.1 \cdot 480 \cdot \sqrt{(2/3)}$ V, $i_{x,sym}(t_x^-) = 22.2$ kA. Finally, $i_{x,max} = 37.4$ kA, based on (4.6).

Since the impedance Z_x calculated for this case has a different value from that obtained for the single-phase case previously discussed in this work, the calculation of the elements of the snubber has to be done again. For the same thyristor (part number N3175HE160) and the same damping ratio (1.25%), one will obtain $C = 3.5$ μF, $R = 1.44$ Ω, $P_r = 7.6$ W, and $I_{pk} \leq 300$ A.

The design of the components for the three-phase quenching device became a simple task. To validate the calculation, the simulation model shown in Figure 4.39 will be executed. The setup is composed by the power supply and AF models from IEEE-NFPA trial #46, the quenching device with the values specified above, a 10 Ω / 1 μH, Y-connected three-phase linear load, and an adjustable three-phase current source. These last two items were included so that the simulation is even more close to the real system. It will be executed initially with the current source deactivated and the following time stamps: the fault starts at 48.8 ms and the quenching device operates at 50.8 ms. See figures 4.40, 4.41a, and 4.41b. A sampling time of 1 μs has been used.

Notice how the clamping of the busbar voltage to 235 V results in the proper quenching of the three-phase arcing fault. Observe also that no undesired transient is seen in the line voltage waveforms, demonstrating the effectiveness of the RC snubber. Finally, notice how the peak current trough the quenching device is according to the predicted maximum value of 37.4 kA that would be verified if it had been turned on 8.0 ms after the zero-crossing of phase voltage. These results are verified when the three phases of the quenching device operate as expected. However, it is worth the confirmation of whether it is true in case of failure.

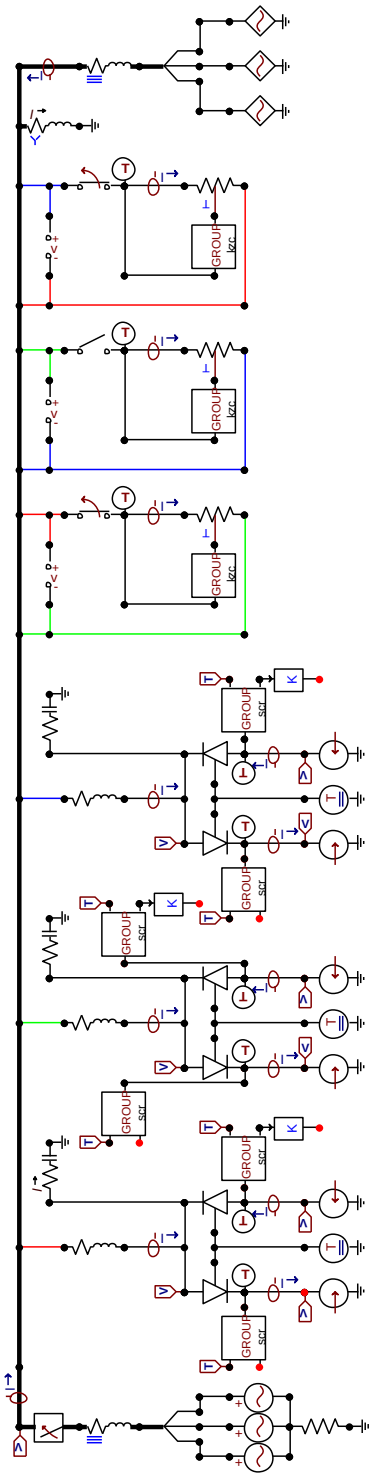


Figure 4.39 Complete simulation model implemented in ATPDraw.

Like verified for the single-phase system previously analysed in this work, the influence of the current source was certified to be insignificant to the effectiveness of the

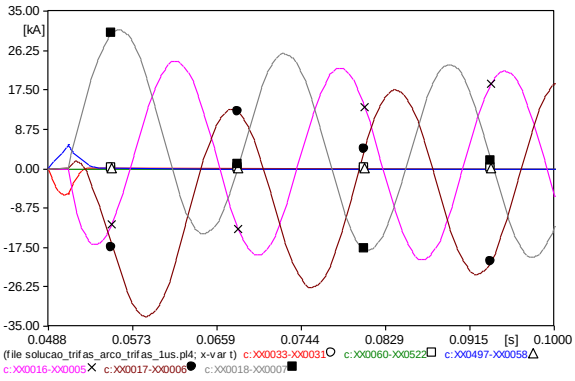
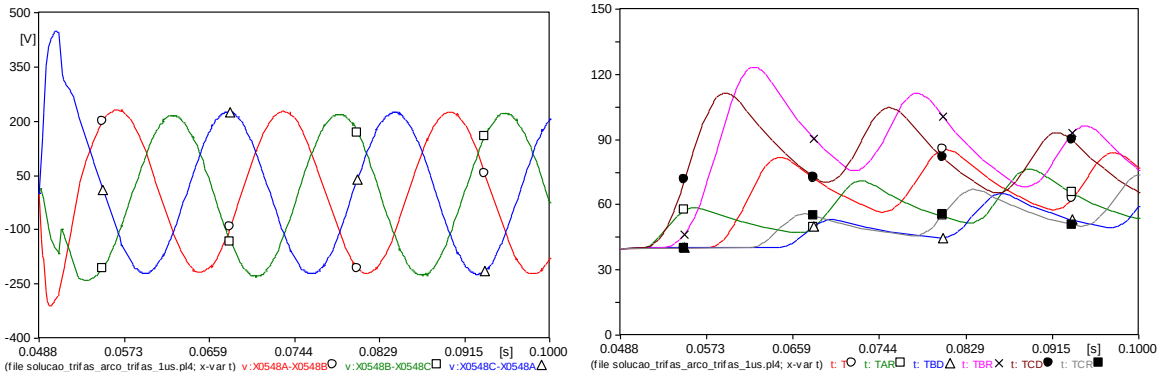


Figure 4.40 Phase current waveforms: arcing fault (A-B, B-C, C-A: red, green, blue) and quenching device (A-T, B-T, C-T: magenta, brown, gray).



(a) Line voltages: A-B (red / circle), B-C (green / square), C-A (blue / triangle).

(b) Instantaneous virtual junction temperature: phase A (red, green), B (blue, magenta), and C (brown, gray).

Figure 4.41 Waveforms from the simulation shown by Figure 4.39.

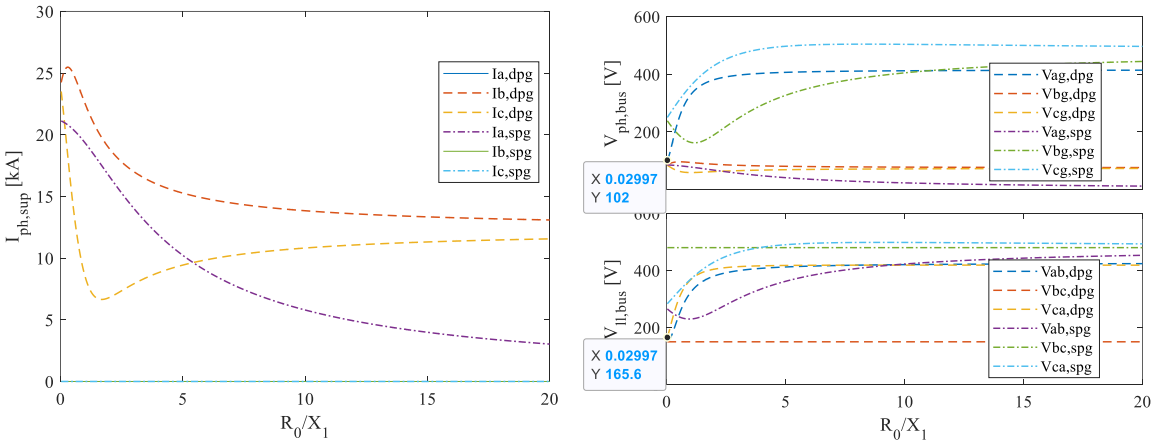
quenching device, even if unbalanced or with harmonic content. Such configurations have been tested with an amplitude of 1 kA.

4.3.3 Failure Analysis

The quenching device discussed in this work must operate successfully whenever requested, i.e., the arcing fault must be eliminated. However, there is the possibility, although remote, that one thyristor or even one entire phase of the quenching device does not work as expected due to a gate-driver failure, bad connection, etc. Two questions arise here: (i) whether the arcing fault is eliminated or not; and (ii) the impact of such condition to the current through the AF quenching device.

Failure of One or More Entire Phases

According to the symmetrical component theory (Grainger and Stevenson, 1994), double- and single-phase-to-ground short-circuit result respectively in currents equal to 173% and 150% of the three-phase current for a solidly grounded neutral system. Despite having no impact over three-phase, three-phase-to-ground and phase-to-phase short-circuit currents, neutral grounding impedance contributes to the decrease of single- and double-phase-to-ground short-circuit currents. Figure 4.42a shows curves relating the steady state RMS phase currents (I_A, I_B, I_C) through the quenching device in case of operation of phases B and C - *double-phase-to-ground* (DPG), and in case of operation of phase A only - *single-phase-to-ground* (SPG), for various values of neutral grounding resistance. Figure 4.42b shows curves for steady state RMS phase and line voltages in the busbar. The power system and the AF quenching device considered are exactly that treated over the previous subsection. In both plots the abscissa axis is presented as the ratio between zero-sequence resistance of the power system (R_0) and positive-sequence reactance of the power system (X_1). According to Subsection 2.1.1, effectively grounded systems are characterized by $0 < R_0/X_1 < 1$.



(a) Quenching device phase currents.

(b) Phase (V_{AG}, V_{BG}, V_{CG}) and line (V_{AB}, V_{BC}, V_{CA}) busbar voltages.

Figure 4.42 Symmetrical RMS quantities obtained when only phases B and C operate (DPG) and when only phase A operates (SPG), as a function of the ratio R_0/X_1 of the power system.

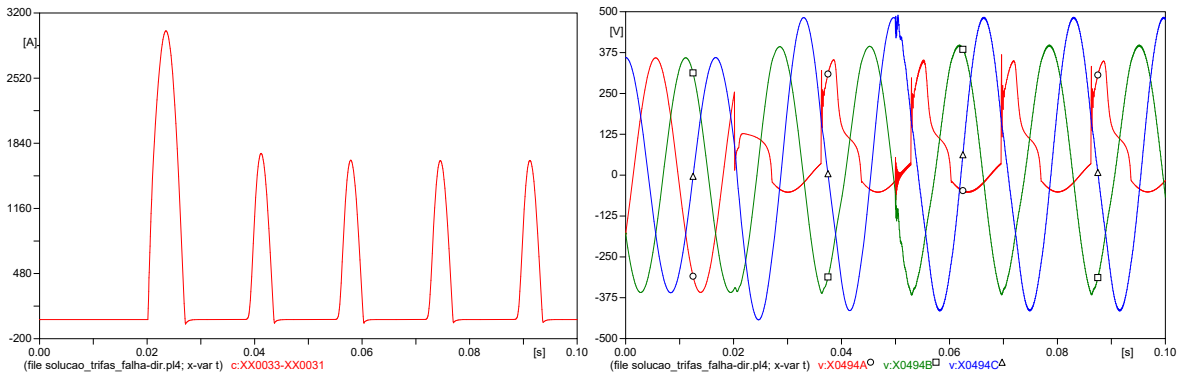
As formerly demonstrated in this work, it is necessary that the busbar peak phase voltage is kept below 135 V to guarantee that a single-phase arcing fault is properly eliminated. For three-phase fault, it is necessary that the line peak voltage is kept below 235 V. It is clear from Figure 4.42b that this is not accomplished for single-phase

operation. For double-phase operation, bus voltages acceptably below the threshold are achieved only for extremely small R_0/X_1. Transient overvoltage has not been considered in this analysis, but it would surely make this scenario even worse. In conclusion, any open-circuit phase failure makes the device incapable of handling both single- and three-phase arc faults. Finally, Figure 4.42a makes clear that the current through the quenching device would be much higher than it is for three-phase operation (14.3 kA), leading to undesired overrating of thyristors and shunt impedance.

Figures 4.42a and 4.42b have been produced based on an algorithm developed and implemented in MATLAB.

Failure of One Thyiristor of a Phase

The simulation results demonstrated below were taken from the single-phase fault, three-phase quenching device case discussed in Subsection 4.3.1, with $L_x = 23.4$ μH and $R_x = 8.8$ mΩ and considering the failure of one of the thyristors of phase A by not triggering it in the simulation. In order to reach the worst-case scenario, the thyristors of the other phases have been not triggered as well. Figure 4.43a shows the waveform of the current through the arcing fault, while Figure 4.43b illustrates the line-to-ground busbar voltages. Notice how the voltage is effectively clamped only during the negative half-sine period.

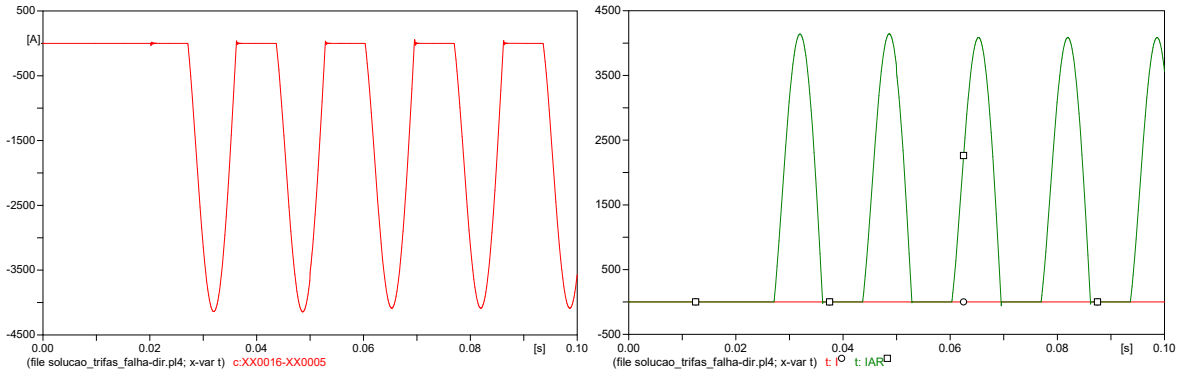


(a) Fault current.

(b) Bus voltage: phases A (red / circle), B (green / square), and C (blue / triangle).

Figure 4.43 Waveforms obtained for the AF quenching device operating without the downward thyristor of phase A during a phase A-to-ground fault.

Figure 4.44a represents the waveform of the current through phase A of the electronic quenching device, while Figure 4.44b displays the current waveforms through the thyristors of the phase A of the quenching device.

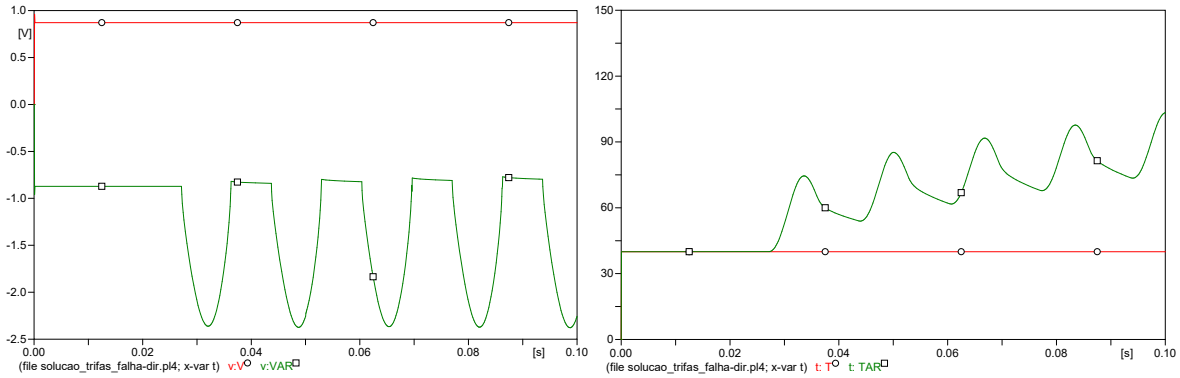


(a) Quenching device (branch A) current.

(b) Currents through the thyristors of phase A of the quenching device.

Figure 4.44 Waveforms obtained for the AF quenching device operating without the downward thyristor of phase A during a phase A-to-ground fault.

Finally, Figure 4.45 shows the voltage drop and the virtual junction temperature calculated for both thyristors. Notice that since the current through the thyristor that did not operate is null, its voltage drop is represented solely by the first term of the right side of (2.17).



(a) Voltage drop.

(b) Virtual junction temperature.

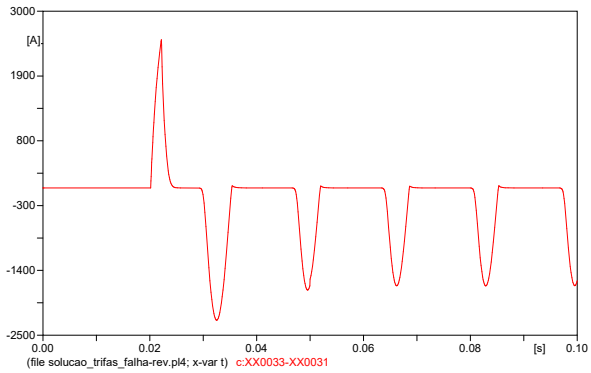
Figure 4.45 Waveforms obtained for the AF quenching device operating without the downward thyristor of phase A during a phase A-to-ground fault.

The results show that the current through the arcing path is eliminated for more than half the time during the fault and that the voltage across the arc is reduced even during some of the time interval when the current through the thyristor is null. It is enough to conclude that the AF quenching device can contribute to the reduction of the incident energy even under a failure[17]. The failure of the other thyristor of the same

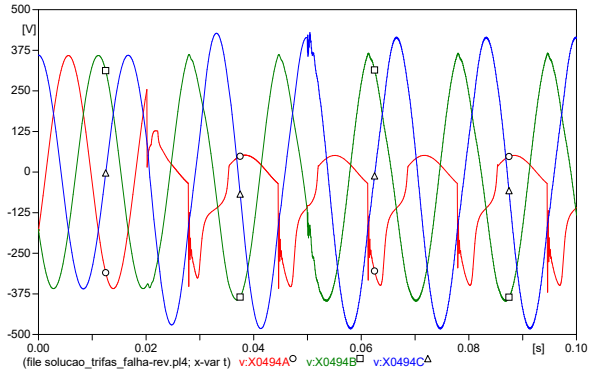
[17]Remember: it is not the goal of this work to evaluate IE levels.

phase has been also simulated. The results are very similar to those presented above, as it can be seen in Figure 4.46. The main difference is that the device that remains active is now directly biased at the instant the quenching device starts operating (22.1 ms), thus promptly cutting down the fault current right at its beginning.

There are many other conditions that should be evaluated to fulfill a complete failure analysis on the AF quenching device, notably whether: (i) the type of fault is different from that evaluated here; (ii) the thyristors (one or more) of the other phases are operating normally; (iii) the damaged device belongs to a phase diverse from that one in which the fault is taking place. The simulation of these combinations along with the evaluation of the results will be left as a recommendation for a future work.

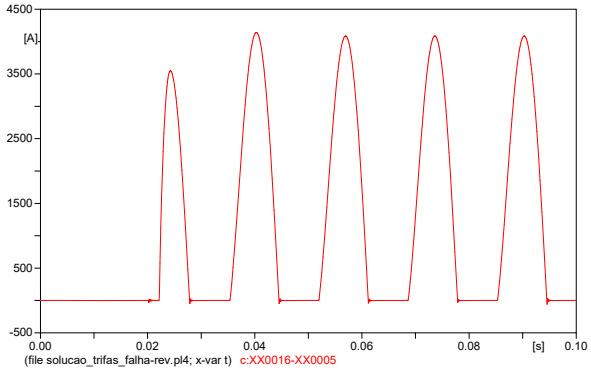


(a) Fault current.

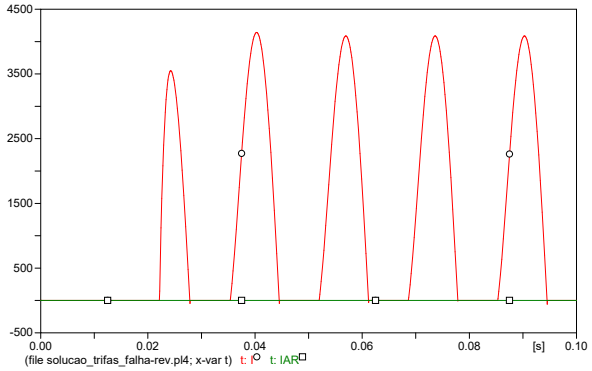


(b) Bus voltage: phases A (red / circle), B (green / square), and C (blue / triangle).

Figure 4.46 Waveforms obtained for the AF quenching device operating without the upward thyristor of phase A during a phase A-to-ground fault.

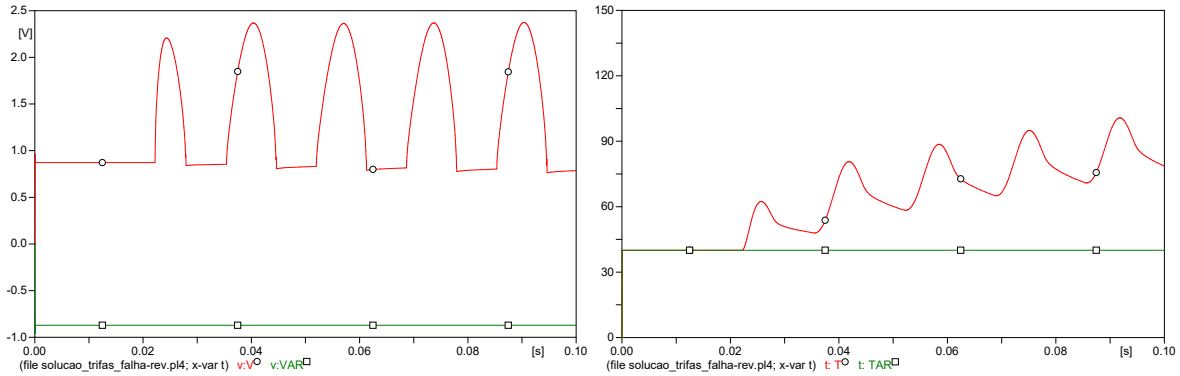


(a) Quenching device (phase A) current.



(b) Currents through the thyristors of phase A.

Figure 4.47 Waveforms obtained for the AF quenching device operating without the upward thyristor of phase A during a phase A-to-ground fault.



(a) Voltage drop.

(b) Virtual junction temperature.

Figure 4.48 Waveforms obtained for the AF quenching device operating without the upward thyristor of phase A during a phase A-to-ground fault.

Early Failure Detection

A procedure for the online assessment of the overall AF quenching device can be performed by means of triggering the thyristors of a given phase slightly before the zero-crossing of the respective phase voltage. It is expected that the thyristor that is forward biased turns on immediately and turns off by natural commutation at the zero-crossing of the current. The measurement of the current through the quenching device path during this interval allows the verification of its appropriate operation. To test both thyristors that compose the electronic switch, it is necessary one activation for the negative and another for the positive zero-crossing. The main disadvantage of this scheme is that it demands the implementation of a phase-control algorithm. On the other hand, such procedure is useful for many purposes. First, it performs a complete system verification, including the gate-drivers, programmable devices, cabling, etc. Second, diagnostic functions can be run also during this test, providing information on the overall system health. Notice that this task runs independently of planned maintenance jobs and occurrence of arcing faults, besides being carried out online. It can be set to be executed automatically once a day, for example. Figure 4.49 gives an example of the application of this technique for the thyristors associated with the negative zero crossing, for the power system studied in this section.

4.4 Experimental Results

In this section, the experimental setup and the collected results will be explained in details. The presentation of the achievements will be done in the same order they have

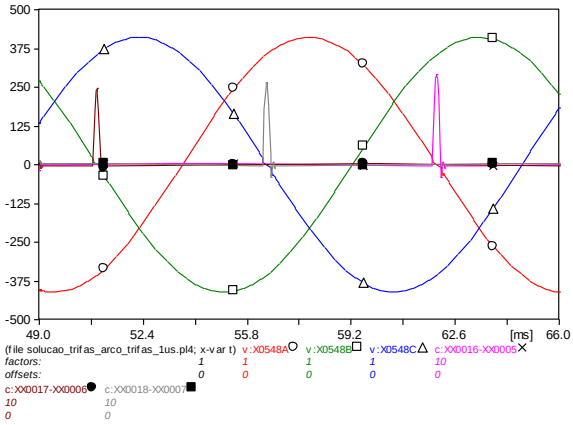


Figure 4.49 Example of online verification of the quenching device operative status.

been produced over time. Schemes, photos and oscillograms have been incorporated to the text to illustrate the findings.

4.4.1 Test Setup

In view of the tests that should be executed to validate the propositions of this work and the particularities brought by the current levels involved in these experiments, a special test setup had to be built.

There are two power supplies that could be used for the experimental tests presented, both three-phase, solid grounded neutral, according to Table 4.12. Each one comes from the secondary side of a dedicated Δ-Y power transformer that feeds the laboratory. For a phase-to-phase-to-ground bolted fault, the short-circuit current values would increase to[18] 173%.

Table 4.12 Main characteristics of the available test power system

V_r [V]	R_{Th} [mΩ]	L_{Th} [μH]	X_{Th}/R_{Th}	$\dot{Z}_{Th}$ [mΩ]	I_{sc} [kA]
220/127	9.9	30.7	1.17	15.2$\angle$49.5°	5.6
440/254	33	100	1.14	50.0$\angle$48.6°	3.4

Upstream Current-Limiting Reactors

For the sake of personal safety and asset preservation, current-limiting reactors have been calculated to be installed in series with the power system, so that both the

[18] According to Fortescue teorem. For phase-to-ground fault, the current increases 150%, and for phase-to-phase fault it decreases to 86.6%.

bolted and arcing fault currents would be reduced. The upstream protective devices between the transformer secondary and the spot where the tests will be executed are a slow-acting 300 A fuse model 3AC1 and a backup 300 A thermomagnetic CB, model TJK438300 from GE, with the magnetic trip adjusted at its maximum value of 3.0 kA. Even with the current-limiting reactors, it is possible that these devices actuate.

Since unbalanced short-circuit currents are being considered in this study[19], a bank composed by three single-phase, dry-type, air-core reactors has been adopted. By doing so, these elements can be applied also as the shunt impedances inside the prototype, if desired. The values of 20 μH and 40 μH have been chosen based on the 440 V power system, which has the highest Thévenin equivalent impedances and therefore need higher values of reactance, i.e., 1 μH is more significative in the 220 V than in the 440 V system. For the 440 V system, 20 μH will produce three-phase short-circuit current reduction to a value slightly higher than 75% of the original level, while 40 μH will reduce it to a level way below 75%. Moreover, these reactors can be associated to achieve a current level below 50% of the prospective three-phase bolted fault current. Notice that the steady-state current through these devices is null. A very conservative rate of 2.4 was considered for the asymmetry factor. It is way above that one that correspond directly to the X/R ratio of the laboratory[20].

Since such reactors are not off-the-shelf items, their price have been found to be almost prohibitive. At the time these items have been bought (March, 2021), the cost were roughly BRL 13,000 each, including taxes. They have been assembled using aluminium as the conductor, and still the mass of each piece achieved 25 kg, with dimensions of roughly 30 cm x 30 cm x 50 cm (widht x length x height).

Characterization of the Power Thyristors

The experiments have been done by feeding the high-voltage side of a single-phase, multi-tap testing transformer and by providing a low-impedance connection at the low-voltage side by short-circuiting it through the *device under test* (DUT), which is the ac switch composed by two antiparallel thyristors (namely T_{odd} - left, upward - and T_{even} - right, downward - in case of PCT or PPT) as shown[21] in Figure 4.50, or a single device in case of BCT. Since the nominal ratio of the transformer is 660/600/550/480/440:15,

[19] Which would incur in zero-sequence magnetic flux in a three-phase reactor.
[20] $\kappa < 1$, see Figure 3.3 again.
[21] The native upstream protective devices - a CB and a fuse - have been not represented.

a high current value was expected to flow in the secondary side[22], compatible with the levels of the surges previously defined in Table 4.4.

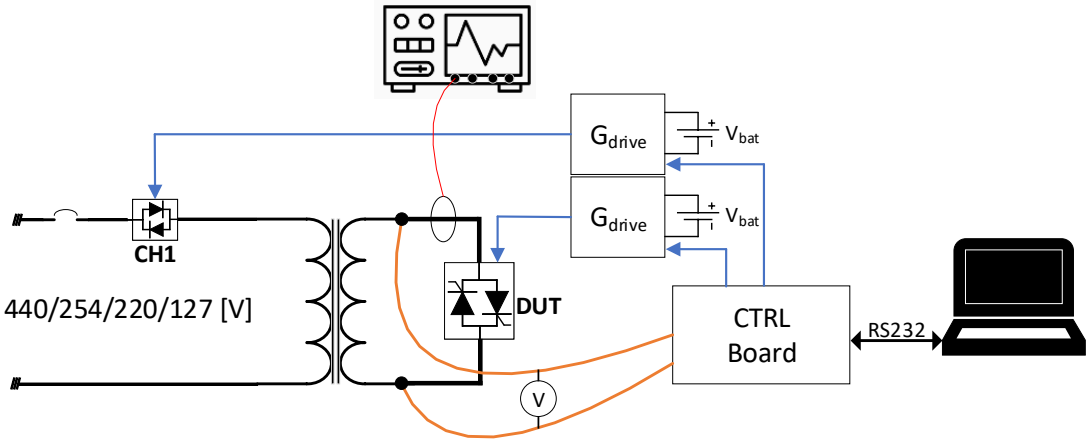


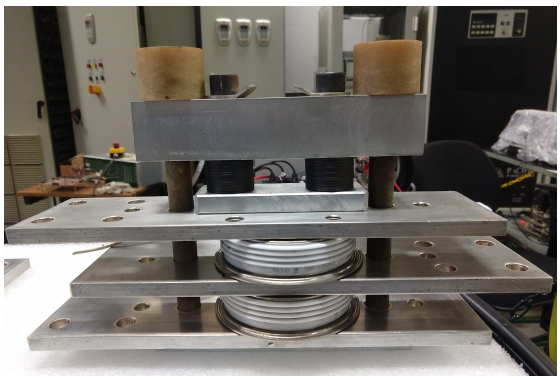
Figure 4.50 Simplified schematic of the experimental setup for surge current application.

The electronic switch CH1 is also composed by two thyristors connected in antiparallel, but its function is to connect the power supply to the transformer primary, which is the high-voltage, low-current side. The DUT is connected to the transformer secondary, which is the low-voltage, high-current side. Isolated, 6 kHz pulse gate-drivers have been employed for firing the thyristors. The test starts by closing the switch CH1 to allow the magnetization (inrush) of the transformer. Then the open-circuit secondary voltage is measured and a *phase-locked loop* (PLL) algorithm is executed so that the thyristors of the DUT start being fired at a previously defined point of the wave. Then the high current surge initiates. A preset time interval is then waited for before opening the switch CH1, finishing the test. The thyristors of the DUT are kept being triggered all over the test, mimicking as best as possible the real conditions that they will be subjected to in the real application - the AF quenching device. For safety purposes, the interface between the control board of the test system and the user was implemented to be done remotely by means of push buttons and emergency switches.

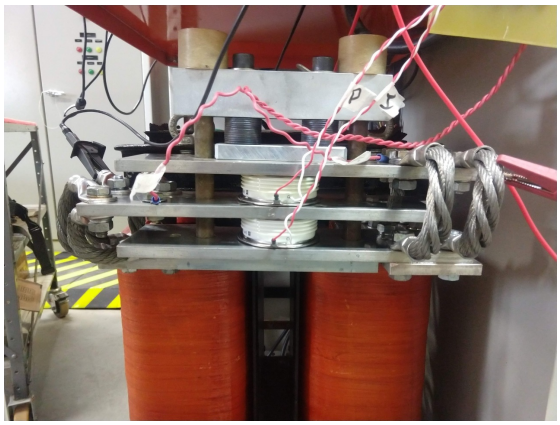
The transformer tap, the value of the power supply voltage (127 V, 220 V, 254 V or 440 V), the point of the 1st quarter of the sinusoidal wave at which the test starts (from 0 to 90°) and the duration of the test (number of cycles) are adjustable. The values of these variables are explicitly detailed for each one of the results that will be presented below. These parameters were calculated in order to reproduce as close as possible

[22]This transformer was specifically designed so that it withstand up to 25 kA of secondary RMS current during a time interval up to 1 s each 15 min. It is a very peculiar equipment specifically designed for this project. The secondary side is formed by a single turn made of aluminum bars.

the surges #1, #2, #3 and #4 of Table 4.4. Each surge was applied to a brand-new switch, which was assembled strictly according to the data sheet recommendations (Switzerland, 2013) - see Figure 4.51 below.



(a) Thyristors assembled in the clamping unit.



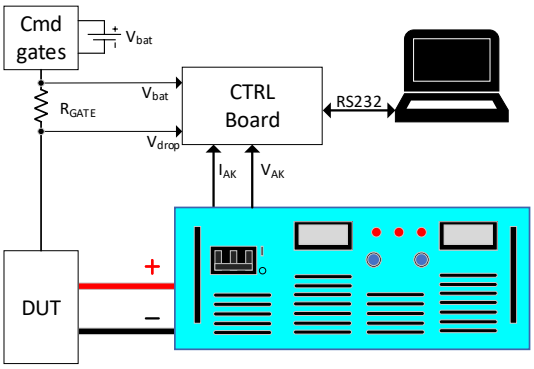
(b) ac switch connected to the transformer.

Figure 4.51 Preparation of an ac switch for the application of a surge current.

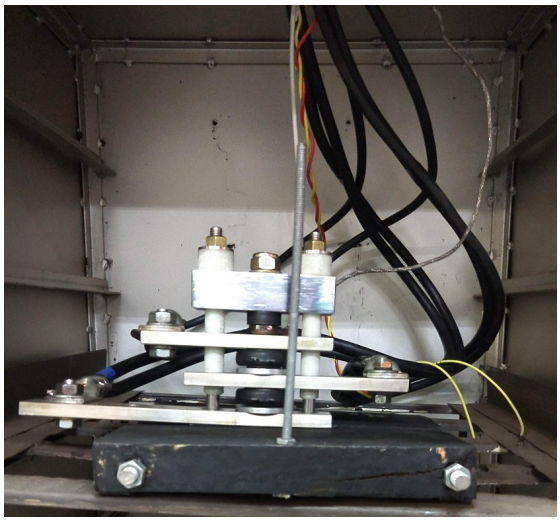
In addition to the setup prepared for the application of ac current surges, an arrangement has been built to the characterization of the thyristors, as it can be seen in Figure 4.52. Right after being submitted to a current surge, the devices are inserted into a heat chamber and their resistance is measured at a known temperature (under thermal equilibrium) by means of an insulation resistance meter[23]. A multimeter has been utilized as well for the measurement of low resistances found in cases where the device was damaged and it could not be verified by means of the high resistance meter. Then a known dc current profile is applied by means of a dc, high-current power supply[24] controlled in closed loop, and the voltage drop across the device is measured and compared with the results obtained before that surge.

Figure 4.53 shows the complete test bench, including measurement and control apparatus. It is a very flexible setup that includes both ac and dc, high-amplitude current sources and confers repeatability to the experiments. The variables are registered by the oscilloscopes and also by means of a serial communication link between the dc power supply and the microcomputer. This test setup opens the possibility to the execution of future works on the same field of the AF quenching device, like power electronics-based short-circuit current-limiting devices for onshore oil platforms, for example.

[23]Model MIC-10K1 from Sonel.
[24]Model ESS from TDK-Lambda.



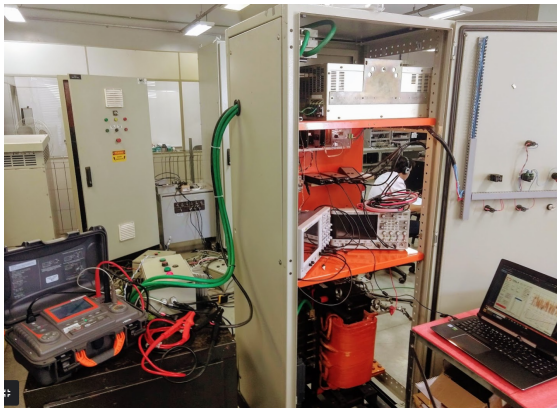
(a) Test scheme.



(b) Heat chamber.

Figure 4.52 Experimental setup for thyristor characterization.

(a) Protection / command panelboard (left) and test setup (right).



(b) Heat chamber (left), dc supply (right, top), measurement (center) and transformer / DUT (bottom).

Figure 4.53 Overview of the built test bench including measurement / control devices.

4.4.2 Experiments on Power Thyristors

This subsection presents experimental results regarding tests with the thyristors previously evaluated in Subsection 4.2 via simulations. The execution of these experiments has the main goal of validating the design procedure formerly discussed in Subsection 3.2.2 for the calculation of the ride through capability of a thyristor submitted to single- or multi-cycle power-frequency, variable amplitude current sine-waves. Such procedure allows for the prediction, during design phase, of the possibility of catastrophic

failure of a given thyristor exposed to any ac sinusoidal current waveform. These conditions have been chosen so that the device is exposed to operational circumstances close to those that will be found in the AF quenching device. Since a large number of experiments have been accomplished, only the most interesting will be shown here.

The flowchart of Figure 4.54 below presents the test procedure that has been adopted in this work, where N_s is the number of ac tests that a given ac switch was subjected to. New current surges were applied one at a time and the devices have been characterized right after it. This strategy has been carried out until the a failure has been detected in a device by means of the characterization test. The application of a new surge has not been done until the devices have cooled down to ambient temperature. The application of the ac current surge will be called here a "test", as it has been before in the simulations (see Table 4.6 again). The name "surge" will be applied from now on referring to one of the current profiles aforementioned in Table 4.4, which by their turn are related to one of the thyristors of the ac switch (a sequence of half-sine waves). The terms "set" and "device" still have exactly the same meaning of Subsection 4.2, i.e., the part numbers considered in this subsection are exactly the same that have been modeled and simulated. The test was performed on an ac switch composed by two thyristors (T_{odd} and T_{even}), but the characterization was done separately on each one of the devices that compose the switch.

Since the upstream power system, including the multi-tap transformer, had equivalent reactance high enough to limit device di/dt, no turn-on (neither turn-off) snubbers have been inserted for these tests. Table 4.13 presents the sequence followed for the execution of the experiments. The results will be presented ahead in this section. For devices #1, #2, and #8, the loop contained in the flowchart of Figure 4.54 has been carried out 15, 11 and 18 times respectively. For device #1, the 15 ac tests have been divided between four clamps as explained below:

- Thyristors T_7 and T_8 have been subjected to tests from AC_06 to AC_15. Device T_7 has been detected to be damaged[25] during the characterization test after ac test AC_15.
- Thyristors T_5 and T_6 have been subjected to tests from AC_03 to AC_05. Device T_5 has been damaged by ac test AC_04.
- Thyristors T_3 and T_4 have been subjected to test AC_02. Device T_3 was damaged after the test.

[25]Such condition has been previously planned to happen, as it will be shown later.

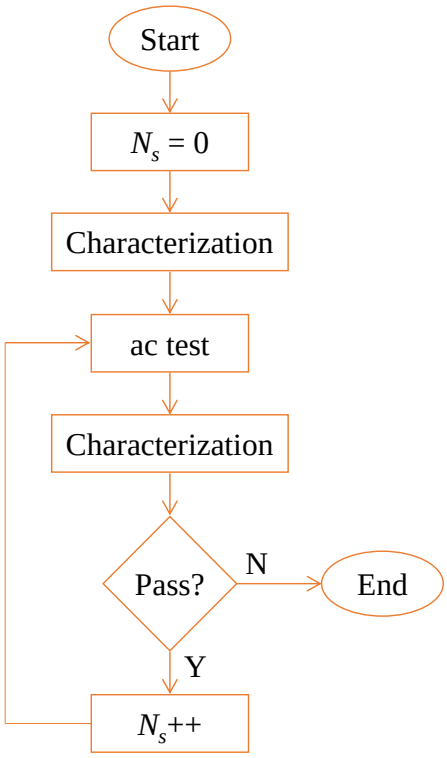


Figure 4.54 Flowchart of the experiments.

- Thyristors T_1 and T_2 have been subjected to test AC_01, being the device T_1 verified as damaged by means of the characterization test performed after the ac test.

In each case, the failure of a thyristor has been detected by means of the characterization test at $N_s = 10$ for the clamp formed by T_7 and T_8, $N_s = 2$ for the clamp[26] formed by T_5 and T_6, and $N_s = 1$ for the clamps formed by T_3/T_4 and T_1/T_2.

For device #2, all the 11 tests have been applied to the same single clamp composed by T_9 and T_{10}, while for device #8, all the 18 tests have been applied to the clamp formed by T_{11} and T_{12}.

The waveform of the current programmed in the current source (see Figure 4.52a again) for the characterization of the devices was composed by a slope with increasing current ($\approx$ 1 kA/s) followed by a step with decreasing current ($\approx$ 1 kA/μs). This waveform has been applied for the characterization of all the devices along all the executed batteries of tests.

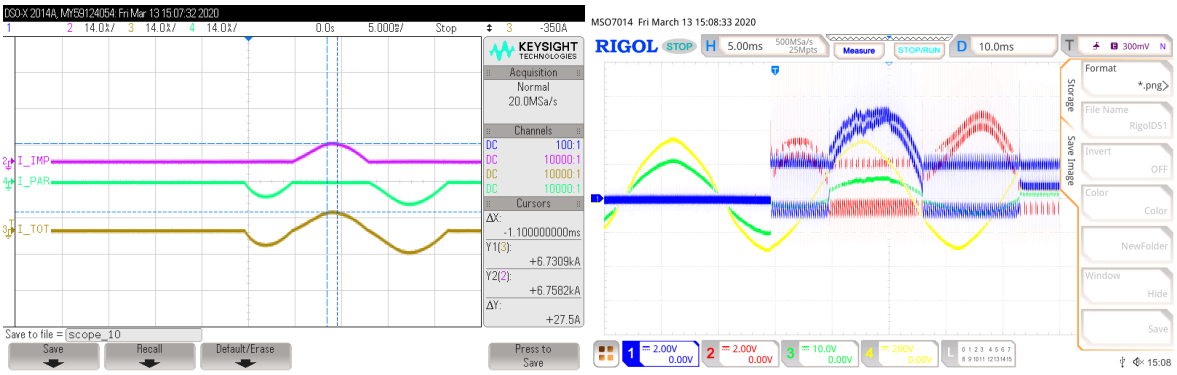
[26]When the test AC_05 was performed, the switch was already damaged.

Table 4.13 Characteristics of the tests and the devices that were tested

Test	*Surge*	*Set*	*Device*	T_{odd}	T_{even}
AC_15	#3	#1	#1	T_7	T_8
AC_04	#4			T_5	T_6
AC_02	#1			T_3	T_4
AC_01	#2			T_1	T_2
AC_11	NA		#2	T_9	T_{10}
AC_18		#3	#8	T_{11}	T_{12}

Device 1 / Test AC_15

Figure 4.55a shows the registered waveforms of the secondary current (Ch_3), current through thyristor T_8 (Ch_4) and current through thyristor T_7 (Ch_2), while primary voltage (Ch_4) and secondary voltage (Ch_3) waveforms are shown[27] in Figure 4.55b. Thyristor T_8 is the one that was submitted to a current waveform with the characteristics of surge #3 previously defined in Table 4.4. Figure 4.56 shows a comparison between measured and theoretical voltage drop across T_8, as well as between measured[28] and theoretical power and virtual junction temperature. The calculations have been made both by discrete-time recursive convolution and equivalent power pulse methods. As one can notice, minimal difference is verified between the results.



(a) Secondary current (Ch_3 - yellow), i_{T_8} (Ch_4 - green), and i_{T_7} (Ch_2 - magenta).

(b) Primary (Ch_4 - yellow) and secondary (Ch_3 - green) voltages. Ch_2 (red) and Ch_1 (blue) are the gate-to-cathode voltages of the thyristors.

Figure 4.55 Waveforms registered during test AC_15.

As previously calculated, thyristor T_8 did not fail due to surge #3. The electrical resistance of the device was measured before and after surge, at $T_{htc} = 40$ °C, where

[27] Gate-to-cathode voltages have been also registered, but they will not be used in this work.
[28] And indirectly calculated from the measured variables.

T_{htc} represents the temperature adjusted in the heat chamber for the characterization test. The results are presented in Table 4.14. A negligible change is observed.

Table 4.14 Electrical resistance of thyristor T_8 measured at 40 °C, before and after the application of surge #3

T_{htc} [°C]	R_{ak} [MΩ]		R_{ka} [MΩ]	
	Before	After	Before	After
40	354	318	341	292

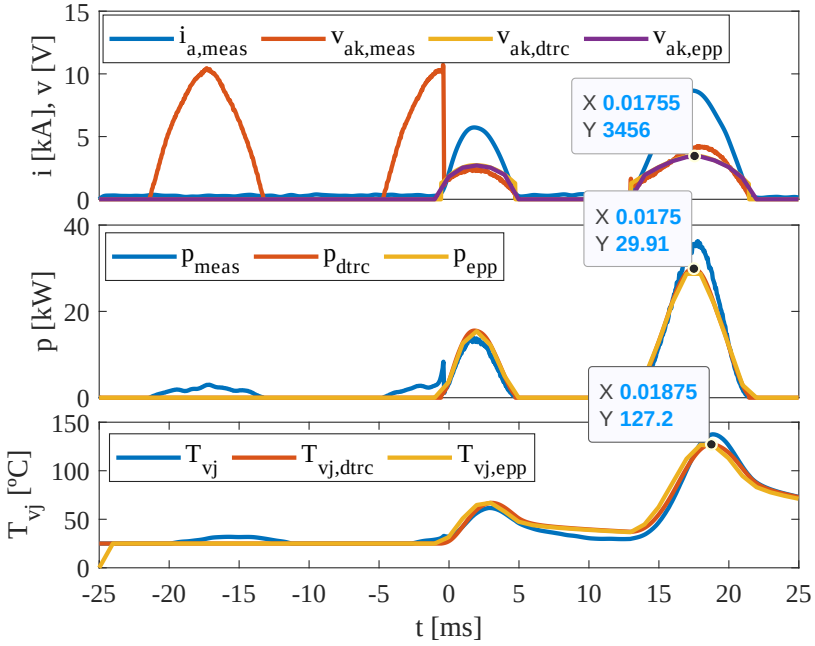
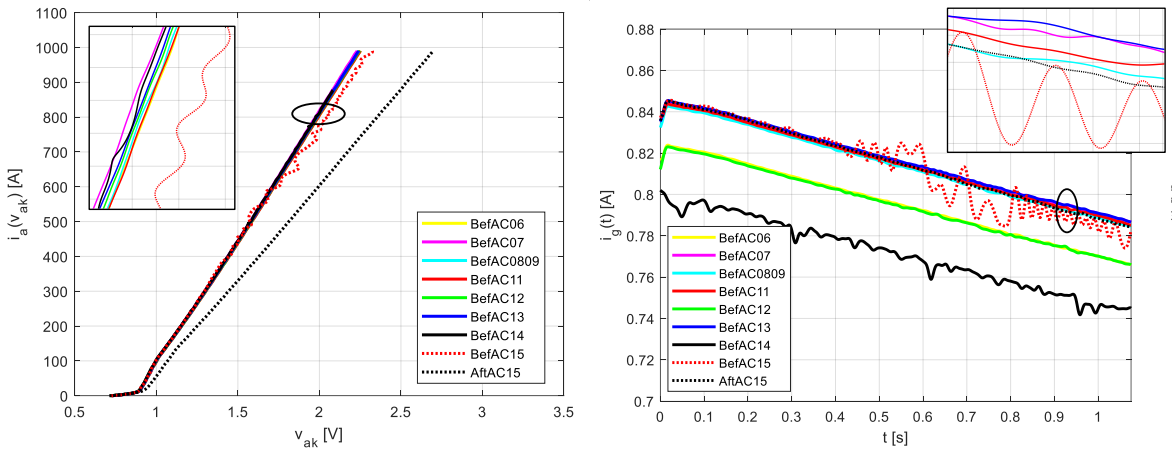


Figure 4.56 Comparison between measured and calculated voltage, power and virtual junction temperature, using DTRC and EPP techniques for thyristor T_8 submitted to surge #3. Data tips in mV.

Subsection C.1.1 presents the results collected from T_8 along the execution of the sequence defined in Figure 4.54, including both surge and characterization tests. In this case, the ac switch was subjected to tests from AC_06 to AC_15, being them executed at lower current levels in the beginning, by the application of lower voltages to the upper taps of the transformer. This was done this way to avoid the operation of a surge current profile harsher than that defined by #3.

In addition to the verification that T_8 would in fact support the surge #3, such a long test sequence allowed the achievement of the degradation of T_7, as it can be seen in Figure 4.57. It shows the results collected during the characterization tests of the

device along the execution of the ac tests. As one can observe, the voltage drop across the device has increased. The interested reader may find the complete test results for this device in Subsection C.2.1, particularly in Figure C.11.



(a) Slope part of the anode current waveform. (b) Gate current.

Figure 4.57 Characterization of T_7 at $T_{htc} = 60°C$.

Detailed information on device #1 can be found in reference (Semikron, 2018).

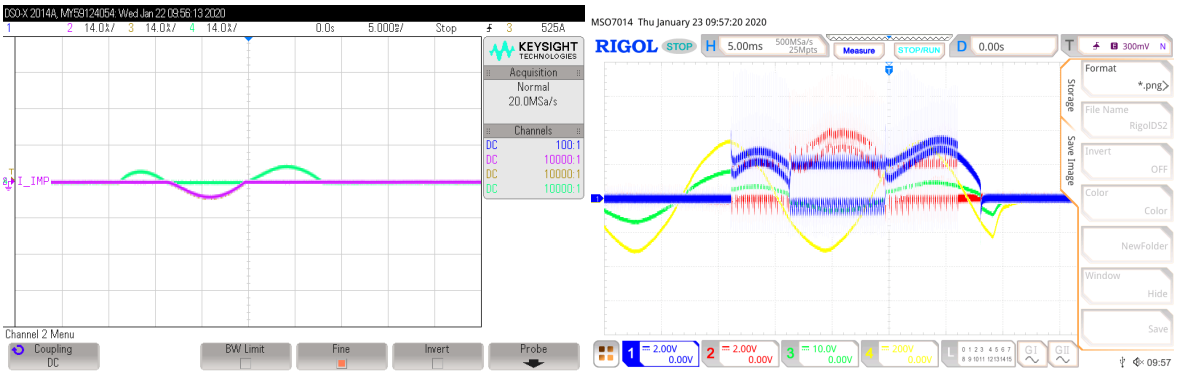
Device 1 / Test AC_04

Figure 4.58 presents the waveforms recorded during test AC_04. Figure 4.59 shows a comparison between measured and calculated quantities for thyristor T_6. Again, calculated values show great concordance with measured ones. There is practically no difference between electrical resistances of the device measured before and after the application of the current surge. Table 4.15 presents the measured values, which were obtained at 60 °C and at 40 °C.

Table 4.15 Electrical resistance of thyristor T_6 measured at 60 °C and 40 °C, before and after the application of surge #4

T_{htc} [°C]	R_{ak} [MΩ]		R_{ka} [MΩ]	
	Before	After	Before	After
60	55.8	53.3	59.3	56.1
40	277	280	289	292

The results have proven that thyristor T_4 in fact can ride through the surge profile #4. The complete results can be found in Subsection C.1.2. Additionally, T_5 has failed by degradation, as one can verify in the results presented in Subsection C.2.2.



(a) i_{T_6} (Ch_4 - cyan) and i_{T_5} (Ch_2 - magenta). (b) Primary (Ch_4 - yellow), secondary (Ch_3 - green), and gate-to-cathode (Ch_2 and Ch_1) voltages.

Figure 4.58 Waveforms registered during test AC_04.

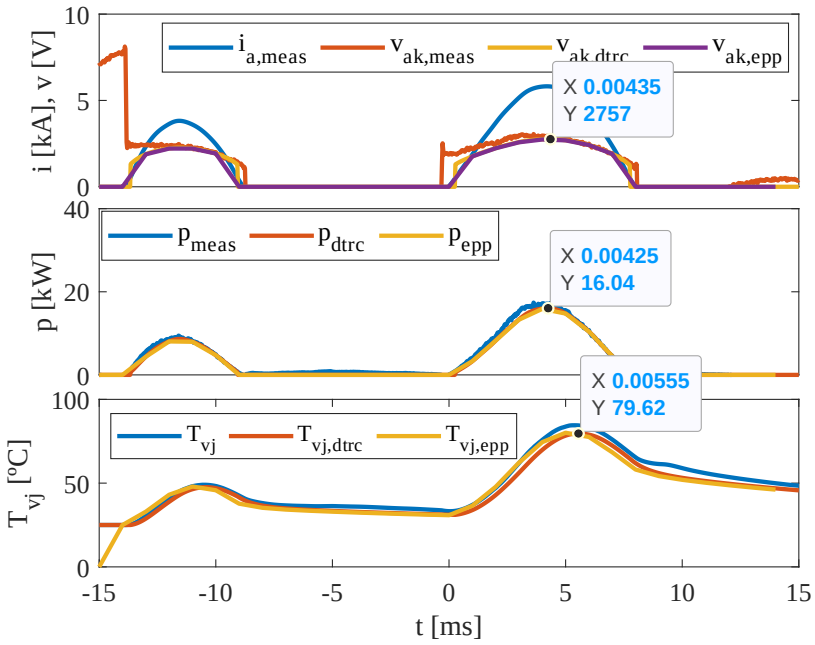
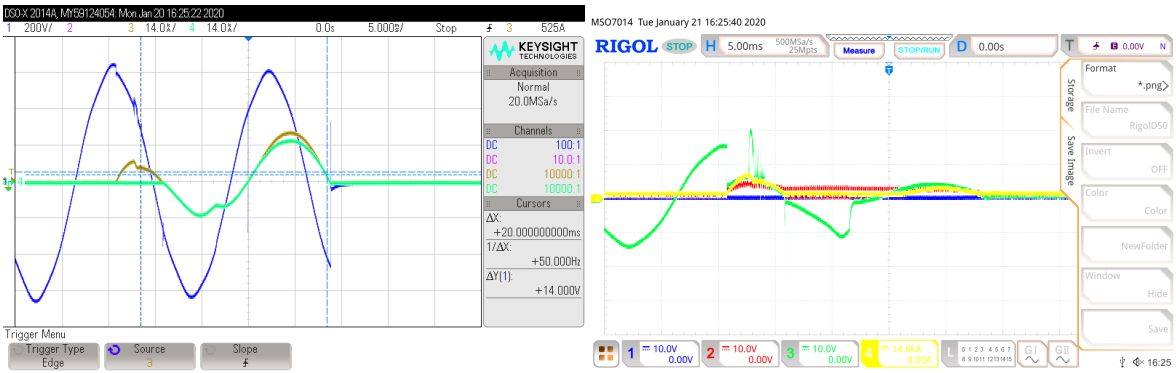


Figure 4.59 Comparison between measured and calculated voltage, power and virtual junction temperature, using DTRC and EPP techniques for thyristor T_6 submitted to surge #4. Data tips in mV.

Device 1 / Test AC_02

Figure 4.60a shows the registered waveforms of primary voltage (Ch_1), secondary current (Ch_3) and current through thyristor T_3 (Ch_4), while secondary voltage (Ch_3) and current through thyristor T_4 (Ch_4) are shown in Figure 4.60b. As one can notice, T_4 carries current first in this test, while the secondary voltage is positive, and then

T_3, when the voltage becomes negative. At some point in the waveform, a transient is verified where the resistance of T_3 appears change to a lower value (the voltage decreases while the current increases). When the voltage becomes positive again, thyristor T_3 keeps carrying current. The peak current through T_4 is now extremely below the value it has reached at the beginning of the test. T_3 failed catastrophically, as it was anticipated for device #1 subjected to surge #1. The device has carried 13 kA, but it failed at some point after this.



(a) Primary voltage (Ch_1 - blue), secondary current (Ch_3 - yellow) and i_{T_3} (Ch_4 - cyan).

(b) Secondary voltage (Ch_3 - green) and i_{T_4} (Ch_4 - yellow).

Figure 4.60 Waveforms registered during test AC_02.

Figure 4.61 shows that there is an expressive difference between measured and calculated voltage, power and virtual junction temperature. The actual (estimated) temperature reaches almost 300 °C and the device fails catastrophically. Measured values of electrical resistance of the device before and after the test are presented in Table 4.16. A measurement at 25 °C was included. It shows that the resistance is highly dependent on the temperature even after the catastrophic failure and that it may not be easily detectable at ambient temperature, since the value of the resistance is highly below its original value but at the same time is extremely above the typical value verified for a short-circuit condition.

The overal measurement results can be find in Subsection C.2.3. Figure C.17 is particularly relevant because it shows that the resistance of the damaged device became highly sensitive to the temperature.

Device 1 / Test AC_01

Figure 4.62 shows the waveforms recorded during this test. The odd thyristor was the first to start conducting in this test. As it can be seen, the device failed catastrophically

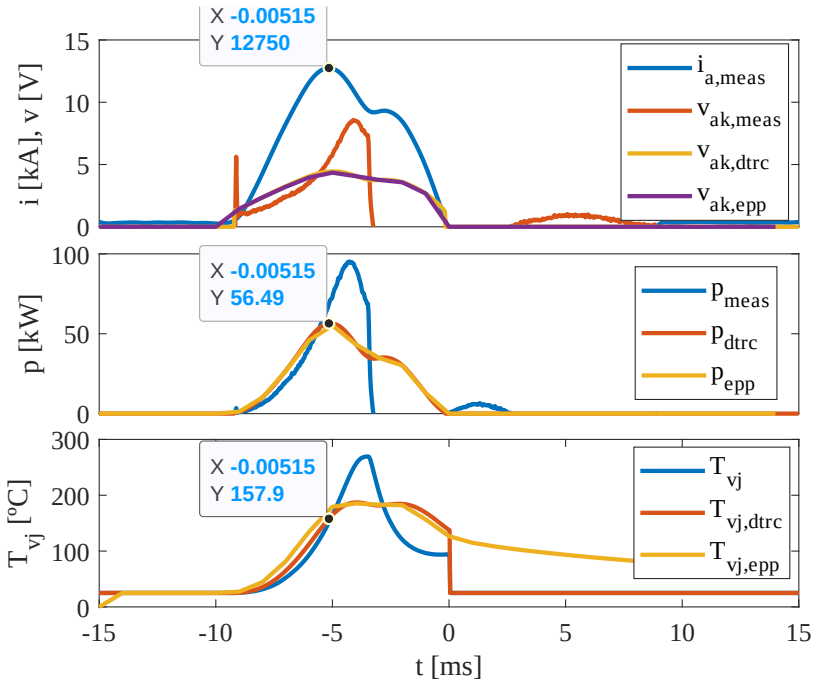


Figure 4.61 Comparison between measured and calculated voltage, power and virtual junction temperature, using DTRC and EPP techniques for thyristor T_3 submitted to surge #1. Data tips in mV.

immediately after the 15 kA peak. As in surge #1 (test AC_02), the current waveform changes its pattern after 15 kA: instead of falling, its value keeps rising even under decreasing voltage. This change has to do with the huge difference seen between measured and calculated quantities, which are now even more accentuated than in case of surge #1, as it can be seen in Figure 4.63. Another difference is that the resistance of the device is now low even after it has cooled down to ambient temperature, as it can be seen in the data presented by Table 4.17.

Table 4.16 Electrical resistance of thyristor T_3 measured at different temperatures, before and after the application of surge #1

T_{htc} [°C]	R_{ak} [MΩ]		R_{ka} [MΩ]	
	Before	After	Before	After
60	67.2	$15.0{\cdot}10^{-8}$	61.9	$15.0{\cdot}10^{-8}$
40	327	$24.0{\cdot}10^{-8}$	313	$24.0{\cdot}10^{-8}$
25	-	$55.0{\cdot}10^{-2}$	-	$66.0{\cdot}10^{-2}$

Figure 4.62 Primary (Ch_1 - blue) and secondary (Ch_2 - magenta) voltage, secondary current (Ch_3 - yellow) and i_{T_3} (Ch_4 - cyan) – surge #2.

Table 4.17 Electrical resistance of thyristor T_1 before and after the application of surge #2

T_{htc} [°C]	R_{ak} [MΩ]		R_{ka} [MΩ]	
	Before	After	Before	After
60	66.7	-	65.2	-
40	406	-	400	-
25	-	$1.00 \cdot 10^{-6}$	-	$1.00 \cdot 10^{6}$

The results collected during the execution of the tests are fully presented in Subsection C.2.4 for T_1. Thyristor T_2 had not any change observed in its terminal characteristics after the tests, as it can be find out in Subsection C.1.4.

As it has been disclaimed before in this text, the microscopic evaluation of the devices is out of the scope of this work. Even so, some of the devices have been sawed after the tests so that their inner structure could be visualized. Figure 4.64 shows photographs of thyristors T_1 and T_5 after being divided into two parts. Notice how T_5 exhibits charred portions that can be seen with the naked eye.

Up to this point, the proposals presented in this dissertation for the calculation of the voltage drop (which is an extrapolation - it has not been presented by the manufacturer data sheet at the levels reached during the surge), virtual junction temperature (which is an estimation - it cannot be physically measured) and dynamic energy dissipation have been successfully proof. The differences verified between voltage measurement and calculation are mainly due the connection of the differential voltage probes - it could not be perfectly repeated between the tests because the probes had

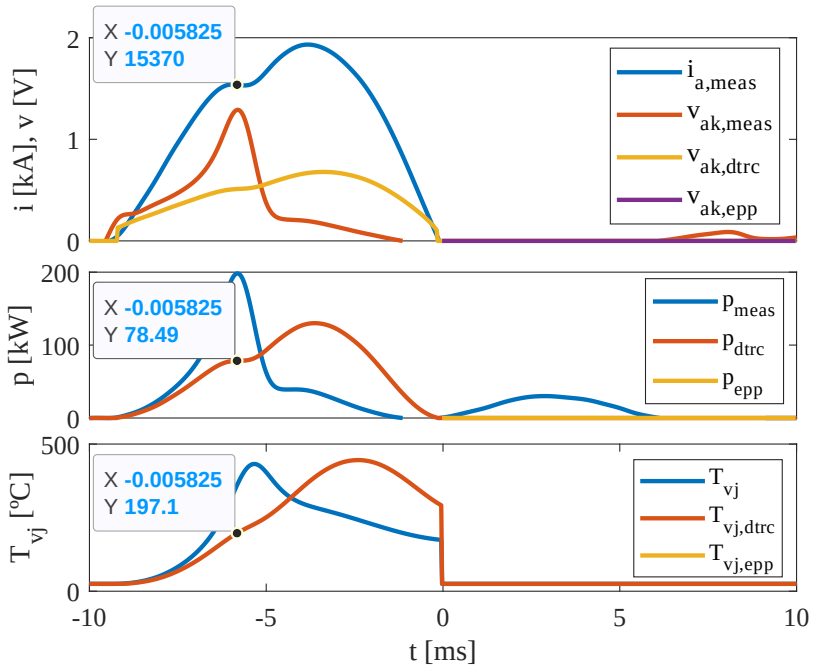


Figure 4.63 Comparison between measured and calculated voltage, power and virtual junction temperature, using DTRC and EPP techniques for thyristor T_1 submitted to surge #2. Data tips in mV.

(a) T_1, after current surge #2.

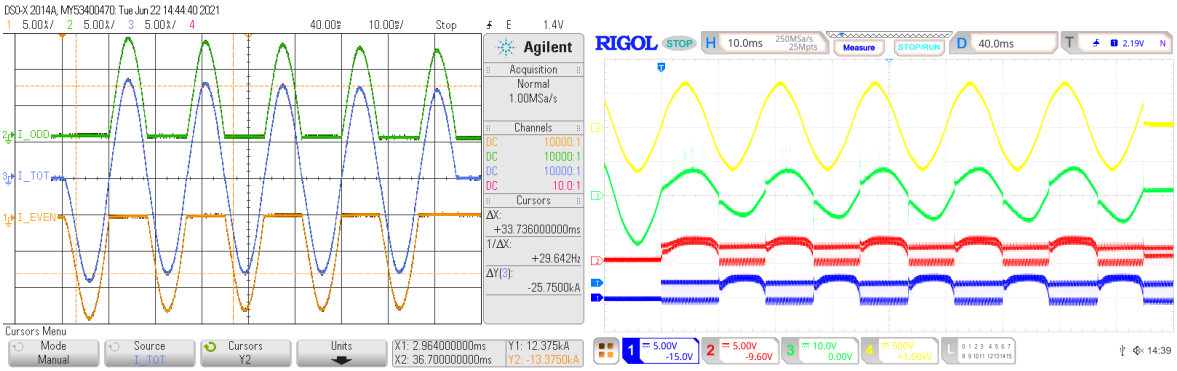
(b) T_5, after current surge #4.

Figure 4.64 Pictures of the damaged thyristors.

to be connected after each ac test and reconnected again before the execution of a new one. In the case of the characterization tests, some variation in the measurements can be surely attributed to the variation of the temperature of the heat chamber between the tests - it could not be perfectly repeated over the tests as well, and the temperature control of the equipment were performed by means of a single sensor, which does not represent the mean temperature inside the chamber.

Device 2 / Test AC_11

Just like in the simulations, the experiments have been performed over other thyristor models to give generality to the study presented in this work - see Table 4.13 again. Detailed information of device #2 can be found in reference (ABB, 2020). The clamp formed by T_9 and T_{10} has been subjected to 11 ac tests with progressively increasing current. Figure 4.65 shows the waveforms recorded during test AC_07, which has been executed by feeding the 660 V tap of the transformer by the 440 V power system. Before this test, not even a minimal variation in the properties of the device has been detected during the characterization tests - the resistance of the device (both T_9 and T_{10}) during blocking state was $\approx$ 54 MΩ and the leakage current was $\approx$ 20 μA at 1 kV and 60 °C. After the application of test AC_07, the forward blocking resistance of device T_9 has fallen down to $\approx$ 12 kΩ.



(a) Current through the ac switch (Ch_3 - blue) and i_{T_9} (Ch_2 - green).

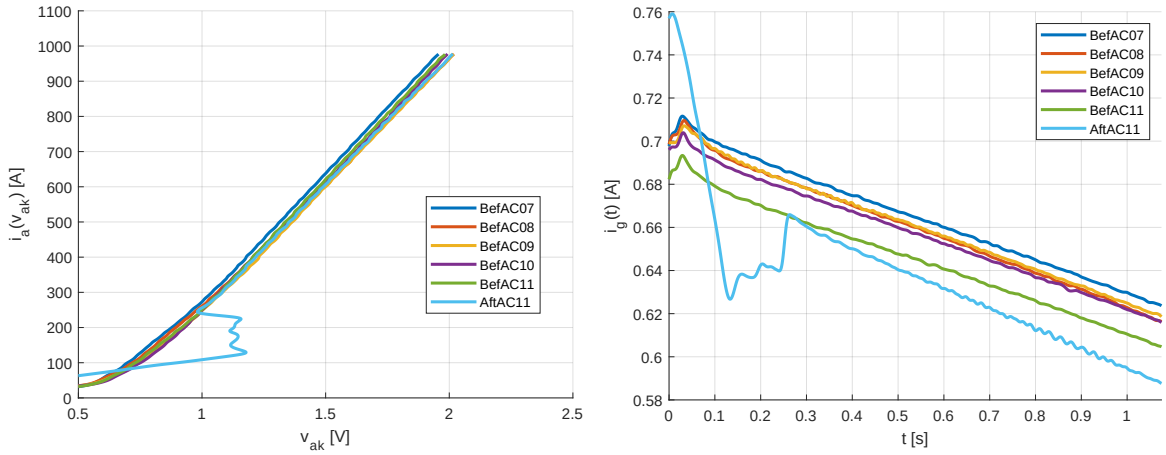
(b) Gate-to-cathode voltage of T_9 (Ch_1 - blue), primary (Ch_4 - yellow) and secondary (Ch_3 - green) transformer voltages.

Figure 4.65 Waveforms registered during test AC_07 (dvc #2).

Then tests AC_08 and AC_09, both identical to AC_07, have been executed and no change has been verified in the characterization tests. Then the power supply has been connected to the 600 V tap of the transformer instead of the 660 V tap, and test AC_10 has been executed. After the experiment, the forward blocking resistance of

device T_9 has fallen down to ≈ 1 kΩ, but its reverse blocking resistance did not change. Finally, test AC_11, identical to test AC_10 has lead to the failure of the device. Its resistance has been verified to be as low as 100 mΩ.

Figure 4.66 shows the results of the characterization tests (specifically the verification of the forward characteristic at 60 °C is presented in the figure) all over the execution of the ac tests. It is clear that after the execution of test AC_11 the forward voltage drop of the device became higher, at least for the low-current portion of the curve, indicating that the device has failed. Due to the high quantity of tests needed to reach the failure, it is not possible to state if it can be characterized as a catastrophic failure or a wear-out failure - which is more probable.



(a) Slope part of the anode current waveform.

(b) Gate current.

Figure 4.66 Characterization of T_9 at $T_{htc} = 60$ °C.

Device 8 / Test AC_18

Figure 4.67 presents the oscillography captured during a 20 kA surge current applied to the clamp composed by T_{11} and T_{12}, in which device #8 (Littelfuse, 2016b) has been utilized. Based on the data sheet information, and applying the design procedure of Subsection 3.2.2, it was estimated that the device could safely ride through 20 cycles[29]. However, one should bear in mind that in the design procedure proposed in this work, it is considered that there is no heat transfer from junction to the case in the calculation of T_{vj}, which tends to be false (yet conservative) for long (≥100 ms) surge current profiles. On the other hand, the part of the procedure based on the calculation of c_d is valid without reservations for all the I_{TSM} (or $I_{T(OV)}$) range presented by the

[29] i.e., 20 half-sine waves, one every single power-frequency cycle.

manufacturer in the data sheet curves. For the device evaluated in this subsection, the maximum is 100 cycles. Therefore, the results achieved tend to be conservative as the duration of the current surge becomes higher. In the test discussed here, the device T_{11} failed during the 22nd cycle. It has totally lost its voltage blocking capability, both forward and reverse. In fact, the simulations previously ran in Subsection 4.2.4 for $T_{vj}(0) = 40$ °C, $f = 60$ Hz, $\theta_{hc} = 90°$ and $X/R = 1.8$ for $I_{sym,pk} = 20$ kA and $N_{cyc} = 5$, which are conditions close to that at which this experiment has been initially performed[30], it was expected that the device would nor reach $T_{vj,max}$ neither c_{max}.

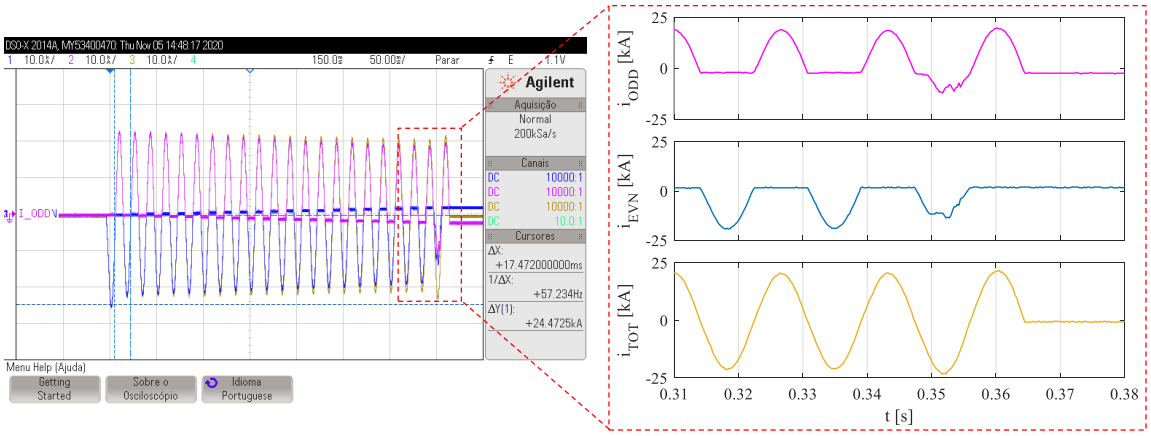


Figure 4.67 Waveforms registered during test AC_18 (dvc #8). Current through the switch (Ch_3 - yellow) and current through T_{11} (Ch_2 - magenta).

Another important consideration is that at this point of the experimental tests, the laboratory setup available for this work was being used at its full capability. It was not possible to increase the current amplitude, then the only possibility left was to increase the duration of the test to achieve the damage limit of the device[31].

4.4.3 Complete Prototype

This subsection presents the development of the prototype of a switchgear that has been built to be subjected to real arcing fault tests. It is a 440 V equipment composed by three columns: incoming (where the power system is connected), eliminator (which abrigates the electronic AF quenching device) and feeder (where the arcing fault is produced by a thin bare copper wire). The design and specification of the elements of the quenching device for such prototype are detailed below.

[30] ac tests AC_01, AC_02, ..., have been executed with a lower duration.
[31] This the main reason why device #1 has been fully explored in this dissertation.

Shunt Impedances

The current-limiting reactors previously discussed in Subsection 4.4.1 have been specified so that they could be used for the reduced current level tests to be performed at 220 V and 440 V in the laboratory. Besides, it has been taken into account the possibility of utilizing them as the shunt impedances of the prototype. However, the prototype is intended to be tested at the conditions that it would be subjected to in field, basically a feeding power system with rated short-circuit of 25 kA and[32] $X/R = 13$. From these information, one can calculate the upstream equivalent impedance $\dot{Z}_{Th} = 11.1\angle 85.6°$ mΩ at 60 Hz, i.e. $R_{Th} = 851$ $\mu\Omega$ and $L_{Th} = 29.3$ μH. The short-circuit peak current for other types of fault can be calculated as well: $1.732 \cdot 25$ kA $= 43.3$ kA for phase-to-phase-to-ground, $1.5 \cdot 25$ kA $= 37.5$ kA for phase-to-ground and $0.866 \cdot 25$ kA $= 21.6$ kA for phase-to-phase fault, considering a solid-grounded neutral. Though the execution of single-phase-to-ground arcing fault tests is possible and this type of fault is a real possibility in practice, IEC TR 61641:2014 (Commission, 2014) and IEEE Std C37.20.7 (IEE, 2018) define that a switchgear or MCC must be submitted to three-phase arcing faults without ground when tested under internal AF conditions. Therefore, this is the case that will be considered.

Notice that in this scenario the equivalent impedance of the upstream power system is significantly lower than the value previously calculated in the simulations considered in Subsection 4.3.2 ($\dot{Z}_{Th} = 13.4\angle 84.8°$ mΩ at 60 Hz). Moreover, the X/R ratio is now slightly higher than that of the simulations (13 instead of 11). These constraints demand that the value of the shunt impedance is lower than that adopted in the simulations, which were $L_x = 15.9$ μH with a quality factor equal to 5. Finally, the voltage level is lower (440 V instead of 480 V), the bus gap of the prototype that has been built for this work is higher (50 mm instead of 25 mm), which contributes to increase the voltage necessary to sustain the arcing fault, and there is a parasitic inductance due to the roughly 2 m of busbar that exists along the column where the AF quenching device is installed, which results in a self inductance of 2 μH (Electronics, 2019). Among all these factors, only the increased bus gap would allow for the increase of the shunt impedance value. All the others demand that the impedance is reduced. Together with all of these theoretical aspects, the previous experience that the authors had with the reactors specified and bought as shown in Subsection 4.4.1 demonstrated that they are excessively expensive, heavy and bulky to be used as the shunt impedances of the prototype. Moreover, the inductance of the smaller of them, which is 20 μH, is still higher than the value of 15.9 μH that was achieved previously in the simulations,

[32] Values informed by Petrobras.

turning it not adequate for the tests that are to be performed at the conditions close to those found in the industry. On the other hand, the minimum value of 2 μH should be met as it has been calculated in (3.8). For all the above, a reactor has been built in the laboratory to be used in the experiments. It is a 2-turn, 40-cm diameter coil assembled using a 120 mm^2 450/750 V PVC insulated power cable. Its inductance has been previously calculated using the online tool aforementioned in Subsection 3.2.1. Both the teoretical and measured[33] values were equal to 3.2 μH. Such a low inductance will cope with all the requirements, besides resulting in a busbar voltage less than 135 V peak considered in the simulations previously presented in this work[34].

Figure 4.68a shows the coil already installed into the switchgear prototype. The price was negligible, as well as the efforts to assemble the coil. It was securely held using pressure connectors and nylon straps. Notice how the design became compact. It opens up the way to assemble the electronic AF quenching device completely inside a single compartment. More studies have to be done on the determination of the best cable gauge and the arrangement of the three coils to avoid the effects of mutual inductance. In this case, the linear length of the cable is $\ell_{cbl} = 2 \cdot (\pi \cdot d_{coil}) = 2.5$ m, where d_{coil} is the diameter of the coil. Since the per-length resistance of a 120 mm^2 cable is $R_{dc} = 0.15$ mΩ/m (at 70 °C) (Group, 2020), then the quality factor of the coil at 60 Hz is equal to 3.2. Higher values can be achieved by using higher gauge cables, at the cost of difficulting the assemble of the coil inside the compartment. For the sake of comparison, the quality factor the 20 μH reactor[35] purchased is 6.8.

Power Thyristors

For the assemble of the prototype, a thyristor model with parameters very similar to those previously adopted in the simulations of Subsection 4.3.2 (N3175HE160) (Westcode, 2014) has been utilized: part number N3533ZC200 (Westcode, 2021). It is completely compatible with the experiments executed in this work, besides being immediately available for assemble.

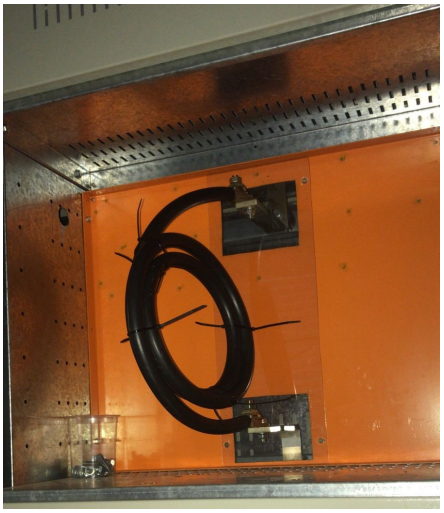
Turn-off Snubbers

Since the thyristors have identical ratings in comparison to those of the device adopted in Subsection 4.3.2 as the reference for the design, the turn-off snubbers have been

[33]The measurement has been performed using a LCR meter model Agilent 4263B.

[34]This has to do with personal safety as well - for the first trials, it is better to be conservatively than optimistic.

[35]Its dc resistance ($\approx$ 1.1 mΩ) (see Figure 4.68b) has been measured by using a low resistance meter model MMR-620 from Sonel.



(a) Shunt reactor manually assembled.

(b) Commercial reactor.

Figure 4.68 Basic pictures representative of the reactors.

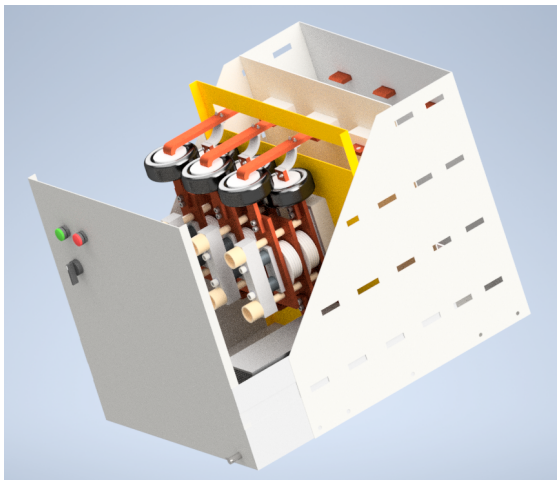
kept as calculated there. The part numbers respectively specified for the resistor and the capacitor are presented below:

- PWR221T-30-1R50F / Bourns: $R = 1.25\ \Omega$ / $P = 10$ W.
- C4ATMBW4470A3LJ / Kemet: $C = 4.6\ \mu$F / $I_{pk} = 600$ A at 120 Hz.

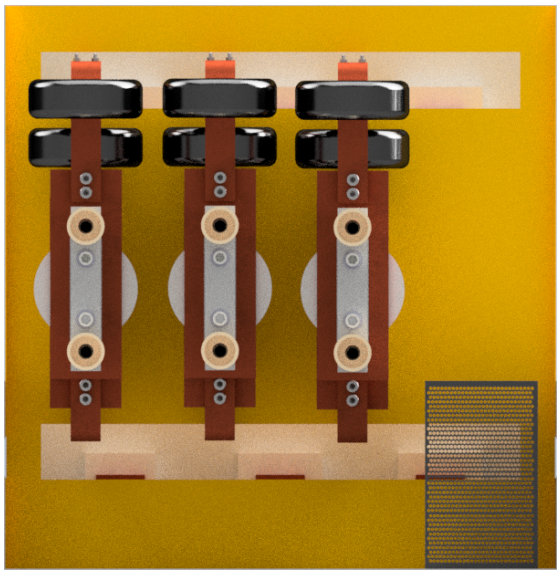
These components have been assembled in a *printed circuit board* (PCB).

Final Result

Figure 4.69 illustrates the drawings of the AF quenching device inside the enclosure. It has been designed to have a withdrawable construction, i.e., it can be easily replaced once needed, and the execution of maintenance tasks is facilitated as well. Such construction form has been inspired by Figure 1.9. However, since the shunt impedances have been allocated out of the AF main enclosure, as one can observe in the picture of Figure 4.70, the AF eliminator became larger than desired, even after changing from the original bulk reactors to the coils built using insulated power cables. The incorporation of these coils inside the enclosure where the electronic parts are allocated will be left for a future work.



(a) Perspective view.



(b) Top view.

Figure 4.69 Complete compartment design.

Figure 4.70 Real switchgear prototype.

4.4.4 Experiments on Arc-Flash Elimination

This subsection presents the final experiments performed in this work, which consist of subjecting the switchgear prototype to the occurrence of arcing faults that are then eliminated by the electronic AF quenching device, so that the propositions previously discussed can be proven. The tests are divided into two parts. First, trials that have been executed at TESLA Power Engineering laboratory, in UFMG, will be presented. In order to ensure safety for people and for the prototype, these tests have been progressively executed from soft - reduced current levels - to full operational conditions. The second part has been executed at the High Current laboratory (AP1) of Centro de Pesquisas de Energia Elétrica (Cepel / Eletrobras), where the switchgear has been subjected to the same tests that would be executed to certify an arc-resistant switchgear. It was fully tested according to IEC TR 61641:2014 and testified to be compliant with the technical report.

Trials Executed at UFMG

A total of 5 tests are presented here. To achieve reduced current levels in the tests, the current-limiting reactors of 20 μH have been inserted in series with the 440 V power system, along with a 130 m long power cable of 10 mm^2, which increases the upstream impedance by $R_{cbl,ac} \approx 238$ mΩ and $X_{cbl} \approx 16.9$ mΩ (Group, 2020). In addition, a 40 m long power cable with the same gauge (which results in $R_{cbl,ac} \approx 73.2$ mΩ and $X_{cbl} \approx 5.2$ mΩ) has been inserted between the switchgear output and a remote point where there is a short auxiliary copper bus short-circuited by a thin bare copper wire that triggers the arcing fault. Figure 4.71 presents an overview of such test setup.

The 40 μH current-limiting reactors have been used as the shunt impedances for the first tests. This could be seamlessly done since the impedance of the feeding power system has been increased by inserting the 20 μH associated with the 130 m long coil. As it has been discussed in Chapter 3, the shunt impedance forms a voltage divider with the upstream power system impedance, and therefore the effectiveness of the AF quenching device can be compromised if the power system impedance is reduced, but increasing it is not a concern.

The 5 tests will be presented below following the same sequence in which they have been performed. In each one, the execution has been done twice, the first one with the AF quenching device disabled and the second one with the equipment in normal operation. It is important to disclaim that during some of these tests, the thermomagnetic CB of the laboratory installation has tripped before the incoming CB

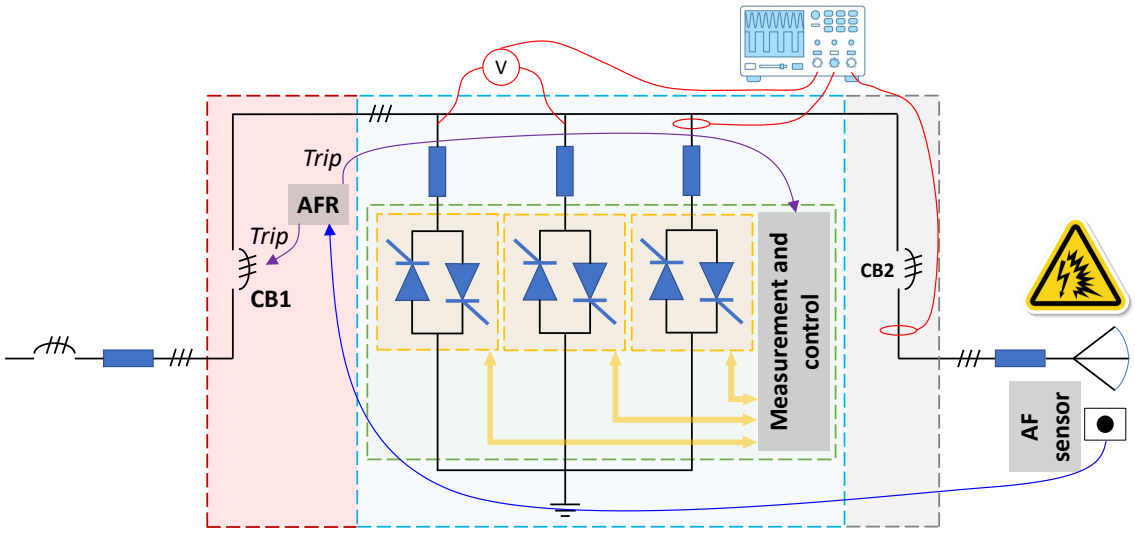


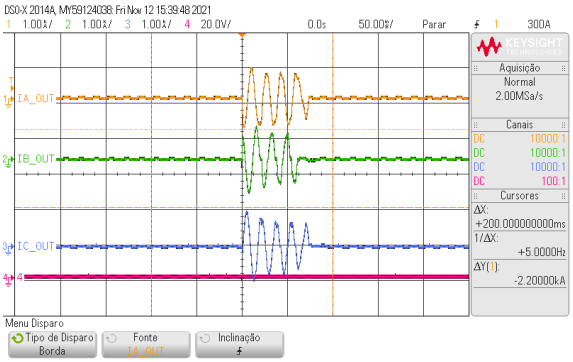
Figure 4.71 Schematic of the laboratory experiments.

of the switchgear. This situation has been verified especially for the tests with the highest current values, where the instantaneous overcurrent function of the breaker has been sensitized during the very beginning of the test and then the equipment completed this opening during the operation of the quenching device.

The first test (test P1: quenching device disabled - P1a, and quenching device active - P1b), has been executed with the configuration shown in Figure 4.71. Figures 4.72 and 4.73 show the waveforms registered during the execution of the tests P1a and P1b respectively. The trip signal from the AFR is also shown in Figure 4.73b. Notice how the busbar voltages are immediately quenched when the trip signal is toggled. In this case, however, the time interval ($\approx$ 25 ms) from the beginning of the fault and the toggling of the trip signal was significantly longer than expected, especially due to the low fault currents and the consequent long period of time required to burn out the triggering wire. The flat-topped line-to-line busbar voltage has reached values of roughly 350 V during the fault, which has been promptly reduced to less than 100 V with the operation of the quenching device. Figure 4.74 illustrates a comparison between the AF filmed during the tests at their worse (more intense) frames. These frames did not occur at the same instant from the beginning of their respective experiments.

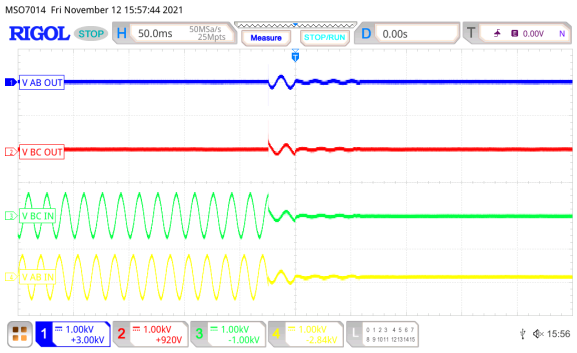
Before the execution of test P2, the 20 μH current-limiting reactors have been removed from the setup. With the quenching device active, the trip signal was issued approximately 7 ms after the beginning of the fault, which has been completely extinguished then in less than 3 ms. The peak current through the fault was roughly 3

(a) Busbar voltage (line-to-line).

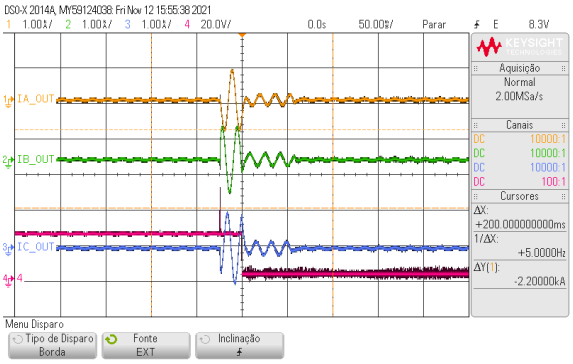


(b) Current through the arc.

Figure 4.72 Waveforms captured during trial P1a.



(a) Busbar voltage (line-to-line).

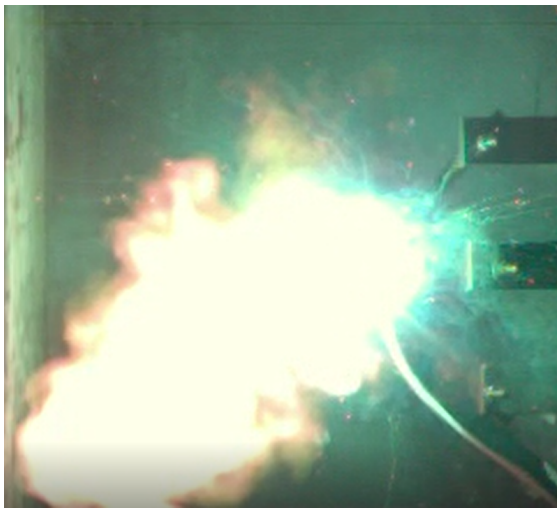


(b) Current through the arc and trip signal (Ch_4 - purple).

Figure 4.73 Waveforms captured during trial P1b.

kA. The busbar voltage during the fault reached peak vaules of 600 V, which has been reduced to less than 200 V from the moment that the suppressor started its operation. To proceed to test P3, the 130 m long coil has been removed from the setup. From this point on, there was no current-limiting impedance intentionally included in the test setup. Without the quenching device, peak fault current of 5 kA has been achieved during the test, and the fault lasted for roughly 50 ms. With the device active, the AFR spent 1.2 ms from the beginning of the fault to assert the trip signal. The current transfer from the arcing path to the quenching device path was complete in less than 4 ms. The peak fault current was reduced to 2.4 kA and the peak current through the device was equal to 7 kA. Both the trials P2 and P3 achieved successful results, but for reasons of text length, their oscilographies will not be shown.

Before the execution of test P4, the 40 m long power cable connected between the output of the switchgear and the remote auxiliary copper bus was replaced by a



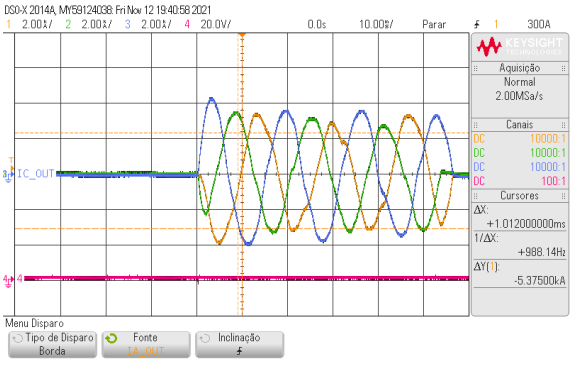
(a) Trial P1a.

(b) Trial P1b.

Figure 4.74 Frames recorded during tests P1a and P1b at their more intense moments.

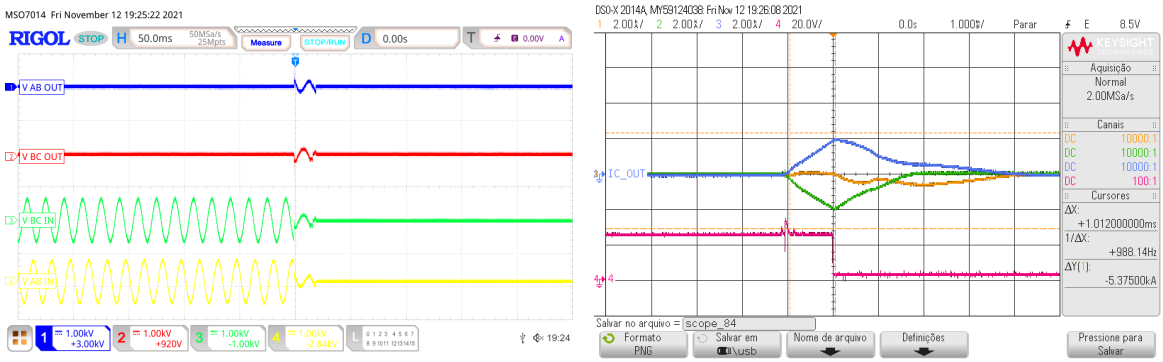
short cable. Figure 4.75 presents the results acquired with the AF quenching device inoperative (P4a). The fault survived for approximately 60 ms, with the peak line-to-line busbar voltage less than 600 V and peak AF current of 4.3 kA. By repeating the test with the AF quenching device operative, the fault elimination was initiated practically at the same time the trip signal was issued by the AFR, which occurred 1 ms after the fault started. The time taken to complete the transfer of the arcing fault current to the quenching device was nearly 4 ms. The current through the device continued flowing for 19 ms, reaching a peak value equal to 7 kA. Figures 4.76 and 4.77 show the waveforms captured during the test P4b.

(a) Busbar voltage (line-to-line).



(b) Current through the arc.

Figure 4.75 Waveforms captured during trial P4a.



(a) Busbar voltage (line-to-line).

(b) Current through the arc and trip signal.

Figure 4.76 Waveforms captured during trial P4b.

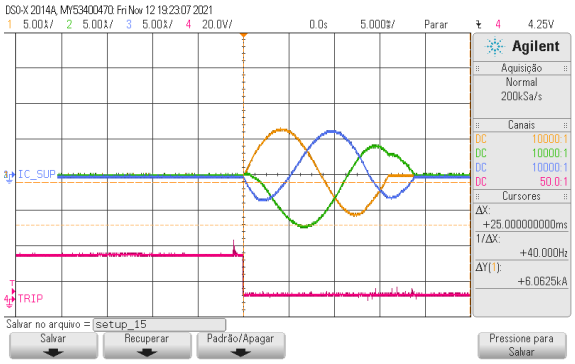


Figure 4.77 Waveforms captured during trial P4b - quenching device current.

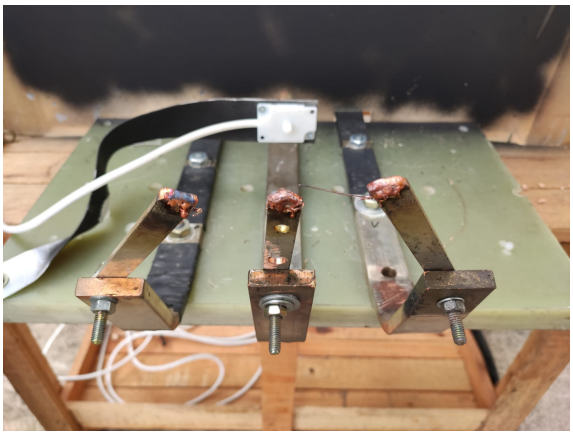
Figure 4.78a illustrates a frame of a video recorded during the execution of test P4a, while Figure 4.78b shows the auxiliary busbar and the thin bare copper wire right after the execution of test P4b. Notice how a considerable part of the wire was found to be undamaged.

Before the accomplishment of the last test, P5, the shunt impedance of 40 μH was finally replaced by the 3 μH coil[36] previously shown in Figure 4.68a. Figures 4.79 and 4.80a represent the waveforms captured during the test, which has been performed only with the AF quenching device active. The time to detect the arc by the AFR did not change in comparison to test P4b, but the time spent to transfer the current from the arcing path to the quenching device decayed to less than 600 μs. The peak current through the quenching device increased to 11 kA.

The electrical energy irradiated during the test has been calculated from the .csv files recorded during the experiment. To do so, the power-invariant Clarke transformation

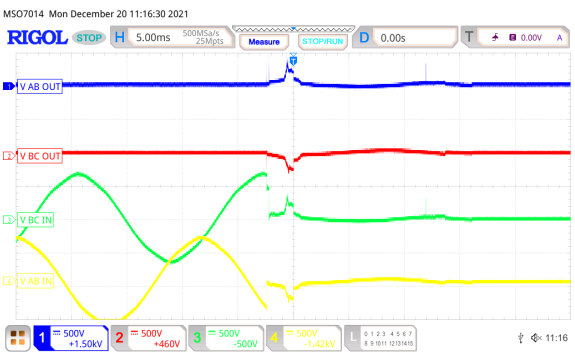
[36]In addition to the inductance of the coil, the busbar has a stray inductance between 1 μH and 2 μH, since its length is approximately 2 m.

(a) A frame of a video recorded during trial P4a.

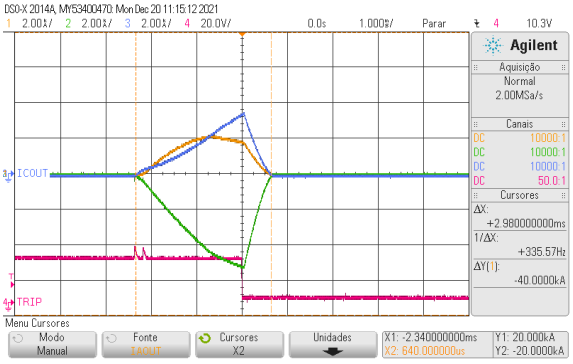


(b) Auxiliary busbar and thin copper wire after trial P4b.

Figure 4.78 Pictures taken during trial P4.



(a) Busbar voltage (line-to-line).



(b) Current through the arc and trip signal.

Figure 4.79 Waveforms captured during trial P5.

was applied to the line-to-line voltages (v_{AB}, v_{BC} and v_{CA}) and line currents (i_A, i_B and i_C). Then the three-phase active power P_a has been calculated by:

$$P_a = v_\alpha \cdot i_\alpha + v_\beta \cdot i_\beta, \tag{4.12}$$

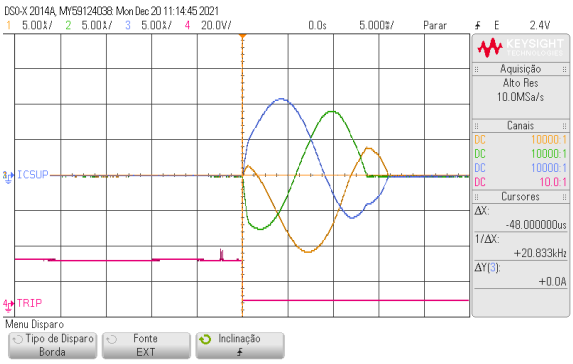
where the reference axes have been chosen according to the phase sequence of the recorded waveforms (ABC), considering the 'α' axis aligned with axis 'A' and 'β' axis spatially displaced by 90° clockwise from 'α'. Finally, the electrical energy E_a has been calculated by taking the area under P_a and transforming the result from joules to cal:

$$E_a = \frac{1}{4.18} \cdot \sum_{m=1}^{n} P_a(m) \cdot \Delta t, \tag{4.13}$$

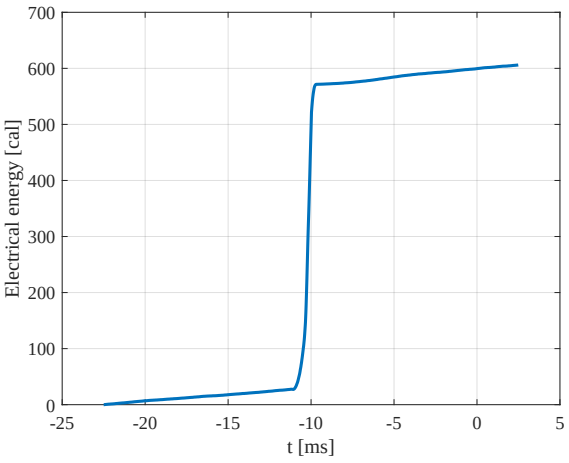
where m is the pointer for the discrete-time interval $\Delta t \approx 25\ \mu s$ to be summed to the result. Figure 4.80b presents the result obtained for the experiment P5. The calculated value quantify electrical energy, not incident energy. The calculation of the IE demands that an electro-thermal energy conversion process is modeled according to the physical and electrical parameters of the switchgear, which in turn results in an energy density in cal/cm^2. Considering conservatively that all the energy calculated in (4.13) propagates directly[37] to the open front door of a typical compartment of a switchgear and the operator is working just at this surface, a superficial energy density can be calculated as:

$$E_{a,sfc} = \frac{600}{80^2} = 0.09\ cal/cm^2, \tag{4.14}$$

where the frontal size of the compartment is 31.5" x 31.5". This value is greatly below the threshold of 1.2 cal/cm^2. Furthermore, since the majority of three-phase arcing faults start as a single-phase to ground, such an energy value will rarely be a reality provided that the quenching device is fast enough to avoid fault escalation, which is accomplished by the proposed electronic scheme. For the sake of comparison, the IE that would result from an arcing fault occurring with similar parameters of trial P5 in a switchgear without the AF quenching device would result in an incident energy level between 1.80 cal/cm^2 and 2.04 cal/cm^2 for a *fault clearing time* (FCT) of 200 ms. This result has been obtained by simulating the scenario in the software ETAP® according to IEEE 1584-2018 method.



(a) Current through the quenching device.



(b) Electrical energy irradiated.

Figure 4.80 Waveforms related to trial P5.

[37] Or is 100% reflected from the other surfaces of the cubicle.

Trials Executed at Cepel

Seven additional tests have been performed on the prototype on January 2022. These tests have been executed at the High Current Laboratory of Cepel and according to the IEC TR 61641:2014. The purpose is to assess the ability of the assembly to limit the risk of personal injury, damage of assemblies and its suitability for further service as a result of an internal arcing fault. By the standard, they have to be executed on a three-phase arcing fault produced by a triggering wire in the same way that it has been done for the preparatory tests executed for this work[38]. The severity of the trials has been progressively increased up to the standard conditions that are adopted to test an arc-resistant SWGR: upstream power system with open-circuit voltage equal to 105% of the rated voltage, power factor of 0.25 (asymmetry factor of 2.1), three-phase symmetrical RMS short-circuit of 25 kA (peak current of approximately 52.5 kA) and duration of 300 ms (Commission, 2014; Eaton, 2015). Specifically for the last test - see Figure 4.81, the thyristors have been changed to part number N4085ZD120 (Littelfuse, 2021) to cope with the high peak current that would result from the high asymmetry factor. No damage has been verified on the thyristors after the tests. In all trials, the 3 μH coil has been used as the shunt impedance. All the 7 conditions determined by the standard for the protection of people and of the SWGR have been achieved.

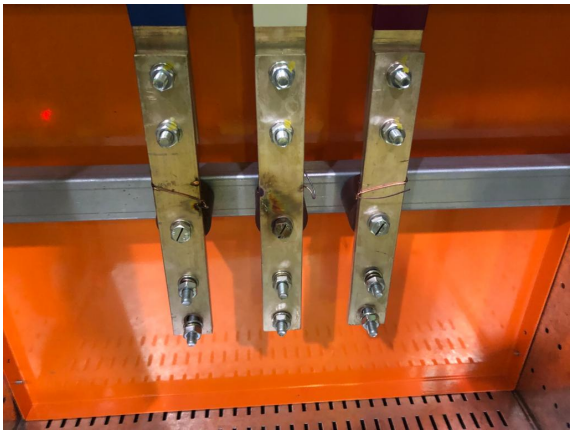
4.5 Summary

It has been shown in this chapter, both from extensive simulation and experimental results, that the electronic AF quenching device is effective for shunt arcing fault elimination in industrial / commercial LV power systems. The guidelines delineated in Chapter 3 for the design of the elements of the quenching device, from the shunt impedances to the turn-off snubbers, have been successfully proved. These guidelines do not excempt the engineer from developing a complete model of the power system where the the AF quenching device is being installed.

Specifically regarding the power thyristors, which are key elements for the effectiveness and reliable operation of the quenching device, the evaluation conducted along this chapter have been done to assess the behavior of the device under the high-current surge that it is subjected to when the equipment operates. The study focused on

[38]The author of this work agrees with reference (Nelson et al., 2014), which states that "since in industrial systems more than 98% of faults originate as phase-ground, the current testing procedures for arcing faults where the initiating mechanism is a three-phase fault appears to be inappropriate and of limited academic value."

(a) SWGR and attached burn indicators.



(b) Triggering wire condition after the last trial.

Figure 4.81 Prototype being tested at Cepel.

the performance of the device during the surge, i.e., intra-event (catastrophic), not inter-events (cumulative damage). The data sheets give information enough to guarantee that the device can ride through the specific set of conditions applied to test it (which are standardized), but there is no direct correlation between those conditions and the circumstances imposed to the operation of the device when applied in the AF quenching device. As well as in the tests performed for the data sheets, it is necessary that a period of time long enough for the device to cool down to room temperature is awaited before it is exposed to a new event. This condition was kept during the experiments executed in this work and will be surely look after during the operation in field.

As one can notice in the presented results, PCT has been the best qualifying device for all the three sets evaluated in this work. Moreover, the higher the value of the I_{TSM} and the lower the value of V_{RRM}, the best the behavior of the device for the type of surge used in this work. The main explanation for the insufficient performance of PPT has to do with the fact that such device is more "elastic" than PCT, i.e., it reaches the highest T_{vj} values in the first current semi cycle, and for this reason does not accommodate the temperature rise due to the following walf-sine waves. Moreover, there are PPT in the market that can not block reverse voltage. BCTs have the advantage of easy assemble, but their halves must be triggered separately, demanding the same gate-driver hardware than PPT and PCT. Two pieces of the device #9

(102/63 mm) can be changed by one of device #11 (150/100 mm), for example. This leads to a lower physical volume, but a higher press-fit apparatus. There is no difference from device #9 to one "half" of device #11 from electrical and thermal aspects.

The application of Stage 1 of the methodology discussed in this chapter can contribute significantly to the specification of thyristors for application in ac surge conditions. Stage 2 can be applied as an auxiliary method but will surely lead to a conservative result. The price of the devices has not been considered in this work but shall be included into the selection procedure as well as the availability and lead time.

The design procedure proposed in this work has been experimentally verified by testing a specific group of commercially available devices, especially PCTs, but it may be useful for any bipolar thyristor type, for example *gate turn-off* (GTO) and *integrated gate-commutated* (IGCT) thyristors. It was also shown that the device resistance is a very important failure indicator, which may be useful for evaluation of degradation. Algorithms suitable to this purpose can be studied in future works, taking advantage of the results collected during the experiments executed for this dissertation.

Finally, the results obtained during the arcing fault experiments have made clear that once the AF quenching device is properly applied to the power system, the calculation of IE levels becomes dispensable. Instead, the computation of the electrical energy dissipated during the fault is more appropriate, being extremely advantageous since it does not involve geometric parameter-based empirical equations.

Chapter 5

Final Remarks

"Pray without ceasing."
1 Thessalonians, 5:17

5.1 Conclusion

This work has proposed and validated a methodology for the calculation of the shunt impedances and specification of the thyristors and snubbers of a power thyristor-based three-phase low-voltage arc-flash quenching device. The equipment is entirely devoted to the limitation of the catastrophic consequences of an arcing fault to their electrical boundary, i.e., the effects are eliminated even before the event progress to its thermal / mechanical phase (or at least at its very beginning). This dissertation went deep into the design concerns, still exploring the basic aspects needed for the operation of the equipment. However, the prototype that has been built opens the doors for the implementation of advanced algorithms, including monitoring and diagnostic strategies.

The specification of power elements of the AF quenching device has been addressed in this work. Discrete-time models of these components, as well as modeling of real registers of arcing faults, have been explored. In addition, the possible impacts of the main failures that can happen during the operation of the equipment have been examined. The main conclusion regarding this matter is that if one or more of the six thyristors fail, the effectiveness of the quenching device cannot be guaranteed, even if the IE level is reduced. Such condition is unacceptable. In the scope of this work, it

has been considered the application of active, real-time monitoring of these devices, both during their operation and hot stand-by states, so that online diagnosis can be continuously run and any abnormally developing failure can be anticipated.

The amount of simulation and experiments performed pave the way for the execution of studies considering the peculiarities of any given scenario, from the modeling of a fault to the specification of the power components of the equipment. Moreover, the strategies established in this work can be exploited for the design of related apparatus operating in applications that use power thyristors and diodes, for example bypass switches of power conditioners and fault current limiters.

5.2 Future Work

It would be very audacious trying to exhaust the subject in this single work. There was not enough study to conclude that the strategies presented here are the definite guide for the design and operation of power thyristor-based arc-flash quenching devices, but relevant contributions have been proven to be valid, which is a strong indicative that the work goes in the right way. The following items, which have been noticed during the execution of this work, called the attention of the author.

1. Built of a new prototype including all the improvements detected throughout the execution of the experiments presented in this work, as well as its test in field.

2. Test experimentally the early failure detection scheme presented in Subsection 4.3.3. It allows the evaluation of the overall condition of the system, including the identification of the v vs. i locus of the thyristors.

3. Give a statistical treatment to the large volume of information attained during the simulations and experiments, so as to support a more detailed parametric analysis. Tools like Principal Component Analysis can be considered.

4. Extend the thyristor fault analysis for other possible combinations of devices.

5. Development of a data base and a graphic tool for the optimum design of the power elements of the quenching device, given the parameters of the power system, the data sheet ratings, the associated costs, etc.

6. Expand the study for higher short-circuit current levels.

7. Further study on the application of the technology in MV power systems.

8. Perform more experimental tests including possible failure of the elements of the quenching device and *electromagnetic compatibility* (EMC) tests to verify if the equipment does not start operating unintentionally.

9. Execute additional tests with single-phase-to-ground arcing faults, since they comprise the predominant scenario among the occurrences in the industry.

5.2.1 Shunt Impedance

The main proposition regarding the shunt impedance is the improvement of the study done in Section 4.2 by defining a geometric locus on the plane from the points plotted in the figures. It should subsidise the safe application of the thyristors in the quenching device, given the expected long-term variation of the equivalent impedance of the upstream power system.

Another relevant contribution on this matter may be found by investigating possible consequences of skin effect on the behavior of the resistive portion of the shunt impedance, which can be significant during the quenching device turn-on transient.

5.2.2 Thyristors

1. The physical meaning of the constants a_r and b_r could be deeply studied.

2. The microscopic-level investigation of the thyristors utilized in the experiments.

3. Improvement of the thyristor behavior at turn-on by increasing the width of the first pulse applied by the gate-driver.

4. Take advantage of the signals provided by the measurement and control system, so that algorithms for real-time self-diagnosis, condition monitoring and failure prediction run both during the surge and the hot stand-by state:

    - Since one of the main failure precursors of a power thyristor is the leakage current, its measurement could help in detecting a latent defect.
    - During the idle operation of the equipment and strictly when there is no maintenance tasks being executed at the protected switchgear, the procedure previously described in this work for early failure detection can be executed. These tests can be useful even for commissioning the equipment in field. Other tests can be included, but they should be carefully studied and

properly developed: (i) triggering the thyristors while they are reverse-biased and verifying possible variations in the leakage current; and (ii) monitoring the gate-to-cathode voltage while the device is in blocking state.

- Real-time calculation of the gate-to-cathode voltage drop while the device is in conduction. It was verified to be greater than a threshold level in this situation (Amaral et al., 2015). Combined with the measurement of the thyristor current, it can be used to immediately detect the failure of the device.
- Since it is expected that a minimum leakage current circulates through the devices during the hot stand by state, then the verification of no such current during this state can be understood by the control system as an open-circuit failure (loss of a connection, for example).
- The monitoring of the turn-off snubbers should be also done, since transient overvoltage could be dangerous both from the safety point of view (fault restrike) and preservation of the thyristors (excessive rate of rise of voltage).
- Calculation of the voltage drop and virtual junction temperature of the device during the surge. It can be done by the control system once the recursive convolution technique is properly deployed to a *digital signal processor* (DSP). A temperature observer can be also implemented based on the measurement of the temperature of the case of the power device.

5. Investigate the effect of high peak junction temperature on the degradation of the thyristors, based on reference (Somos et al., 1993), for example.

6. Carry out functional tests over the measurement and control system prototype, for example forcing the failure of an intelligent gate-driver to check the commutation to its redundant counterpart without any impact on the quenching effectiveness.

7. Define quantitative metrics for the electronic cards of the prototype, like *probability of failure on demand* (PFD). Investigate the need for fault tolerance.

8. Perform reliability analyses and use the results to review the layout of the PCBs. Apply complementary tools like fault tree analysis.

9. Redesign the measurement and control system within the PCB form traditionally adopted for the expansion cards of an *intelligent electronic device* (IED).

10. Execution of vibration, temperature cycling and other complementary tests.

11. Perform more simulations with a lower time step (for example 1 μs) so that the impact of the turn-off snubber on the reverse recovery of the thyristors can be properly evaluated.

12. Assess the applicability of optical trigger circuits to improve the immunity of the quenching device against spurious operation.

5.2.3 Arcing Fault

1. Calculation and comparative analysis between the electrical energy dissipated by the arc in all the tests performed. It should include a close view on the possible effects of reactive power on the model presented in Figure 3.1 since both voltages and currents include harmonic content.

2. Execution of more simulation for calculating the electrical energy reduction when there is a failure on the AF quenching device, for example if one of the thyristors of one phase is not triggered. The possible effect of the shunt impedance can be included as well. The energy level will be surely affected depending on the type of arcing fault and the type of failure. All combinations should be evaluated.

3. Modelling and statistical treatment of the arc-flash registers from IEEE-NFPA.

References

Ieee guide for the application of neutral grounding in electrical utility systems–part i: Introduction. *IEEE Std C62.92.1-2016 (Revision of IEEE Std C62.92.1-2000)*, pages 1–38, 2017. doi: 10.1109/IEEESTD.2017.7891430.

Ieee guide for testing switchgear rated up to 52 kv for internal arcing faults. *IEEE Std C37.20.7-2017 (Revision of IEEE Std C37.20.7-2007)*, pages 1–86, 2018. doi: 10.1109/IEEESTD.2018.8283880.

66pacific. Coil inductance calculator, 2021. URL https://www.66pacific.com/calculators/coil-inductance-calculator.aspx. Online; Last accessed on Feb, 12th, 2022.

ABB. Application note 5sya2049-01 - voltage definitions for phase control and bi-directionally controlled thyristors, Mar 2007.

ABB. Application note 5sya - surge currents for phase control thyristors, Mar 2012.

ABB. Application note 5sya 2006-03 - bi-directionally controlled thyristors, Aug 2013.

ABB. I_S-limiter^{TM} - the world's fastest limiting and switching device, Jan 2014.

ABB. Ufes^{TM} - ultra-fast earthing switch, Jan 2015.

ABB. Arclimiter^{TM} - arc flash mitigation solution for low voltage equipment using ufes, 2017.

ABB. Ultra-fast earthing switch: Ufes - active internal arc protection, 2018.

ABB. Phase control thyristor - 5stp07d1800, May 2020.

R. Abboud, J. Needs, A. Rodriguez, and D. Bhattacharya. Advances in motor protection relay features. In *2016 Petroleum and Chemical Industry Technical Conference (PCIC)*, pages 1–9, June 2016.

K. Ahn, Y. Jeong, S. Lee, S. Park, and Y. Kim. Development of arc eliminator for 7.2/12 kv switchgear. In *2015 3rd International Conference on Electric Power Equipment – Switching Technology (ICEPE-ST)*, pages 198–200, Oct 2015. doi: 10.1109/ICEPE-ST.2015.7368437.

H. Akiyama, T. Sakugawa, T. Namihira, K. Takaki, Y. Minamitani, and N. Shimomura. Industrial applications of pulsed power technology. *IEEE Transactions on Dielectrics and Electrical Insulation*, 14(5):1051–1064, 2007. doi: 10.1109/TDEI.2007.4339465.

B. Allard, H. Morel, K. Ammous, X. Lin-Shi, D. Bergogne, O. Brevet, and P. Bevilacqua. Application of averaged models to real-time monitoring of power converters. In *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, volume 2, pages 486–491 vol.2, June 2001. doi: 10.1109/PESC.2001.954161.

S. Alsalemi, S. Almadhoun, M. Najad, A. M. Massoud, and R. Soliman. Design of a controlled solid state device for fault current limitation and arc flash suppression. In *2017 IEEE Symposium on Computer Applications Industrial Electronics (ISCAIE)*, pages 48–53, April 2017. doi: 10.1109/ISCAIE.2017.8074948.

F. V. Amaral, S. M. Silva, J. A. S. Brito, and B. J. C. Filho. Analysis and characterization of an active bypass switch for series connected power conditioners. In *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, pages 1–5, Nov 2015. doi: 10.1109/COBEP.2015.7420120.

R. F. Ammerman and P. Sen. Modeling high-current electrical arcs: A volt-ampere characteristic perspective for ac and dc systems. In *2007 39th North American Power Symposium*, pages 58–62, 2007. doi: 10.1109/NAPS.2007.4402286.

J. Andrea, P. Schweitzer, and E. Tisserand. A new dc and ac arc fault electrical model. In *2010 Proceedings of the 56th IEEE Holm Conference on Electrical Contacts*, pages 1–6, Oct 2010. doi: 10.1109/HOLM.2010.5619541.

J. Andrea, P. Besdel, O. Zirn, and M. Bournat. The electric arc as a circuit component. In *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, pages 003027–003034, Nov 2015. doi: 10.1109/IECON.2015.7392564.

Arcteq. Aq-1000 arc quenching device (low-voltage), 2021. URL https://www.arcteq.fi/products/aq-1000-arc-quenching-system/. Online; Last accessed on Jan, 06th, 2022.

M. Arefi and A. Abur. A strategic procedure to limit arc flash energy levels. In *SoutheastCon 2015*, pages 1–6, April 2015. doi: 10.1109/SECON.2015.7133025.

J. Arrillaga and R. Watson. *Power System Harmonics*. Wiley, USA, 2003.

I. S. Association. Arc flash ie and iarc calculators, 2020a. URL https://ieee-dataport.org/open-access/arc-flash-ie-and-iarc-calculators. Online; Last accessed on Feb, 20th, 2022.

I. S. Association and N. N. F. P. Association. Arc flash phenomena, 2019. URL https://ieee-dataport.org/open-access/arc-flash-phenomena. Online; Last accessed on May, 20th, 2020.

N. F. P. Association. National electrical code 2020, 2020b. URL https://www.nfpa.org/codes-and-standards. Online; Last accessed on Jan, 06th, 2022.

N. F. P. Association. Nfpa 70e-2021 - standard for electrical safety in the workplace, 2021. URL https://www.nfpa.org/codes-and-standards. Online; Last accessed on Jan, 06th, 2022.

J. Y. Ayoub and M. Valdes. The effect of using minimum and maximum utility fault contributions on arc flash study results - a case study. In *2015 IEEE IAS Electrical Safety Workshop*, pages 1–5, Jan 2015. doi: 10.1109/ESW.2015.7094869.

H. Boenig, J. Schwartzenberg, L. Willinger, D. Piccone, D. Lopez, and H. Smolleck. Design and testing of high power, repetitively pulsed, solid-state closing switches. In *IAS '97. Conference Record of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting*, volume 2, pages 1022–1028 vol.2, 1997. doi: 10.1109/IAS.1997.628986.

B. Bonatto. *EMTP Modelling of Control and Power Electronic Devices*. PhD thesis, The University of British Columbia, 2001.

M. Bottaro, T. O. de Carvalho, L. E. Caires, H. E. Sueta, P. F. Obase, H. Tatizawa, and I. B. Raposo. Analysis of asymmetrical component influence on arc current in the determination of arc thermal performance value of protective personal equipment. *IEEE Transactions on Industry Applications*, 55(2):2130–2137, March 2019. ISSN 1939-9367. doi: 10.1109/TIA.2018.2875852.

D. Broussard. Understanding short-circuit motor contribution, Jun 2013.

R. M. Bugaris and D. R. Doan. Arc-flash incident energy variations: A study of low-voltage motor control center unit configurations and incident energy exposure. *IEEE Industry Applications Magazine*, 20(3):40–45, May 2014. ISSN 1077-2618. doi: 10.1109/MIAS.2013.2288386.

R. M. Bugaris and D. T. Rollay. Arc-resistant equipment. *IEEE Industry Applications Magazine*, 17(4):62–70, 2011. doi: 10.1109/MIAS.2010.939620.

M. Bukovitz. Active arc quenching standards - improving critical electrical system reliability and eliminating the requirement for arc-rated ppe, 2020.

C. G. Burnette, L. B. Farr, and G. Ogles. Power system study at a century-old paper mill. In *2017 Annual Pulp, Paper And Forest Industries Technical Conference (PPFIC)*, pages 1–6, June 2017. doi: 10.1109/PPIC.2017.8003859.

R. J. Burns, A. D. Baker, and D. E. Hrncir. Current-limiting arc flash quenching system for improved incident energy reduction. *IEEE Transactions on Industry Applications*, 55(2):2138–2143, 2019. doi: 10.1109/TIA.2018.2876639.

R. Campbell and D. Dini. Occupational injuries from electrical shock and arc flash events, march 2015. URL https://www.nfpa.org/-/media/Files/News-and-Research/Resources/Research-Foundation/Research-Foundation-reports/Electrical/RFArcFlashOccData.ashx?la=en.

M. Cepek. Novel techniques and procedures for the assessment of fault current withstand capability of power thyristors. *IEEE Transactions on Power Electronics*, 14(2):323–328, March 1999. ISSN 0885-8993. doi: 10.1109/63.750186.

D. Chamund and C. Rout. An5948 - reliability of high power bipolar devices, Sept 2009a.

D. Chamund and C. Rout. An5950 - understanding i^2 phase control thyristor datasheets, Sept 2009b.

D. Chamund, N. Y. A. Shammas, and P. Taylor. Modelling of power semiconductor devices for pulse power applications. In *2009 44th International Universities Power Engineering Conference (UPEC)*, pages 1–5, Sep. 2009.

X. Cheng, W. J. Lee, and X. Pan. Modernizing substation automation systems: Adopting iec standard 61850 for modeling and communication. *IEEE Industry Applications Magazine*, 23(1):42–49, Jan 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600732.

M. Clapper. Ge arc vault™ protection system - ge dea-489e, Oct 2015.

I. E. Commission. Enclosed low-voltage switchgear and controlgear assemblies - guide for testing under conditions of arcing due to internal fault, 2014.

I. E. Commission. Low-voltage switchgear and controlgear - part 9-1: Active arc-fault mitigation systems - arc quenching devices, 2019.

I. E. Commission. Low-voltage switchgear and controlgear assemblies - part 1: General rules, 2020.

C. Conceição. Estudo e projeto de um sistema rápido de supressão de arco baseado em tiristores de potência. Master's thesis, Universidade Federal de Minas Gerais, Programa de Pós-Graduação em Engenharia Elétrica, Belo Horizonte, 2015.

M. E. Corporation. Product information / high power devices / thyristors, 2020. URL https://www.mitsubishielectric.com/semiconductors/products/highpower/thyristors/index.html. Online; Last accessed on Nov, 10th, 2020.

T. Crnko and S. Dyrnes. Arcing fault hazards and safety suggestions for design and maintenance. *IEEE Industry Applications Magazine*, 7(3):23–32, May 2001. ISSN 1077-2618. doi: 10.1109/2943.922447.

T. M. Crnko. Current-limiting fuse update - new style fuse for protection of semiconductor devices. *IEEE Transactions on Industry Applications*, IA-15(3):308–312, May 1979. ISSN 0093-9994. doi: 10.1109/TIA.1979.4503658.

L. Dai, J. Hu, Y. Yang, F. Lin, and Q. Zhang. Research on transient junction temperature rise of pulse thyristor. In *2016 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, pages 482–487, July 2016. doi: 10.1109/IPMHVC.2016.8012911.

H. A. Darwish and N. I. Elkalashy. Universal arc representation using emtp. *IEEE Transactions on Power Delivery*, 20(2):772–779, April 2005. ISSN 0885-8977. doi: 10.1109/TPWRD.2004.838462.

J. C. Das. Design aspects of industrial distribution systems to limit arc flash hazard. *IEEE Transactions on Industry Applications*, 41(6):1467–1475, Nov 2005. ISSN 0093-9994. doi: 10.1109/TIA.2005.858274.

J. C. Das. Protection planning and system design to reduce arc flash incident energy in a multi-voltage-level distribution system to 8cal/cm^2(hrc 2) or less—part i: Methodology. *IEEE Transactions on Industry Applications*, 47(1):398–407, Jan 2011. ISSN 0093-9994. doi: 10.1109/TIA.2010.2091377.

J. C. Das. *Arc Flash Hazard Analysis and Mitigation*. Wiley, 2012.

B. de Metz-Noblat, F. Dumas, and C. Poulain. Cahier technique no. 158 - calculation of short-circuit currents, Sep 2005.

M. D. Divinnie, J. K. Stacy, and A. C. Parsons. Arc flash mitigation using active high-speed switching. *IEEE Transactions on Industry Applications*, 51(1):28–35, Jan 2015. ISSN 0093-9994. doi: 10.1109/TIA.2014.2328792.

F. Dixon, M. T. Yunas, V. Wedelich, J. Howard, H. E. Brown, S. N. Sauer, Y. M. Xu, T. Markello, and W. Sheikh. Mitigating arc flashes using iec 61850: Examining a case at a chemical and refining facility. *IEEE Industry Applications Magazine*, 20(1): 64–69, Jan 2014. ISSN 1077-2618. doi: 10.1109/MIAS.2013.2282563.

M. D'Mello, M. Noonan, H. Aulakh, and J. Mirabent. Arc flash energy reduction—case studies. *IEEE Transactions on Industry Applications*, 49(3):1198–1204, May 2013. ISSN 0093-9994. doi: 10.1109/TIA.2013.2252413.

G. W. Drewiske. Engineering incident energy analysis and remediation project in a midwestern pulp and paper mill. *IEEE Transactions on Industry Applications*, 50 (1):104–112, Jan 2014. ISSN 0093-9994. doi: 10.1109/TIA.2013.2288232.

C. Dubilier. *Application Guide, Snubber Capacitors - Designing an RC Snubber*. Cornell Dubilier, http://www.cornell-dubilier.com.

J. R. Dunki-Jacobs. The effects of arcing ground faults on low-voltage system design. *IEEE Transactions on Industry Applications*, IA-8(3):223–230, May 1972. ISSN 0093-9994. doi: 10.1109/TIA.1972.349750.

J. R. Dunki-Jacobs. The escalating arcing ground-fault phenomenon. *IEEE Transactions on Industry Applications*, IA-22(6):1156–1161, 1986. doi: 10.1109/TIA.1986.4504848.

A. Dunlop. Semiconductor devices for pulsed power applications, Mar 2000.

D. B. Durocher. Arc-flash compliance implementation at industrial processing facilities. *IEEE Transactions on Industry Applications*, 51(2):1295–1302, March 2015. ISSN 0093-9994. doi: 10.1109/TIA.2014.2360018.

Dynex. An4870 - effects of temperature on thyristor performance, July 2002.

M. D'Mello, M. Noonan, M. E. Valdes, and J. Benavides. Arc flash hazard reduction at incoming terminals of lv equipment. *IEEE Transactions on Industry Applications*, 52(1):701–711, Jan 2016. ISSN 0093-9994. doi: 10.1109/TIA.2015.2478391.

Eaton. Understanding current standards can protect switchgear users from the risks of internal arc flash events, Aug 2015.

Eaton. Arc flash limiter (afl) conversion system, Jun 2018.

Eaton. Instructions for installation, operation and maintenance of the arc quenching device (aqd), Feb 2019.

Eaton. Arc quenching magnum ds low-voltage switchgear, 2021. URL https://www.eaton.com/us/en-us/catalog/low-voltage-power-distribution-controls-systems/arc-quenching-magnum-ds-low-voltage-switchgear.html. Online; Last accessed on Jan, 06th, 2022.

M. Eblen and T. Short. Low-voltage arc sustainability. In *2017 IEEE IAS Electrical Safety Workshop (ESW)*, pages 1–13, Jan 2017. doi: 10.1109/ESW.2017.7914841.

R. El-Mahayni, J. Bugshan, and R. Pragale. Arc-flash mitigation: A systematic approach for company standard power system schemes. *IEEE Industry Applications Magazine*, 23(3):24–32, May 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600694.

C. Electronics. Flat wire inductance calculator, 2019. URL https://chemandy.com/calculators/flat-wire-inductor-calculator.htm. Online; Last accessed on Feb, 12th, 2022.

L. O. Eriksson, D. E. Piccone, L. J. Willinger, and W. H. Tobin. Selecting fuses for power semiconductor devices. *IEEE Industry Applications Magazine*, 2(5):19–23, Sep. 1996. ISSN 1077-2618. doi: 10.1109/2943.532150.

S. Faried, Wolfgang, and L. Proelss. Arc flash - new regulations and the advantages of the ultra fast grounding switch. In *2017 Petroleum and Chemical Industry Technical Conference (PCIC)*, pages 245–252, Sept 2017. doi: 10.1109/PCICON.2017.8188743.

J. Ferro. Arc protected assembly - how to increase safety of the switchgear, 2018. URL https://new.abb.com/docs/librariesprovider78/colombia-ecuador-docs/system-pro-e-power_safe-distribution.pdf?sfvrsn=1893a614_2. Online; Last accessed on Dec, 28th, 2021.

H. L. Floyd, J. J. Andrews, M. Capelli-Schellpfeffer, and D. P. Liggett. An overview of the state-of-the-art in electrical safety technology, work practices and management systems. In *Conference Record of the 2003 Annual Pulp and Paper Industry Technical Conference, 2003.*, pages 123–140, June 2003. doi: 10.1109/PAPCON.2003.1216908.

E. C. for Electrotechnical Standardization. En 50110-1: Operation of electrical installations - part 1: General requirements, 2013. Online; Last accessed on Feb, 09th, 2022.

G. H. Fox. Design guidelines for safer low-voltage distribution systems. *IEEE Transactions on Industry Applications*, 51(3):2060–2070, May 2015. ISSN 0093-9994. doi: 10.1109/TIA.2014.2360958.

G. H. Fox. Design guidelines for safer low-voltage distribution systems—part ii: Motor circuits. *IEEE Transactions on Industry Applications*, 52(2):1314–1320, March 2016. ISSN 0093-9994. doi: 10.1109/TIA.2015.2483600.

T. Gammon and J. Matthews. Instantaneous arcing-fault models developed for building system analysis. *IEEE Transactions on Industry Applications*, 37(1):197–203, 2001. doi: 10.1109/28.903147.

T. Gammon, W. J. Lee, Z. Zhang, and B. C. Johnson. "arc flash" hazards, incident energy, ppe ratings, and thermal burn injury - a deeper look. *IEEE Transactions on Industry Applications*, 51(5):4275–4283, Sept 2015. ISSN 0093-9994. doi: 10.1109/TIA.2015.2431644.

GE. How to reduce exposure to arc flash hazards, 2015.

GE. Multilin 350 arc flash detection system installation, testing and maintenance, 2017a.

GE. Det-1004 application and technical guide: Energy-reducing maintenance switch - relt function in ge circuit breaker trip units & power switch control relays, Jun 2017b.

GE. Reatores com núcleo de ar, 2017c.

C. Gemme, M. Pasinetti, and R. Piccardo. A matter of timing, 2008.

T. Ghanbari, E. Farjah, and N. Tashakor. Thyristor based bridge-type fault current limiter for fault current limiting capability enhancement. *IET Generation, Transmission & Distribution*, 10:2202–2215(13), June 2016. ISSN 1751-8687. URL https://digital-library.theiet.org/content/journals/10.1049/iet-gtd.2015.1364.

L. B. Gordon, L. Cartelli, and N. Graham. A complete electrical shock hazard classification system and its application. *IEEE Transactions on Industry Applications*, 54(6):6554–6565, Nov 2018. ISSN 1939-9367. doi: 10.1109/TIA.2018.2803768.

J. J. Grainger and W. D. Stevenson. *Power System Analysis*. McGraw-Hill, USA, 1994.

A. Greenwood and A. Selzer. Electrical transients in power systems. 1971.

G. D. Gregory and K. J. Lippert. Applying low-voltage circuit breakers to limit arc-flash energy. *IEEE Transactions on Industry Applications*, 48(4):1225–1229, July 2012. ISSN 0093-9994. doi: 10.1109/TIA.2012.2201029.

P. Group. Guia de dimensionamento de cabos para baixa tensão, 2020.

C. Gu, P. Wheeler, A. Castellazzi, A. J. Watson, and F. Effah. Semiconductor devices in solid-state/hybrid circuit breakers: Current status and future trends. *Energies*, 10(4), 2017. ISSN 1996-1073. doi: 10.3390/en10040495. URL http://www.mdpi.com/1996-1073/10/4/495.

A. Haluik. Improving electrical safety : Risk perception and decision making in hazard analysis. *IEEE Industry Applications Magazine*, 23(3):33–41, May 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600719.

S. Hasan, E.-S. El-Refaie, A. H. K. Alaboudy, and A. Hamada. An ac hybrid current limiting and interrupting device for low voltage systems. *Alexandria Engineering Journal*, 57(3):1535 – 1548, 2018. ISSN 1110-0168. doi: https://doi.org/10.1016/j.aej.2017.03.049. URL http://www.sciencedirect.com/science/article/pii/S1110016817301436.

T. Hazel, J. Lavaud, and B. Leforgeais. Using pyrotechnic current-limiting devices: A case study of what went right. *IEEE Industry Applications Magazine*, 23(5):50–59, Sept 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600726.

D. L. Hodgson, M. A. McKinney, and S. D. DeGrate. Reducing arc-flash hazards: One company's efforts to systematically improve electrical safety. *IEEE Industry Applications Magazine*, 19(3):34–46, May 2013. ISSN 1077-2618. doi: 10.1109/MIAS.2012.2215647.

M. Hoffman, J. Dickens, and M. Giesselmann. Investigation of pulse power thyristor thermal variations. In *Digest of Technical Papers. PPC-2003. 14th IEEE International Pulsed Power Conference (IEEE Cat. No.03CH37472)*, volume 1, pages 143–145 Vol.1, 2003. doi: 10.1109/PPC.2003.1277679.

A. Q. Huang. Power semiconductor devices for smart grid and renewable energy systems. *Proceedings of the IEEE*, 105(11):2019–2047, Nov 2017. ISSN 0018-9219. doi: 10.1109/JPROC.2017.2687701.

B. Hughes, V. Skendzic, D. Das, and J. Carver. High-current qualification testing of an arc-flash detection system. In *38th Annual Western Protective Relay Conference*, October 2011.

G. A. Hussain, L. Kumpulainen, M. Lehtonen, and J. A. Kay. Preemptive arc-fault detection techniques in switchgear and controlgear—part ii. *IEEE Transactions on Industry Applications*, 50(3):1649–1658, May 2014. ISSN 0093-9994. doi: 10.1109/TIA.2013.2286322.

G. A. Hussain, M. Shafiq, J. A. Kay, and M. Lehtonen. Preemptive arc fault detection techniques in switchgear—part iii: From the laboratory to practical installation. *IEEE Transactions on Industry Applications*, 51(3):2615–2623, May 2015. ISSN 0093-9994. doi: 10.1109/TIA.2014.2362958.

G. A. Hussain, M. Shafiq, and M. Lehtonen. Predicting arc faults in distribution switchgears. In *2016 17th International Scientific Conference on Electric Power Engineering (EPE)*, pages 1–6, May 2016. doi: 10.1109/EPE.2016.7521722.

G. Idarraga Ospina, D. Cubillos, and L. Ibanez. Analysis of arcing fault models. In *2008 IEEE/PES Transmission and Distribution Conference and Exposition: Latin America*, pages 1–5, 2008. doi: 10.1109/TDC-LA.2008.4641860.

IEEE. Recommended practice for electric power distribution for industrial plants. *Std 141-1993*, pages 1–768, April 1994. doi: 10.1109/IEEESTD.1994.121642.

IEEE. Recommended practice for industrial and commercial power systems analysis (brown book). *Std 399-1997*, pages 1–488, Aug 1998. doi: 10.1109/IEEESTD.1998.88568.

IEEE. Recommended practice for protection and coordination of industrial and commercial power systems (ieee buff book). *Std 242-2001 (Revision of IEEE Std 242-1986) [IEEE Buff Book]*, pages 1–710, Dec 2001. doi: 10.1109/IEEESTD.2001.93369.

IEEE. Recommended practice for the design of reliable industrial and commercial power systems. *Std 493-2007 (Revision of IEEE Std 493-1997) - Redline*, pages 1–426, June 2007.

IEEE. Guide for motor control centers rated up to and including 600 v ac or 1000 v dc with recommendations intended to help reduce electrical hazards. *Std 1683-2014*, pages 1–47, Aug 2014. doi: 10.1109/IEEESTD.2014.6866103.

IEEE. Recommended practice for the application of low-voltage circuit breakers in industrial and commercial power systems. *Std 3004.5-2014*, pages 1–106, Feb 2015. doi: 10.1109/IEEESTD.2015.7036035.

IEEE. Ieee application guide for ac high-voltage circuit breakers $>$ 1000 vac rated on a symmetrical current basis. *IEEE Std C37.010-2016 (Revision of IEEE Std C37.010-1999)*, pages 1–123, April 2017. doi: 10.1109/IEEESTD.2017.7906465.

IEEE. Guide for performing arc-flash hazard calculations. *Std 1584-2018 (Revision of IEEE Std 1584-2002)*, pages 1–134, Nov 2018. doi: 10.1109/IEEESTD.2018.8563139.

F. Illahi, I. El-Amin, and M. U. Mukhtiar. The application of multiobjective optimization technique to the estimation of electric arc furnace parameters. *IEEE Transactions on Power Delivery*, 33(4):1727–1734, 2018. doi: 10.1109/TPWRD.2017.2758320.

E. Jacks. The fundamental behavior of high-speed fuses for protecting silicon diodes and thyristors. *IEEE Transactions on Industrial Electronics and Control Instrumentation*, IECI-16(2):125–133, Sep. 1969. ISSN 0018-9421. doi: 10.1109/TIECI.1969.230429.

C. F. James Lagree and M. DeFloria. Safer by design: arc energy reduction techniques, April 2018.

N. Kamsali, B. Prasad, and J. Datta. The electrical conductivity as an index of air pollution in the atmosphere. In F. Nejadkoorki, editor, *Advanced Air Pollution*, chapter 20. IntechOpen, Rijeka, 2011. doi: 10.5772/17163. URL https://doi.org/10.5772/17163.

R. Kapoor, A. Shukla, and G. Demetriades. State of art of power electronics in circuit breaker technology. In *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 615–622, Sep. 2012. doi: 10.1109/ECCE.2012.6342764.

P. Katare, R. Chennu, S. S. Reddy, A. Awasthi, and B. Ramachandra. Evaluation of arc conductance for high current fault arcs. In *2017 7th International Conference on Power Systems (ICPS)*, pages 854–858, Dec 2017. doi: 10.1109/ICPES.2017.8387408.

D. Katsiris and D. Scheuerman. Arc-flash mitigation: How to comply with nec 2017, Jun 2018.

J. A. Kay and L. Kumpulainen. Maximizing protection by minimizing arcing times in medium-voltage systems. *IEEE Transactions on Industry Applications*, 49(4): 1920–1927, July 2013. ISSN 0093-9994. doi: 10.1109/TIA.2013.2255253.

J. A. Kay, J. Arvola, and L. Kumpulainen. Protecting at the speed of light. *IEEE Industry Applications Magazine*, 17(3):12–18, May 2011. ISSN 1077-2618. doi: 10.1109/MIAS.2010.939635.

A. Khakpour, S. Franke, S. Gortschakow, D. Uhrlandt, R. Methling, and K. Weltmann. An improved arc model based on the arc diameter. *IEEE Transactions on Power Delivery*, 31(3):1335–1341, June 2016. ISSN 0885-8977. doi: 10.1109/TPWRD.2015.2473677.

A. Khakpour, D. Uhrlandt, R.-P. Methling, S. Gorchakov, S. Franke, M. Imani, and K.-D. Weltmann. Impact of temperature changing on voltage and power of an electric arc. *Electric Power Systems Research*, 143:73–83, 02 2017. doi: 10.1016/j.epsr.2016.10.009.

King-Jet Tseng, Yaoming Wang, and D. M. Vilathgamuwa. An experimentally verified hybrid cassie-mayr electric arc model for power electronics simulations. *IEEE Transactions on Power Electronics*, 12(3):429–436, May 1997. ISSN 0885-8993. doi: 10.1109/63.575670.

M. Kizilcay and K. Koch. Numerical fault arc simulation based on power arc tests. *European Transactions on Electrical Power*, 4:177 – 185, 05 2007. doi: 10.1002/etep.4450040302.

M. Kizilcay and T. Pniok. Digital simulation of fault arcs in power systems. *European Transactions on Electrical Power*, 1(1):55–60, 1991. doi: https://doi.org/10.1002/etep.4450010111. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/etep.4450010111.

M. Kizilcay and P. L. Seta. Digital simulation of fault arcs in medium-voltage distribution networks. 2005.

S. G. Koutoula, I. V. Timoshkin, M. D. Judd, S. J. MacGregor, M. P. Wilson, M. J. Given, T. Wang, and E. I. Harrison. A study of energy partition during arc initiation. *IEEE Transactions on Plasma Science*, 44(10):2137–2144, Oct 2016. ISSN 0093-3813. doi: 10.1109/TPS.2016.2579312.

K. Krause, D. Burns, S. Hutchinson, and J. Arvola. Managing arc flash: Collaborative solutions in medium-voltage switchgear. *IEEE Industry Applications Magazine*, 20 (1):70–78, Jan 2014. ISSN 1077-2618. doi: 10.1109/MIAS.2013.2282560.

K. N. Krause, S. A. Hutchinson, D. Burns, and J. Arvola. Collaborative arc flash management solutions in medium voltage switchgear. In *2012 Petroleum and Chemical Industry Conference (PCIC)*, pages 1–9, Sept 2012. doi: 10.1109/PCICON.2012.6549686.

L. Kumpulainen, G. A. Hussain, M. Lehtonen, and J. A. Kay. Preemptive arc fault detection techniques in switchgear and controlgear. *IEEE Transactions on Industry Applications*, 49(4):1911–1919, July 2013. ISSN 0093-9994. doi: 10.1109/TIA.2013.2258314.

L. Kumpulainen, G. A. Hussain, M. Rival, M. Lehtonen, and K. Kauhaniemi. Aspects of arc-flash protection and prediction. *Electric Power Systems Research*, 116:77 – 86, 2014. ISSN 0378-7796. doi: https://doi.org/10.1016/j.epsr.2014.05.011. URL http://www.sciencedirect.com/science/article/pii/S0378779614001990.

L. Kumpulainen, A. Jäntti, J. Rintala, and K. Kauhaniemi. Benefits and performance of iec 61850 generic object oriented substation event-based communication in arc protection. *IET Generation, Transmission Distribution*, 11(2):456–463, 2017. ISSN 1751-8687. doi: 10.1049/iet-gtd.2016.1003.

S. E. Laboratory. Sel arc-flash solutions - arc-flash protection at the speed of light, July 2017.

N. LaFlair, M. H. McKinney, and R. Hadidi. Arc flash risk assessment for a megawatt scale medium voltage research and testing facility. In *2017 North American Power Symposium (NAPS)*, pages 1–5, Sep. 2017. doi: 10.1109/NAPS.2017.8107231.

E. Larsen, M. E. Valdes, G. H. Fox, K. Rempe, and C. G. Walker. Updating the ieee color books: A review of ieee standard 3004.5. *IEEE Industry Applications Magazine*, 23(1):50–57, Jan 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600728.

C. Latzo. *Approaches to Arc Flash Mitigation in 600 Volt Power Systems*. PhD thesis, University of South Florida, 2011.

R. H. Lee. The other electrical hazard: Electric arc blast burns. *IEEE Transactions on Industry Applications*, IA-18(3):246–251, May 1982. ISSN 1939-9367. doi: 10.1109/TIA.1982.4504068.

W. J. Lee, T. Gammon, Z. Zhang, B. Johnson, and J. Beyreis. Arc flash and electrical safety. In *2013 66th Annual Conference for Protective Relay Engineers*, pages 24–35, April 2013. doi: 10.1109/CPRE.2013.6822024.

N. Liang, Z. Zhang, Y. Gou, C. Liu, Z. Yang, J. Chen, F. Zhuo, and F. Wang. Failure mechanism analysis and physics-of-failure lifetime prediction method for press-pack thyristor of converter valve. In *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pages 1157–1161, May 2018. doi: 10.23919/IPEC.2018.8507978.

X. Liang, B. Bagen, and D. W. Gao. An effective approach to reducing arc flash hazards in power systems. *IEEE Transactions on Industry Applications*, 52(1):67–75, Jan 2016. ISSN 0093-9994. doi: 10.1109/TIA.2015.2477269.

V. B. Litovski, S. P. L. Blond, and B. P. Ross. Transient circuit implementation of arc models with particular focus on arcs in low-voltage power cables. *Electric Power Systems Research*, 147(C):105–114, 2017. doi: 10.1016/j.epsr.2017.02.025.

Littelfuse. *AN1001 - Fundamental Characteristics of Thyristors*. Littelfuse, Sept 2013.

Littelfuse. How protection relays solve electrical problems, 2015.

Littelfuse. Af0500 arc-flash relay application guide, Apr 2016a.

Littelfuse. Littelfuse arc-flash relay saves plant from catastrophic damage, Feb 2017a.

Littelfuse. Af0500 arc-flash relay (revision 0-e-120817), Aug 2017b.

I. Littelfuse. Phase control thyristor - n2600mc180, Jan 2016b.

I. Littelfuse. Phase control thyristor - n4085zd120, Jan 2021.

C. Liu, W. Chen, Y. Shi, H. Tao, Q. Zhou, H. Zuo, B. Qiao, Y. Xia, Z. Xiao, W. Gao, N. Chen, X. Xu, Q. Zhou, Z. Li, and B. Zhang. A novel insulated gate triggered thyristor with schottky barrier for improved repetitive pulse life and high-di/dt characteristics. *IEEE Transactions on Electron Devices*, 66(2):1018–1025, 2019. doi: 10.1109/TED.2018.2887137.

D. G. Loucks. Arc flash safety in 400v datacenters, Jun 2013.

R. Luna, B. Cassidy, and J. Franco. Reducing arc-flash risk. *IEEE Industry Applications Magazine*, 17(4):18–27, July 2011. ISSN 1077-2618. doi: 10.1109/MIAS.2010.939626.

C. S. Mardegan and R. Rifaat. Insights into applications of ieee standards for ground-fault protection in industrial and commercial power systems. *IEEE Transactions on Industry Applications*, 51(4):2854–2861, July 2015. ISSN 0093-9994. doi: 10.1109/TIA.2015.2391434.

W. Marszalek and Z. W. Trzaska. Dynamical models of electric arcs and memristors: The common properties. *IEEE Transactions on Plasma Science*, 45(2):259–265, Feb 2017. ISSN 0093-3813. doi: 10.1109/TPS.2016.2645879.

J. A. Martinez-Velasco. *Modelling of Power Components for Transients Studies*, chapter 2, pages 11–73. John Wiley & Sons, Ltd, 2020. ISBN 9781119480549. doi: https://doi.org/10.1002/9781119480549.ch2. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/9781119480549.ch2.

Mersen. Medium voltage controllable fuse, Sep 2020.

C. Meyer and R. W. D. Doncker. Solid-state circuit breaker based on active thyristor topologies. *IEEE Transactions on Power Electronics*, 21(2):450–458, March 2006. ISSN 0885-8993. doi: 10.1109/TPEL.2005.869756.

S. Microelectronics. *AN437 Rev. 2 - RC Snubber Circuit Design for TRIACs*. ST Microelectronics, Oct 2007.

S. Mohajeryami, M. Arefi, and Z. Salami. Arc flash analysis: Investigation, simulation and sensitive parameter exploration. In *2017 North American Power Symposium (NAPS)*, pages 1–6, Sep. 2017. doi: 10.1109/NAPS.2017.8107182.

H. Mokhtari and M. Hejri. A new three phase time-domain model for electric arc furnaces using matlab. In *IEEE/PES Transmission and Distribution Conference and Exhibition*, volume 3, pages 2078–2083 vol.3, Oct 2002. doi: 10.1109/TDC.2002.1177781.

J. V. Motto, W. H. Karstaedt, J. M. Sherbondy, and S. G. Leslie. Modeling thyristor and diodes; on-state voltage and transient thermal impedance, effective tools in power electronic design. In *IAS '97. Conference Record of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting*, volume 2, pages 1182–1189 vol.2, Oct 1997. doi: 10.1109/IAS.1997.629010.

J. W. Motto. A new quantity to describe power semiconductor subcycle current ratings. *IEEE Transactions on Industry and General Applications*, IGA-7(4):510–517, July 1971. ISSN 0018-943X. doi: 10.1109/TIGA.1971.4181333.

J. W. Motto. Thyristor steady state current ratings past, present and future. In *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, pages 1256–1263 vol.2, Oct 1993. doi: 10.1109/IAS.1993.299083.

J. W. Motto, W. H. Karstaedt, J. M. Sherbondy, and S. G. Leslie. Thyristor(diode) on-state voltage, the abcd modeling parameters revisited including isothermal overload and surge current modeling. In *IAS '96. Conference Record of the 1996 IEEE Industry Applications Conference Thirty-First IAS Annual Meeting*, volume 3, pages 1481–1488 vol.3, Oct 1996. doi: 10.1109/IAS.1996.559264.

J. W. Motto, W. H. Karstaedt, J. M. Sherbondy, and S. G. Leslie. Electro-thermal modeling of multi-megawatt power electronic applications using pspice^{TM}. In *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat.No.98CH36242)*, volume 2, pages 982–990 vol.2, Oct 1998. doi: 10.1109/IAS.1998.730265.

R. Nasereddine, I. Amor, A. Massoud, and L. B. Brahim. Ac solid state circuit breakers for fault current limitation in distributed generation. In *2013 7th IEEE GCC Conference and Exhibition (GCC)*, pages 446–449, Nov 2013. doi: 10.1109/IEEEGCC.2013.6705820.

J. P. Nelson. Improved electrical safety through high resistance grounding. *IEEE Transactions on Industry Applications*, 51(6):5198–5203, Nov 2015. ISSN 0093-9994. doi: 10.1109/TIA.2015.2397171.

J. P. Nelson, J. D. Billman, and J. E. Bowen. The effects of system grounding, bus insulation, and probability on arc flash hazard reduction—the missing links. *IEEE Transactions on Industry Applications*, 50(5):3141–3152, Sep. 2014. ISSN 0093-9994. doi: 10.1109/TIA.2014.2308399.

J. P. Nelson, J. D. Billman, J. E. Bowen, and D. A. Martindale. The effects of system grounding, bus insulation, and probability on arc flash hazard reduction—part 2: Testing. *IEEE Transactions on Industry Applications*, 51(3):2665–2675, May 2015. ISSN 0093-9994. doi: 10.1109/TIA.2014.2372091.

NEMA. Abp 1-2016: Selective coordination of low-voltage circuit breakers, Jun 2016.

F. Nepveux. In a flash - use of instantaneous trip functions with current-limiting fuses to reduce arc flash energy without losing coordination. *IEEE Industry Applications Magazine*, 13(5):68–72, Sep. 2007. ISSN 1077-2618. doi: 10.1109/MIA.2007.901734.

W. E. Newell. Dissipation in solid-state devices–the magic of i1 + n. *IEEE Transactions on Industry Applications*, IA-12(4):386–396, July 1976a. ISSN 0093-9994. doi: 10.1109/TIA.1976.349442.

W. E. Newell. Transient thermal analysis of solid-state power devices–making a dreaded process easy. *IEEE Transactions on Industry Applications*, IA-12(4):405–420, July 1976b. ISSN 0093-9994. doi: 10.1109/TIA.1976.349444.

K. Nowak, J. Janiszewski, and G. Dombek. Thyristor arc eliminator for protection of low voltage electrical equipment. *Energies*, 12(14), 2019. ISSN 1996-1073. doi: 10.3390/en12142749. URL https://www.mdpi.com/1996-1073/12/14/2749.

K. Nowak, J. Janiszewski, and G. Dombek. A multi-sectional arc eliminator for protection of low voltage electrical equipment. *Energies*, 13(3), 2020. ISSN 1996-1073. doi: 10.3390/en13030605. URL https://www.mdpi.com/1996-1073/13/3/605.

K. Nowak, J. Janiszewski, and G. Dombek. The possibilities to reduce arc flash exposure with arc fault eliminators. *Energies*, 14(7), 2021. ISSN 1996-1073. doi: 10.3390/en14071927. URL https://www.mdpi.com/1996-1073/14/7/1927.

P. Parikh, D. Allcock, R. Luna, and J. Vico. A novel approach for arc-flash detection and mitigation: At the speed of light and sound. *IEEE Transactions on Industry Applications*, 50(2):1496–1502, March 2014. ISSN 0093-9994. doi: 10.1109/TIA.2013.2288239.

G. Parise, L. Martirano, and M. Laurini. Simplified arc-fault model: The reduction factor of the arc current. *IEEE Transactions on Industry Applications*, 49(4):1703–1710, July 2013. ISSN 0093-9994. doi: 10.1109/TIA.2013.2256452.

G. Parise, L. Parise, and E. Berenato. Basic measures assisting the avoidance of arc flash. *IEEE Transactions on Industry Applications*, 54(2):1842–1847, March 2018. ISSN 1939-9367. doi: 10.1109/TIA.2017.2779109.

R. Pastore, M. Weiner, H. Singh, S. Schneider, R. Fox, and G. Ayres. Evaluation of scrs as millisecond switches for electric gun launchers. In *Ninth IEEE International Pulsed Power Conference*, volume 1, pages 360–, 1993. doi: 10.1109/PPC.1993.513349.

D. Paul and P. B. R. Chavdarian. Undercurrent protection power system: A novel ground-fault protection relay scheme. *IEEE Industry Applications Magazine*, 21(1):23–32, Jan 2015. ISSN 1077-2618. doi: 10.1109/MIAS.2014.2345797.

P. Pawar and A. Patil. Use of diode as a crowbar for electromagnetic launcher. In *2016 International Conference on Automatic Control and Dynamic Optimization Techniques (ICACDOT)*, pages 563–567, 2016. doi: 10.1109/ICACDOT.2016.7877648.

J. N. Pearse and P. G. Newberry. Fast acting fuses for the protection of semiconductors. *IEEE Transactions on Industrial Electronics and Control Instrumentation*, IECI-17(4):332–338, June 1970. ISSN 0018-9421. doi: 10.1109/TIECI.1970.229883.

C. Peng, X. Song, A. Q. Huang, and I. Husain. A medium-voltage hybrid dc circuit breaker—part ii: Ultrafast mechanical switch. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(1):289–296, March 2017. ISSN 2168-6777. doi: 10.1109/JESTPE.2016.2609391.

F. P. Pessoa, J. S. Acosta, and M. C. Tavares. Parameter estimation of dc black-box arc models using genetic algorithms. *Electric Power Systems Research*, 198: 107322, 2021. ISSN 0378-7796. doi: https://doi.org/10.1016/j.epsr.2021.107322. URL https://www.sciencedirect.com/science/article/pii/S0378779621003035.

T. Podlesak, F. Simon, and S. Schneider. Single shot and burst repetitive operation of thyristors for electric launch applications. *IEEE Transactions on Magnetics*, 37(1): 385–388, 2001. doi: 10.1109/20.911860.

R. Pragale, A. Patel, and R. Bresden. Arc flash kpi compliance at a large oil and gas company. *IEEE Transactions on Industry Applications*, 54(1):889–894, Jan 2018. ISSN 0093-9994. doi: 10.1109/TIA.2017.2743173.

F. Profumo, A. Tenconi, S. Facelli, and B. Passerini. Instantaneous junction temperature evaluation of high-power diodes (thyristors) during current transients. *IEEE Transactions on Power Electronics*, 14(2):292–299, March 1999. ISSN 0885-8993. doi: 10.1109/63.750182.

A. Queiroz. Utilização de relés digitais para mitigação dos riscos envolvendo arco elétrico. Master's thesis, Universidade de São Paulo, São Paulo, 2011.

H. Radmanesh and S. H. Fathi. Fast ac reactor-based fault current limiters application in distribution network. *High Voltage*, 3:232–243(11), September 2018. URL https://digital-library.theiet.org/content/journals/10.1049/hve.2017.0195.

H. Radmanesh, S. H. Fathi, G. B. Gharehpetian, and A. Heidary. A novel solid-state fault current-limiting circuit breaker for medium-voltage network applications. *IEEE Transactions on Power Delivery*, 31(1):236–244, Feb 2016. ISSN 0885-8977. doi: 10.1109/TPWRD.2015.2466094.

R. Rajvanshi and T. Hawkins. Insulated bus bars in low-voltage systems: Reducing arc duration and energy emissions. *IEEE Industry Applications Magazine*, 23(3): 48–53, May 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600733.

S. H. Rau, Z. Zhang, W. J. Lee, and D. A. Dini. Arc flash visible light intensity as viewed from human eyes. *IEEE Transactions on Industry Applications*, 53(5): 5068–5077, Sept 2017. ISSN 0093-9994. doi: 10.1109/TIA.2017.2715823.

J. S. Read and R. F. Dyer. Power thyristor rating practices. *Proceedings of the IEEE*, 55(8):1288–1301, Aug 1967. ISSN 0018-9219. doi: 10.1109/PROC.1967.5829.

R. Rifaat, B. Baily, G. Dalke, B. Duncan, C. J. Mozina, L. J. Powell, J. Fischer, A. Y. Wu, J. Weber, and J. Daley. Bus and breaker fail protection for industrial and commercial power systems part i: Introduction and bus protection summary-working group report. In *2007 IEEE Industry Applications Annual Meeting*, pages 890–897, Sep. 2007. doi: 10.1109/07IAS.2007.139.

D. T. Roberts, M. Doherty, and L. A. Lane. The human contribution to workplace incidents: Addressing the human element in electrical safety. *IEEE Industry Applications Magazine*, 23(3):42–47, May 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600735.

R. G. Rodrigues, D. E. Piccone, W. H. Tobin, L. W. Willinger, J. A. Barrow, T. A. Hansen, J. Zhao, and L. Cao. Operation of power semiconductors at their thermal limit. In *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, volume 2, pages 942–953 vol.2, Oct 1998. doi: 10.1109/IAS.1998.730259.

G. J. Rohwein, L. D. Roose, and W. M. Portnoy. Characterization of high power thyristors. In *Digest of Technical Papers. Tenth IEEE International Pulsed Power Conference*, volume 1, pages 336–341 vol.1, July 1995. doi: 10.1109/PPC.1995.596502.

G. Roscoe, T. Papallo, and M. Valdes. Fast energy capture. *IEEE Industry Applications Magazine*, 17(4):43–52, July 2011. ISSN 1077-2618. doi: 10.1109/MIAS.2010.939625.

C. Rout. An5381 - case non-rupture current ratings, Feb 2014a.

C. Rout. An6161 - turn-off time, leakage current and reverse recovery current under conditions other than the datasheet, Dec 2014b.

C. Rout. An6196 - gate power calculations, Mar 2017.

D. Roybal. Standards and ratings for the application of molded-case, insulated-case, and power circuit breakers. *IEEE Transactions on Industry Applications*, 37(2): 442–451, 2001. doi: 10.1109/28.913707.

C. Safety. Arc flash accident-injury statistics: An alarming reality, 2020. URL https://www.conney.com/websphere/ResourcesTabs/Knowledge-Base/Whitepapers/ArcFlash_Whitepaper.pdf. Online; Last accessed on Dec, 28th, 2021.

I. Safety and H. News. Arc flash incidents: The annual toll in the u.s., 2014. URL https://www.ishn.com/articles/98643-arc-flash-incidents-the-annual-toll-in-the-us. Online; Last accessed on Dec, 10th, 2018.

O. Safety and U. D. o. L. Health Administration. Common electrical hazards in the workplace including arc flash, 2018. URL www.osha.gov. Online; Last accessed on Mar, 17th, 2021.

S. A. Saleh, A. S. Aljankawey, R. Errouissi, and M. A. Rahman. Experimental performance of the phase-based digital protection against arc flash faults. In *2015 IEEE Industry Applications Society Annual Meeting*, pages 1–10, Oct 2015. doi: 10.1109/IAS.2015.7356954.

H. Salisbury. Arc flash statistics - the surprising costs of an arc flash, 2014. URL https://www.salisburybyhoneywell.com/en/sas/resources/arc-flash-statistics. Online; Last accessed on Dec, 28th, 2018.

V. A. Sankaran, J. L. Hudgins, C. A. Rhodes, and W. M. Portnoy. A numerical approach based on transient thermal analysis to estimate the safe operating frequencies of thyristors. *IEEE Transactions on Power Electronics*, 6(4):679–686, Oct 1991. ISSN 0885-8993. doi: 10.1109/63.97768.

V. A. Sankaran, J. L. Hudgins, and W. M. Portnoy. High-energy pulse-switching characteristics of thyristors. *IEEE Transactions on Power Electronics*, 8(4):347–354, Oct 1993. ISSN 0885-8993. doi: 10.1109/63.261003.

T. R. Sauve, R. P. Anderson, T. Bower, and K. R. Mickler. Designing and specifying mccs to reduce hazards and risks, using ieee 1683. In *2017 Petroleum and Chemical Industry Technical Conference (PCIC)*, pages 387–396, Sept 2017. doi: 10.1109/PCICON.2017.8188759.

A. Sawicki, L. Switon, and R. Sosinski. Process simulation in the ac welding arc circuit using a cassie-mayr hybrid model. 90:41s–44s, 03 2011.

E. T. Schonholzer. Fuse protection for power thyristors. *IEEE Transactions on Industry Applications*, IA-8(3):301–309, May 1972. ISSN 0093-9994. doi: 10.1109/TIA.1972.349761.

P. Schueller. Cahier technique no. 163 - lv breaking by current limitation, Sep 1998.

J. Seedorff. Arc-flash protection - key considerations for selecting an arc-flash relay, Mar 2015.

SEL. Sel arc flash solutions: Arc-flash protection at the speed of light, July 2017.

D. Semi. Phase control thyristor - dcr3030v42, Jan 2014.

D. Semi. Power semiconductor - product guide 2019, June 2019.

O. Semiconductor. *HBD855/D Rev. 1 - Thyristor Theory and Design Considerations Handbook*. ON Semiconductor, Phoenix, USA, Nov 2006.

Semikron. Discrete - explanations - thyristors / diodes, Mar 2015.

Semikron. Phase control thyristor - skt-553/18e sg, Aug 2018.

L. Sevov and M. Valdes. Differential protection in low-voltage buses: An exploration of principles and models. *IEEE Industry Applications Magazine*, 23(5):28–39, Sept 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600688.

A. Shukla and G. D. Demetriades. A survey on hybrid circuit-breaker topologies. *IEEE Transactions on Power Delivery*, 30(2):627–641, April 2015. ISSN 0885-8977. doi: 10.1109/TPWRD.2014.2331696.

Siemens. Techtopics no. 44 - anatomy of a short circuit, Jun 2016.

Siemens. Updated - 2017 national electrical code (nec) 240.87 - questions and answers, Jun 2017.

Siemens. Siquench - arc quenching device for medium-voltage switchgears, 2019.

Siemens. Arc fault prevention and protection for medium-voltage switchgear and low-voltage switchboards, 2021. URL https://new.siemens.com/global/en/products/energy/medium-voltage/systems/siquench/siquench-sivacons8plus.html. Online; Last accessed on Jan, 06th, 2022.

A. P. Silard. High-temperature physical effects underlying the failure mechanism in thyristors under surge conditions. *IEEE Transactions on Electron Devices*, 31(9): 1334–1340, Sep. 1984. ISSN 0018-9383. doi: 10.1109/T-ED.1984.21709.

J. Simms and G. Johnson. Protective relaying methods for reducing arc flash energy. *IEEE Transactions on Industry Applications*, 49(2):803–813, March 2013. ISSN 0093-9994. doi: 10.1109/TIA.2013.2240645.

C. Smith and C. Rout. An4840 - gate triggering and gate characteristics, July 2014.

T. Smith, C. Burnette, and M. Valdes. Does every millisecond really count - a comparison of protection based arc flash mitigation techniques. In *2016 IEEE Pulp, Paper Forest Industries Conference (PPFIC)*, pages 53–59, June 2016. doi: 10.1109/PPIC.2016.7523466.

I. L. Somos, D. E. Piccone, L. J. Willinger, and W. H. Tobin. Power semiconductors empirical diagrams expressing life as a function of temperature excursion. *IEEE Transactions on Magnetics*, 29(1):517–522, Jan 1993. ISSN 0018-9464. doi: 10.1109/20.195629.

I. L. Somos, D. E. Piccone, L. J. Willinger, and W. H. Tobin. Power semiconductors-a new method for predicting the on-state characteristic and temperature rise during multicycle fault currents. *IEEE Transactions on Industry Applications*, 31(6):1221–1226, Nov 1995. ISSN 0093-9994. doi: 10.1109/28.475691.

S. Song, J. Kim, S. Choi, I. Kim, and S. Choi. New simple-structured ac solid-state circuit breaker. *IEEE Transactions on Industrial Electronics*, 65(11):8455–8463, Nov 2018. ISSN 0278-0046. doi: 10.1109/TIE.2018.2809674.

J. Sperl, C. Whitney, and A. Milner. Arc flash hazard regulation and mitigation. In *2009 62nd Annual Conference for Protective Relay Engineers*, pages 417–425, March 2009. doi: 10.1109/CPRE.2009.4982530.

L. H. Sperow. Fuse selection for power semiconductor conversion equipment. *IEEE Transactions on Industry Applications*, IA-9(1):33–40, Jan 1973. ISSN 0093-9994. doi: 10.1109/TIA.1973.349884.

U. Standards. Arcing fault quenching equipment, 2016.

A. D. Stokes and D. K. Sweeting. Electric arcing burn hazards. *IEEE Transactions on Industry Applications*, 42(1):134–141, Jan 2006. ISSN 0093-9994. doi: 10.1109/TIA.2005.861911.

A. Switzerland. Application note 5sya 2034-02: Gate-driver recommendations for phase-control and bi-directionally controlled thyristors, 2013.

A. T. Teklić, B. Filipović-Grčić, and I. Pavić. Modelling of three-phase electric arc furnace for estimation of voltage flicker in power transmission network. *Electric Power Systems Research*, 146:218–227, 2017. ISSN 0378-7796. doi: https://doi.org/10.1016/j.epsr.2017.01.037. URL https://www.sciencedirect.com/science/article/pii/S0378779617300469.

K. M. Thomas, B. Backlund, O. Toker, and B. Thorvaldsson. The bidirectional control thyristor (bct). In *Proceedings of the International Power Conversion Conference*, pages 369–378. Intertec International, Inc, 1998.

H. W. Tinsley, M. Hodder, and A. M. Graham. Arc flash hazard calculations. *IEEE Industry Applications Magazine*, 13(1):58–64, Jan 2007. ISSN 1077-2618. doi: 10.1109/MIA.2007.265802.

M. E. Valdes and J. J. Dougherty. Advances in protective device interlocking for improved protection and selectivity. *IEEE Transactions on Industry Applications*, 50(3):1639–1648, May 2014. ISSN 0093-9994. doi: 10.1109/TIA.2013.2285941.

M. E. Valdes, S. Hansen, and P. Sutherland. Optimized instantaneous protection settings: Improving selectivity and arc-flash protection. *IEEE Industry Applications Magazine*, 18(3):66–73, May 2012. ISSN 1077-2618. doi: 10.1109/MIAS.2012.2186008.

M. E. Valdes, R. M. Bugaris, and C. M. Wellman. Behind the scenes of ieee 1683: A look into the creation of a standard. *IEEE Industry Applications Magazine*, 23(1): 26–33, Jan 2017a. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2600741.

M. E. Valdes, S. Hinton, and F. Martinez. Arc flash in the national electrical code: Articles 240.87, 240.67; intent and reality, does the code achieve its goals? do you achieve its goals? In *2017 IEEE Industry Applications Society Annual Meeting*, pages 1–10, Oct 2017b. doi: 10.1109/IAS.2017.8101680.

D. J. Ventruella. Arc flash hazard—when overestimating underestimates a problem. *IEEE Transactions on Industry Applications*, 55(3):3287–3293, 2019. doi: 10.1109/TIA.2019.2897673.

J. Vitins, J. Steiner, and J. Welleman. High power semiconductors for pulsed switching. In *7th Pulsed Power Conference*, pages 352–357, 1989. doi: 10.1109/PPC.1989.767496.

J. Vobecky. The bidirectional phase control thyristor. *IEEE Transactions on Electron Devices*, 67(7):2844–2849, 2020. doi: 10.1109/TED.2020.2991690.

F. Volle, S. V. Garimella, and M. A. Juds. Thermal management of a soft starter: Transient thermal impedance model and performance enhancements using phase change materials. *IEEE Transactions on Power Electronics*, 25(6):1395–1405, June 2010. ISSN 0885-8993. doi: 10.1109/TPEL.2010.2040632.

C. G. Walker. Arc-flash energy reduction techniques: Zone-selective interlocking and energy-reducing maintenance switching. *IEEE Transactions on Industry Applications*, 49(2):814–824, March 2013. ISSN 0093-9994. doi: 10.1109/TIA.2013.2244831.

W. D. Walker and W. F. Weldon. Thermal modeling and experimentation to determine maximum power capability of scr's and thyristors. *IEEE Transactions on Power Electronics*, 14(2):316–322, March 1999. ISSN 0885-8993. doi: 10.1109/63.750185.

P. R. Walsh and M. M. Price. Reducing arc-flash hazards: Installing mv-controllable fuses on the secondary side of the transformer in a pumped storage plant. *IEEE Industry Applications Magazine*, 23(5):21–27, Sep. 2017. ISSN 1077-2618. doi: 10.1109/MIAS.2016.2623347.

Westcode. An application note for leakage current against temperature and applied voltage, Mar 2012a.

Westcode. An application note for possible failure modes in press pack devices, July 2012b.

I. U. Westcode. Types n3175he160 and n3175he180 data sheet, 2014.

I. U. Westcode. Types n3533z#140 to n3533z#220 data sheet, Feb 2021.

B. W. Williams. *Power Electronics - Devices, Drivers, Applications, and Passive Components*. Barry W Williams, 2006.

A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann. Application manual - power semiconductors, Mar 2015.

H. Wu, L. Yuan, L. Sun, and X. Li. Modeling of current-limiting circuit breakers for the calculation of short-circuit current. *IEEE Transactions on Power Delivery*, 30 (2):652–656, April 2015. ISSN 0885-8977. doi: 10.1109/TPWRD.2014.2305166.

Q. Yin and R. Ding. Review of arc models in distribution networks. *MATEC Web of Conferences*, 61:02016, 01 2016. doi: 10.1051/matecconf/20166102016.

L. Yuan, L. Sun, and H. Wu. Simulation of fault arc using conventional arc models. *Energy and Power Engineering*, 5(4B):833–837, Sep 2013. doi: 10.4236/epe.2013.54B160.

M. Zeller, A. Hargrave, and D. Haas. Using the sel-751 and sel-751a for arc-flash detection, Jan 2011.

X. Zhang, J. Zhang, and G. Pietsch. Estimation of the arc power during a three-phase arc fault in mv electrical installations. *IEEE Transactions on Plasma Science*, 35(3): 724–730, 2007. doi: 10.1109/TPS.2007.897666.

Z. Zhang, B. Ma, and A. Friberg. Thyristor working as arc eliminator protecting electrical apparatus in low voltage power system. In *2015 IEEE International Conference on Industrial Technology (ICIT)*, pages 1216–1219, March 2015. doi: 10.1109/ICIT.2015.7125263.

L. Zhou, Y. Yijun, Z. Shan, and W. Weifu. Applications and discussions of arc flash protection relay as a main busbar protection in mv switchboards. In *2014 China International Conference on Electricity Distribution (CICED)*, pages 1806–1813, Sept 2014. doi: 10.1109/CICED.2014.6992265.

Appendix A

Publications, Awards and Patent Applications

A.1 Publications

Below are listed the main (specifically related to this dissertation) and other (extra) publications that the author of this work has been involved with during the doctorate period - from May, 2017 to March, 2022.

A.1.1 Conference Papers

Main

1. F. V. Amaral, M. H. M. Z. Oliveira, C. A. Conceição, S. M. Silva, C. O. Inácio and B. de J. Cardoso Filho, "On the Application of a Power Electronics-based Arc-Flash Suppressor," *2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)*, Santos, Brazil, 2019, pp. 1-6. https://doi.org/10.1109/COBEP/SPEC44138.2019.9065328.

2. F. Amaral, S. Silva, C. Conceição, G. Guimarães, C. Inácio and B. Cardoso, "Catastrophic Failure Prediction for Phase Control Thyristors in AC Pulsed Power Applications," *2020 IEEE Industry Applications Society Annual Meeting*, Detroit, MI, USA, 2020, pp. 1-10. https://doi.org/10.1109/IAS44978.2020.9334892.

3. F. Amaral, S. Silva, C. Conceição, G. Guimarães and B. Cardoso, "Increasing the Ride-Through Fault Capability of a Power Electronics-Based Arc-Flash

Suppressor," *2021 14th IEEE International Conference on Industry Applications (INDUSCON)*, São Paulo, Brazil, 2021, pp. 1198-1205. https://doi.org/10.1109/INDUSCON51756.2021.9529644.

4. F. Amaral, G. Guimarães, S. Silva, C. Conceição and B. Cardoso, "Performance Comparison between Phase Control, Pulse Power and Bidirectional Power Thyristors under ac Surge Conditions," *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, 2021, pp. 1-11.

5. F. Amaral, S. Silva, C. Conceição, G. Guimarães and B. Cardoso, "Design Considerations for a Reliable Power Electronics-based Arc-Flash Suppressor," *2021 IEEE Industry Applications Society Annual Meeting (IAS)*, Vancouver, BC, Canada, 2021, pp. 1-10. https://doi.org/10.1109/IAS48185.2021.9677219.

6. F. Amaral, S. Silva, C. Conceição and B. Cardoso, "A Review on Arc-Flash Protective Methods for Industrial and Commercial Power Systems," *X IEEE Electrical Safety Workshop Brasil (ESW)*, Virtual, Brazil, 2021, pp. 1-9.

Extra

1. A. Machado et al., "Control of a SiC-based Cascaded Multilevel Converter cell for solar applications," *2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2017, pp. 1-7. https://doi.org/10.1109/PEDG.2017.7972496.

2. T. Parreiras, A. Machado, F. Amaral, G. Lobato, J. Brito and F. B. Cardoso, "Forward dual-active-bridge solid state transformer for a SiC-based cascated multilevel converter cell in solar applications," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2989-2996. https://doi.org/10.1109/APEC.2017.7931122.

3. R. C. de Oliveira, F. V. Amaral, F. C. Oliveira and B. L. F. Souza, "Solar generation impact on voltage of rural power distribution networks: A case study," *2018 Simposio Brasileiro de Sistemas Eletricos (SBSE)*, 2018, pp. 1-6. https://doi.org/10.1109/SBSE.2018.8395736.

4. F. Amaral, S. Rezende, R. Gomes, M. Porto, D. Maiuste and B. Cardoso, "Directly Feeding Large DC Loads Through PV Power Plants: Experimental

Validation," *2019 IEEE Industry Applications Society Annual Meeting*, 2019, pp. 1-9. https://doi.org/10.1109/IAS.2019.8912401.

A.1.2 Journal Papers

Main

F. Amaral, S. Silva, C. Conceicao, G. Fontoura, C. Inacio and B. Cardoso, "Assessment of Catastrophic Failure for Phase Control Thyristors in ac Pulsed Applications," in *IEEE Transactions on Industry Applications*. https://doi.org/10.1109/TIA.2021.3065896.

Extra

1. F. V. Amaral, T. M. Parreiras, G. C. Lobato, A. A. P. Machado, I. A. Pires and B. de Jesus Cardoso Filho, "Operation of a Grid-Tied Cascaded Multilevel Converter Based on a Forward Solid-State Transformer Under Unbalanced PV Power Generation," in *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5493-5503, Sept.-Oct. 2018. https://doi.org/10.1109/TIA.2018.2827002.

2. T. M. Parreiras, A. P. Machado, F. V. Amaral, G. C. Lobato, J. A. S. Brito and B. C. Filho, "Forward Dual-Active-Bridge Solid-State Transformer for a SiC-Based Cascaded Multilevel Converter Cell in Solar Applications," in *IEEE Transactions on Industry Applications*, vol. 54, no. 6, pp. 6353-6363, Nov.-Dec. 2018. https://doi.org/10.1109/TIA.2018.2854674.

A.2 Awards

1. Meritorious Paper Award at the *2020 IEEE Industry Applications Society Annual Meeting* - see the certificate ahead in the next page.

2. Best work presented at the *16° Encontro de Engenharia Elétrica da Petrobras*, 2021 - participation as a co-author.

A.3 Patent Applications

A patent application (BR1020220203997) has been filled based on the achievements of this work. The authors have found an enhanced way for the proposal of a more compact, simple and reliable and cheaper solution that goes beyond the scope of this dissertation.

Meritorious Paper Award

The Metals Industry Technical Committee of the Industry Applications Society
Institute of Electrical and Electronics Engineers
Presents this Prize Paper Award to

Fernando Amaral, Sidelmo Silva, Claudio Conceição, Gustavo Guimarães, Cleber Inácio and Braz Cardoso

For writing and presenting the paper entitled

Catastrophic Failure Prediction for Phase Control Thyristors in AC Pulsed Power Applications

55th IEEE IAS Annual Meeting, October 10-16, 2020, Detroit, MI

IEEE
Advancing Technology for Humanity

Igor Pires
Chairman

Juan M. Lopera
Paper Review Chairman

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Appendix B

Arcing Fault Parametric Evaluation

To provide an evaluation of the impact of each parameter of (3.1) to $g(t)$, a sinusoidal, 60 Hz current waveform $i(t)$ was adopted to calculate $g(t)$ with the parameters of trial #67[1] from Table 4.1. The amplitude of $i(t)$ is 1 kA and the duration is 2 cycles. The original values of τ, ℓ, R_O, V_O and G_{min} were divided and multiplied by two to assess the impact of each one. Figure B.1 presents the results for $g(t)$, while Figure B.2a shows the arc voltage $v(t)$, which was calculated by taking $i(t)/g(t)$. Figure B.2b illustrates the locus produced by plotting the instantaneous values of v as a function of i.

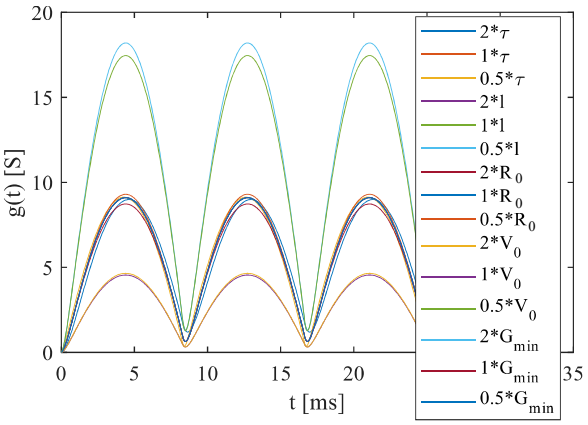
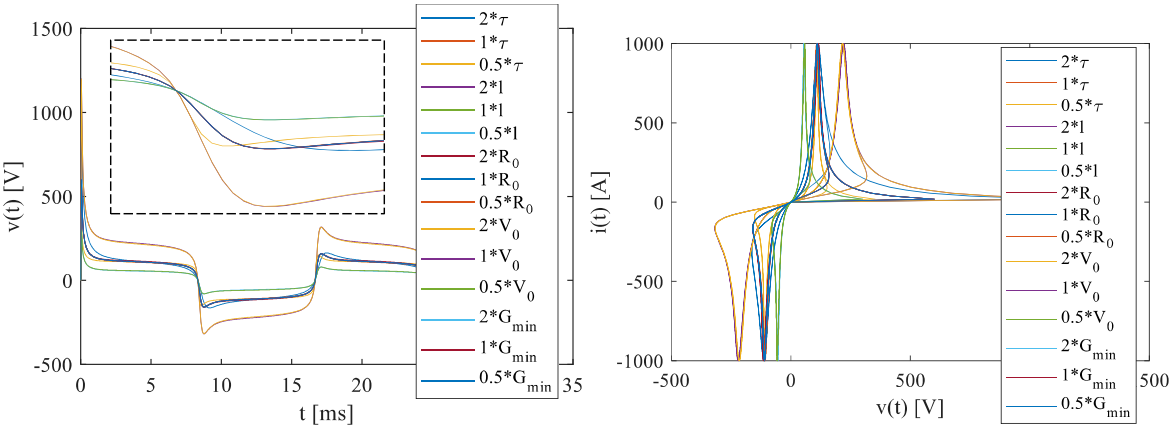


Figure B.1 The effect produced on arc conductance $g(t)$ by doubling and by halving each one of the fault parameters shown in Table 4.1, for a 1 kA, 60 Hz sinusoidal current $i(t)$.

Regarding Figure B.1, higher peak value ($\approx$ 18 S) is verified for $g(t)$ in two curves: $0.5 \cdot \ell$ and $0.5 \cdot V_O$. On the other hand, lower peak value ($\approx$ 4.5 S) is verified for $g(t)$

[1]See the real waveforms in Figure 2.2.



(a) Arc voltage $v(t)$.

(b) Arc current vs. voltage locus.

Figure B.2 The effect produced by doubling and by halving each one of the fault parameters shown in Table 4.1, for a 1 kA, 60 Hz sinusoidal current $i(t)$.

in the curves $2 \cdot \ell$ and $2 \cdot V_O$. It suggests that the arc length and the constant voltage per arc length have an inversely proportional impact on the arc conductance. Higher values of ℓ and V_O lead to lower conductance, and hence the sustainability of the arcing fault becomes more difficult. For all the other cases, the peak conductance is around 9 S. Therefore, τ and G_{min} has little or no impact on the peak conductance. The impact of R_O is not significative since the arcing voltage is essentially rectangular, i.e., $R_O << V_O$. This is essentially true for any free air arc-flash.

In Figure B.2a, lower steady-state voltage is verified for the cases in which $g(t)$ is higher ($0.5 \cdot \ell$ and $0.5 \cdot V_O$), while higher steady-state voltage is observed for the cases in which $g(t)$ is lower ($2 \cdot \ell$ and $2 \cdot V_O$). This result is a direct consequence of the impact of $g(t)$ since $v(t) = i(t)/g(t)$ and can be interpreted as more voltage being necessary to sustain less conductive arcs. However, another consequence is exclusively verified because of the value of τ. For $2 \cdot \tau$, the peak transient arc voltage is higher and takes more time to vanish. For $0.5 \cdot \tau$, its value is lower, and it finishes faster. Therefore, it is easily concluded that τ has a direct impact on the waveform of the transient arc voltage after zero crossing.

Finally, G_{min} has appreciable effect only at the beginning of the fault, when $i(t) \approx 0$, $g(t - \Delta t) \approx 0$ and $g(t) \approx G_{min} \cdot \Delta t/(\tau + \Delta t)$. Since $v(t) = i(t)/g(t)$, a higher G_{min} results in higher $g(t)$, which in turn demands less voltage to strike the arc.

Appendix C

Registered Test Measurements

This appendix presents complementary results from the experiments previously reported in Subsection 4.4.2, specifically those executed on the Device #1 of Set #1. The information presented in this appendix has been collected during the characterization tests described in Subsection 4.4.1. Since the ac switch is composed by two thyristors, which have been named as T_2/T_1, ..., T_8/T_7, then the results have been organized here so that even thyristors are dealt with in the first section, while the odd thyristors are treated in the second one. The devices that have subjected to a large quantity of low-current tests achieved some degree of degradation, while those ones that have been exposed to high-current surge profiles achieved the catastrophic failure state.

C.1 Even Thyristors

None of the even thyristors has been identified to be under catastrophic failure, but degradation has been identified in some cases as detailed below.

C.1.1 Tests AC_06 to AC_15

Device T_8 presented a huge change in its terminal behavior after test AC_15, which can be clearly seen in the curves of Figure C.1 as well as in the resistance values shown by the green table of Figure C.2. The resistances between cathode and anode terminals have been verified to be decreased from MΩ to kΩ after the sequence of 10 tests performed.

T8 / V*x*I @ 60 ºC / Slope

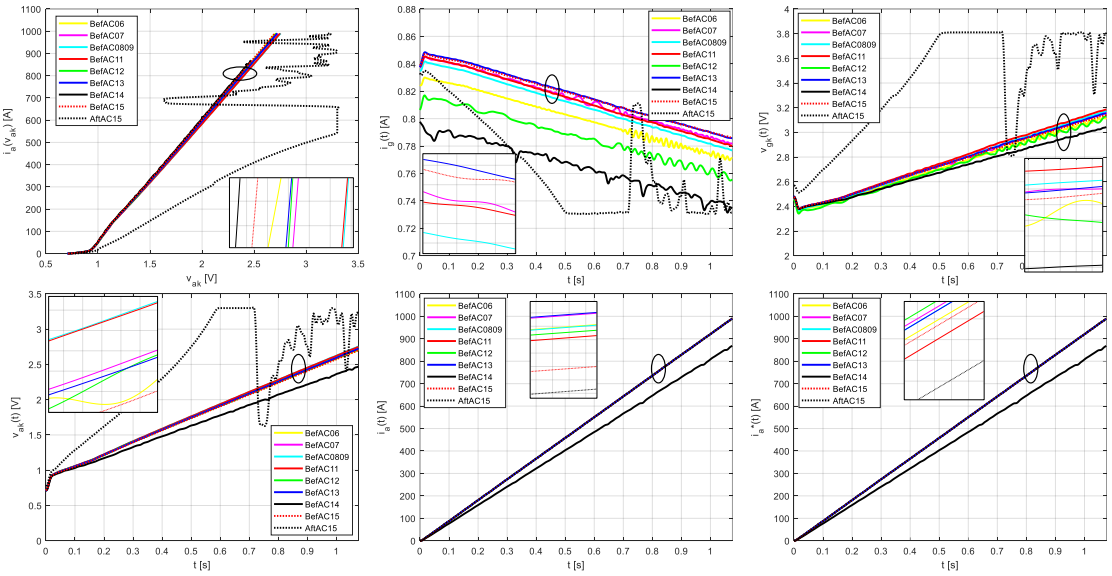


Figure C.1

T8 / Leakage @ 60 ºC; R @ T_{amb}

Before AC_06	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	13,1	526	59,6	12,3	526	59,6
	18,7	1050	59,6	17,6	1050	59,6

Before AC_07	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,5	526	59,9	11,6	526	59,8
	17,7	1051	59,7	16,6	1051	59,8

Before AC_08 and AC_09	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,7	525	59,8	12,1	526	59,9
	18,2	1051	59,9	17,1	1051	59,9

Before AC_11	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,5	526	59,8	11,8	526	59,9
	17,9	1051	59,9	16,9	1051	59,9

Before AC_12	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,5	526	59,7	11,7	525	59,8
	17,8	1051	59,7	16,8	1051	59,7

Before AC_13	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,3	526	59,8	11,5	526	59,7
	17,6	1051	59,7	16,5	1051	59,7

Before AC_14	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,3	526	59,7	11,5	526	59,7
	17,5	1051	59,7	16,4	1051	59,7

Before AC_15	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,1	526	59,6	11,5	526	59,7
	17,4	1051	59,6	16,4	1051	59,7

R @ Tamb					
Rgk [Ω]	Rkg [Ω]	Rag [Ω]	Rga [Ω]	Rak [Ω]	Rka [Ω]
19,70	19,70	200k0	202k9	73k2	74k5

Figure C.2

C.1.2 Tests AC_03 to AC_05

Device T_6 did not fail catastrophically nor degraded, as can be seen in the measurements presented in Figure C.3. The leakage current measured at 60 °C after each test did not show any significant variation. Notice that in this case the sequence of tests included 3 trials, which is greatly below the sequence of 10 trials that T_8 has endured.

T6 / Leakage @ 60 ºC; R @ T_{amb}

	Forward			Reverse		
Before AC_03	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	14,9	525	60,2	14,1	525	60,1
	20,7	1050	60,1	19,2	1050	60,1

	Forward			Reverse		
Before AC_04	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	13,4	526	59,2	13,0	526	59,3
	18,8	1050	59,3	17,7	1050	59,2

	Forward			Reverse		
After AC_04	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	14,2	525	59,6	13,9	525	59,7
	19,7	1050	59,6	18,7	1050	59,6

R @ Tamb					
Rgk [Ω]	Rkg [Ω]	Rag [Ω]	Rga [Ω]	Rak [Ω]	Rka [Ω]
17,13	16,87	5M324	5M594	5M326	5M569

Figure C.3

C.1.3 Test AC_02

Device T_4 has been subjected to one single test, after which it has been verified to be damaged by degradation. The electrical resistance between cathode and anode terminals has decreased to kΩ. The leakage currents measured at 60 °C have increased a little, as one can verify in the information provided by Figure C.5.

T4 / V*x*I @ 60 ºC / Slope

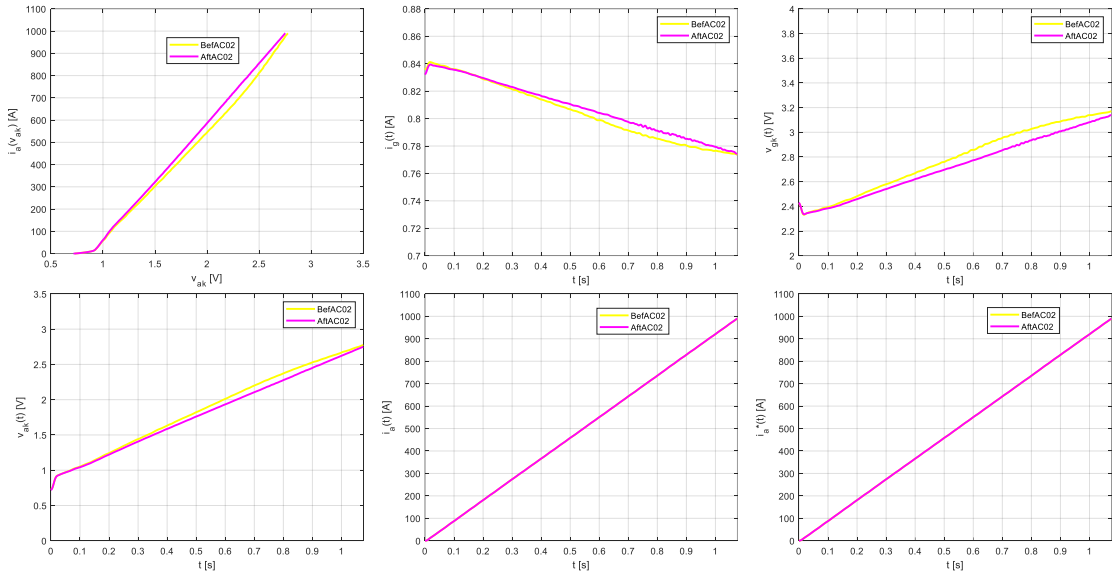


Figure C.4

T4 / Leakage @ 60 ºC; R @ T_{amb}

Before AC_02	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	12,7	526	59,9	11,2	526	59,4
	17,0	1050	59,7	15,0	1050	59,3

After AC_02	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	14,1	525	60,1	12,4	525	59,9
	19,1	1050	60,0	16,6	1050	59,9

R @ Tamb					
Rgk [Ω]	Rkg [Ω]	Rag [Ω]	Rga [Ω]	Rak [Ω]	Rka [Ω]
19,25	19,25	0M493	6M230	0M255	3M250

Figure C.5

C.1.4 Test AC_01

Despite the small difference observed in the curves of Figure C.6, device T_2 did not present any appreciable variation in the terminal resistances measured after the tests.

T2 / V*x*I @ 60 ºC / Slope

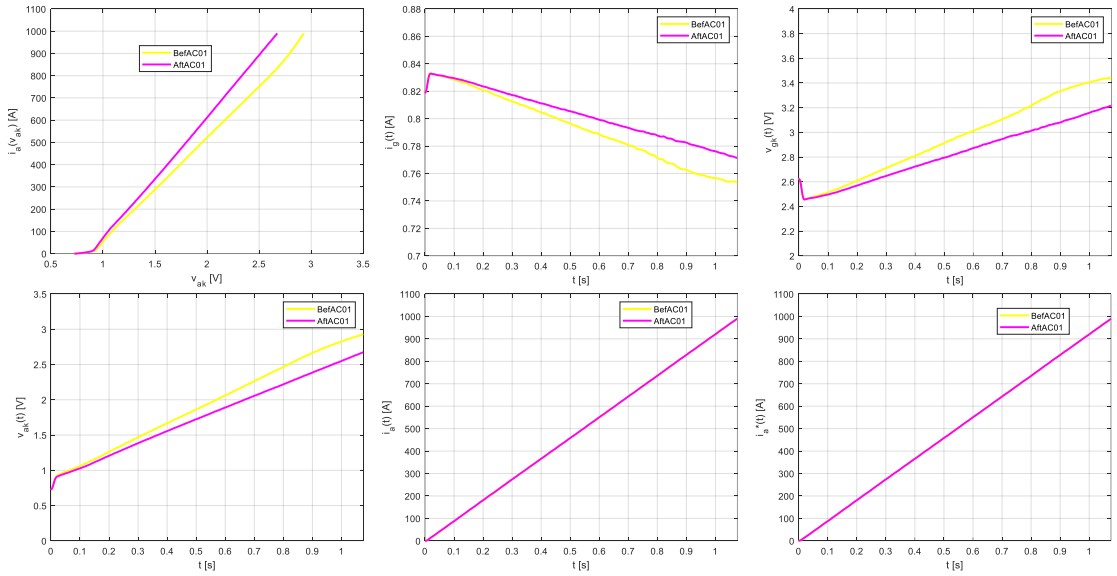


Figure C.6

T2 / Leakage @ 60 ºC; R @ T_{amb}

	Forward			Reverse		
Before AC_01	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	15,8	526	60,6	15,6	526	60,5
	22,9	1052	60,6	22,0	1052	60,4

	Forward			Reverse		
After AC_01	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	14,7	526	59,8	14,7	526	60,0
	21,4	1051	59,7	21,0	1051	59,9

R @ Tamb					
Rgk [Ω]	Rkg [Ω]	Rag [Ω]	Rga [Ω]	Rak [Ω]	Rka [Ω]
19,52	19,40	3M70	3M90	3M74	3M95

Figure C.7

C.2 Odd Thyristors

All the odd thyristors have been found to be damaged after the tests. Device T_7 degraded, while the other three have failed catastrophically.

C.2.1 Tests AC_06 to AC_15

The measurements presented by figures C.8 and C.11 show that the terminal resistances of device T_7 have decreased to kΩ after the long sequence of trials. At 60 °C the change is more noticeable than at 40 °C. The measurements performed after the device cooled down to room temperature, using a multimeter, confirmed how strong was the damage produced in the device by the sequence of trials. Figures C.9 and C.10 illustrate the change observed in the static characteristic curve of the device, which is also appreciable both at 60 °C and 40 °C.

T7 / Leakage @ 40 ºC

Before AC_06	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	2,11	526	40,1	2,14	526	40,1
	2,81	1051	40,1	2,84	1051	40,1

Before AC_07	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	1,94	525	39,8	1,97	525	39,9
	2,62	1050	39,8	2,64	1050	39,9

Before AC_08 and AC_09	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	1,94	526	39,5	2,00	526	39,8
	2,63	1050	39,6	2,64	1050	39,7

Before AC_11	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	1,96	525	39,9	1,96	525	39,9
	2,62	1050	39,9	2,60	1050	39,9

Before AC_12	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	2,08	525	40,2	2,10	525	40,2
	3,77	1050	40,2	2,77	1050	40,2

Before AC_13	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	1,93	525	39,6	1,95	526	39,7
	2,58	1050	39,6	2,60	1050	39,7

Before AC_14	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	1,96	526	40,2	1,96	526	40,2
	2,64	1051	40,2	2,62	1051	40,2

Before AC_15	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	2,04	526	40,3	2,01	526	40,3
	2,69	1051	40,4	2,68	1051	40,3

After AC_15	Forward		Reverse	
	R [kΩ]	T [°C]	R [kΩ]	T [°C]
	3,66	39,6	3,66	39,6

Figure C.8

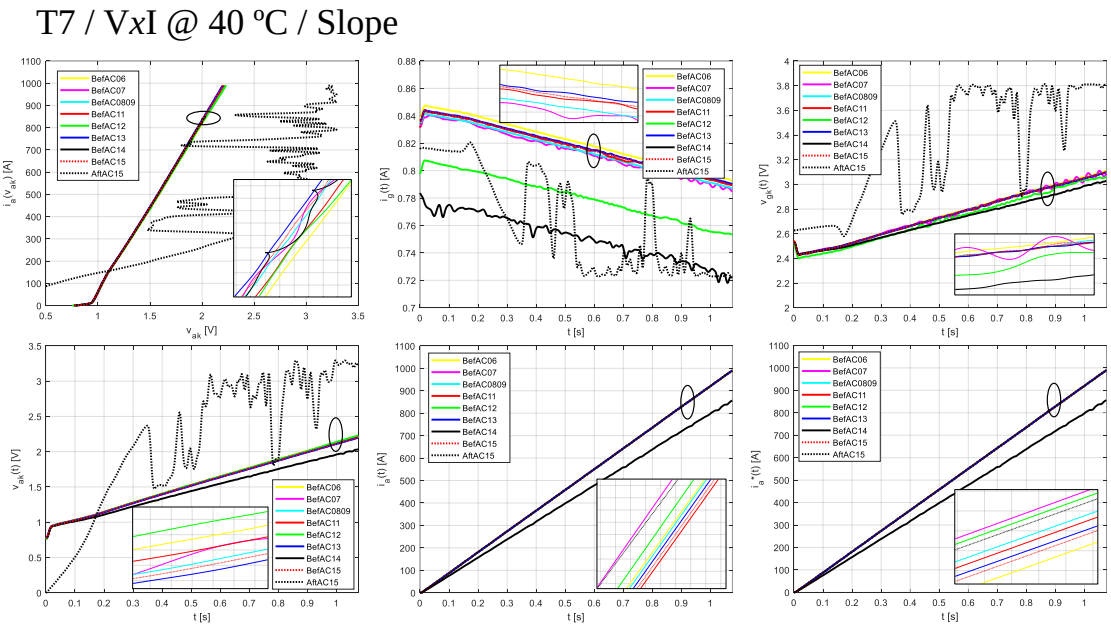


Figure C.9

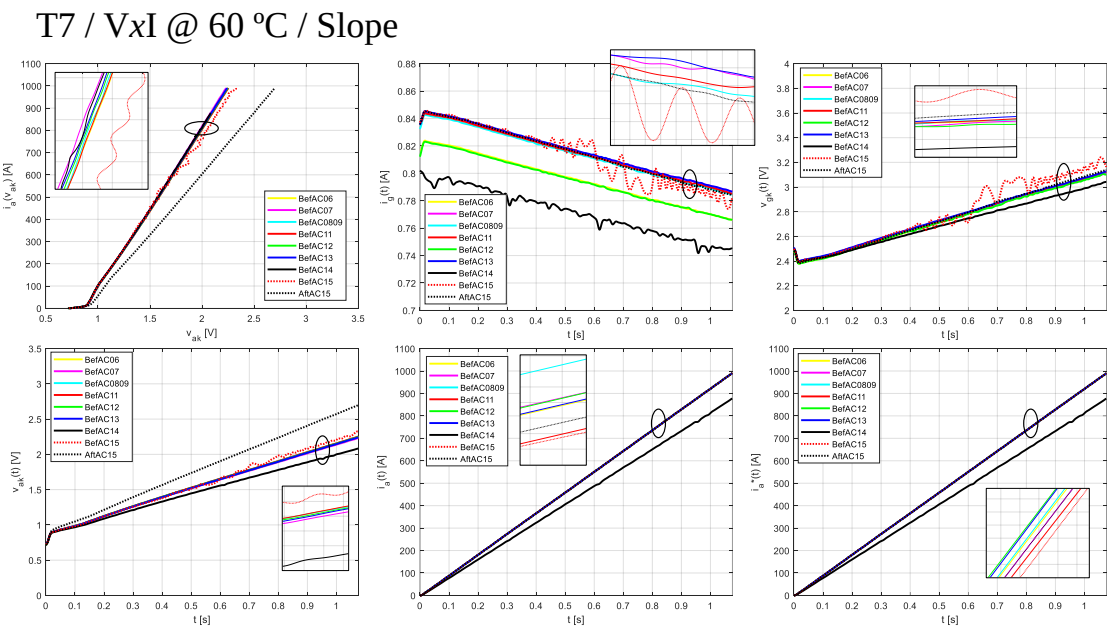


Figure C.10

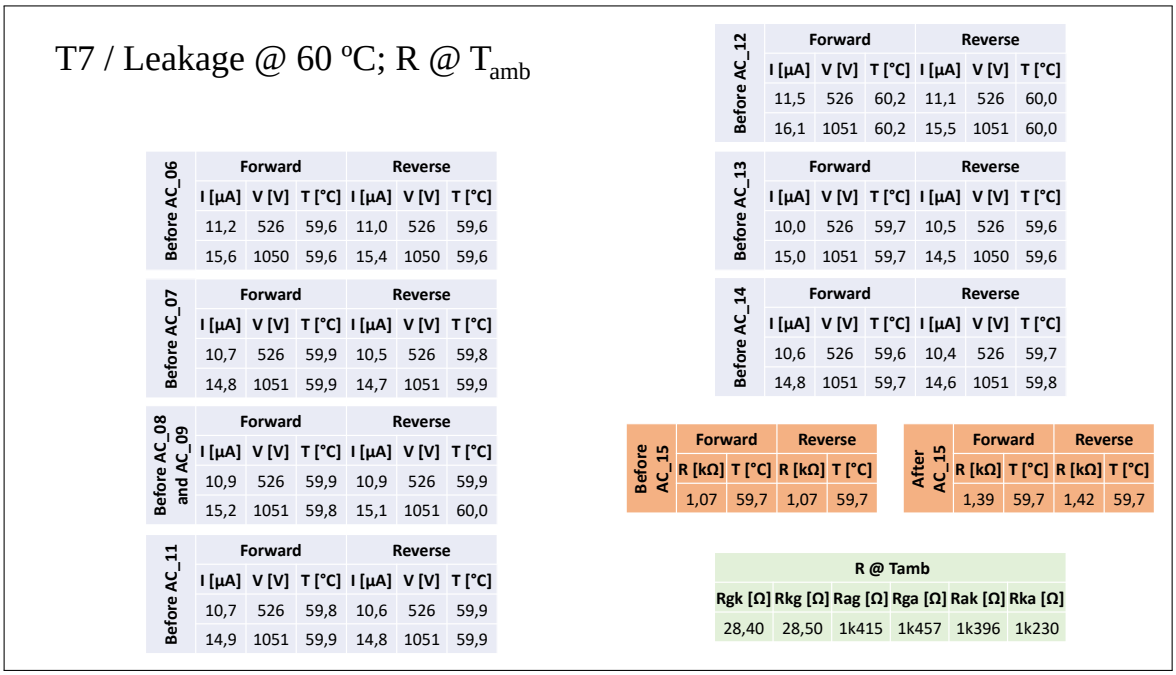


Figure C.11

C.2.2 Tests AC_03 to AC_05

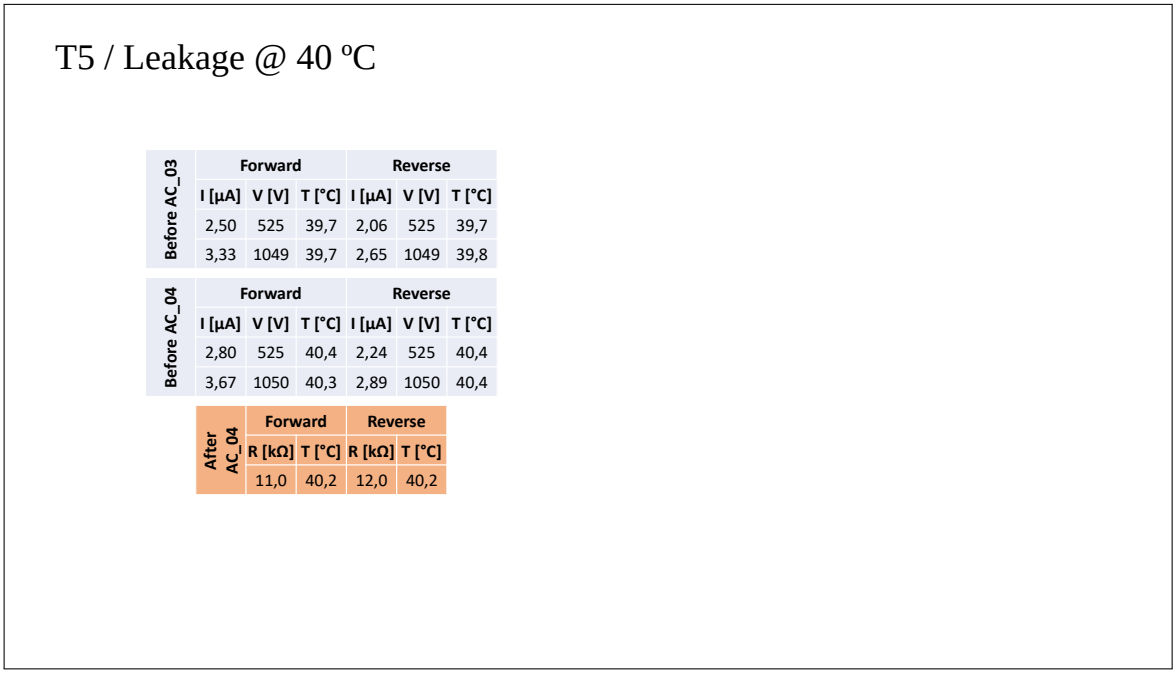


Figure C.12

Figures C.12 and C.15 illustrate how device T_5 has failed catastrophically, since its resistance has fallen down to less than 1 Ω after the execution of trial AC_04. The characteristic v vs. i curve of the device has changed a lot along the tests.

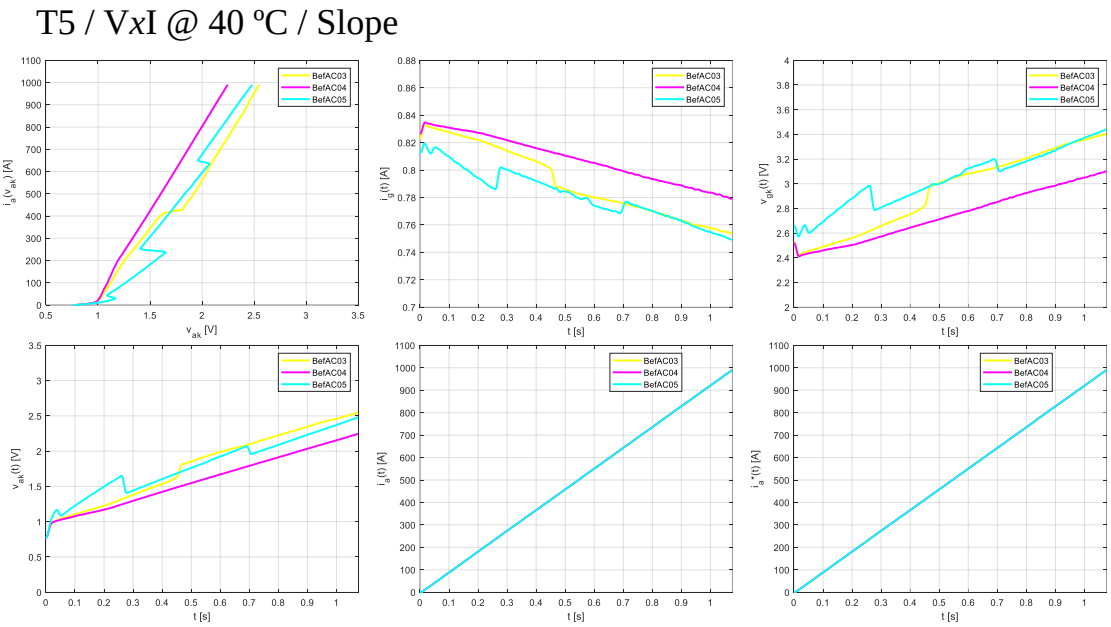


Figure C.13

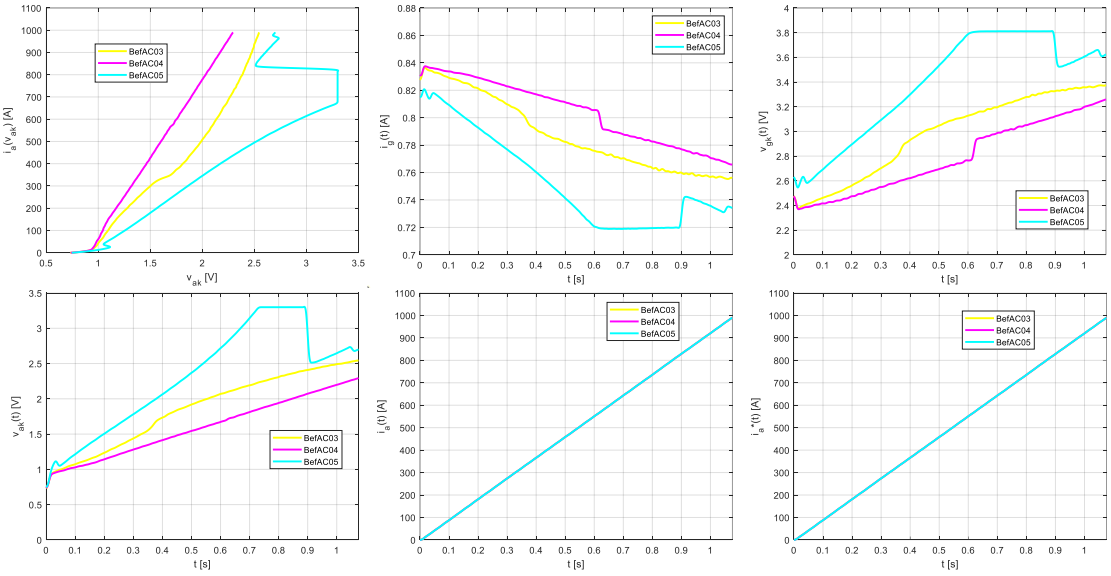


Figure C.14

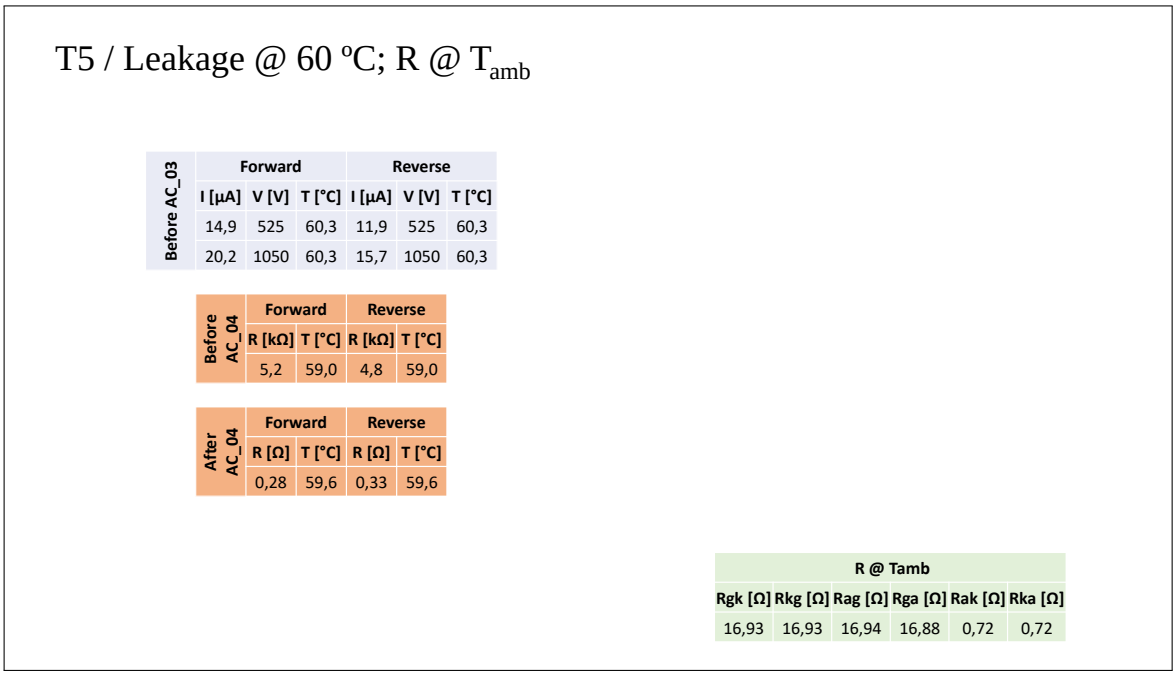


Figure C.15

C.2.3 Test AC_02

Figures C.16 and C.17 show that thyristor T_3 has been failed catastrophically.

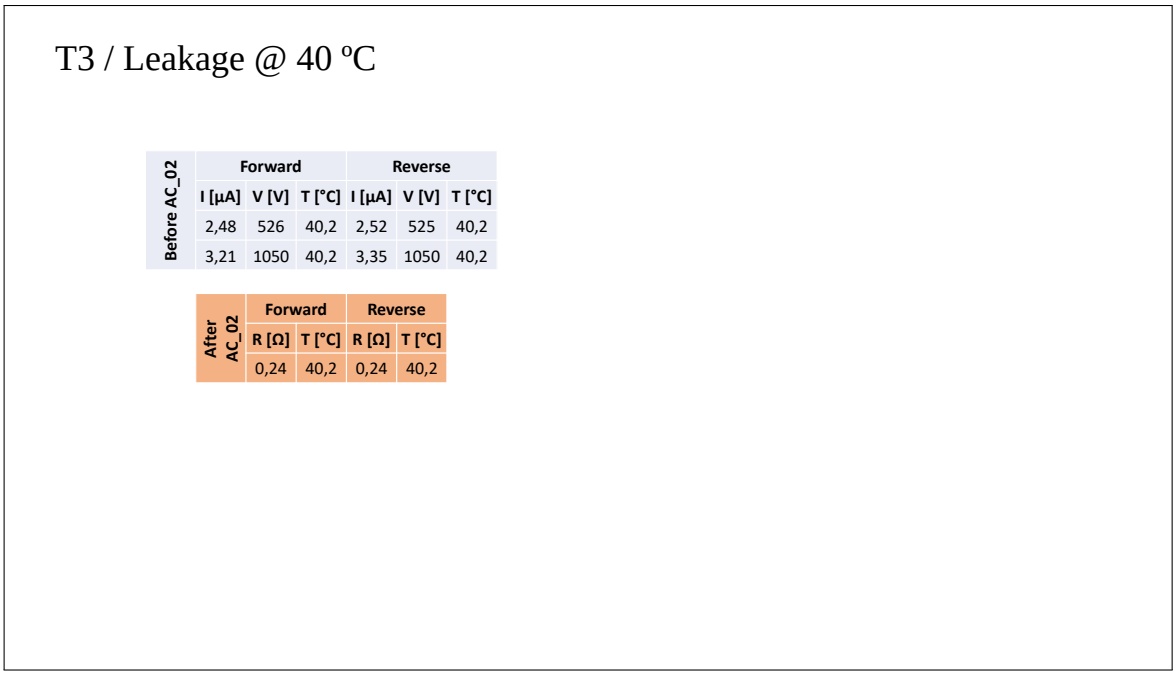


Figure C.16

T3 / Leakage @ 60 ºC; R @ T_{amb}

Before AC_02	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	11,6	525	59,9	12,1	526	60,1
	15,6	1050	59,8	17,0	1050	60,1

After AC_02	Forward		Reverse	
	R [Ω]	T [°C]	R [Ω]	T [°C]
	0,15	60,2	0,15	60,2

R @ Tamb					
Rgk [Ω]	Rkg [Ω]	Rag [Ω]	Rga [Ω]	Rak [Ω]	Rka [Ω]
2,47	2,47	2M47	2M41	0M55	0M66

Figure C.17

C.2.4 Test AC_01

Figure C.18 shows that T_1 has failed catastrophically during test AC_01.

T1 / Leakage @ 60 ºC; R @ T_{amb}

Before AC_01	Forward			Reverse		
	I [µA]	V [V]	T [°C]	I [µA]	V [V]	T [°C]
	10,4	526	60,8	11,0	526	60,7
	15,8	1052	60,7	16,1	1052	60,6

R @ Tamb					
Rgk [Ω]	Rkg [Ω]	Rag [Ω]	Rga [Ω]	Rak [Ω]	Rka [Ω]
1,28	1,36	1,33	1,28	1,00	1,00

Figure C.18