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School of Engineering
Graduate Program in Electrical Engineering

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Performance Comparison of Single-Phase PV Inverter Topologies Regarding Efficiency and Power Density

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Performance Comparison of Single-Phase PV Inverter Topologies Regarding Efficiency and Power Density

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FOLHA DE APROVAÇÃO

"PERFORMANCE COMPARISON OF SINGLE-PHASE PV INVERTER TOPOLOGIES REGARDING EFFICIENCY AND POWER DENSITY"

AUREAN BELO GUIMARAES JUNIOR

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I dedicate this work to my family, my friends, and my dear wife Edicelma.

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I would like to express my gratitude, first and foremost, to God for always being with me and my family, helping us in ways we may never fully comprehend. I extend my thanks to my wife, Edicelma, for standing by my side during both joyous and challenging moments, for her patience, and understanding throughout periods where anxiety created challenges in the development of this work.

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"The fear of the Lord is the beginning of wisdom: and the knowledge of the holy is understanding."

Proverbs 9:10

RESUMO

A performance de topologias de inversores monofásicos em relação à sua densidade de potência e eficiência é investigada nesta dissertação. O principal objetivo é avaliar as vantagens competitivas entre as topologias e determinar qual é mais viável para implementação em aplicações de energia fotovoltaica. Neste trabalho, um algoritmo de força bruta multiobjetivo é implementado para gerar diversos designs de inversores para cada topologia, criando um espaço de soluções. A otimização usando a técnica da frente de Pareto seleciona designs ótimos para comparação com as topologias em estudo. Ao contrário de muitos estudos encontrados na literatura, este algoritmo multiobjetivo utiliza um banco de dados de componentes reais e suas informações de datasheet em vez de métricas médias da indústria, portanto, o resultado do algoritmo de design relaciona-se a uma implementação real da estrutura do conversor, portanto, os índices de desempenho referem-se a um sistema real em vez de um limite teórico da indústria. Por fim, este estudo multiobjetivo leva em consideração o design de cada dispositivo eletrônico, magnético e dissipador de calor, onde cada topologia pode fornecer um espaço de solução mais ótimo do que outra topologia.

Palavras-chave: Inversores monofásicos, Energia fotovoltaica, algoritmo multi-objetivo, Eletronica de potência, Fronteira de Pareto

ABSTRACT

The performance of single-phase inverter topologies in relation to their power density and efficiency is investigated in this dissertation. The main objective is to assess the competitive advantages among topologies and determine which one is more viable for implementation in photovoltaic energy applications. In this work, a brute force multi-objective algorithm is implemented to generate various inverter designs for each topology, creating a solution space. Optimization using the Pareto-front technique selects optimal designs for comparison with the topologies under study. Unlike many studies found in the literature, this multi-objective algorithm uses a database of real components and their datasheet information instead of industry average metrics, hence the outcome of the design algorithm relates to an actual implementation of the converter structure, therefore the performance indexes refer to a real system rather than a theoretical industry boundary. Finally, this multi-objective study takes into account the design of each electronic, magnetic, and heatsink device, where each topology can provide a more optimal solution space than another topology.

Keywords: Single-phase inverters; Photovoltaic energy; Multi-objective algorithm; Power electronics; Pareto-front.

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1 INTRODUCTION

1.1 Contextualization

1.1.1 Brazilian energy matrix

The continuous and exponential growth of the world population has been challenging the global energy model. The goal of developing and expanding sustainable energy sources has driven increasing interest in cleaner energy forms, aiming to mitigate significant alterations to the planet's climate conditions (MIRANDA, 2013). On a global scale, according to (IEA, 2021), between 1971 and 2019, the total energy supply (TES) increased by 2.6 times in energy demand (from 230 EJ to 606 EJ). Nevertheless, non-renewable sources like fossil fuels (oil and coal) saw significant declines. For instance, oil's share of the total energy supply dropped from 44% to 31% between 1971 and 2010, while coal consistently held its second position as the largest contributor to the global energy matrix, accounting for 162 EJ in 2019.

Consequently, renewable energy sources like hydro, biofuels, and others have gained greater importance due to climate change concerns and the investigation for a more sustainable energy matrix. As Figure 1 shows, between 1971 and 2019, renewable energy sources experienced a notable increase a 12.9% (29.67 EJ) share of the electricity matrix to 14.1% (85.45 EJ), respectively, considering hydro, biofuels, and other renewables. However, the dependence on non-renewable sources such as coal, oil, and natural gas as primary energy sources remains noticeably predominant.

Turning to a national scenario, according to (URBANETZ et al., 2019), the reason for the growth of solar energy in Brazil occurred after the release of Normative Resolution No. 482/2012 of ANEEL, which regulated the energy compensation system. Additionally, it can be considered that the demand for solar energy source technology was derived through scientific contributions and government incentives for creating new sustainable energy sources in the country.

Continuing in the national scenario, Figure 2 depicts the Brazilian energy matrix that is composed not only of non-renewable sources but also of renewable sources, together representing all available energy sources in the country necessary to perform work, whether mechanical, electrical, thermal. Indeed, Brazil has an energetic matrix that utilizes more renewable sources than the rest of the world. Combining wood and charcoal, hydro, sugarcane, wind, solar, and other renewables, all together account for 47.4%, nearly half of the energy matrix. In terms of solar energy production, the percentage of solar power plants is still insignificant compared to other sources. Therefore, we can speculate that

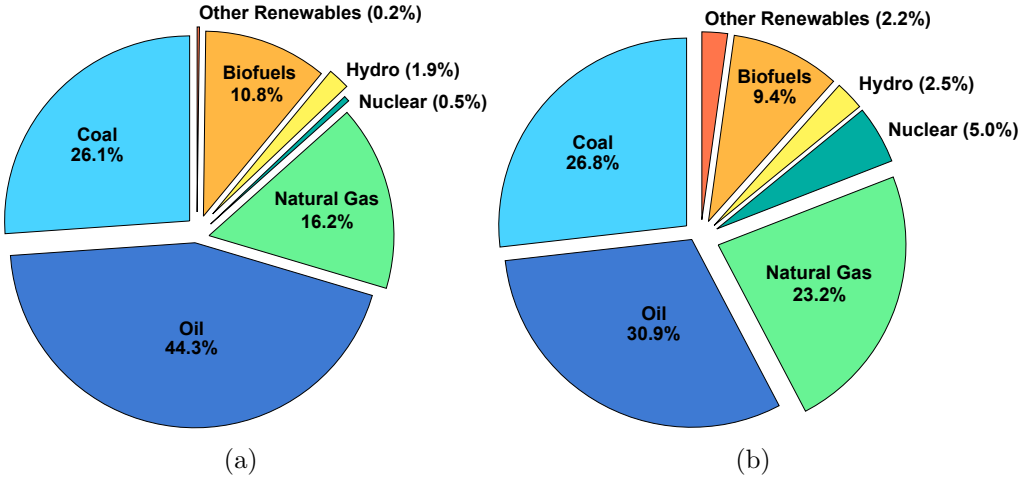

Figure 1 – World Energy Balance. (a) In 1971, (b) In 2019
Font: adapted from (IEA, 2021)

over the years, as solar energy production technology becomes more accessible, there will be greater demand for this innovation.

Regarding the Brazilian electric matrix, e.i, all types of energy sources that are available to be converted into electricity. Figure 3 illustrates that the Brazilian electricity grid is predominantly composed of 63.1% hydro, followed by wind generation (12.1%), biofuels (8.1%), and solar photovoltaic (4.4%). This information is noteworthy as it signifies Brazil's growing efforts to reduce the usage of non-renewable energy sources.

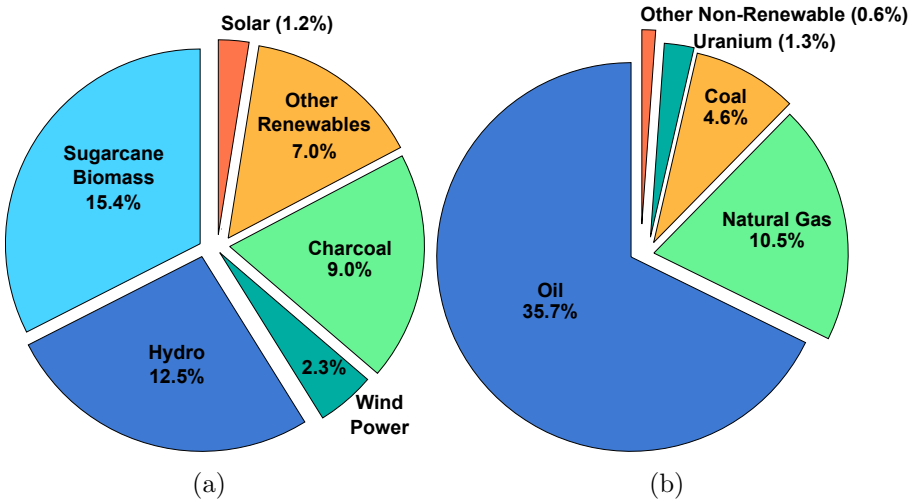

Figure 2 – Breakdown of total energy supply in Brazil - TES 2022. (a) Renewables, (b) Non-Renewables
Font: adapted from (EPE, 2023)

According to (BARBOSA et al., 2017), the Northeast of Brazil has been showing lower interannual variability for solar irradiation, ranging from 5.7 to 6.1 kWh/m2. This indicates that the region is technically feasible for the implementation of solar energy, as

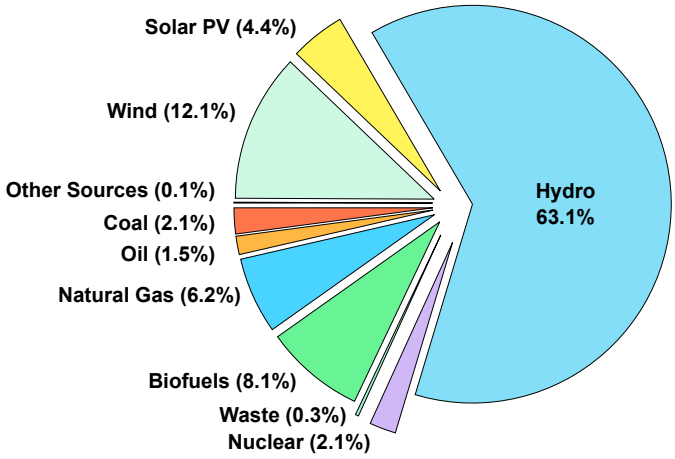

Figure 3 – Brazilian electricity generation sources in 2022
Font: adapted from (EPE, 2023; IEA, 2021)

the annual radiation index is 11,400 MW/year. Consequently, the implementation of this technology in this region of Brazil will not only bring social benefits to the local population but also drive the country as a whole towards a more sustainable energy matrix, aligning with a global agenda currently concerned with climate change worldwide.

1.1.2 Inverters in renewable energy systems

Renewable energy sources are typically connected to the utility grid through an inverter. Depending on the application, such as grid-connected inverters, these can be classified as grid-forming, grid-feeding, and grid-supporting inverters (SILVA, 2019). According to (HACKEL; FARKAS; DAN, 2015), grid-forming inverters are extremely important for the operation of a microgrid, or other system, in the absence of the main grid because these devices have the capacity to generate frequency and voltage references, similar to an uninterruptible power supply (UPS). On the other hand, grid-feeding inverters are not capable of generating frequency and voltage references, thus they must always operate connected to the main grid, and in the circumstance of its absence, at least one grid-forming inverter must operate when a microgrid is operating in island mode. Finally, grid-supporting inverters are devices that operate both as grid-forming and grid-feeding since their main objective is to contribute to the regulation of the utility grid by injecting active and reactive power.

The efficiency of inverters in systems connected to the Brazilian electrical grid is one of the most important criteria in terms of qualification because it allows for the comparison of equipment with similar characteristics. This point does not refer to the maximum efficiency that inverters can achieve but rather takes into consideration the fact that the inverter does not operate at full power all the time (PINTO; ZILLES; ALMEIDA, 2011). According to the authors, the explanation for the equation (1.1) is that the weighting coefficients are based on the solar radiation profile in Brazil and represent the contribution

of each irradiance band of the national average to the annual irradiation, assuming that at 1000 W/m^2 we have the nominal output power of the inverter. Figure 4 illustrates the points of a generic *efficiency x loading* curve used in the calculation of Brazilian Efficiency, with the blue circles on the curve representing the points of average total efficiencies at the indicated loadings, and the red bars representing the participation of each irradiance band of the national average in the annual irradiation.

$$\begin{aligned}\eta_{BR} =& 0.02\eta_{TMED10\%} + 0.02\eta_{TMED20\%} + 0.04\eta_{TMED30\%+} \\ & 0.12\eta_{TMED50\%} + 0.32\eta_{TMED75\%} + 0.48\eta_{TMED100\%}\end{aligned} \tag{1.1}$$

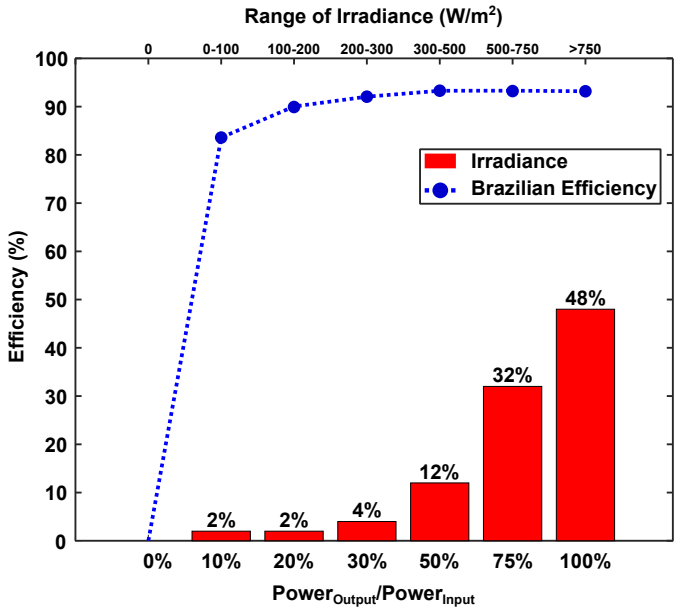

Figure 4 – Illustration of the points of a generic efficiency x loading curve used in calculating the Brazilian Efficiency.
Font: adapted from (PINTO; ZILLES; ALMEIDA, 2011)

Therefore, based on the results presented by (PINTO; ZILLES; ALMEIDA, 2011), it is worth noting that this study was conducted to define the converter's efficiency concerning its use based on local irradiation. However, other works, such as those presented by (BURKART, 2016), follow a research line focused on optimizing these inverters. Observing the state of the art, new technologies or more modern components contribute to building more efficient equipment with lower power density and higher reliability. In other words, there is a whole optimization study aimed at seeking new, more sophisticated equipment with better performance.

1.2 Motivation

In recent years, promoting the energy transition from a fossil-fuel based energy matrix to a more renewable one, alongside with enabling net zero energy solutions to

buildings and industrial facilities, have been the focus of the energy sector worldwide. Solar Photovoltaic (PV) power generation plays a crucial role in the success of these endeavors, since it poses as the fastest growing renewable energy resource, responding for over 65% of the total global renewable power capacity additions in 2022 (IEA, 2023), of which nearly half of those additions are related to distributed PV units.

In this context, improving the performance of Solar PV systems, *eg*, increasing efficiency and reducing footprint and cost, is a necessity for the industry, since it allows for enhancing power generation capacity utilization as well as making the solution more accessible to the broad public. This philosophy can be extended to the design of the solar PV inverters, through a multiobjective approach that searches for possible design solutions that improve performance indexes such as efficiency, power density, cost, reliability, etc (BURKART, 2016). Indeed, a higher performance power electronic system ensures continuous productivity growth and opens a range of applications for the development of clean energy generation (TEODORESCU; LISERRE; RODRIGUEZ, 2011).

The use of a multiobjective design approach not only allows for the definition of the optimal configuration of a given converter topology, but also enables the confrontation of different design proposals, since the limitations, advantages and disadvantages of each topology, component's technology and modulation schemes can be quantified in terms of the Pareto-front of each solution performance space. As a practical example, in (NEUMAYR, 2020a; NEUMAYR, 2020b), the authors evaluate the design approaches proposed for the Google Little Box Challenge, which was a competition proposed by Google Inc. in association with the IEEE that rewarded the single-phase inverter design that could implement a 2kVA/450Vdc/230Vac with over 95% efficiency and with the higher power density. In those papers, a Pareto-front analysis approach was used to investigate the best performance designs of a variety of topological and modulation solutions and thus define the best candidate for the competition, in result a 14.8 kW/dm^3 and 96% efficiency converter was designed.

1.3 Objectives

In this master's thesis we focus on the evaluation of the performance of single-phase solar PV inverter topologies, in terms of their efficiency and power density. This investigation aims at understanding whether particular converter topologies would have competitive advantages for the application in solar PV systems and how a multiobjective approach could lead to optimal performance designs.

1.3.1 Specific objectives

As specific objectives for this Thesis, it can be cited:

1. Build a *Matlab/Simulink* platform to analyze the operation of distinct converters applied to PV inverters, ie, provide converter simulation, passive elements automated design and estimation of power losses and component's volume;
2. Incorporate a database of electronic devices, such as power switches, diodes, capacitors and magnetic cores, for realistic estimation of performance indexes;
3. Evaluate the Pareto-front of the performance indexes efficiency and power density for each selected topology for a range of switching frequencies and compare those results to determine competitive advantages between topologies.

1.4 Publications

The results of this master's thesis studies have been published in the following conference paper, presented at the 17th Brazilian Power Electronics Conference and 8th IEEE Southern Power Electronics Conference, in Florianopolis.

- A. B. Guimaraes Junior and T. R. Oliveira, "Performance Comparison of Single-Phase PV Inverter Topologies Regarding Efficiency and Power Density," 2023 IEEE 8th Southern Power Electronics Conference and 17th Brazilian Power Electronics Conference (SPEC/COBEP), Florianopolis, Brazil, 2023, pp. 1-8,

1.5 Thesis structure

In Chapter 2, the theoretical foundation of this work will be presented, covering topics such as the modeling of a photovoltaic panel, a discussion of solar inverter architecture explaining the energy conversion stages, and, most importantly, a description of each topology under study. Concerning the topologies, subjects related to the chosen PWM modulation, the operational states of the switches, and the characteristics of each topology will be addressed. Following this, a brief study of the filters that interface between the converter and the grid will be presented, along with how each behaves in attenuating harmonics produced by the inverter during switching. Finally, if not the main part of this work, the multi-objective design will be detailed, showcasing the algorithm responsible for constructing an inverter based on real components inserted into a database, as well as the methodology by which the Pareto frontier is explained fundamentally for the results of this work.

In Chapter 3, the results obtained through simulations using Simulink and the multi-objective algorithm employed in this work will be presented. However, this chapter comprises two case studies, showcasing the performance of each inverter topology based on the Pareto frontier. Case Study I has the main parameter of an 800V DC bus to enclose both full-bridge and NPC topologies. Due to the split capacitor in NPC topologies, the DC bus voltage is divided by 2, resulting in the converter synthesizing a maximum of 400V in each half-cycle. Therefore, Case Study II will only present results for full-bridge topologies, given that the inverter will operate with a 400V DC bus voltage, as NPC topologies are unable to synthesize grid voltage with this voltage. Thus, based on a cost function, only one inverter design for each topology is chosen, showcasing the distribution of losses and volume, as well as each component used to build such inverters.

Moving on to Chapter 4, the conclusion of this work is presented. In this section, a comprehensive discussion of the overall results obtained throughout the study is explored. Additionally, future work and potential areas for improvement are summarized. Last but not least, a reflection on the significance of the findings and their implications for the field is provided.

2 THEORETICAL FOUNDATION

As previously discussed, the aim of this thesis is to assess the performance of different Solar PV Inverter topologies in search for competitive advantages between them through the use of a multiobjective design approach. In this chapter, we present the Theoretical Foundations of the work proposed herein, where we explore the structure and modeling of PV systems, the architecture and PWM modulation of classical inverter topologies employed in the industry, as well as we discuss the algorithm of the considered multiobjective converter design.

2.1 Photovoltaic system model

A PV system can be classified based on the end-use application which can be grid-connected or stand-alone. Grid-connected PV systems are able to convey power into the utility grid, allowing for the transfer of surplus power from the consumer installation back to the grid, thus not requiring a storage device to ensure power balance. It requires that the PV inverter is synchronized with the utility grid voltage, which demands the use of synchronization methods such as the implementation of a PLL to operate efficiently. Moreover, grid-connected PV systems ought to compy with grid codes at the point of common coupling, thus harmonic injection, unintentional islanding events and other power quality issues must be attended by the inverter control system. Furthermore, stand-alone systems require the incorporation of a battery storage system to smooth out the PV power generation and guarantee power balance between the PV system and the supplied load. Therefore, the PV system needs to be designed to supply the entirety of the load energy demand, whereas the inverter must withstand the total power capacity of the installation. All those situations make the stand-alone solution much more expensive than the grid-connected one, hence, it is suitable for applications where no utility grid is available.

The main component of PV power generation unit is the PV panels, which, when exposed to sunlight, converts the sun irradiation into electricity. The PV panels are composed of multiple PV cells associated in series and parallel. The PV cell is build as a reversed biased PN junction that uses the energy transferred by photons hitting the depletion layer to produce charge carriers that will be displaced to the doped by the potential barrier. The cell can be modeled as depicted in Figure 5, where I_{PV} represents the photo-generated current, I_d is PN junction current, R_p represents the self-consumption of the PV cell and R_S is the body resistance of the cell.

As shown in (VILLALVA; GAZOLI; FILHO, 2009a) and (VILLALVA; GAZOLI;

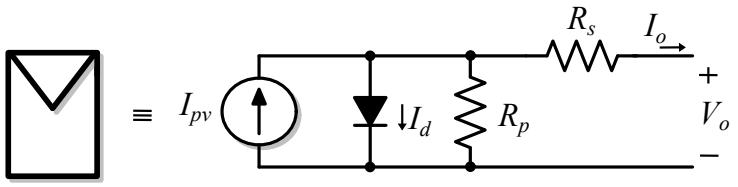

Figure 5 – Photovoltaic Practical Model
Font: The author

FILHO, 2009b), the characteristic $I - V$ curve of a PV cell can be described by equation (2.1). It can serve a single cell, or a panel, where I_{pv} would be regarded as the photo-generated current times the number of cells connected in parallel (N_p). I_d is defined by the Shockley diode equation as shown in (2.2).

$$I_o = I_{pv} - I_d - \frac{V_o + R_s I_o}{R_p} \tag{2.1}$$

$$I_d = I_s \left[exp\left(\frac{q(V_o + R_s I_o)}{akTN_s} \right) - 1 \right] \tag{2.2}$$

Where I_s is the reverse saturation or leakage current of the diode, q is the electron charge ($1.60217646 \cdot 10^{-19}$C), N_s is the number of cells connected in series, k is the Boltzmann constant ($1.3806503 \cdot 10^{-23}$J/K), T is the temperature of the $p - n$ junction in Kelvin [K], and a is the diode ideality constant.

Implementing this circuit in simulation software requires that R_s, R_p, and a can be estimated. Previous studies have reported that R_s represents the influence of the sum of several structural resistances of the PV devices, and R_p exists due to the leakage current of the PV cell $p - n$ junction. In addition, it is demonstrated by (VILLALVA; GAZOLI; FILHO, 2009a) a method for adjusting the pair (R_s, R_p) that guarantees that maximum power calculated using the model ($P_{max,m}$) is equal to the maximum power point from the PV module datasheet($P_{max,d}$), i.e., $P_{max,m}$=$P_{max,d}$. To summarize, the value of a is arbitrarily chosen and it is around $1 \leq a \leq 1.5$ which can affect the curvature of the characteristic $I - V$ curve and marginally improve the model accuracy.

For instance, by applying the methodologies introduced in (VILLALVA; GAZOLI; FILHO, 2009a) and (VILLALVA; GAZOLI; FILHO, 2009b) to a SunPower X21-470-COM Panel, whose electrical specifications are provided by the manufacturer and listed in table 1, it was possible to extract the I-V and P-V characteristic curves from the electrical panel. Another important information obtained from this methodology is the values of R_s and R_p, which are 0.5160Ω and 610.6201Ω, respectively for that panel. Since the Inverter behavior is independent of the chosen PV panels, in this thesis the SunPower X21-470-COM model was considered for the simulation model.

The significance of the characteristic IxV and PxV curves is to demonstrate the

Table 1 – SunPower X21-470-COM Electrical Data

Maximum Power (Pmax)	470 W
Rated Voltage (Vmpp)	77.6 V
Rated Current (Impp)	6.06 A
Open-Circuit Voltage (Voc)	91.5 V
Short-Circuit Current (Isc)	6.45 A

Font: Manufacturer Datasheet

PV panel's performance considering different operation conditions. External agents, such as shading on the panels and temperature rising, are variables that influence the panel performance.

Figure 6 depicts the P-V curve, that is, the variation of power regarding the panel voltage. For temperature variation, considering constant irradiation, it is possible to observe that the power decreases as the temperature rises. Similarly, if the temperature is constant while the irradiance changes then the power decreases as the irradiance decreases.

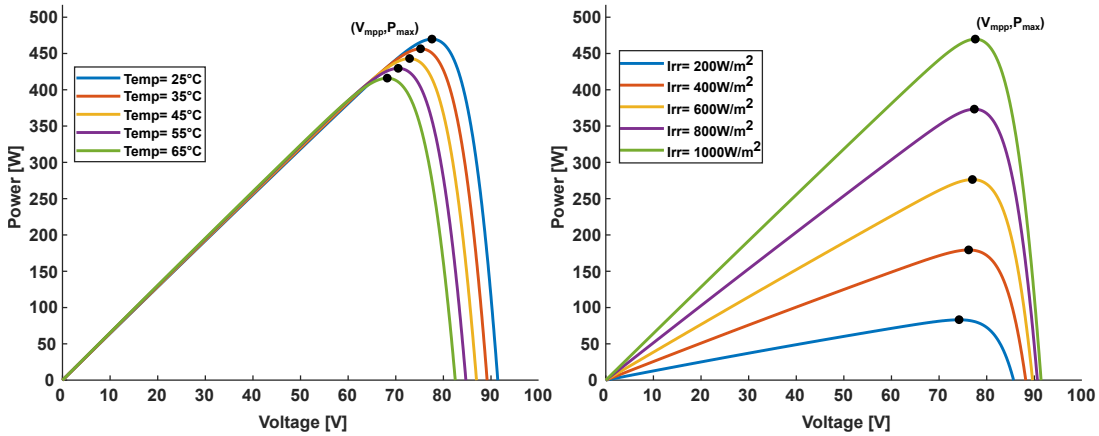

Figure 6 – Curve P-V
Font: The author

Figure 7 shows the I-V curve, that is, the variation of output current with respect to the panel voltage. In cases which the irradiance remains constant and the temperature changes, it leads to a leftward shift in the I-V curve. Which means that in temperature above 25°C, the open-circuit voltage decreases. On the other side, maintaining constant the temperature and changing the irradiance, it is possible to note the proportionality between the irradiance and electrical current. Thus, as the irradiance decreases, the electrical current decreases as well.

As a consequence of the variation of the panel maximum power point (MPP) with externalities, it is necessary the implementation of tracking algorithms, so that the panel can be kept in its MPP independently of the environmental conditions. Named as Maximum Power Point Tracker (MPPT), it is an algorithm used to extract the maximum power from PV panels, assuring maximum power generation capacity. In (SARVI; AZADIAN, 2022), it is presented an overview of different MPPT algorithms, whose main objective is

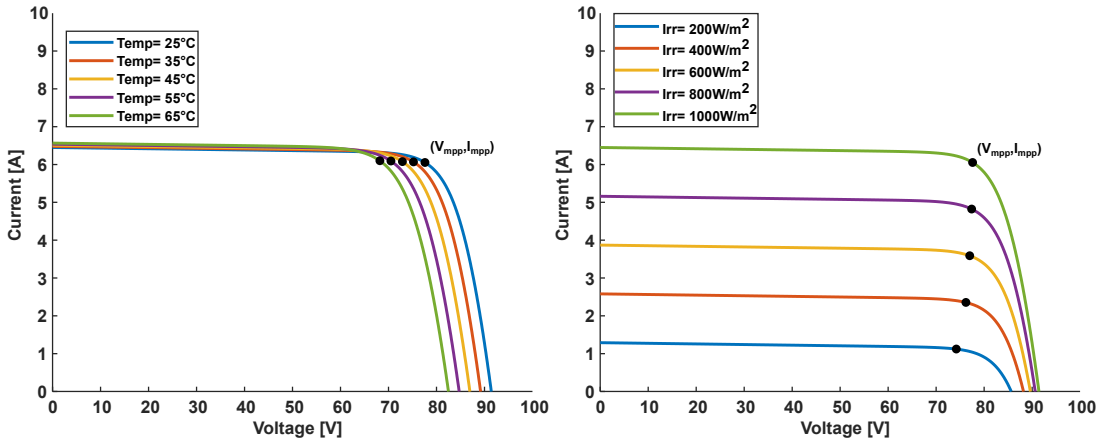

Figure 7 – Curve I-V
Font: The author

to demonstrate the advantages and disadvantages of each one.Is beyond the scope of this thesis to delve into MPPT strategies, therefore, for the studies conducted in this work, we have considered a Perturb and Observe (P&O) method, which is a widely used method in both academia and industry.

2.2 Conversion architecture of PV inverters

In this chapter, two grid-connected solar PV inverter architectures will be presented: the single-stage and the dual-stage. Figure 8 illustrates the single-stage architecture. In this architecture all features of the PV inverter are performed by the DC/AC converter, ie, the inverter must perfom the MPPT as well as to control the power injection into the utility grid and the power quality ate the point of common coupling (PCC). Although more efficient, this approach requires that the sampling time used in the MPPT algorithm must be compatible with computation of the inverter output power, ie, steps in the P&O algorithm take several grid cycles to occur, hence the MPPT is quite slow. Moreover, since the inverter behaves as a step-down converter, the PV panels must always exhibit a higher voltage than the AC grid peak voltage. Furthermore, regarding single-phase applications, the instantaneous imbalance between the DC and AC sides power results in a double-line-frequency voltage ripple, which is converted in power generation oscillations. Consequently, a large number of electrolytic capacitors are required to achieve stable operation and maintain high MPPT algorithm performance, effectively suppressing the 2ω ripple. As a consequence, a high volume of decoupling capacitors is expected, increasing the possibility of equipment failure when it operates in extreme conditions, such as high temperatures (YUAN et al., 2019; LI et al., 2016).

On the other hand, a two-stage inverter, as shown in Figure 9, consists of two converters separated by a DC bus. The first stage comprises a DC/DC converter responsible for executing the MPPT algorithm to extract the maximum power from the PV panels.

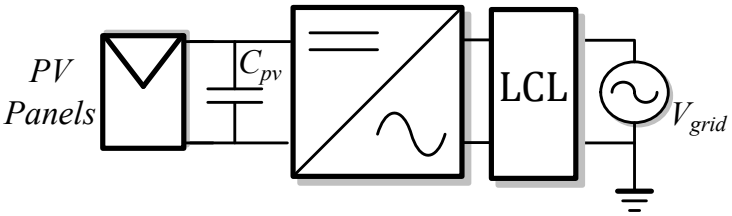

Figure 8 – Single Stage PV Inverter
Font: The author

Meanwhile, the second stage, formed by a DC/AC converter, is responsible for regulating the DC bus and injecting the extracted power into the grid, while complying with the grid codes. This architecture is less efficient than the previous one, but it allows for lower DC bus capacitance, and faster MPPT convergence, which impacts the inverter cost, density, and reliability.

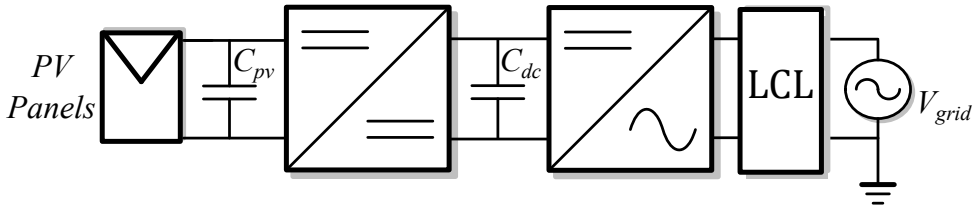

Figure 9 – Two Stage PV Inverter
Font: The author

Given these facts, this work will consider the dual-stage inverter. However, the main focus will be on the DC/AC converter, responsible for grid current control and DC bus regulation. This architecture is more advantageous for single-phase PV applications due to the independence of control between the stages, where the DC bus capacitor serves as an active power decoupling element. This enables the DC/DC converter to maintain a constant DC power, and the inverter to deliver pulsating AC power (J, 2011). Thus, it becomes convenient to work with various other inverter topologies without altering the operating characteristics of the DC/DC stage.

Therefore, the DC/DC converter won't be considered in the multi-objective algorithm. The study proposed in this paper is focused on the inverter side, i.e., the Boost converter, although present in the simulations, is not included in the computation of the performance indexes, which implies that the same Boost converter design would be used in all considered implementations in Matlab/Simulink.

2.3 DC/AC converter topologies

The literature presents a vast number of inverter topologies proposals, of which several can be considered for PV systems application. In this work a selection of single-phase topologies commonly associated with PV inverters and commonly employed by the industry was considered for the proposed investigation. In this section, we present the

considered topologies and discuss their structure, operation principles and PWM strategies commonly employed for each one. Most topologies derive from the classical Ful-bridge Topology or the Three-level NPC (Neutral Point Clamped).

2.3.1 Structures derived from H-bridge topology

In this topic, 3 different types of topologies derived from the H-Bridge will be shown. Additionally, each PWM modulation strategy used will be explained, and how such modulation schemes influence the switching states. The topologies used in this section are the Full-bridge, H5, and HERIC.

2.3.1.1 Full-bridge inverter

The most common inverter topology is depicted in Figure 10 named a Full-bridge inverter. It is composed of 4 switches and 2 switching legs.

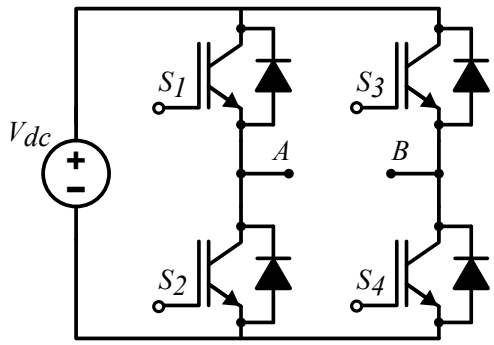

Figure 10 – Full Bridge Inverter
Font: The author

The full-bridge inverter may work with three sorts of PWM strategies such as bipolar, unipolar, and hybrid PWM.

- Bipolar PWM - This type of PWM strategy consists of switching (S1, S4) and in opposite (S2, S3) at high frequency, following a conventional two-level Sinusoidal PWM (SPWM) pattern. The outcome is a two-level output voltage, which imposes a higher harmonic content at the output filter, but does not produces common-mode voltages at the DC side;
- Unipolar PWM - In this case, each switching leg is commuted following a SPWM pattern, but the reference signal of both PWM modulators are mirrored by 180° from each other. As a result, each leg produces a two-level voltage, but the combined output voltage has a three-level waveform, which reduces harmonic content, but introduces common-mode voltages at the DC side;

- Hybrid PWM - In this strategy, one leg is switched at grid frequency and the other one is switched at high frequency. The main problem of this PWM scheme is dealing with the zero voltage state when the reference signal crosses the zero voltage.

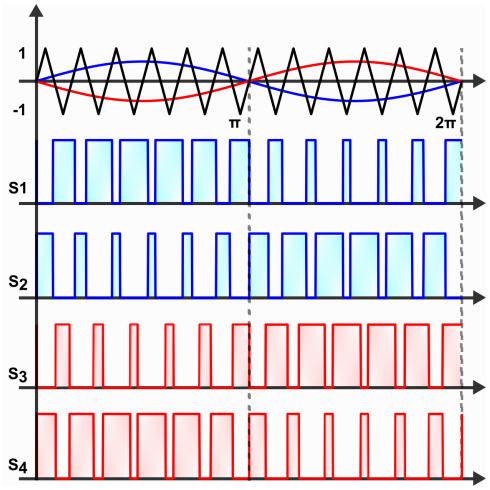

Figure 11 – Unipolar PWM Strategy for the Full Bridge Topology
Font: The author

The most common PWM strategy implemented on this inverter topology, for PV application, is the unipolar modulation. Figure 11 depicts the unipolar modulation strategy. As aforementioned, the switching legs commutation are controlled by 180° mirrored reference signals, which generate a switching pattern as shown in the figure. Based on this strategy, the operation modes of the inverter can be divided into four:

- Mode 1 - The pair of switches (S1 and S3) during either the positive half cycle or the negative half cycle will conduct in a short space of time to deal with the zero state voltage. Figure 12(a)(b) is shown the operation of the switches (S1 and S3) in a zero state voltage during the positive half cycle and the negative half cycle, respectively.
- Mode 2 - During the positive half cycle the current passes via (S1 and S4) from the DC link to the grid as depicted in Figure 12(c).
- Mode 3 - As well as Mode 1, the pair of switches (S2 and S4) will conduct in a very short time during either the positive half cycle or the negative half cycle to mitigate the zero state voltage. Figure 12(e)(f) shows, respectively, the operation of these switches in the positive and negative half cycle.
- Mode 4 - In the same manner as Mode 2, Figure 12(d) shows the operations during the negative half cycle of switches (S2 and S3) which the current passes through the DC link to the grid.

The zero voltage states in the inverter operation are responsible for the production of a common-mode voltage between the DC and AC side. Since this voltages can lead to

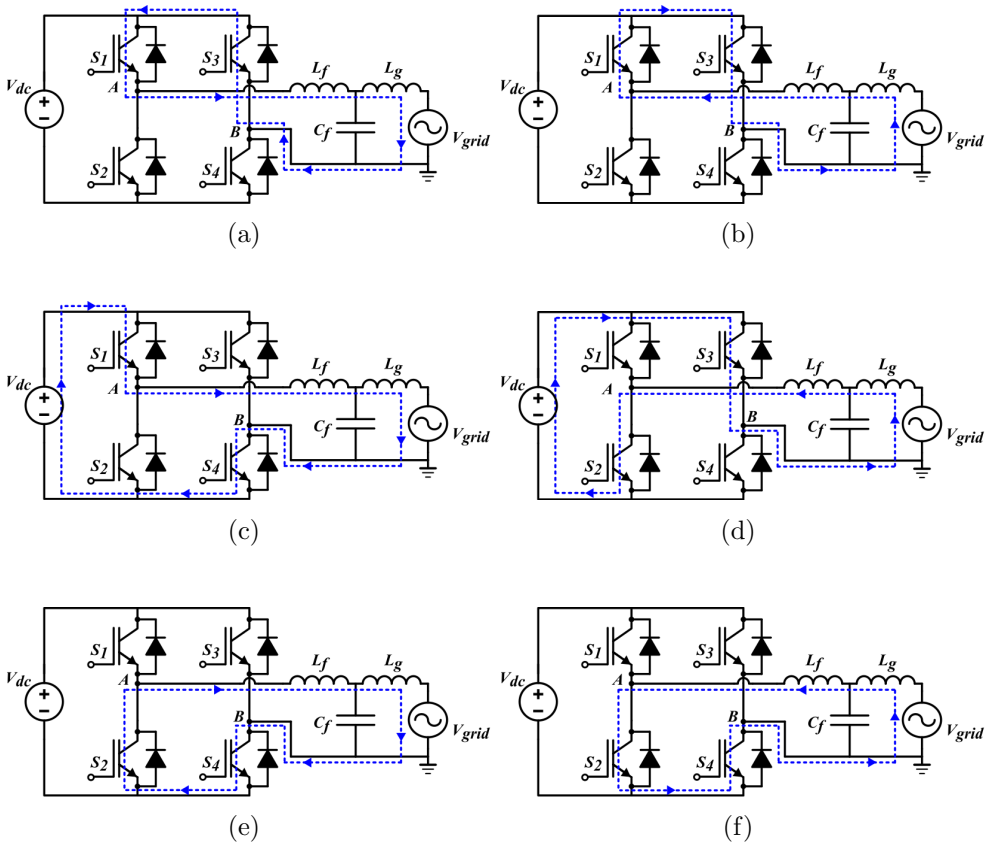

Figure 12 – Full Bridge inverter modes of operation
Font: The author

leakage currents in the PV panels, strategies must be considered to mitigate them. For the Full-bridge topology, a possible solution can be the utilization of floating common-mode filters (DONG et al., 2012). The common-mode filters were not included in the design procedure of the investigated topologies, but their possible employment will be regarded in the discussion of the results.

2.3.1.2 H5 inverter (SMA)

The H5 inverter is a structure derived from conventional H-bridge topology with one additional switch on the DC side of the inverter, which was proposed and patented by SMA Solar Technology in 2005(VICTOR et al., 2005). Figure 13 is depicted the H5 Inverter which is composed of 5 switches. Moreover, the fifth switch disconnects the PV array from the grid in a zero state, which cuts off the path for leakage current(ALBALAWI; ZAID, 2018).

The most common PWM strategy used with this topology is the hybrid PWM, which switching pattern is depicted in Figure 14. The PWM operation can be summarized as follows:

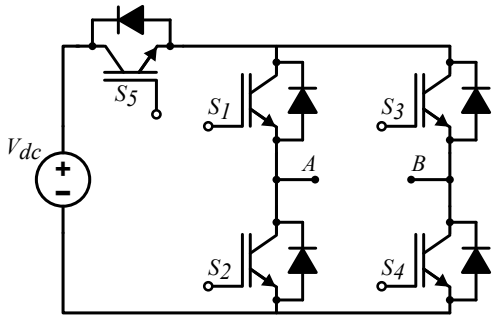

Figure 13 – H5 Inverter (SMA)
Font: The author

- The switches (S1 and S3) operate in opposition to each other at the grid frequency. (S1) is on during the positive half cycle, and it is off during the negative half cycle. On the other hand, (S2) is off during the positive half cycle and it is on during the negative half cycle.
- The switches (S2 and S4) are switched at high frequency. (S4) is operating during the positive half cycle, while (S2) is turned off. On the opposite side, (S2) is operating during the negative half cycle, while (S4) is turned off.
- The switch (S5) is switched at high frequency with either (S4) in the positive half cycle or (S2) in the negative half cycle.

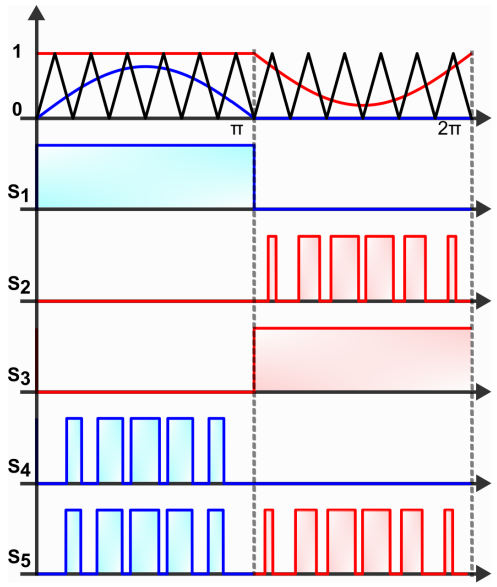

Figure 14 – PWM Strategy for the H5 Bridge Topology
Font: The author

The operation of the H5 inverter may be explained into four modes:

- Mode 1 - During the positive half cycle the current passes through S5, S1, and S4 from the DC link to the grid as depicted in Figure 15(a).

- Mode 2 - Is named zero state mode since there is no energy transfer from the DC link to the grid. The grid current freewheels via S1 and D3 (Diode of S3) as shown in Figure 15(b).
- Mode 3 - During the negative half cycle the current passes through S5, S3, and S2 as depicted in Figure 15(b).
- Mode 4 - As demonstrated in mode 2 when the modulated signal crosses zero states. Then S3 and D1 freewheel the grid current as shown in Figure 15(d).

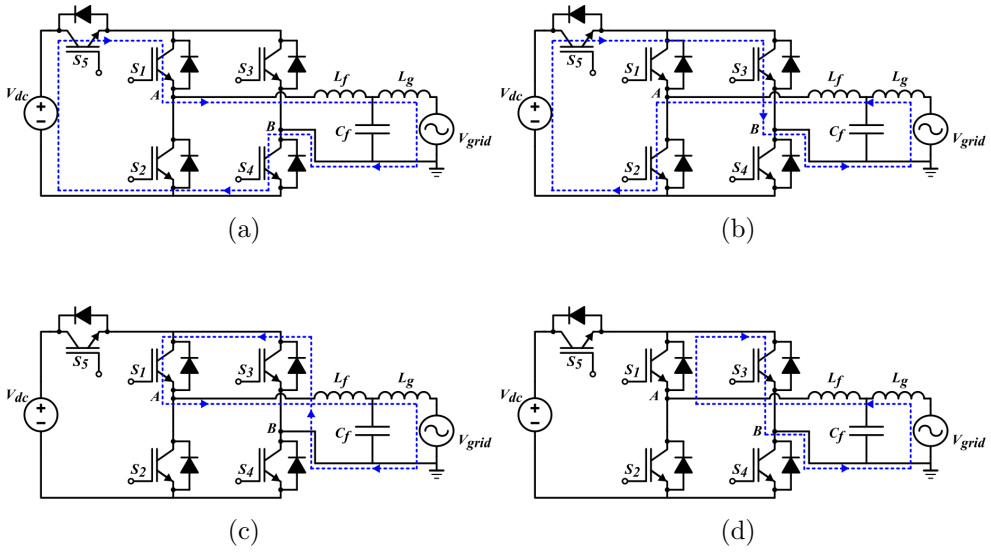

Figure 15 – H5 inverter modes of operation
Font: The author

In (TEODORESCU; LISERRE; RODRIGUEZ, 2011) is explained that the advantage of using H5 topology is due to the 3-level voltage across the filter leading to lower core losses. Moreover, according to the authors, by implementing the hybrid PWM strategy this inverter may have high efficiency of up to 98% due to no reactive power exchange between the interface filter and DC link. Even though there is one more extra switch, another factor that helps this topology to have high efficiency is one of the legs switching at grid frequency.

2.3.1.3 HERIC inverter (Sunways)

The Highly Efficient and Reliable Inverter Concept, known as HERIC, was developed by Sunways Inc. in 2006(SCHMIDT; SIEDLE; KETTERER, 2004). This topology is also derived from the conventional H-bridge in which a bypass leg with 2 extra switches has been added to the AC side, in order to decouple the PV panel from the grid during the zero voltage states(TEODORESCU; LISERRE; RODRIGUEZ, 2011). Figure

16 shows the HERIC topology which is composed of 6 switches: (S1 and S4) as well as (S2 and S3) are switched at high frequency. And (S5 and S6) are switched at grid frequency.

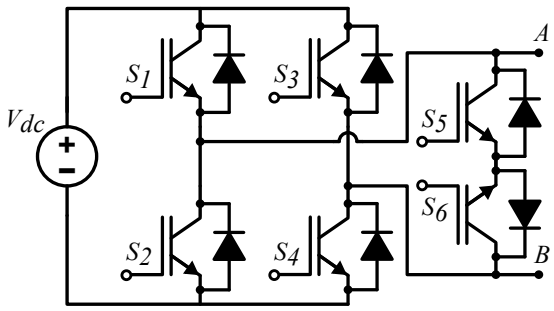

Figure 16 – HERIC inverter (Sunways)
Font: The author

The PWM strategy used in this topology is depicted in Figure 17. The hybrid PWM will work as follows:

- The switches (S1 and S4) operate at high frequency during the positive half cycle.
- As complementary, the switches (S2 and S3) operate at high frequency during the negative half cycle.
- The switch S5 operates at grid frequency and it is turned on during the positive half cycle. On the opposite side, switch S6 also operates at grid frequency but it is only turned on during the negative half cycle.

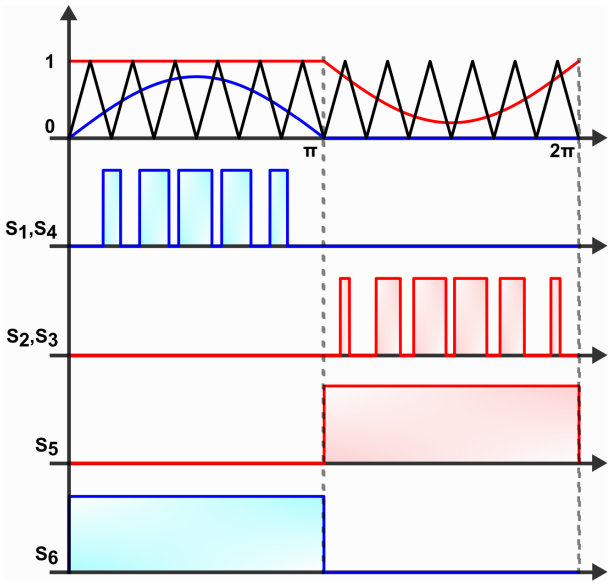

Figure 17 – PWM Strategy for the HERIC Bridge Topology
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The operation of the HERIC inverter may be divided into four modes:

- Mode 1 - During the positive half cycle the current flux passes via (S1 and S4) from the DC link to the grid as depicted in Figure 18(a).
- Mode 2 - During the zero voltage state the grid current freewheels through S6 and D5 (Diode of S5) as shown in Figure 18(c).
- Mode 3 - throughout the negative half cycle the current passes through (S2 and S3) from the DC link to the grid as shown in Figure 18(b).
- Mode 4 - The grid current freewheels through S5 and D6 (Diode of S6) during the zero voltage state as depicted in Figure 18(d).

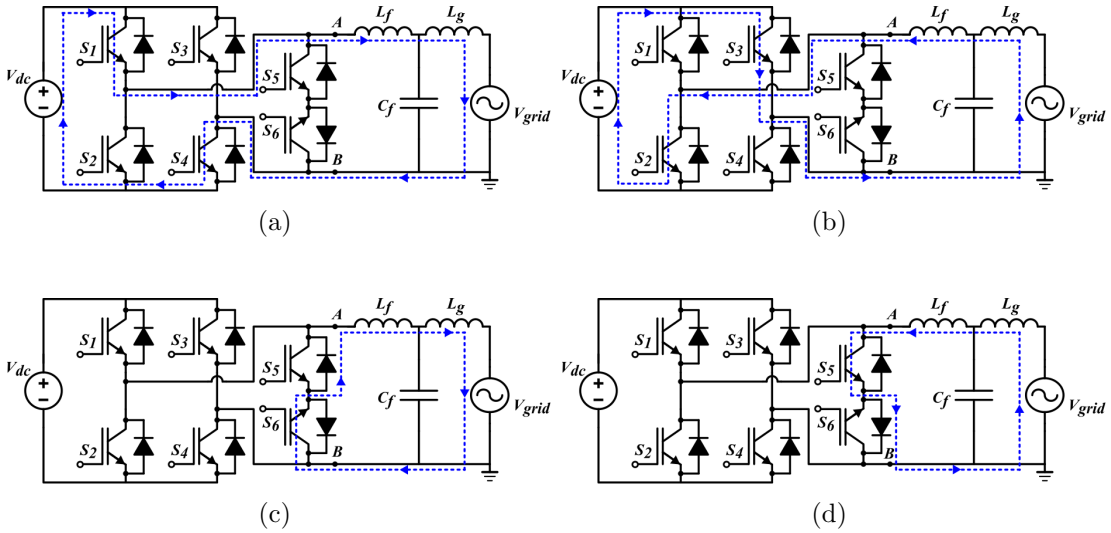

Figure 18 – HERIC inverter modes of operation
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It has been claimed in (TEODORESCU; LISERRE; RODRIGUEZ, 2011) that the behavior of HERIC and H5 are similar due to the functionality of decoupling the PV panel from the grid during the zero voltage state. The main difference between HERIC and H5 is that HERIC needs only 2 switches to conduct the current while H5 needs 3 switches, hence higher conduction losses are expected.

2.3.2 Structures derived from NPC topology

In this section, 2 topologies derived from the NPC will be discussed. In addition, it will be explained how the PWM strategy in each topology influences the switching states. Therefore, the topologies under study in this section are the NPC half-bridge and the Conergy NPC.

2.3.2.1 Neutral Point Clamped (NPC) half-bridge inverter

The conventional NPC, depicted in Fig. 19, was firstly introduced in a patent by Baker (BAKER, 1979) and then described in (NABAE; TAKAHASHI; AKAGI, 1981). It is a three-level half bridge topology that consists of 4 switches and 2 diodes, that clamps the switch voltages to the neutral point of the DC link, thus reducing the voltage stress on these switches and also, due to the three-level output voltage waveform, reduces the voltage stress on the grid inductance, allowing for filter size reduction. Moreover, during zero voltage states, the grid current freewheels via (S2,D+) or (S3,D-), hence no common-mode voltage is imposed on the DC link (MA et al., 2015).

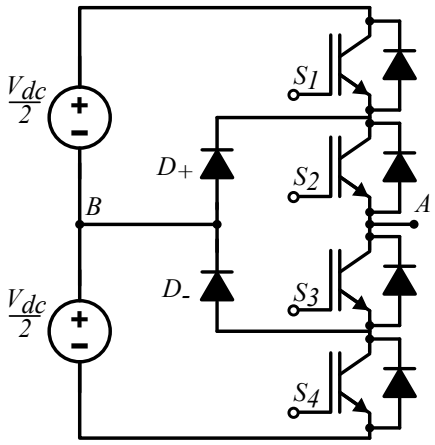

Figure 19 – NPC Half-Bridge Inverter
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The modulation strategy used in NPC inverters usually employs multicarrier PWM such as PD (Phase Disposition), POD (Phase Disposition Opposition) or APOD (Alternative Phase Disposition Opposition)(AGRAWAL; TANDEKAR; JAIN, 2016). For the studies conducted in this work, a PD strategy has been selected. The PWM pattern used to drive this topology is presented in Fig. 20, and described as:

- The switch (S1) operates at high frequency whereas (S2) operates at grid frequency during the positive half cycle.
- On the other hand, during the negative half cycle, switch (S4) operates at high frequency and switch (S3) operates at grid frequency.

The operation of the half bridge NPC inverter may be divided into four modes:

- Mode 1 - During the positive half cycle the current flux passes via (S1 and S2) from the DC Link to the grid as depicted in Figure 21(a).
- Mode 2 - During the zero voltage state the grid current freewheels through S2 and D+ as shown in Figure 21(b).

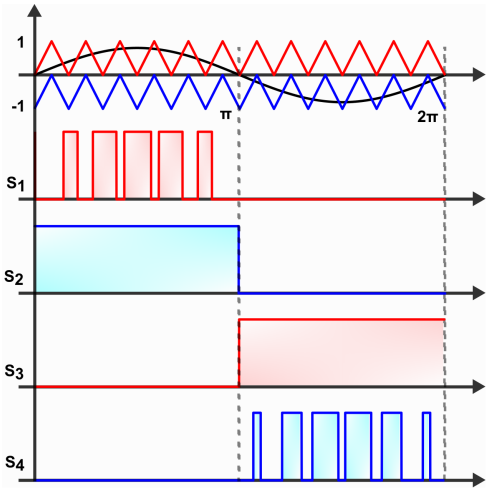

Figure 20 – PWM Strategy for the NPC Half Bridge Topology
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- Mode 3 - throughout the negative half cycle the current passes through (S4 and S3) from the DC Link to the grid as shown in Figure 21(c).
- Mode 4 - The grid current freewheels through S3 and D- during the zero voltage state as depicted in Figure 21(d).

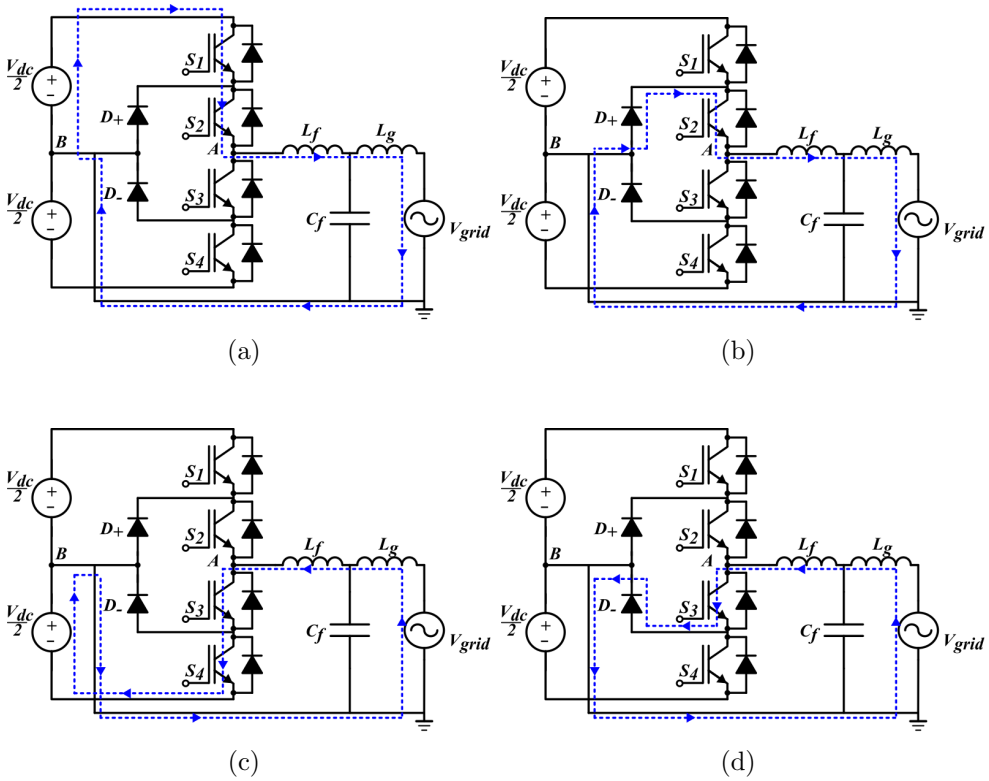

Figure 21 – NPC half-bridge inverter modes of operation
Font: The author

2.3.2.2 Conergy NPC inverter

The T-Type Neutral Point Clamp (NPC), commonly known as Conergy NPC and depicted in Fig. 22, is derived from the conventional NPC, which employs only four switches, instead of six power devices. It was patented by Conergy in 2007 (P. Knaup, 2009), and the reduced number of switches enables lower conduction losses. However, the voltage stresses of the outter switching leg (S1,S2) is equal to the DC link voltage, whereas in inner leg (S+,S-) are clamped to half the DC link voltage. In comparison to a conventional NPC, where all switches are exposed to half the DC link voltage, an increase in switching losses can be expected.

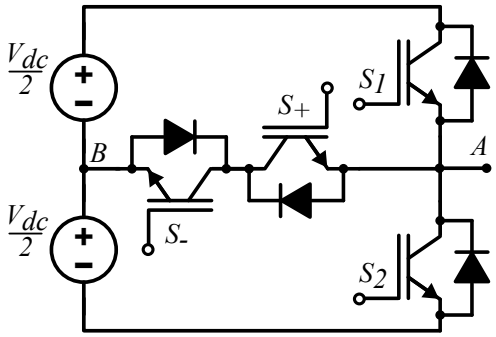

Figure 22 – Conergy NPC T-Type Inverter
Font: The author

NPC topologies can perform a variety of multilevel PWM strategies (FENG; AGELIDIS, 2002). In this paper, a phase-disposition (PD) PWM was considered to drive both NPC converters. Regarding the T-Type NPC the PWM patterns are depicted in Fig. 23, and described as:

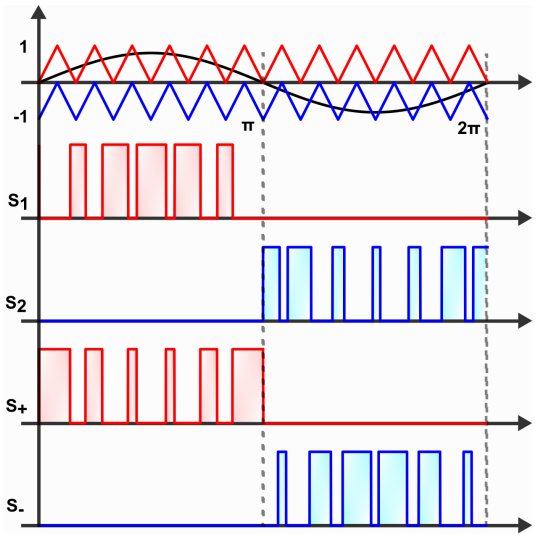

Figure 23 – PWM Strategy for the NPC T-Type Topology
Font: The author

- The switch (S1) operates at high frequency and switch (S+) operates as complementary during the positive half cycle.

- On the other hand, during the negative half cycle, switch (S2) operates at high frequency and switch (S-) operates as complementary.

The operation of the NPC T-Type inverter may be divided into four modes:

- Mode 1 - During the positive half cycle the current flux passes via (S1) from the DC link to the grid as depicted in Figure 24(a).
- Mode 2 - During the zero voltage state the grid current freewheels through D- and S+ as shown in Figure 24(b).
- Mode 3 - throughout the negative half cycle the current passes through (S2) from the DC link to the grid as shown in Figure 24(c).
- Mode 4 - The grid current freewheels through D+ and S- during the zero voltage state as depicted in Figure 24(d).

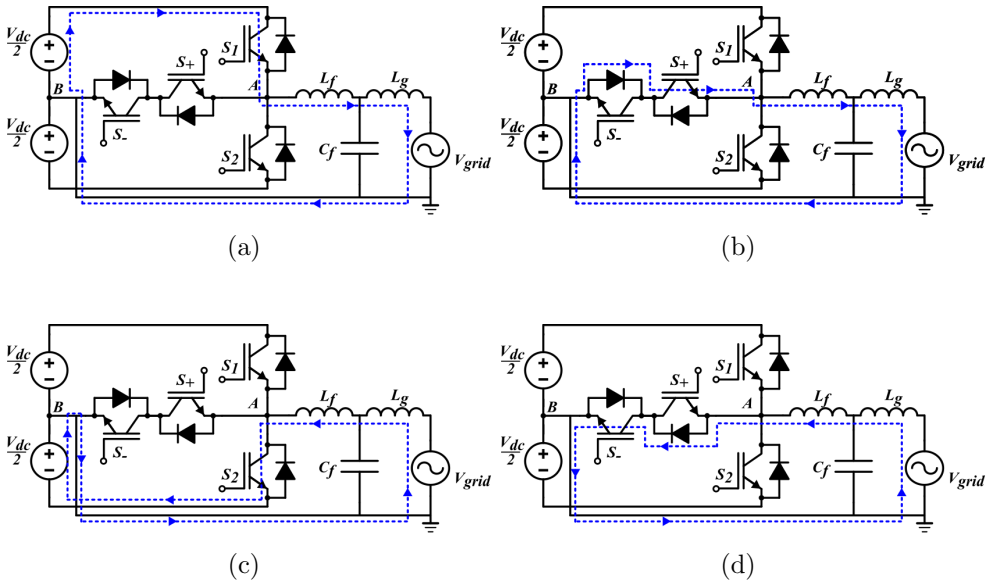

Figure 24 – NPC T-Type inverter modes of operation
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2.4 Grid interface filter

The connection between the utility grid and the inverter is established through an interface filter, Figure 25, whose main function is to filter high-frequency harmonic components generated by the switching pattern.

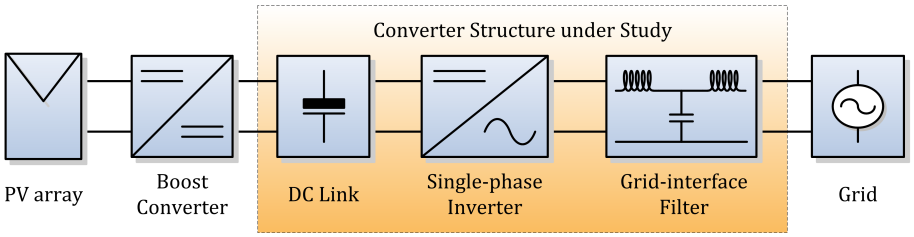

Figure 25 – Single-phase PV inverter general structure
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To reduce the harmonics injected by the converters several filter topologies may be used such as inductive (L), inductive-capacitive (LC), and inductive-capacitive-inductive (LCL).

The following subsections demonstrate the modeling for these filters. However, In this work, an LCL filter will be employed, as depicted in Figure 30. Due to its ability to achieve high attenuation of harmonics at the switching frequency, the LCL filter is capable of minimizing the distortion of the electrical current injected into the grid (REZNIK et al., 2014).

2.4.1 L filter

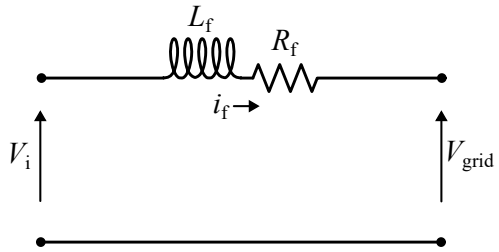

Figure 26 – L Filter
Font: The author

The inductive filter (L), as depicted in Figure 26, is a first-order filter with an attenuation of 20dB per decade across the entire operating range. It is a simple filter consisting of just an inductor connected between the inverter output and the electrical grid. Another important factor is that this filter is not suitable for low-frequency applications, since when L filters have relatively large volume and inductance, it affects the plant dynamics and increases the system response time. On the other hand, if the inductance is too small, it may not be sufficient to reduce the harmonics generated by the semiconductors during switching (YAGNIK; SOLANKI, 2017; LETTL; BAUER; LINHART, 2011).

The modeling of the L filter is simple. For better visualization, Figure 27 depicts the block diagram of the filter, where it can be observed that the grid voltage is a disturbance. Thus, the transfer function is given by expression 2.3, noting that it is a first-order system.

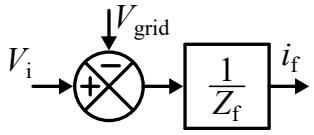

Figure 27 – L Filter block diagram
Font: The author

$$\frac{I_f(s)}{V_i(s)} = \frac{1}{Z_f} \tag{2.3}$$

Where $Z_f = sL_f + R_f$, and represents the impedance on the inverter side.

For applications requiring converters of many kilowatts, it becomes expensive to work with an L filter due to the high value of the inductance required to attenuate the harmonics produced by the inverter. Additionally, the system's dynamic response becomes poor.

2.4.2 LC filter

The inductive-capacitive filter (LC), as shown in Figure 28, is a second-order filter composed of an inductor and capacitor parallel to the electrical grid. This type of filter is more advantageous than the L filter as it provides attenuation at 40dB per decade. However, LC filters have a resonance frequency that must be carefully designed; otherwise, the circuit impedance will be minimal, allowing a greater amount of current to pass through the LC filter (KIM; CHOI; HONG, 2000).

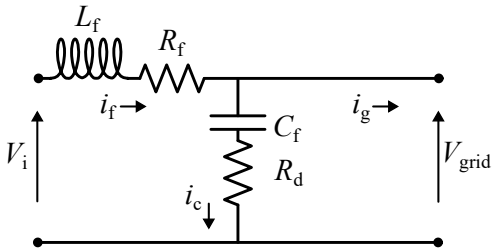

Figure 28 – LC Filter
Font: The author

The modeling of the LC filter is simple when viewed through the block diagram in Figure 29. It can be observed that the grid current serves as a disturbance to the system. Thus, the transfer function can be derived from expression 2.4.

$$\frac{V_g(s)}{V_i(s)} = \frac{Z_c}{Z_f + Z_c} \tag{2.4}$$

Where $Z_f = sL_f + R_f$, and represents the impedance on the inverter side. And, $Z_c = 1/sC_f + R_d$ is the impedance of the capacitive filter.

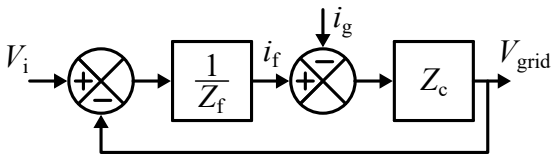

Figure 29 – LCL Filter block diagram
Font: The author

One of the drawbacks of the LC filter, in addition to the resonance frequency, is the direct connection of the capacitor to the electrical grid, which can cause significant connection transients. These transients may destabilize the current control when connected to the grid.

2.4.3 LCL filter

The inductive-capacitive-inductive (LCL), as depicted in Figure 30, is a third-order filter capable of attenuating 60dB per decade. This filter is more desirable for grid-connected converters due to its lower cost and smaller size in applications above several kilowatts. In addition, the second impedance helps to decrease transients when the converter connects to the grid.

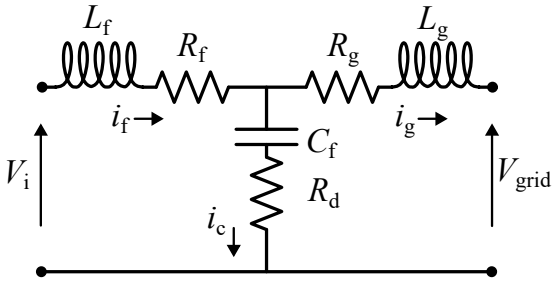

Figure 30 – LCL Filter
Font: The author

The simplest way to model the LCL filter is by using a block diagram rather than circuit equations. Figure 31 illustrates the representation derived from the LCL filter circuit. It is evident that the grid voltage serves as a disturbance to the system. However, similar to the LC filter, the LCL filter possesses a resonance frequency that must be carefully designed to avoid interference with the current control loop.

Making the transfer function more sophisticated, the impedances are denoted as $Z_f = sL_f + R_f$, $Z_f = sL_g + R_g$, and $Z_c = 1/sC_f + R_d$.

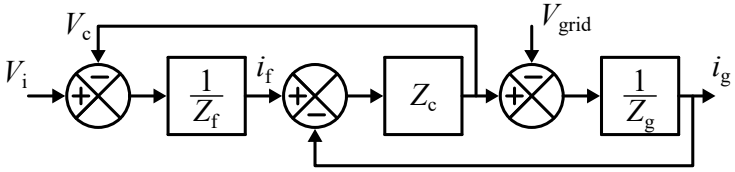

Figure 31 – LCL Filter block diagram
Font: The author

$$\frac{I_f(s)}{V_i(s)} = \frac{Z_g + Z_c}{Z_g Z_c + Z_f Z_c + Z_g Z_f} \tag{2.5}$$

$$\frac{I_g(s)}{V_i(s)} = \frac{Z_c}{Z_g Z_c + Z_f Z_c + Z_g Z_f} \tag{2.6}$$

$$\frac{I_g(s)}{I_f(s)} = \frac{Z_c}{Z_g + Z_c} \tag{2.7}$$

2.4.4 Overall discussion

Given the comprehensive study presented on the filters, Figure 32 illustrates the frequency response diagram, providing a visual representation of the behavior of each filter. The L filter maintains a constant attenuation of -20dB/dec throughout its entire frequency range. In the case of the LC filter, there is a notable region where resonance occurs, resulting in elevated gain. Subsequently, the filter attenuates at a rate of -40dB/dec. Finally, the LCL filter begins with an attenuation of -20dB/dec, and after the resonance frequency, it transitions to attenuating at -60dB/dec.

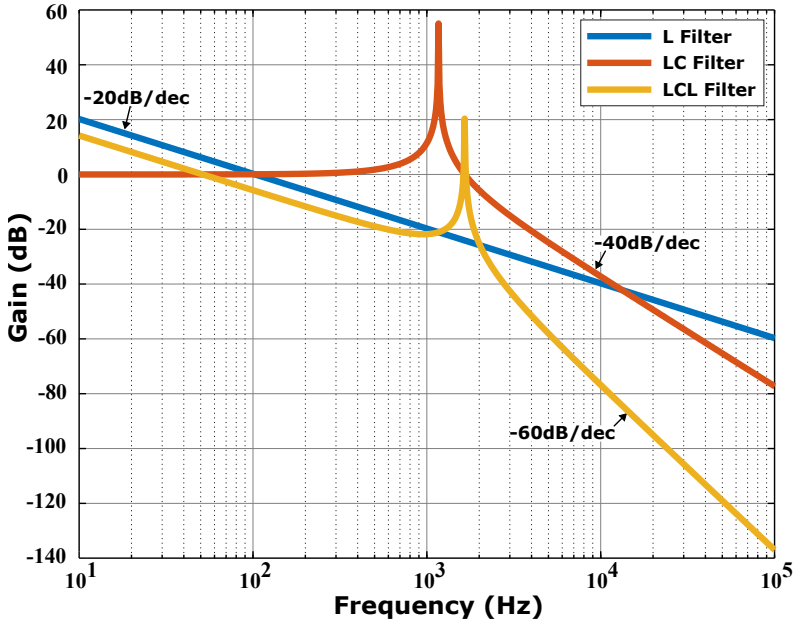

Figure 32 – Frequency response of interface filter
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There are various methods to mitigate the influence of the filter's resonance frequency on control, one of which involves the use of both passive and active components, known as damping techniques. The most cost-effective and straightforward approach is to employ a resistor in series with the capacitor, termed passive damping. However, this technique negatively impacts the filter's attenuation and increases losses. On the other hand, as explained in (GOMES; CUPERTINO; PEREIRA, 2018), there are alternative methods for damping through control, using gains or transfer functions, referred to as active damping. Consequently, the adverse effects of the resonance frequency become less detrimental to the inverter control.

To illustrate the impact of employing passive damping, Figure 33 displays the frequency response of the LCL filter concerning variations in the damping resistor in series with the filter capacitor. It is noteworthy that as the resistance increases, the gain at the resonance frequency decreases. However, the filter's attenuation becomes less effective. For instance, when $R_d = 3\Omega$, the gain at the resonance frequency approaches zero, but the filter's attenuation is approximately -40dB/dec. Consequently, one must consider the trade-off between filter attenuation and resonance frequency when selecting the damping resistor. Additionally, it's crucial to recognize that higher resistance leads to increased joule losses.

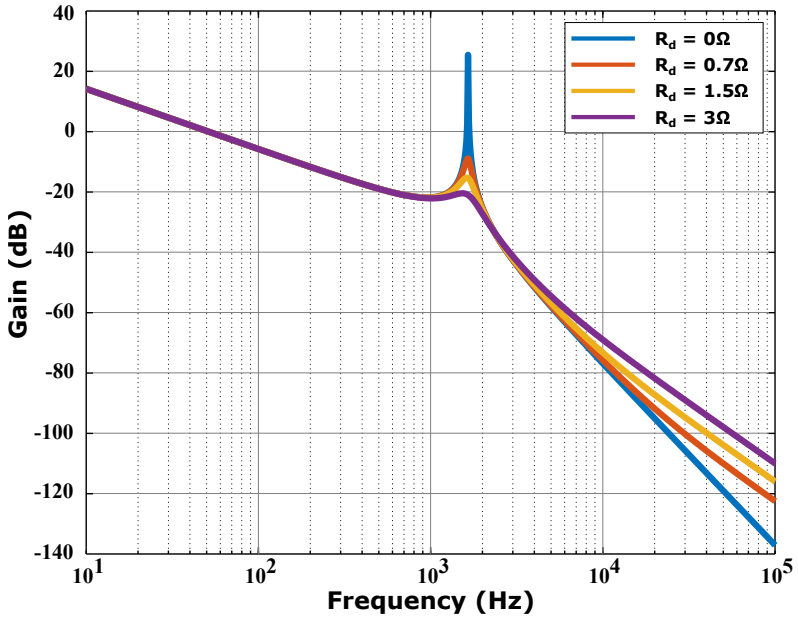

Figure 33 – LCL Filter frequency response diagram varying the R_d resistance
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2.5 Multi-objective studies

Power converter design focuses on selecting a converter topology and specifying its elements to meet user-defined criteria regarding power, voltage and temperature ratings, compliance to application standards, dynamic response, etc. Moreover, performance indexes such as efficiency, cost, reliability, are often used as design constraints that guide designers' choices, e.g. switching frequency, voltage and current ripples, filter cut-off frequencies, etc; and also determines whether a particular solution would be feasible. These performance indexes, however, are not independent, i.e., improving one index may worsen one or several others, that added to the high number of degrees of freedom present in converter design hampers the ability of the designer to identify the optimal solutions for a given specification.

A multi-objective design approach, based on multi-physics detailed mathematical modeling of the converter components and their interaction, can use computational aid to perform multiple designs for a range of input specifications and assess the performance indexes of each solution. In this approach, analytical modeling or brute force simulation can both be used to extract accurate information regarding a converter behavior and current/voltage waveform and, by means of component's datasheet/experimental data, to compute power losses, volume, cost, weight, etc, for each, thus enabling the definition of a point in the performance space, whose axes are the desired performance indexes. Therefore, with the employment of a Pareto-front optimization algorithm, the cloud of possible solutions can be processed and the set of optimal solutions for a given converter is identified (BURKART, 2016; KOLAR et al., 2010).

In this work, a brute force algorithm is devised that, based on simulation data as well as a database of semiconductors, capacitors, magnetic cores and heatsinks, can perform a feasible design of a converter and compute its performance indexes, chosen to be Efficiency and Power Density (kW/dm^3). This algorithm will then be used to evaluate the performance of each converter topology for a case study.

In this section, the structure of the proposed algorithm will be disclosed.

2.5.1 Multi-objective algorithm architecture

The basic architecture for the multi-objective converter design algorithm is illustrated by the Flowchart in Fig. 34. It can be noticed that the routine relies on simulated data in order to perform the specific design of each converter element. Therefore, a unique routine must be assembled for each converter topology. Moreover, a database with electronic devices' information must be available for the definition of material lists for each design and the computation of losses, volume and cost parameters. The database was built

in SQLite and it stores datasheet and cost information for real IGBT, diodes, electrolytic and MKP capacitors, extruded heatsinks and powder cores.

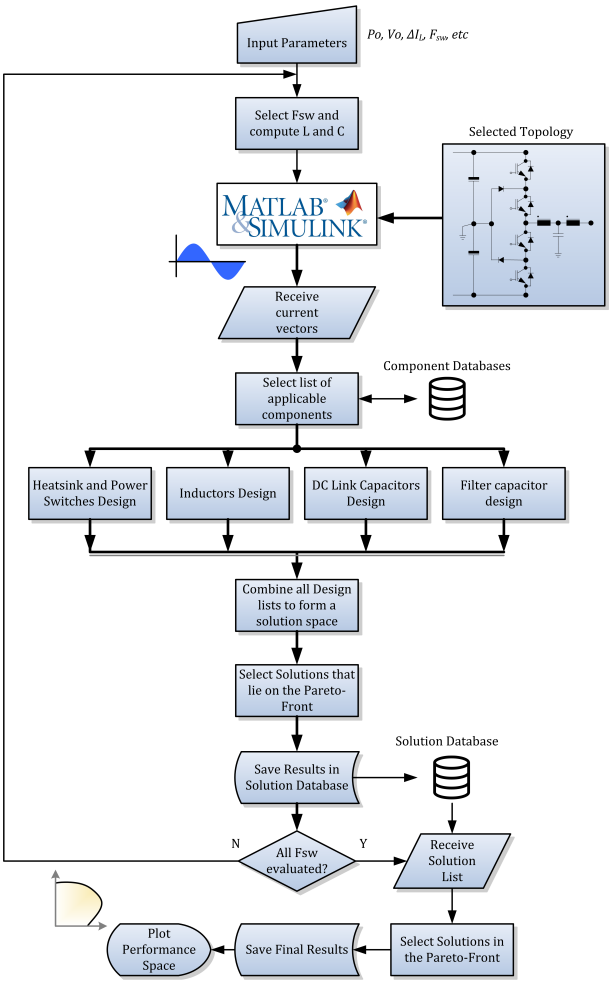

Figure 34 – Routines Flow Chart
Font: The author

The design algorithm operates as follows: Firstly, the user defines a set of input parameters, such as, converter topology, output power and voltage ratings, DC Link voltage, output inductor current ripple, and a list of switching frequencies to be evaluated by the software. Afterwards, this information is used to compute the value for each capacitance and inductance in the selected topology. A LCL grid-interface filter was considered for all circuits, the design of its reactive elements is addressed in several papers in the technical literature (PEÑA-ALZOLA et al., 2014; LISERRE; BLAABJERG; HANSEN, 2005; REZNIK et al., 2014; GOMES; CUPERTINO; PEREIRA, 2018). In this paper, the procedure described in (GOMES; CUPERTINO; PEREIRA, 2018) was adopted for the designing of LCL filter elements. Moreover, the DC link capacitance was computed to provide a DC link voltage ripple lower than 5%. Once the reactive elements are defined, a MATLAB/Simulink simulation is performed what provides the current vectors for all elements, e.g., semiconductors, capacitors, inductors, etc; which are later processed in the design routines. In these routines, a database is used to select a set of components that

can be used in the implementation of each element, then their datasheet information is employed to design the physical component and estimate its power losses, volume and cost. Therefore, the output of the design routines is a list of possible components' designs. Once all individual lists are defined, for a particular switching frequency, the algorithm combines them all in a set of converter design solutions. It uses Pareto-front optimization to store only the Pareto optimal solutions for each frequency. At the end, the solutions for all frequencies are combined and a new analysis is performed to extract the Pareto-front of all designs.

2.5.2 Inductor design

Before the algorithm designs the inductor, it is essential to calculate both the required inductance of the Lf and Lg in the LCL filter. Therefore, before gathering the Simulink environment to simulate the complete inverter with the desired topology, it is crucial to calculate the inductances and capacitances, among other components. These elements play a fundamental role in determining the control of the inverter.

Among the various methods for calculating the LCL filter, this work is based on the current ripple in the inductor. In (REZNIK et al., 2014), an algorithm is presented for calculating the inductance, capacitance, and damping resistor of the LCL filter in a straightforward manner based on the attenuation of the current ripple.

The figure 35 illustrates the algorithm for calculating the LCL filter based on (REZNIK et al., 2014). The input variables include the nominal inverter power (S_n), grid frequency (f_g), switching frequency (f_{sw}), DC bus voltage (V_{dc}), and grid voltage (V_g). Subsequently, the base values for impedance and capacitance of the filter are computed as shown in expressions (2.8) and (2.9), respectively.

$$Z_b = \frac{V_g^2}{S_n} \tag{2.8}$$

$$C_f = 0.05\frac{1}{\omega_g Z_b} \tag{2.9}$$

Note that the value 0.05 in the equation (2.9) refers to 5% of the rating power which is a consideration of the maximum power factor variation seen by the grid (REZNIK et al., 2014). Certainly, it is up to the designer to determine whether a design factor greater than 5% is appropriate. This decision depends on the need to compensate for the inductive reactance of the filter.

After determining the values of C_f and Z_b, the algorithm calculates the value of inductance L_f, i.e., the inductor positioned at the output of the inverter. According to (REZNIK et al., 2014), the value of L_f is given by expression (2.10). The authors

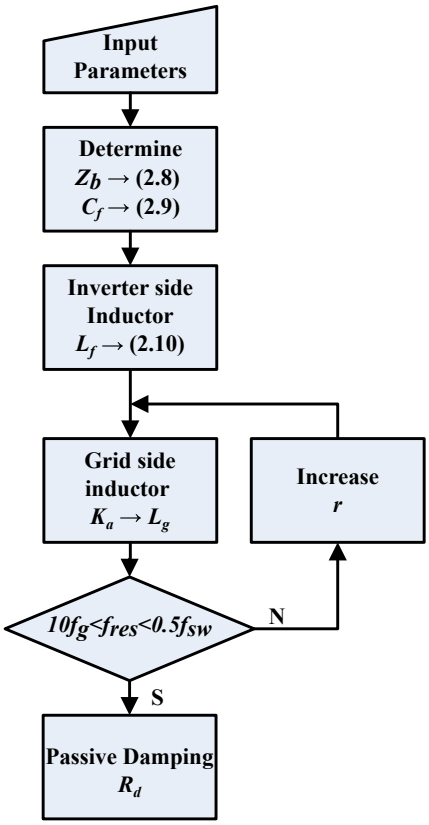

Figure 35 – LCL filter design flow chart
Font: The author

considered the inverter modulation factor, indicated by m, as 0.5 for a typical SPWM scheme.

$$L_f = \frac{2V_{dc}}{3f_{sw}\Delta I_{Lmax}}(1-m)m \tag{2.10}$$

The crucial factor is that in the literature, the ripple value is calculated based on the maximum current value of the inverter. In this work and the authors' suggestions, a value of 0.1, or 10%, was considered, as shown in expression (2.11).

$$\Delta I_{Lmax} = 0.1\frac{S_n\sqrt{2}}{V_g} \tag{2.11}$$

After defining the value of L_f, the algorithm enters a loop to determine the value of r, a proportionality constant between the inductances on the grid side and the inverter side, as shown in expression (2.12) and it must be greater than zero. According to the literature, K_a is a function that relates the harmonic current generated by the inverter to the current injected into the grid. Thus, as shown in equation (2.13), K_a depends on r, which directly influences the value of the inductance on the grid side. However, it is worth noting that this process is only used to attenuate the inductance on the grid side.

Therefore, it is up to the designer to decide whether it is interesting to attenuate the grid inductor; otherwise, setting r equal to 1 means that L_g and L_f will be equal.

$$L_g = rL_f \tag{2.12}$$

$$K_a = \frac{1}{|1 + r(1 - L_f C_f \omega_{sw}^2)|} \tag{2.13}$$

An important point is the resonance frequency of the filter, as already mentioned in Section 2.4, which, if not properly designed, can cause disturbances in the inverter control system. The resonance frequency is defined, as shown in equation (2.14), depending exclusively on the inductors L_f and L_g and the capacitance of the filter (C_f). It is necessary to ensure that the resonance frequency is lower than half of the switching frequency and higher than 10 times the frequency of the electrical grid, as shown in expression (2.15).

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_f + L_g}{L_f L_g C_f}} \tag{2.14}$$

$$10 f_g < f_{res} < 0.5 f_{sw} \tag{2.15}$$

Note that if the condition in (2.15) is not satisfied, the value of r is incremented until finding an L_g that is within the resonance frequency range. However, it is possible to define K_a in order to ensure a desired attenuation, where a specific r will be found, as shown in Figure 36, illustrating the variation of K_a in relation to r for each switching frequency used in this study.

Note that if a attenuation value of K_a of 5% is chosen, a value of r of at least 0.1 is required if the switching frequency is 10kHz, and slightly over 0.02 if the switching frequency is 40kHz. Thus, it is observed that as the switching frequency increases, a smaller inductance in relation to L_f is required.

Finally, after determining the inductances and capacitance of the filter, the damping resistance is chosen by equation (2.16) as suggested by (REZNIK et al., 2014), which is of great importance for reducing the effects of resonance frequency on the inverter control, as previously depicted in the form of a frequency response diagram in Figure 33, where resistance values are shown to evaluate the behavior of the LCL filter.

$$R_d = \frac{1}{3\omega_{res} C_f} \tag{2.16}$$

The inductor design routine considers toroidal iron powder cores and follows the desig procedure adopted in (VILKN, 2018). The datasheet already provides the

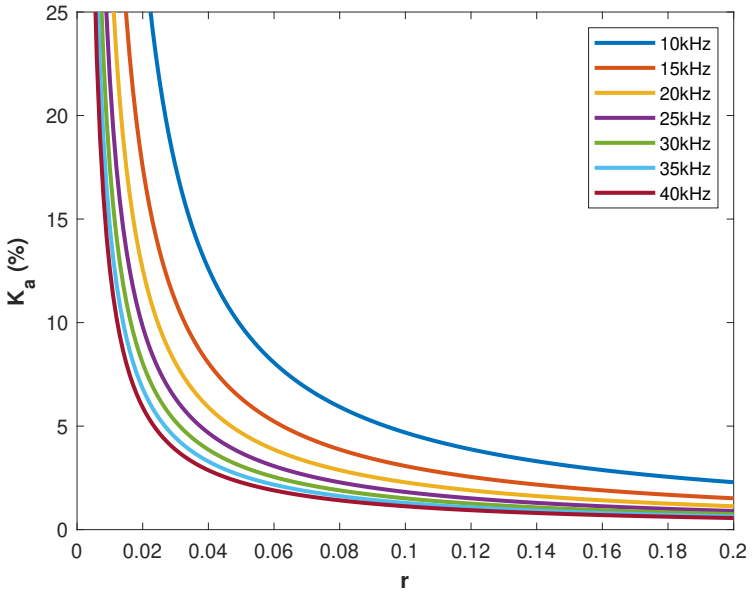

Figure 36 – Variation of K_a in relation to r
Font: The author

specific inductance ($A_L[nH/turn^2]$) for each core, hence the required number of turns was computed as:

$$N = \sqrt{L/A_L} \tag{2.17}$$

Since the core permeability varies with the magnetic field intensity, datasheet information regarding the core magnetization is used to compute the inductance derrating factor (L_{df}), which is defined as:

$$L_{df} = \left(1 - \frac{NB_{max}A_e n_{Stack}}{\hat{I_L}L}\right) \times 100\% \tag{2.18}$$

where, A_e is the core section area, n_{Stack} is the number of stacked cores, $\hat{I_L}$ is the peak inductor current obtained via simulation and B_{max} is the maximum magnetic flux density obtained via datasheet magnetization information for a maximum field intensity $H_{max} = N\hat{I_L}/l_e$, where l_e is the effective length. The designer defines a maximum derrating factor allowed for the inductor design and the algorithm discards every design that does not comply with this constraint.

For the coil design, a current density of 5 A/mm^2 is assumed. A maximum wire gauge is computed as the one with a diameter immediately lower than two skin effect penetration depths. The number of paralled wires is determined to meet the desired current density. The algorithm varies the wire gauge in order to evaluate different coil designs. Once the coil is defined, the utilization factor is calculated as:

$$k_u = (NN_{par}A_{wire})/A_W \tag{2.19}$$

where, A_{wire} is the wire section area, with isolation, N_{par} is the number of paralleled wires and A_W is the core window area. This factor is also used as a constraint to discard solutions that do not fit in the available area. For each suitable inductor design, the core loss is computed by means of traditional Steimetz equations (STEINMETZ, 1892), whereas the copper losses are computed using Dowell curves (DOWELL, 1966). At the end, the core temperature is computed by:

$$T_{core} = T_A + \left[\frac{(P_{core} + P_{copper})[mW]}{A_T[cm^2]}\right]^{0.833} \tag{2.20}$$

where, T_A is th room temperature and A_T is the core surface area, which is also interpolated from the core datasheet. The designer defines the maximum allowed core temperature and those designs that does not meet this constraint are discarded. The total volume of the inductor, extrapolates the datasheet information regarding the dependency of the core diameter and height on the utilization factor.

2.5.3 DC link capacitor design

The DC link capacitor design procedure receives the desired capacitance, the maximum voltage that the capacitor is exposed and the capacitor current vector of which is extracted the peak and rms values. The algorithm will then design a capacitor bank for each component in the database, following these steps:

1. Defines the number of parallel strings (N_P) of capacitors that can conduct the required rms capacitor current;
2. Defines the number of series connected capacitors (N_S) that can withstand the required capacitor voltage;
3. If the bank capacitance is lower than the required capacitance, increase N_P to match it.

Once the capacitor bank is defined, the algorithm computes the power losses by means of:

$$P_{cap} \approx (N_S/N_P)ESR \times I^2_{C,rms} \tag{2.21}$$

where, ESR is the capacitor series resistance. The capacitor bank volume is computed as the sum of the volume of each capacitor.

2.5.4 Switches and heatsink design

The algorithm selects all switches in the database that withstand 1.6x the switch voltage stress in each converter. The developed algorithm assumes the use of the same Part Number for all switches in a converter design, although it is allowed to vary the number of switches in parallel for each solution.

Once the device Part Number is selected for a given situation, the algorithm varies the number of parallel switches from one to four and for each case it computes the switch total power loss (conduction and switching losses for the IGBT and anti-parallel diode). The same procedure is followed for the NPC clamping diodes. The calculation of the power losses uses the switch current vector and datasheet curves, so that:

$$P_{cond,SW} = avg(i_{SW}(t) \times v_{CE}(i_{Sw})), \tag{2.22}$$

$$P_{sw,SW} = \frac{\sum E_{on}(i_{SW,on}) + \sum E_{off}(i_{SW,off})}{T_r}, \tag{2.23}$$

where, i_{SW} is the switch current vector, $v_{CE}(i)$ is the collector-emitter voltage extracted from the datasheet $I_C x V_{CE}$ curve; $i_{SW,on}$ and $i_{SW,off}$ are the switch current values in a turn-on or turn-off transition, respectively; $E_{on}(i)$ and $E_{off}(i)$ are the turn-on and turn-off switching energies, respectively, which are extracted from the datasheet ExI curves; and T_r is the grid voltage period. A similar approach is used for the diode power loss estimation. A more detailed description of the procedure for computing semicondutor power losses based on datasheet information can be found in (COTA, 2016).

Once the power losses are computed, the temperature elevation for the i-th power device is calculated as

$$\Delta T_{SW,i} = R_{\Theta jc,i} \cdot P_{total,i} \tag{2.24}$$

where, $P_{total,i} = P_{cond,i} + P_{sw,i}$. Thus, the required heatsink temperature is computed as $T_{case} = min(T_{jmax} - \Delta T_{SW,i})$, where T_{jmax} is the maximum junction temperature defined by the designer. Afterwards, for each available heatsink, the algorithm varies its length to find a thermal resistance that meets the required heatsink temperature, for a room temperature of 40°C and a pre-defined air velocity. As constraints, the algorithm limits the maximum heatsink length to 60 cm, which is the length in which no marginal decremental thermal resistance is obtained, and the minimum length to what is needed to accommodate all semiconductors with a 1 cm gap between devices.

2.5.5 Performance space definition

Each design routine assembles a list of possible designs for each element, eg, the inductor design routine will output every combination of powder cores and windings that meet the design criteria for a given operation point, in terms of the input data and switching frequency. The same happens for the semiconductor-heatsink pair, as well as for the DC link and filter capacitances. The algorithm then linearly combines all those lists to define a possible design solution, afterwards, the solution space is processed so the losses and volume information of each element are combined to define the solution Efficiency and Power Density. Futhermore, the Pareto-front of the solution space is found and all solutions that not lie in that surface for a given operation point is discarded. The procedure is repeated for all operation points, than all processed solution spaces are combined to form the Performance Space. Afterwards a cost function is used to define the Optimal Solution for the converter. This cost function is defined in equation (2.25), where η relates to the solution's efficiency and ρ, to their Power Density.

$$F = max(\eta \times \rho) \tag{2.25}$$

2.6 Chapter Overview

In this chapter, essential topics for understanding the development of this dissertation work were discussed. Firstly, a two-stage PV inverter to be implemented in the Matlab/Simulink platform will be considered. However, the multi-objective algorithm will only compute the influence of the DC/AC converter even if the Boost converter is present in the PV system simulations. Another point addressed was the presentation of each PWM modulation strategy used in each topology and how such modulation schemes influence the switching state.

In this work, an LCL filter with a passive damping strategy is being considered. Subsequently, it is shown how the influence of a damping resistor affects the frequency response of the filter, reducing the peak of the resonance region but, at the same time, decreasing the filter attenuation.

Finally, the operation of the multi-objective algorithm is presented, where each component of the inverter is designed, and losses and other performance variables are computed. Then, a cost function is defined to select the design that has the maximum product of efficiency and power density.

3 STUDY CASE - SIMULATION RESULTS

This chapter presents the results and analyses derived from simulations conducted in the Matlab/Simulink environment. In this section, two study cases are presented. Study Case I demonstrates the inverter topologies working with 800V DC Link, including all topologies. And after, Study Case II proposes inverters performing with 400V in the DC link only including the H-bridge topologies. In addition, Table 2 summarizes all parameters used in each Study Case.

Table 2 – Table with parameters for H-Bridge and NPC

Parameters	**Values**	
	Case Study I	**Case Study II**
DC link voltage	800V	400V
DC link capacitance	$2mF$	
Rated power	5kW	
Grid voltage	220V / 60Hz	
Inductor ripple current	10% of I_{max}	
Switching frequency range	10kHz - 40kHz	

The reason for different types of DC link voltage is due to the fact that NPC topologies can only synthesize the grid voltage of 220V when operated with a DC link voltage of 800V, due to the split capacitor. This means that in each switching half-cycle, the voltage at the inverter output will be 400V. On the other hand, Study Case II will only have H-Bridge topologies because a DC link voltage of 400V is not sufficient for NPC topologies to function adequately since the peak voltage of the electrical grid is approximately 311V. Another important consideration made in this work was the switching frequency range. The choice of the range from 10kHz to 40kHz is since it is the typical operation range of a Si-IGBT.

Finally, the individual performance of each studied topology will be highlighted, utilizing the Pareto-front approach to identify the best converter designs. This process is conducted with a focus on the efficiency and power density of each converter. It is worth noting that for each inverter topology, a unique script is employed to calculate the symmetries existing between the Si-IGBT switches.

3.1 Methodologies and simulation parameters

The component database, constructed in SQLite, was populated with the elements detailed in Table 3. It is worth noting that, in regard to capacitors and magnetic

cores incorporated into the database, all components from the manufacturer's referenced series/catalog were taken into account.

The design routines also considered the following constraints:

- Maximum junction temperature for IGBTs and Diodes - 90 °C;
- Air velocity of the heatsink fan - 6 m/s;
- Maximum inductor core temperature - 120 °C;
- Maximum inductor core utilization factor - 40%;
- Maximum inductance derating factor - 15%;

Regarding the control system of the inverter, the controller gains were adjusted for each switching frequency in order to ensure output current THD compliance to grid codes. Since the results used in this paper rely on the inverter steady-state behavior, i.e., the dynamics are not relevant to the discussion, the control system will be omitted.

Table 3 – Component list available in the database

Component	**Manufacturer**	**Part Number**	**Rated Voltage/Current**
Diode[1]	Microchip	APT60DQ60BG	600V / 60A
	VISHAY	VS-E5PW6006LHN3	600V / 60A
	Microchip	MSC030SDA070K	700V / 56A
	ST	STPSC20065WY	650V / 20A
Switches[2]	Infineon	IKW50N65ES5	650V / 80A
	IXYS	IXYH50N120C3D1	1200V / 90A
	STMicroelectronics	STGYA50M120DF3	1200V / 100A
	Infineon	IKW15N120BH6	1200V / 30A
	Infineon	IKY50N120CH7	1200V / 75A
	Magnachip	MBQ40T120FES	1200V / 80A
	OnSemi	NGTB40N120FL3WG	1200V / 80A
Electrolytic MPK	TDK	B43706 series	-
	KEMET	ALC70 series	-
	Vishay	193 PUR-SI Solar series	-
Heatsink	PANASONIC	EZPV series	-
	KEMET	C4AQ-P series	-
	TDK	B32320I series	-
Inductor Core	Magnetics	Toroids' Powder Core Catalog	-

[1] rated voltage and current refers to the reverse voltage and forward current supported by the diode, respectively.

[2] rated voltage and current refers to the V_{CE} and I_c supported by the switch, respectively.

3.2 Study Case I

The investigation summarized in Study Case I possessed all the converter topologies designed for a 5 kW single-phase PV inverter linked to a 220 V/60 Hz grid. The input parameters for the multi-objective algorithm included an 800 V DC link voltage, a maximum inductor current ripple of 10%, a DC link capacitance of 2 mF, and a switching frequency ranging from 10 kHz to 40 kHz.

3.2.1 Full-bridge topology

Figure 37 indicates that the Full-bridge inverter topology, operating with the parameters described earlier and utilizing the components listed in the Table 3 database, achieved a maximum efficiency of approximately 96.6% for a power density below 0.5 kW/dm^3, when the switching frequency is set to 10kHz. It is evident, therefore, that constructing a converter trying to achieve the highest efficiency using this topology requires a significant volume. Hence, the use of a cost function, such as expression (2.25), is advisable to find a middle ground and achieve the best cost-benefit for the project.

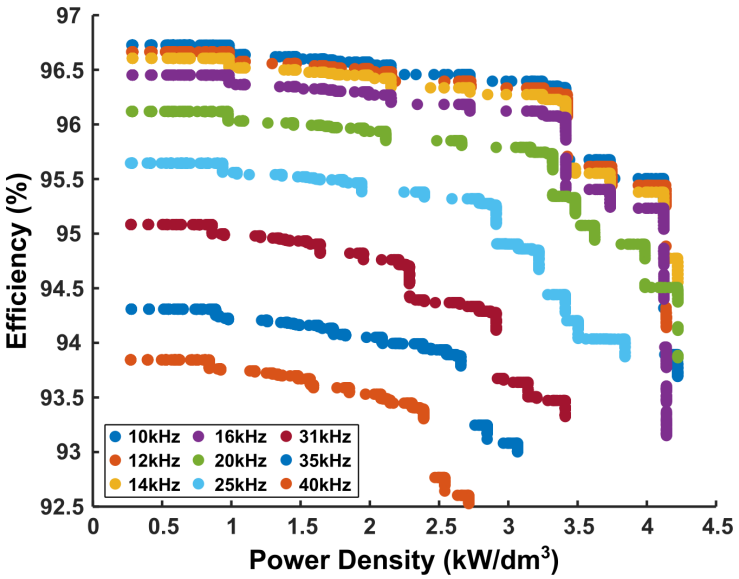

Figure 37 – Full-bridge Pareto frontier for several switching frequencies
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Furthermore, as the switching frequency increases, both efficiency and power density decrease. For instance, the orange curve, representing a switching frequency of 40 kHz, illustrates that the efficiency range for this topology is approximately between 93.8% and 92.5%, with a power density ranging from 0.3 kW/dm^3 to 2.6 kW/dm^3, respectively.

Another important aspect observed in these Pareto curves is that for switching frequencies above 20 kHz, the solution space, meaning both efficiency and power density, decreases. Since the power devices investigated are Si-IGBTs, this confirms the operational

limitations of Si technology. The increase in switching losses not only impacts efficiency but also requires more heatsink area, leading to an increase in volume beyond the improvement in the performance indices of inductors and capacitors. This suggests that, for the current database, the ideal frequency for this topology falls within the range of 10 kHz to 20 kHz.

3.2.2 H5 topology

Figure 38 illustrates the results of the multi-objective algorithm applied to the H5 topology, with efficiency and power density as the studied variables. Similar to the Full-bridge topology, it is evident that constructing a converter with maximum efficiency requires a substantial volume, considering the components listed in the database. Furthermore, in comparison with the Full-bridge inverter, examining the 40 kHz curve (in orange) reveals that the efficiency range of H5 is between 93.6% and 92.5%, while the power density ranges from 0.3kW/dm^3 to 2.2 kW/dm^3, respectively. This indicates that, operating under the same circumstances as a Full-bridge inverter, the H5 topology, requiring a minimum of 5 switches, incurs a penalty in reducing power density.

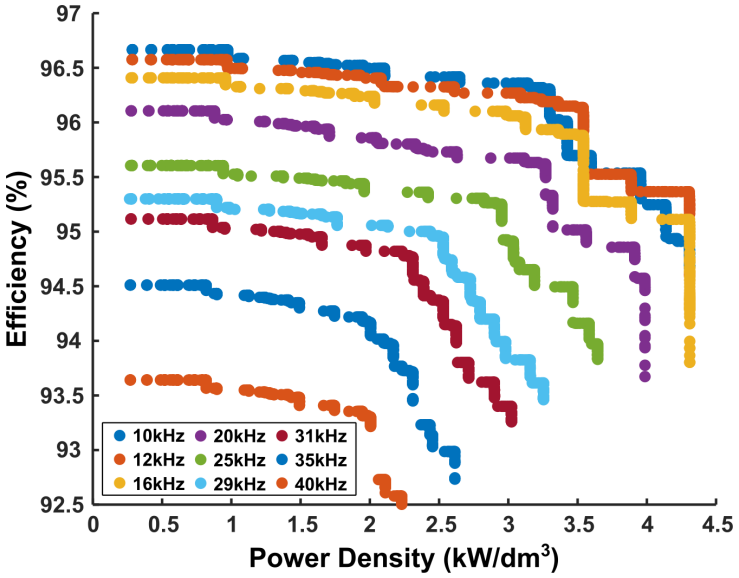

Figure 38 – H5 Pareto frontier for several switching frequencies
Font: The author

From a different perspective, analyzing the curves from 10 kHz to 16 kHz reveals an intersection, suggesting that the ideal switching frequency for the H5 converter is approximately between 10 kHz and 16 kHz, considering the utilized components. Above 16 kHz, the curves contract, indicating a simultaneous decrease in both efficiency and power density. This leads to the inference that by adding a semiconductor (switch S5 in Figure 13) operating at a high frequency throughout the switching cycle, the switching losses in this component are higher compared to the other switches operating in a hybrid manner. Indeed, switching losses are directly proportional to the converter's switching frequency which leads to paralleling switches increasing the volume as well.

3.2.3 HERIC topology

Figure 39 shows the performance of the HERIC topology, which, unlike the Full-Bridge and H5 topologies, did not reach a switching frequency of 40 kHz. The most likely explanation is that the construction of this converter requires a minimum of 6 switches to operate. It's specified as a minimum of 6 switches because, if necessary, they can be connected in parallel, reducing the concentration of losses in a single semiconductor but, on the other side, increasing the inverter's volume.

Note that when the HERIC operates at a frequency of 35 kHz, the Pareto curve is approximately equal to the performance of the Full Bridge and H5 when these topologies operate at 40 kHz. In this case, either Full Bridge or H5 have advantages in both efficiency and power density when comparing the 35 kHz curves of these converters to the HERIC.

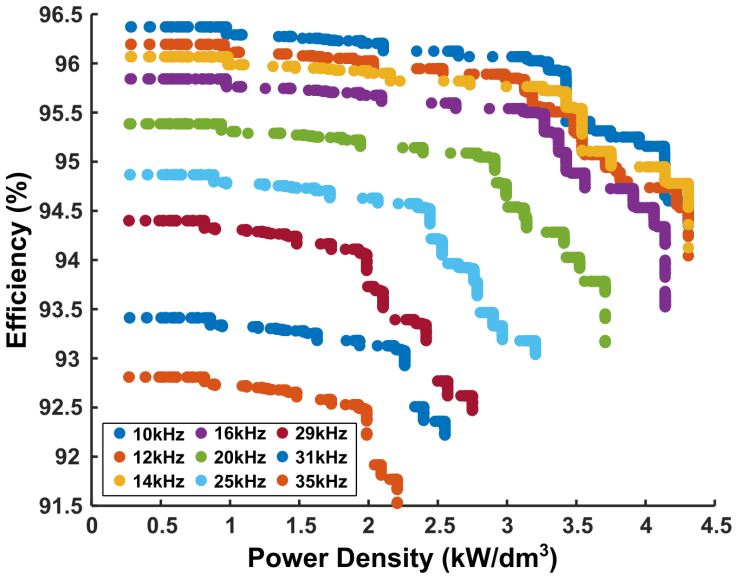

Figure 39 – HERIC Pareto frontier for several switching frequencies
Font: The author

Observing lower frequencies, it becomes evident that the ideal switching frequency range for the HERIC is between 10 kHz and 16 kHz. Beyond 16 kHz, both efficiency and power density contract, meaning that they decrease simultaneously. Another point to note is that due to the number of switches, the HERIC topology is less efficient than the Full Bridge and H5, where its maximum efficiency does not reach 96.5%, even considering the lower power density.

3.2.4 NPC half-bridge topology

Figure 40 illustrates the performance of the NPC half-bridge topology, which, unlike full-bridge topologies, achieved better performance at high switching frequencies in terms of both efficiency and power density. Regarding the power density, this converter can reach approximately 6.5 kW/dm^3 even when operating at high frequencies. It's worth

noting that the Pareto curve contracts slightly as the switching frequency increases, a contrast to full-bridge topologies where the converter volume increases significantly.

An interesting characteristic of this result is that, when the converter operates at 10 kHz (dark blue curve), the efficiency is the lowest across the entire switching frequency range. However, the optimal switching frequency for this converter would be around 20 kHz, as shown in the yellow Pareto curve, where both efficiency and power density outperform the other curves. When the converter operates at switching frequencies higher than 20 kHz, the behavior of the Pareto curve contracts similarly to what occurs in full-bridge topologies.

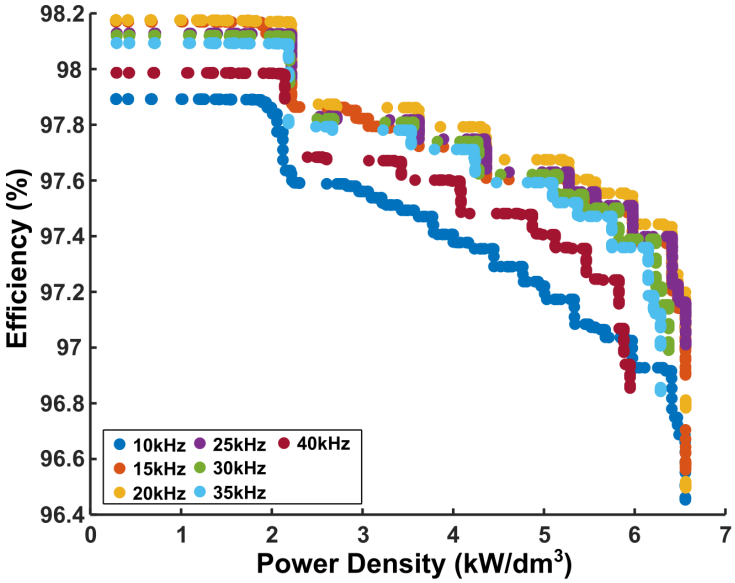

Figure 40 – NPC Half-bridge Pareto frontier for several switching frequencies
Font: The author

The most likely explanation for the superior performance of the NPC half-bridge may lie in the split capacitor of the DC bus. In the case of full-bridge topologies, the DC bus is 800V, and the capacitance is fixed at 2mF, resulting in a bulkier arrangement due to the capacitor bank needing to meet minimum requirements to support both voltage and current. In the case of the NPC, the split capacitor can be seen as two capacitor banks, where the DC bus voltage in each bank is 400V. This allows for a more compact arrangement, enabling the NPC to achieve a higher power density than full-bridge topologies.

3.2.5 Conergy NPC topology

Figure 41 illustrates the Conergy NPC, which, in turn, exhibits performance similar to the NPC Half-Bridge, with clustered Pareto curves. Both topologies, NPC Half-Bridge and Conergy, when operated at high switching frequencies, can deliver higher power density than full-bridge topologies, considering the component database used in this study.

Unlike the NPC Half-Bridge, the ideal switching frequency falls between 15 kHz. Another interesting point is at a frequency of 10 kHz. Note that if the converter operates at this frequency, the power density reaches values higher than at other switching frequencies. Analyzing the region where power density is between 5 kW/dm^3, a set of Pareto curves from different switching frequencies is observed, with efficiency ranging between approximately 93% and 97.4%. Thus, it is evident that a high-efficiency inverter with high power density can be constructed.

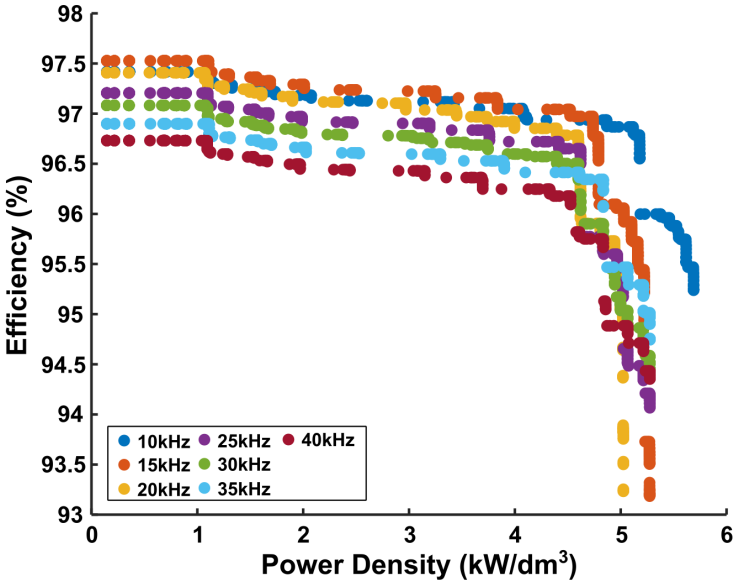

Figure 41 – Conergy NPC Pareto frontier for several switching frequencies
Font: The author

However, similar to the NPC half-bridge topology, the split capacitor provides a significant advantage in the construction of this topology, where the volume of the capacitor bank can be reduced due to the DC bus operating voltage being divided in half. In other words, since the DC bus is 800V, the voltage in each bank of the split capacitor is 400V. Thus, the drawback of operating this topology appears from the need to add measurements to the DC link and further control strategies for split capacitor balancing. Otherwise, the voltage in each split capacitor bank will diverge, causing the inverter to be unable to synthesize the grid voltage appropriately, resulting in irregular inverter operation. However, for study purposes, this aspect does not impact the results of this investigation.

3.2.6 Overall Analyses

The previous sections demonstrated the individual performance of each topology as the switching frequency is altered. However, it becomes necessary to compare the best designs of each topology in a single graph, as shown in Figure 3.6. Regardless of the switching frequency, the points on the Pareto curve for each topology are chosen to highlight the best candidates for more efficient inverters. From Figure 42, the designer

can decide which inverter design is more advantageous to build, considering that there is a trade-off between efficiency and power density. If the designer opts for higher power density, i.e., constructing a less voluminous inverter, on the other hand, the efficiency of the inverter may not be as advantageous, depending on the topology.

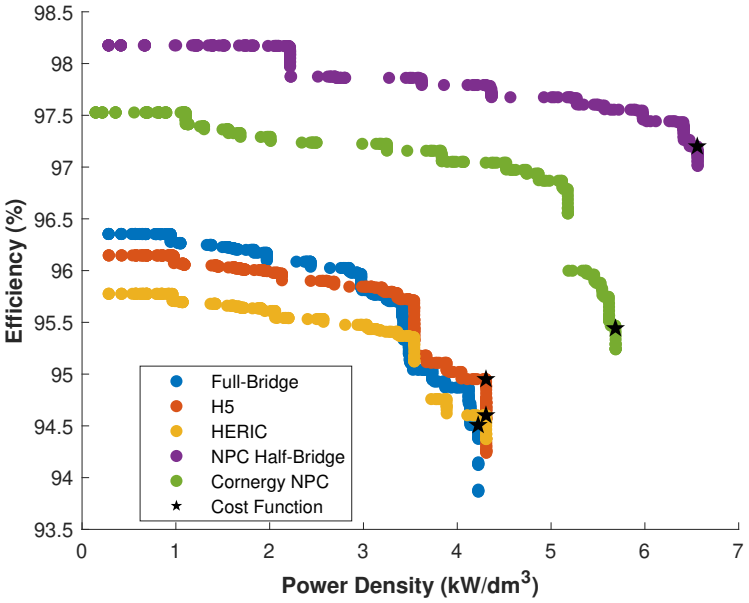

Figure 42 – Comparison of the Pareto-Front of each topologies for a 800V DC link
Font: The author

Analyzing the NPC Half-Bridge first, it is possible to observe that in terms of efficiency and power density, this topology outperforms the others. With the existing component database, constructing a converter using this topology can achieve an efficiency of approximately 98.1%, with the condition that this converter will be extremely voluminous. On the other hand, considering an efficiency of 97.4%, a power density higher than 6 kW/dm^3 can be achieved. This implies building a lightweight converter, which, for a 5 kW converter, means a weight of approximately 6 kg for comparison. However, the disadvantage of this topology is the split capacitor voltage balance, leading to a more complex control of the converter.

Regarding the full-bridge topologies, it is observed that the performance is very close in both efficiency and power density. Therefore, it can be concluded that the decision-making for choosing the topology relies on operational aspects of the converter, such as leakage current and common-mode voltage, among others.

There are several ways to determine the best choice of inverter design for a specific project, and one of them is using a cost function like the one in Equation 2.25. In fact, each point on the Pareto curve represents an optimal design considering the used component database. Therefore, one cannot assert that a design with power density and efficiency, ρ_1 and η_1, is better than another located at ρ_2 and η_2 within the solution space. Based on this principle, the cost function used in this work highlights the points, marked with

black stars, of potential inverter design choices where the product of power density and efficiency is maximized, considering each topology.

Additionally, the designs chosen through the cost function are better visualized in Figure 3.7, illustrating the distribution of volume and losses. In general, the main contributors to the volume are the DC link and the heatsink, while losses are more pronounced in the switches. In the case of NPC topologies, losses are distributed among the switches and the DC link. However, for a better understanding of this result, Table 4 provides a detailed overview of each component used in the best candidate projects selected by the presented cost function.

Therefore, analyzing Table 4 in more detail, it is evident that for the Full-bridge and NPC Half-bridge topologies, the optimal switching frequency is 20 kHz, while for the other topologies, it is 10 kHz. Note that, to achieve approximately similar losses between the DC link and the switches in NPC topologies, this is attributed to the high number of switches, which helps reduce conduction losses, for example. In the case of NPC Half-bridge, there are a total of 10 switches, while in the Conergy topology, there are 12 switches.

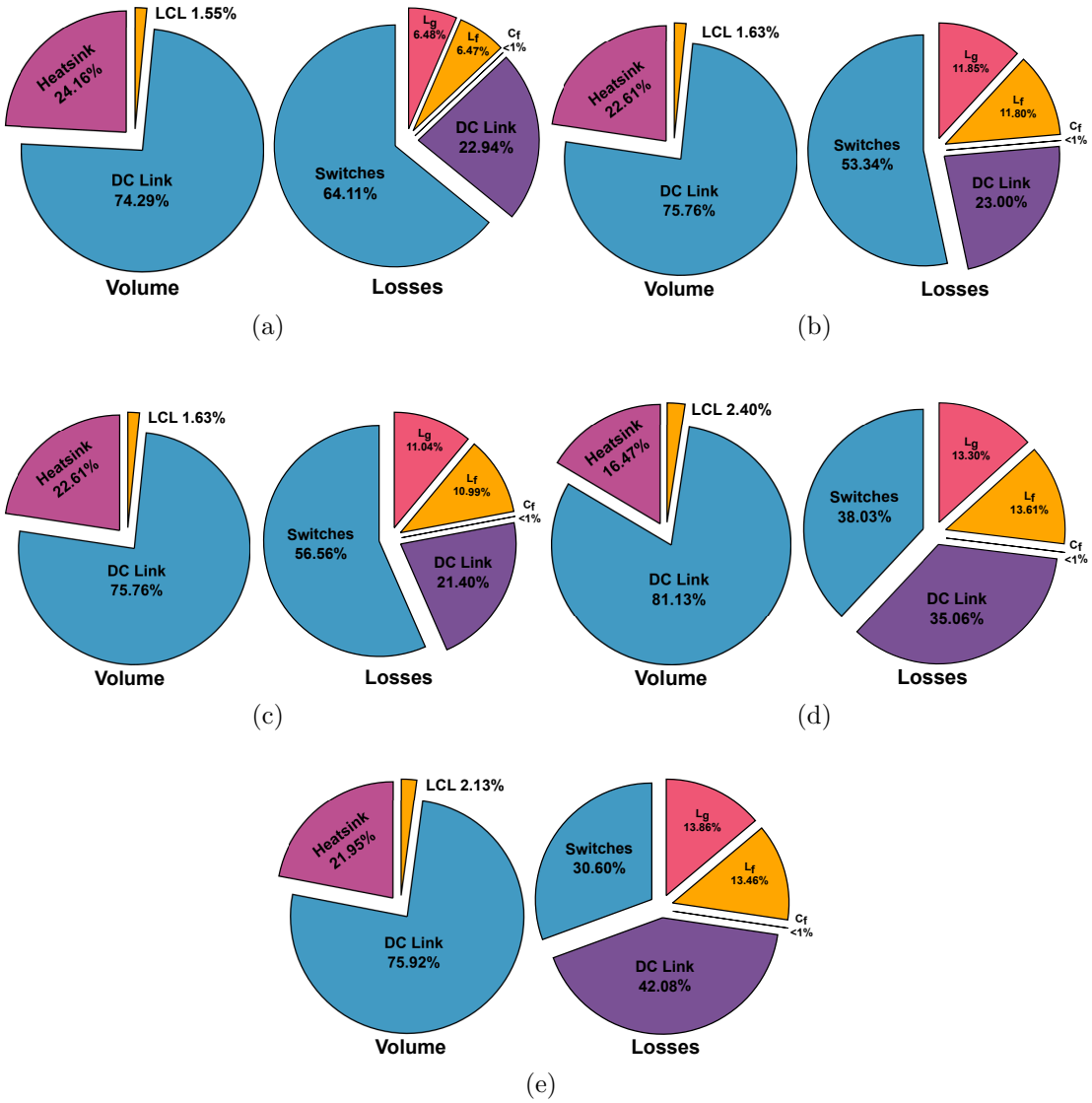

Figure 43 – Distributed volume and losses of each topology when 800V DC link is settled. (a) Full-bridge, (b) H5, (c) HERIC, (d) NPC Half-bridge, (e) Conergy NPC
Font: The author

Table 4 – Best solutions implementation for Study Case I

Description	**Full-Bridge**	**H5**	**HERIC**	**Half-Bridge NPC**	**T-Type NPC**
Switching Frequency	20 kHz	10 kHz	10 kHz	20 kHz	10 kHz
Switches	IKW15N120BH6 S1-S4: x4	MBQ40T120FES S1,S3: x4; S2,S4,S5: x1	IKW15N120BH6 S1-S4: x3; S5,S6: x3	IKW50N65ES5 S1,S4: x4; S2,S3: x2	NGTB40N120FL3WG S1,S2: x4; S_+,S_-: x2
Diode	-	-	-	MSC030SDA070K D_+: x2; D_-: x2	-
Heatsink	HS6835 - 12.16cm 368.3g	HS6835 - 11.16cm 368.3g	HS6835 - 11.16cm 368.3g	HS4425 - 11.16cm 133.9g	HS4425 - 17.16cm 205.9g
L_f and L_g	2,1 mH	4,1 mH	4.1 mH	2.1 mH	4,1 mH
Core	2 x 0058778A2 High Flux 125μ	3 x 0058778A2 High Flux 125μ	3 x 0058778A2 High Flux 125μ	2 x 0058778A2 High Flux 125μ	3 x 0058778A2 High Flux 125μ
Number of turns	49 turns	57 turns	57 turns	49 turns	57 turns
Wire	AWG 18 x 7	AWG 18 x 7	AWG 18 x 7	AWG 18 x 7	AWG 18 x 7
DC Link Capacitor	ALC70A821EJ550 Parallel: 5 , Series: 2	ALC70A821EJ550 Parallel: 5 , Series: 2	ALC70A821EJ550 Parallel: 5 , Series: 2	ALC70A680BC600 Parallel: 18, Series: 1	ALC70A201CD550 Parallel: 18 , Series: 1
Filter Capacitor	C4AQGBU5150P11K	C4AQGBU5150P11K	C4AQGBU5150P11K	C4AQGBU5150P11K	C4AQGBU5150P11K
Weight	4.4822 kg	5.0254 kg	5.2190 kg	3.8449 kg	4.3464 kg
Power Density	4.2227 kW/dm^3	4.3061 kW/dm^3	4.3061 kW/dm^3	6.5585 kW/dm^3	5.0618 kW/dm^3
Efficiency	94.51%	94.95%	94.60%	97.20%	94.49%

3.3 Study Case II

The investigation digested in Study Case II included only the converter derived from Full-bridge topologies designed for a 5 kW single-phase PV inverter linked to a 220 V/60 Hz grid. The input parameters for the multi-objective algorithm included a 400V DC link voltage, a maximum inductor current ripple of 10%, a DC link capacitance of 2 mF, and a switching frequency ranging from 10 kHz to 40 kHz.

3.3.1 Full-bridge topology

Figure 44 illustrates the performance of the full-bridge converter when the DC link operates at 400V. In comparison to the previous result, there is a noticeable increase in power density, and furthermore, a slight improvement in efficiency. Indeed, the volume of the capacitor bank will vary according to the DC link voltage, as connecting capacitors in series is necessary to make the capacitor bank withstand the DC link voltage. On the other hand, capacitors are connected in parallel to increase the overall capacitance.

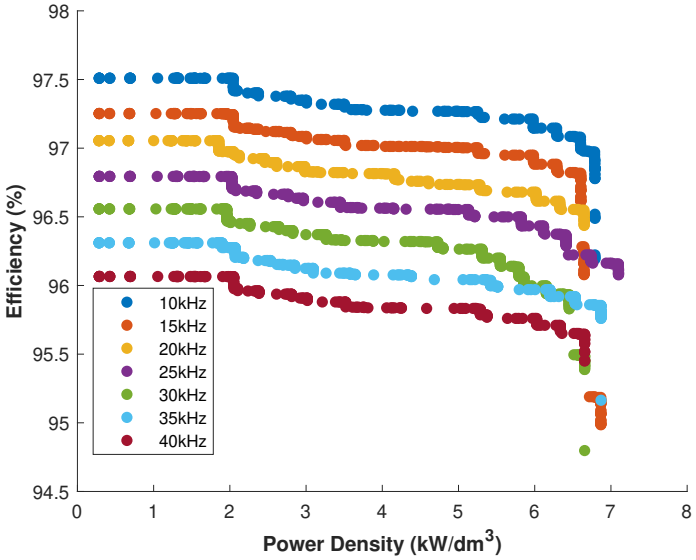

Figure 44 – Full-bridge Pareto frontier for several switching frequencies
Font: The author

Note that when analyzing the region close to 7 kW/dm3, it can be observed that the Pareto curves at each switching frequency cluster, resulting in an efficiency range between approximately 94.7% to 96.5%. This implies that if a designer aims for higher power density, the chosen switching frequency will determine the efficiency the converter will achieve, based on the used component database.

3.3.2 H5 topology

The Figure 45 depicts the H5 topology operating with a 400V DC link. In comparison to the previous result, the same behavior of the Pareto curve is observed for each frequency, contracting both in power density and efficiency. Additionally, superior efficiency and power density are analyzed compared to Figure 3.2, where the maximum efficiency achieved was 97.4%, whereas when operated with an 800V DC link, the maximum efficiency was approximately 96.7% for a switching frequency of 10kHz.

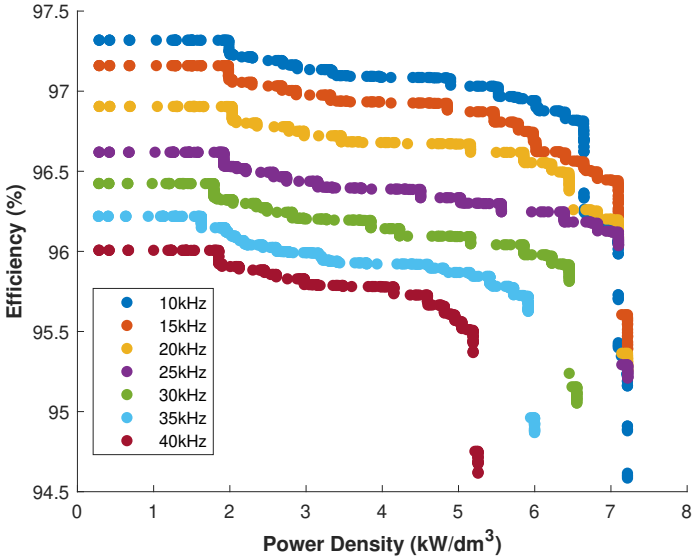

Figure 45 – H5 Pareto frontier for several switching frequencies
Font: The author

In the case where the switching frequency is 40 kHz, it is observed that in terms of efficiency, there is a range where efficiency varies approximately between 96% to 94.5%, for a power density of 0.2 to 5.2 kW/dm3. This is in contrast to the scenario where the bus voltage is 800V, and the maximum power density, for a switching frequency of 35 kHz, reaches around 2.3 kW/dm3, approximately. This discrepancy arises because the algorithm did not find a heatsink, within the existing database, for a switching frequency of 40 kHz.

3.3.3 HERIC topology

Figure 46 depicts the performance of the HERIC inverter subjected to the multi-objective algorithm. Note that the Pareto curve contracts in both efficiency and power density as the switching frequency increases. It is also observed that the maximum efficiency the converter achieves is at low frequencies, specifically at 10kHz, with the condition of low power density, indicating an extremely voluminous converter. Shifting the focus to a more power-density-oriented analysis, observe that in the region around 7 kW/dm3, there is a cluster of Pareto curves with switching frequencies ranging from 10 to 25kHz. This implies

that the designer has more flexibility in choosing the switching frequency as it affects the construction of the inductor, losses in the inductor, and semiconductor switches.

In comparison with Case Study I, it is evident that with a 400V DC link, power density has increased significantly, along with achieving better efficiency. Another crucial point is that, operating with an 800V DC link, the maximum switching frequency was 35kHz, while with a 400V DC link, the converter can go up to 40kHz. Overall, even at high frequencies, with a lower DC link voltage, the converter was more efficient, reaching approximately 93.5%.

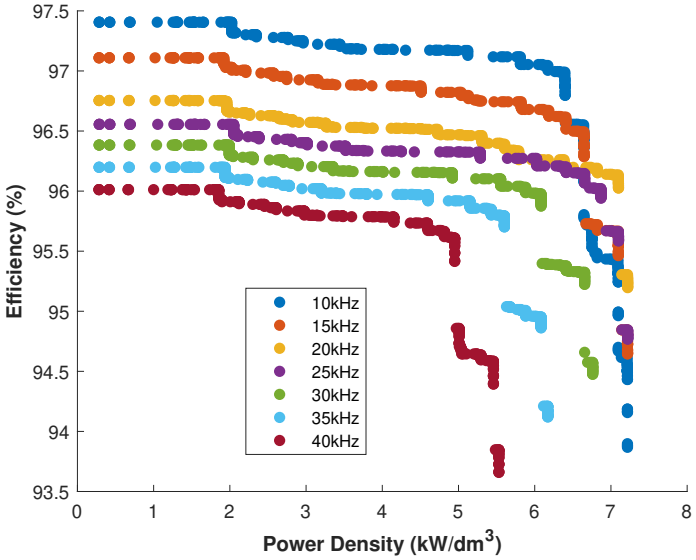

Figure 46 – HERIC Pareto frontier for several switching frequencies
Font: The author

3.3.4 Overall analyses

Before start commenting on Figure 47, it is noteworthy to guarantee that NPC topologies from Study Case I are also plotted for comparison purposes. However, it does not imply that NPC topologies were simulated with a 400V DC link as long as this scenario is not possible. Then, the objective is to compare performances among H-bridge topologies with a 400V DC link and NPC topologies with an 800V DC link.

The results of this case study only refer to full-bridge topologies due to the DC link voltage being 400V, which would not be possible for NPC topologies. Thus, analyzing Figure 47 in a general context, it is noticeable that the performance among the topologies is very close, considering that each converter requires a different number of switches. The converter with the highest efficiency was the full-bridge, followed by the HERIC and H5. This may not seem very intuitive, given that the HERIC requires 6 switches to operate, while the H5 requires only 5. However, the most likely explanation is the arrangement

of the switches, as the HERIC needs 2 switches to transfer power from the solar panels, whereas the H5 requires 3 switches to perform the same process.

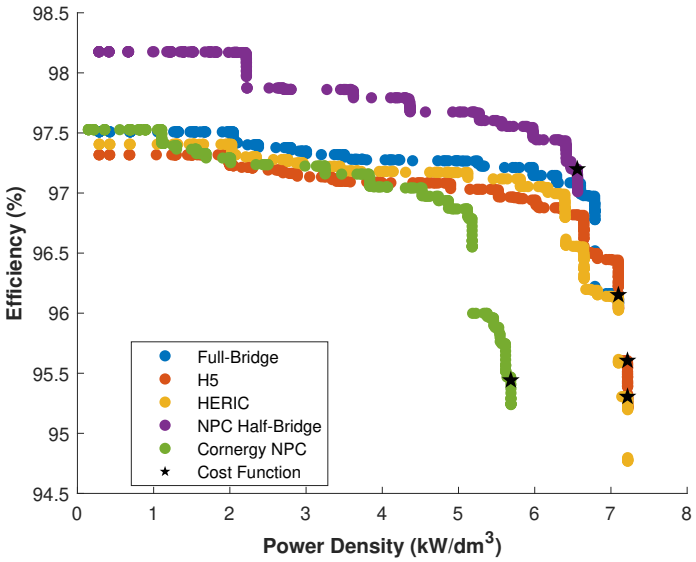

Figure 47 – Comparison of the Pareto-Front of each topologies for a 400V DC link
Font: The author

Just a piece of information in this analysis: Figure 3.11 shows, in addition to the topologies derived from the H-bridge, the NPC topologies from Study Case I that are also plotted for comparison purposes. Something very interesting can be observed: the H-bridge topologies have practically the same power density as the NPC when simulated with a 400V DC link, except for the Conergy NPC. Therefore, it is concluded that there is no competitive advantage between topologies. Although the NPC half-bridge is slightly superior in terms of efficiency compared to the other topologies, this does not justify considering it as a suitable choice among other topologies.

Applying the cost function (2.16), it is observed that the best candidates shown with black stars indicate that in terms of efficiency and density, these converter projects are similar. What will differentiate them is, in fact, the number of components required to build them; however, they will have practically the same performance.

In order to enhance the visualization of each converter, Figure 48 illustrates the distribution of losses and volumes for each converter selected through the cost function. Overall, regardless of the topology, the volume distribution was approximately the same, around 60% for the DC link and 38% for the heatsink. In terms of losses, the Full-bridge showed higher losses in the switches at 76.73%, followed by the LCL filter with a total of 11.87%, and finally, the DC link with 11.40%. On the other hand, the H5 exhibited lower losses in the switches compared to the HERIC, with 62.45%, and finally, in terms of the DC link and filter, the H5 had inferior performance compared to the HERIC.

Finally, Table 5 presents the inverter design, detailing each design parameter. In

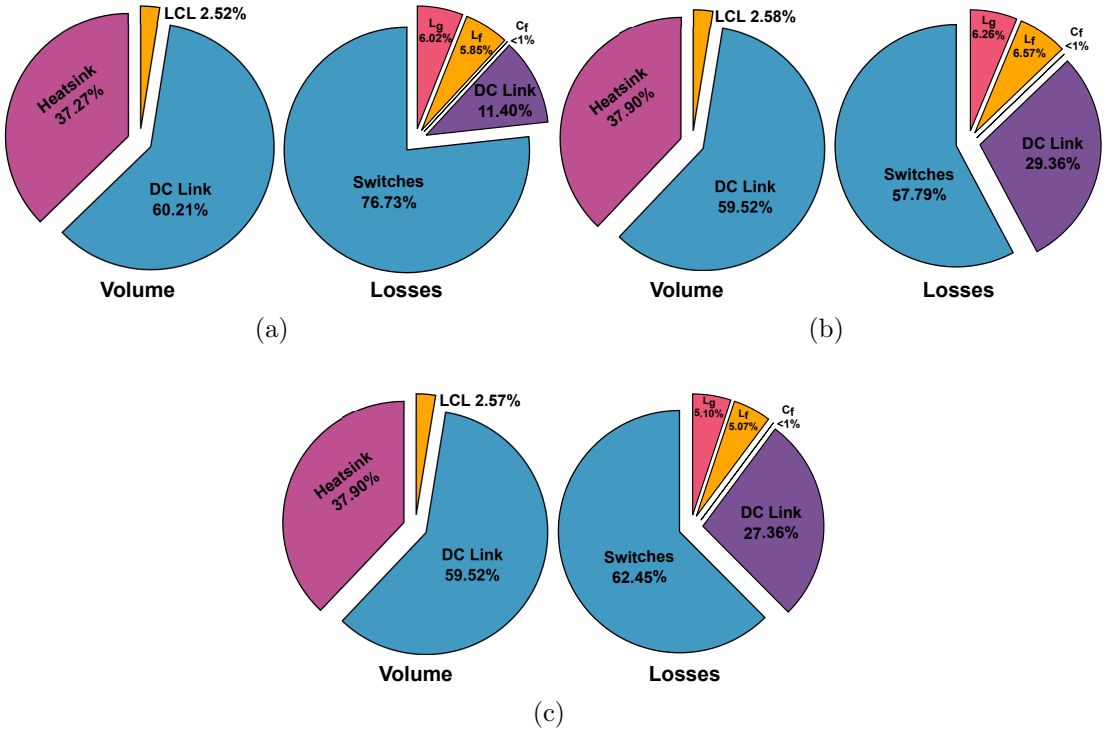

Figure 48 – Distributed volume and losses of each topology when 400V DC link is settled. (a) Full-bridge, (b) H5, (c) HERIC
Font: The author

this case study, it can be observed that with a 400V DC link, the converter can operate at higher frequencies. For the Full-bridge, the optimal switching frequency was 25kHz, resulting in a smaller inductance and a lighter inverter weighing 2.8192 kg. As for the H5, the switching frequency was 15kHz, where the inverter is relatively heavier, weighing as much as the HERIC and Full-bridge. The HERIC, on the other hand, performed better at 20kHz, where this topology features 18 switches, with S1 to S4 each having 3 switches, and S5 and S6 having 3 switches each. In terms of weight, the HERIC is relatively lighter than the H5. Regarding efficiency, the Full-bridge inverter design outperformed the H5 and HERIC by a little over 1%.

3.4 Chapter Overview

This chapter demonstrated the inverter's performance in two different case studies. In Study Case I, the performance of topologies derived from the H-bridge and NPC was observed. Regarding the H-bridge topologies, the Pareto curves show that the inverter's performance is directly influenced by the switching frequency, meaning that as the frequency increases, both efficiency and power density decrease. However, this behavior is not observed in NPC topologies, where mainly in the NPC Half-bridge, as the switching frequency increases, the inverter's efficiency increases, and the power density is not influenced in any

way. Obviously, there is a limit, and in this case, above 20kHz, the NPC half-bridge has its efficiency reduced, but not lower than the Pareto curve at 10kHz.

Table 5 – Best solutions implementation for Study Case II

Description	**Full-Bridge**	**H5**	**HERIC**
Switching Frequency	25 kHz	15 kHz	20 kHz
Switches	IKW50N65ES5 S1-S4: x2	IKW50N65ES5 S1,S3: x4; S2,S4,S5: x1	NGTB40N120FL3WG S1-S4: x3; S5,S6: x3
Heatsink	HS6835 - 11.16cm 368.3g	HS6835 - 11.16cm 368.3g	HS6835 - 11.16cm 368.3g
L_f and L_g	0.83 mH	1.4 mH	1 mH
Core	1 x 0058778A2 High Flux 125μ	1 x 0058778A2 High Flux 125μ	1 x 0058778A2 High Flux 125μ
Number of turns	44 turns	57 turns	49 turns
Wire	AWG 21 x 13	AWG 18 x 7	AWG 18 x 7
DC Link Capacitor	ALC70A181CF600 Parallel: 12, Series: 1	ALC70A101BC550 Parallel: 24, Series: 1	ALC70A101BC550 Parallel: 24, Series: 1
Filter Capacitor	C4AQGBU5150P11K	C4AQGBU5150P11K	C4AQGBU5150P11K
Weight	2.8192 kg	3.5074 kg	3.2757 kg
Power Density	7.0979 kW/dm^3	7.2171 kW/dm^3	7.2177 kW/dm^3
Efficiency	96.15%	95.60%	95.31%

Finally, Study Case II demonstrated that by reducing the DC link voltage level to 400V, the H-bridge topologies showed a different behavior compared to the previous observation. It is followed that in this case, the power density is not affected by the switching frequency for the full-bridge topology; however, it is noted that increasing the frequency leads to a decrease in efficiency. For the H5 and HERIC topologies, the power density starts to decrease from a switching frequency above 25kHz. It is worth mentioning that the NPC topologies, in this case, are not included in this analysis because the output voltage of the inverter in each switching half-cycle is 200V, which is insufficient to synthesize the grid voltage.

4 CONCLUSION

After conducting an extensive investigation of the different topologies studied in this work, summarizing the results becomes extremely important. As described previously, the use of the Pareto Front proved to be a useful tool for identifying the best candidates to become an inverter, based on a database of real components. This methodology was applied in a multi-objective algorithm adapted to each topology scheme due to the symmetry inherent in each of them in terms of switches.

Subsequently, each topology was evaluated using a multi-objective algorithm in which Matlab/Simulink was employed to gather information such as current and voltage from different components. Before the simulation in the Simulink environment, each component of the inverter was designed, including the inductance, capacitance, current control, and voltage control. All this information is essential for Simulink to operate properly. In this study, only the switching frequency was varied from 10kHz to 40kHz, and after each iteration, the inverter components were updated.

Once Simulink completes the simulation, information such as DC Link current, LCL filter current, and others were sent to Matlab, where the multi-object algorithm utilized all this information to build the inverter, including the DC link bank, inductors, number of switches, heatsink, and other components. This process can generate millions of solutions, each of which represents a point in the performance space. Therefore, it is necessary to use the Pareto Front, where the best candidate projects are selected based solely on the power density and efficiency of each inverter. It is worth noting that after applying the Pareto Front, each inverter represents the best solution, and it is up to the designer to choose the best option for a desired project. Therefore, a cost function proved to be useful due to the necessity of selecting at least one project as an example. However, as observed in the results, efficiency decreases as power density increases, presenting a trade-off that designers must consider when making decisions.

Two case studies were conducted in this work: the first one considered a DC link of 800V required for the NPC topologies, while the second one used a 400V DC link which only topologies derived from the H-bridges could operate in this scenario. As discussed previously, NPC topologies, being a half-bridge, require their DC link voltage to be at least double the grid voltage for the inverter to operate adequately. Consequently, it was observed that NPC topologies exhibited higher efficiency and power density compared to full-bridge topologies. The reason for this might be the size of the DC Link bank, which requires a larger volume in full-bridge topologies. However, when full-bridge topologies were simulated with a 400V DC Link, they exhibited better performance than in Study Case I, once again due to the size of the DC Link bank.

Additionally, an extra piece of information concerned the volume and losses distribution of each converter. The DC link and heatsink were mentioned to pose the greatest challenges in building an inverter, comprising more than 90% of the inverter volume even with changes in the DC link voltage. On the other hand, depending on the DC link voltage, the distribution of losses may vary significantly between the DC link voltage bank and the switches. However, when the DC link voltage is around 800V, the losses in the switches account for 64% for the full-bridge topologies and 38% for the NPC half-bridge topologies. On the contrary, the DC link contributes to around 22% for all full-bridge topologies, and 35% and 42% for NPC Half-bridge and Conergy NPC topologies, respectively. When transitioning to a DC link of 400V, the DC link losses decreased significantly, with full-bridge topology exhibiting the best performance at 11.40%, followed by H5 with 29.36% and Heric with 27%. Switches losses were more concentrated, with Full-bridge topology showing 76%, followed by H5 with 57%, and finally, 62% for the HERIC topology.

Given all the discussion presented, it was not possible to conclude that there is a competitive advantage among the topologies, as the results obtained were similar. In Study Case I, it is observed that the NPC topology demonstrated higher efficiency, while the full-bridge topologies were less efficient. Similarly, in terms of power density, the NPC topology performed better. However, when considering only the topologies derived from the full-bridge, it can be concluded that they showed similar performance both in efficiency and power density, since in both Case Studies, the Pareto curves are practically overlapped. This indicates that, despite the different number of switches required for each topology to operate, this does not affect efficiency and power density. In terms of comparison between the Case Studies, it is noted that when the full-bridge topologies were simulated with a 400V DC link and compared with the NPC topology with an 800V DC link, it is observed that, in terms of power density, there is no difference, except for the Conergy NPC case. Following the same logic, comparing both Case Studies, now only for the full-bridge topologies, it was observed that by reducing the DC link from 800V to 400V, there was an increase in efficiency and the power density increased significantly.

4.1 Further work proposals

As a continuation of the work presented in this thesis, we suggest the following topics:

- Introduce cost as a performance index for the multi-objective algorithm involving the construction cost of the inverter, based on the price of each real component inserted in the database. Additionally, prices should be constantly updated, and pricing should follow the dollar exchange rate;

- Evaluate the impact of other output filter topologies and also common-mode filters in the performance indexes of the converter design;
- Investigating the impact of PWM modulations on the filter. This discussion is important because it can be noted how each PWM influences the inductor ripple, as well as the average current.
- Include wide bandgap devices, eg, SiC and GaN, in the design database and evaluate their impact on the system performance;
- Expand the set of converter topologies considered in this investigation, with the inclusion of the DC/DC converter as well.
- Choose 2 topologies, one NPC and another Full-bridge, for experimental testing and project comparison.

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