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Programa de Pós-Graduação em Engenharia Elétrica

William Caires Silva Amorim

EVALUATION OF BATTERY CURRENT HARMONIC SUPPRESSION SCHEMES FOR MMC-BASED ENERGY STORAGE SYSTEMS THROUGH MISSION PROFILE EMULATORS

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William Caires Silva Amorim

"Evaluation of Battery Current Harmonic Suppression Schemes for MMC-Based Energy Storage Systems Through Mission Profile Emulators"

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Coorientador: Prof. Dr. Allan Fagner Cupertino
Coorientador: Prof. Dr. Heverton Augusto Pereira

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WILLIAM CAIRES SILVA AMORIM

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Por:

Prof. Dr. Victor Flores Mendes
DEE (UFMG) - Orientador

Prof. Dr. ALLAN FAGNER CUPERTINO
(UFJF)- Coorientador

Prof. Dr. Heverton Augusto Pereira
(UFV) - Coorientador

Prof. Dr. Lenin Martins Ferreira Morais
DELT (UFMG)

Prof. Dr. Thiago Ribeiro de Oliveira
DELT (UFMG)

Prof. Dr. Pedro Machado de Almeida

(UFJF)

Prof. Dr. Fabricio Bradaschia
(UFPE)

Belo Horizonte, 13 de setembro de 2024.

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"À minha família, bons espíritos, mentores e amigos."

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"Não fui eu que ordenei a você? Seja forte e corajoso!
Não se apavore nem desanime, pois o Senhor,
o seu Deus, estará com você por onde você andar."
(Josué 23:1-9)

Resumo

Nos últimos anos, os Conversores Modulares Multiníveis (do inglês, *Modular Multilevel Converter*) (MMC) têm sido utilizados em aplicações de média/alta tensão, e apontados como uma solução promissora para Sistemas de Armazenamento de Energia em Bateria (do inglês, *Battery Energy Storage Systems*) (BESS). Especialmente, na aplicação BESS, as condições de corrente e tensão nos submódulos (SM) são fundamentais para avaliar a dinâmica térmica, confiabilidade e vida útil das baterias. Para aplicações de média/alta tensão, o MMC é baseado em dezenas ou centenas de SMs. Assim, a implementação completa do sistema MMC pode ser cara e complexa para testes operacionais e de confiabilidade das baterias. Nesse sentido, os chamados Emuladores de Perfis de Missão (do inglês, *Mission Profile Emulator*) (MPE), foram desenvolvidos para emular a tensão e a corrente típicas em um SM para baixa tensão e potência, preservando o conteúdo harmônico. O MPE pode reduzir a necessidade de implementação do conversor completo e contribui para testes mais ágeis da características elétricas do MMC e em especial das baterias, resultando no projeto de conversores mais confiáveis. Neste trabalho, um projeto detalhado e a análise da implementação do MPE para um BESS baseado em MMC são apresentados. O MPE é validado em simulações e em protótipo em escala reduzida. O espectro de corrente de braço e corrente de bateria apresentou conteúdo semelhante comparando equação analítica, simulação e resultados experimentais. Além disso, com o MPE projetado, são avaliadas estratégias passivas (filtros indutivos e capacitivos) e ativas (conversor cc/cc) de filtragem para eliminar componentes harmônicos presentes na corrente da bateria. Os resultados mostraram que a ondulação máxima da corrente de braço do MMC apresenta valores inferiores a 10%, de acordo com o limite para projetar o indutor do MPE. Além disso, os espectros das correntes de braço e da bateria mostraram que os conteúdos harmônicos desses sinais são semelhantes aos resultados experimentais e de simulação, de acordo com o espectro de corrente típico observado no MMC-BESS. A bancada com os principais componentes são descritos e os resultados de condicionamento, controle e operação em regime permanente são apresentados. A metodologia de projeto dos filtros passivos e da topologia do filtro ativo mostrou-se eficaz em termos de redução das componentes harmônicas presentes na corrente da bateria, com o potencial de redução da componente harmônica fundamental igual a 82.9% no filtro passivo e 97.1% na topologia do filtro ativo. O potencial de atenuação verificado nessas componentes impacta positivamente na confiabilidade do BESS em virtude da redução da temperatura das baterias.

Palavras-chaves: Sistema de armazenamento de energia de bateria; emuladores de perfil de missão; conversor multinível modular; BESS baseado em MMC; estratégias de filtragem; redução de harmônicos; filtro LC; filtro CL-LC; topologia de filtro ativo.

Abstract

In recent years, Modular Multilevel Converters (MMC) have been used in medium/high voltage applications and pointed out as a promising solution for Battery Energy Storage Systems (BESS). Especially, in the BESS application, the current and voltage conditions in the submodules (SM) are fundamental to evaluate the thermal dynamics, reliability, and lifetime of the batteries. For medium/high voltage applications, the MMC is based on tens or hundreds of SMs. Thus, the complete implementation of the MMC system can be expensive and complex for operational and reliability testing of batteries. In this sense, the so-called Mission Profile Emulators (MPE) were developed to emulate the typical voltage and current in an SM for low voltage and power, preserving the harmonic content. The MPE can reduce the need to implement the complete converter and contributes to more agile testing of the electrical characteristics of the MMC and especially the batteries, resulting in the design of more reliable converters. This work presents a detailed MPE design and implementation analysis for an MMC-based BESS. The MPE is validated in simulations and a small-scale prototype. The spectrum of arm current and battery current showed similar content comparing analytical equation, simulation, and experimental results. Furthermore, with the designed MPE, passive (inductive and capacitive filters) and active (dc/dc converter) filtering strategies are evaluated to eliminate harmonic components present in the battery current that affect its lifetime. The results showed that the maximum ripple of the arm current presents values lower than 10%, according to the limit for designing the MPE inductor. Furthermore, the arm and battery current spectrum showed that the harmonic contents of these signals are similar to the experimental and simulation results, in agreement with the typical current spectrum observed in MMC-BESS. The experimental results of the proposed system, MPE with filtering strategies in SMs, are presented in this work. The test bench with the main components is described and the conditioning, control, and steady-state operation results are presented. The passive filters and active filter topology design methodology proved effective in reducing the harmonic components present in the battery current, with the potential for reducing the fundamental harmonic component equal to 82.9 % in the passive filter and 97.1 % in the active filter topology. The potential for attenuation of these components would impact the reliability of the BESS due to the reduction of the battery temperature.

Key-words: Battery energy storage system; mission profile emulators; modular multilevel converter; MMC-based BESS; filtering strategies; harmonic reduction; LC filter; CL-LC filter; active filter topology.

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List of abbreviations and acronyms

ABB	Asea Brown Boveri (Swedish-Swiss multinational corporation)
ac	Alternating Current
AVG	Average Value
AWE	Alkaline Water Electrolyzer
BESS	Battery Energy Storage System
BMS	Battery Management System
BP	Bypass Signal
CAES	Compressed Air Energy Storage
CAPEX	Capital Expenditure
DAB	Dual Active-bridge Converter
dc	Direct Current
DFT	Discrete Fourier Transform
DOD	Depth-of-discharge
DSFB	Double-star Full-bridge
DSHB	Double-star Half-bridge
DSOGI	Dual Second Order Generalized Integrator
DSP	Digital Signal Processor
EIS	Electrochemical Impedance Spectroscopy
EMA	Exponential Moving Average
EMS	Energy Management System
EOL	End-of-life
ESS	Energy Storage Systems
ESR	Equivalent Series Resistor

FC	Flying Capacitor
FFT	Fast Fourier Transform
FB	Full-bridge Converter
GE	General Electric
GESEP	Power Electronics and Power Systems UFV laboratory (Gerência de Especialistas em Sistemas Elétricos de Potência)
HB	Half-bridge Converter
HV	High Voltage
HVAC	Heating, Ventilating, and Air Conditioning
HEV	Hybrid Electric Vehicle
HVDC	High-voltage Direct Current
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated-gate Bipolar Transistor
ISO	Independent System Operators
LCCE	Laboratory of Energy Conversion and Control UFMG laboratory (Laboratório de Conversão e Controle da Energia)
LFP	Lithium Iron Phosphate
Li-ion	Lithium-ion
LPF	Low-pass Filter
LT	Lifetime
LV	Low Voltage
MAF	Moving Average Filter
MVC	Minimum Voltage Control
MMC	Modular Multilevel Converter
MV	Medium Voltage
MPE	Mission Profile Emulator
NMC	Nickel Manganese Cobalt

NLC	Nearest Level Control
NaS	Sodium Sulfur
NiCd	Nickel Cadmium
NPC	Neutral Point Clamped
OCV	Open-circuit Voltage
OPEX	Operational Expenditure
Pb-acid	Lead-Acid
PCC	Point of Common Coupling
PCS	Power Conversion System
PI	Proportional-integral
PIMR	Proportional-integral Multi Resonant
PLECS	Piecewise Linear Electrical Circuit Simulation
PLL	Phase-locked Loop
PR	Proportional Resonant
PS-PWM	Phase-shifted Pulse-width Modulation
pu	per unit
PV	Photovoltaic
qZSI	quasi-Z-source Converter
RES	Renewable Energy Systems
RST	Reset Signal
rms	Root Mean Square
RTO	Regional Transmission Organizations
SM	Submodule
STATCOM	Static Synchronous Compensator
SMES	Superconducting Magnetic Energy Storage
SOC	State-of-charge

SOH	State-of-health
SPWM	Sinusoidal Pulse-width Modulation
UPS	Uninterruptible Power Supply
USA	United States of America
THD	Total Harmonic Distortion
THIPWM	Third-harmonic Injection Pulse-width Modulation
VSC	Voltage Source Converter
WPP	Wind Power Plant
ZSI	Z-source Converter

Note: The acronyms used in this work follow standards provide the recommended abbreviations, symbols, and units for IEEE publications.

List of symbols

B	Battery bank in the SM
$B_{m,n}$	Battery in the m position and arranged in the n-th string
C	SM capacitance
C_{Ah}	Battery capacity in Ah
C_1	electrolytic capacitance for ripple attenuation
C_2	electrolytic capacitance for ripple attenuation
C_3	electrolytic capacitance for ripple attenuation
C_4	electrolytic capacitance for ripple attenuation
$C1$	dc-link capacitance of full-bridge module
$C2$	dc-link capacitance of full-bridge module
$C3$	dc-link capacitance of full-bridge module
$C4$	dc-link capacitance of full-bridge module
cd	battery depth-of-discharge in percentage
C_{em}	emulator capacitance
C_{LC}	capacitance of LC filter
C_{max}	maximum capacitance requirement
C_{min}	minimum capacitance requirement
C_r	capacitance of tuned LC branch in CL-LC filter
$C_{r,apl}$	C-rate application requirement
$C_{r,bat}$	battery C-rate
C_{sm}	capacitance of SM in CL-LC filter
C_{y1}	decoupling capacitance
C_{y2}	decoupling capacitance

D_1	top diode of full-bridge converter in the right arm
D_2	bottom diode of full-bridge converter in the right arm
D_3	top diode of full-bridge converter in the left arm
D_4	bottom diode of full-bridge converter in the left arm
D_i	top diode of half-bridge converter
D_j	bottom diode of half-bridge converter
d_1	full-bridge duty cycle for S_1 switch
d_3	full-bridge duty cycle for S_3 switch
d_i	half-bridge duty cycle
d_{em}	MPE global duty cycle
$E_{B,n}$	BESS nominal active energy
E_n	MMC nominal energy storage
$f_{c1,d}$	frequency of the first closed-loop pole in dc/dc converter control
$f_{c2,d}$	frequency of the second closed-loop pole in dc/dc converter control
f_g	grid frequency
f_i	frequency relative to the closed-loop pole
f_s	sampling frequency
$f_{sw,dc}$	dc/dc converter switching frequency
$f_{sw,MPE}$	MPE switching frequency
$f_{sw,SM}$	SM switching frequency
$f_{sw,1}$	switching frequency of full-bridge converter
$f_{sw,2}$	switching frequency of half-bridge converter
G_d	plant transfer function due to the delay in the dc/dc converter
G_i	open-loop transfer function that relates the output voltage of the full bridge with the arm current
G_R	plant transfer function of the dc/dc converter capacitor

$G_{r,OL}$	open-loop transfer function for the SM reference voltage control of the dc/dc converter
G_1	transfer function that relates the battery current with the SM current in the LC filter
$G_{1,v}$	transfer function that relates the capacitor voltage with the SM current in the LC filter
G_2	transfer function that relates the battery current with the SM current in the CL-LC filter
$G_{2,v}$	transfer function that relates the capacitor voltage with the SM current in the CL-LC filter
$g_{u,i}$	upper arm gate signal for the i-th SM
$g_{l,i}$	lower arm gate signal for the i-th SM
G_w	plant transfer function of the dc/dc converter
$G_{w,OL}$	open-loop transfer function for controlling the battery current of the dc/dc converter
$I_{g,pu}$	maximum ac grid current (in pu)
I_{bat}	battery current in SM
$i_{bat,w/sup}$	RMS value of battery current with harmonic suppression
$i_{bat,w/osup}$	RMS value of battery current with no harmonic suppression
$i_{c,n}$	circulating current in n-phase
i_{dc}	dc-link current
$i_{u,n}$	upper arm current of n-phase
$i_{l,n}$	lower arm current of n-phase
$i_{g\alpha^*}$	grid current reference amplitude in α component
$i_{g\beta^*}$	grid current reference amplitude in β component
$i_{g\alpha}$	grid current amplitude in α component
$i_{g\beta}$	grid current amplitude in β component
$i_{g,n}$	grid current amplitude of n-phase

$i^*_{g,\alpha\beta}$	grid current reference
$i^*_{gq,\alpha\beta}$	grid current reference related to the reactive power transfer
$i^*_{gp,\alpha\beta}$	grid current reference related to the active power transfer
i^*_{arm}	instantaneous reference arm current
$\widehat{I}$	peak of grid current
$I^*_{arm,ac}$	ac peak reference arm current
$I^*_{arm,dc}$	dc reference arm current
$I_{IGBT,RMS}$	RMS value of IGBT current
$I_{Diode,RMS}$	RMS value of diode current
$I_{out,RMS}$	output current of full-bridge module
I_{SM}	Submodule input current
k_p	proportional gain of arm current control
$k_{p,w}$	proportional gain of dc/dc converter control
$k_{p,r}$	proportional gain of dc/dc resonant control
k_i	proportional gain of arm current control
$k_{i,w}$	integral gain of dc/dc converter control
$k_{i,r}$	integral gain of dc/dc resonant control
$k_{r,dc}$	resonant gain of dc/dc converter control
$k_{r,1}$	resonant gain of arm current control
$k_{r,2}$	resonant gain of arm current control
L_{arm}	arm inductance
L_b	series inductance in LC filter
L_{em}	MPE coupling inductance
L_f	inductance of LC low-pass component in CL-LC filter
L_{grid}	grid inductance
L_{max}	maximum inductance requirement

L_{min}	minimum inductance requirement
L_r	inductance of LC tuned branch in CL-LC filter
m	Modulation amplitude index
$m_{u,n}$	n-phase upper modulation index
$m_{l,n}$	n-phase lower modulation index
nc	number of battery cycles
$n_{u,n}$	upper arm insertion index of n-phase
$n_{l,n}$	lower arm insertion index of n-phase
N	number of SMs per arm
$N_{s,bat}$	number of batteries in series per string
$N_{p,1}$	number of strings per submodule based on power criterion
$N_{p,2}$	number of strings per submodule based on energy criterion
N_p	number of strings per submodule
$P_{B,n}$	BESS nominal active power
$p_{l,n}$	instantaneous active power of n-phase in lower arm
$p_{u,n}$	instantaneous active power of n-phase in upper arm
$p_{g,n}$	instantaneous active power of n-phase
$\overline{p}_{g,n}$	dc component of instantaneous active power of n-phase
$\widetilde{p}_{g,n}$	ac component of instantaneous active power of n-phase
P_n	MMC rated active power
P_{BESS}	instantaneous BESS power
P^*_{BESS}	reference of instantaneous BESS power
P_g	instantaneous grid power
P_{PV}	instantaneous PV plant power
$p_{u,n}$	instantaneous active power of n-phase in upper arm
Q_n	MMC rated reactive power

R_{arm}	arm inductor resistance
R_{bat}	battery resistance
$R_{bat,em}$	MPE battery internal resistance
R_{bld}	bleeder resistance
R_c	equivalent series resistance of capacitor in LC filter
R_{damp}	damping resistance in LC filter
$R_{d,CL-LC}$	damping resistance in CL-LC filter
R_{em}	equivalent series resistance of MPE coupling inductance
R_f	equivalent series resistance of LC low-pass inductance in CL-LC filter
R_{grid}	grid resistance
R_r	equivalent series resistance of LC tuned branch capacitance in CL-LC filter
R_{sm}	equivalent series resistance of SM capacitor in CL-LC filter
R_{ESR}	equivalent series resistor
S_1	top IGBT of full-bridge converter right arm
S_2	bottom IGBT of full-bridge converter right arm
S_3	top IGBT of full-bridge converter left arm
S_4	bottom IGBT of full-bridge converter left arm
S_i	top IGBT of half-bridge converter
S_j	bottom IGBT of half-bridge converter
S_b	power base for per unit computation
S_n	MMC rated power
SOC^*_{avg}	average SOC reference of the leg-balancing control
$SOC^*_{n,avg}$	average SOC reference in phase n
$SOC_{n,diff}$	difference between the average SOC of the upper and the lower arms
$SOC_{j,avg}$	average SOC of the leg-balancing control for the j-phase

SOC_{max}	maximum SOC operation
SOC_{min}	minimum SOC operation
$SOC_{u,i}$	upper arm SOC value for the i-th SM
$SOC_{l,i}$	lower arm SOC value for the i-th SM
S_T	bypass switch
T	sampling time
T_a	ambient temperature
t_{cal}	time that battery stay in idling mode
T_B	battery temperature
T_j	junction temperature
T_{rr}	time that the PV power fluctuation reaches the minimum value
$t_{on,1}$	on-time for IGBT S_1 in full-bridge converter
$t_{on,3}$	on-time for IGBT S_3 in full-bridge converter
$t_{on,5}$	on-time for IGBT S_5 in half-bridge converter
$T_{sw,MPE}$	switching time of full-bridge converter
$\widehat{V}$	peak of grid voltage
$\widehat{V}_g$	peak of the line-to-line grid voltage
$v_{c,n}$	DSHB internal voltage of n-phase
V_C	SM capacitance-voltage in LC filter
$V_{C,max}$	maximum SM capacitor voltage ripple
$V_{C,min}$	minimum SM capacitor voltage ripple
$V_{C_{sm}}$	SM capacitance-voltage in CL-LC filter
V_{dc}	MMC dc-link voltage
$v_{dc,em}$	dc-link voltage emulator
$V_{dc,l}$	MMC lower dc-link voltage
$V_{dc,mod}$	dc-link voltage of full-bridge module

$V_{dc,u}$	MMC upper dc-link voltage
$V_{dc,min}$	minimum dc-link voltage
V_{IGBT}	IGBT collector-emitter voltage
v_{fb}	full-bridge output voltage
v_{hb}	half-bridge input voltage
v_{hb}^{*}	half-bridge input reference voltage
$V_{L,min}$	minimum arm inductor voltage ripple
$V_{L,max}$	maximum arm inductor voltage ripple
V_{nom}	capacitor rated voltage
$v_{g\alpha}$	grid voltage amplitude in α component
$v_{g\beta}$	grid voltage amplitude in β component
$v_{g,d}^{+}$	positive sequence of grid voltage in direct axle component
$v_{g,d}^{-}$	negative sequence of grid voltage in direct axle component
$v_{g,q}^{+}$	positive sequence of grid voltage in quadrature component
$v_{g,q}^{-}$	negative sequence of grid voltage in quadrature component
$v_{g,n}$	grid voltage of n-phase
$v_{g,n}^{*}$	grid voltage reference of n-phase
V_g	phase RMS grid voltage connected to MMC
$V_{g,l-l}$	line-to-line RMS grid voltage connected to MMC
v_{sm}	SM voltage
$v_{s,n}$	line-to-neutral DSHB voltage
V_m^{*}	Measuring output voltage
$v_{sm,n}^{i}$	i-th SM voltage of n-phase
V_{sm}^{*}	SM reference voltage
$V_{out,RMS}$	output voltage of full-bridge module
$v_{u,n}$	upper arm voltage of n-phase

$v_{l,n}$	lower arm voltage of n-phase
X_b	impedance of series inductance in LC filter
X_f	impedance of series inductance in CL-LC filter
X_r	impedance of inductance in LC tuned branch
x_{pu}	per unit equivalent output impedance of the inverter
α_C	percentage of LC capacitance in CL-LC filter
δ	grid voltage angular displacement
δ_g	voltage margin
ΔI_{arm}	maximum arm current ripple
$\Delta I_{arm,\%}$	maximum arm current ripple in percent
$\Delta I_{arm,1}$	arm current ripple for S_1 ON and S_5 OFF
$\Delta I_{arm,2}$	arm current ripple for S_1 OFF and S_5 ON
$\Delta I_{arm,3}$	arm current ripple for S_1 OFF and S_5 OFF
$\Delta I_{arm,4}$	arm current ripple for S_1 ON and S_5 ON
$\Delta T_{bat,w/sup}$	battery temperature variation with harmonic suppression
$\Delta T_{bat,w/osup}$	battery temperature variation with no harmonic suppression
$\Delta V_{L_{max}}$	maximum voltage ripple in series inductor filter
$\Delta V_{L_{min}}$	minimum voltage ripple in series inductor filter
$\Delta V_{C_{max}}$	maximum voltage ripple in SM capacitance
$\Delta V_{C_{min}}$	minimum voltage ripple in SM capacitance
ΔV_g	maximum ac grid voltage variation in pu
ϕ_g	displacement angle of the output current
ϕ_n	displacement angle of the output current in n-phase
ϕ_m	phase margin of arm current control
θ_v	angular displacements of grid phase
$\theta_{u,n}$	angular displacements of the upper carrier waveforms

$\theta_{l,n}$	angular displacements of the lower carrier waveforms
ω_g	grid angular frequency
ω_n	natural angular frequency
$\omega_{r,1}$	resonant angular frequency
$\omega_{r,2}$	resonant angular frequency
ω_s	angular sampling frequency
ξ	damping ratio

Superscripts

$*$	reference value
i	i-th
PV	photovoltaic

Subscripts

a	phase a
b	phase b
c	phase c
u	upper arm
l	lower arm

Contents

1 Introduction

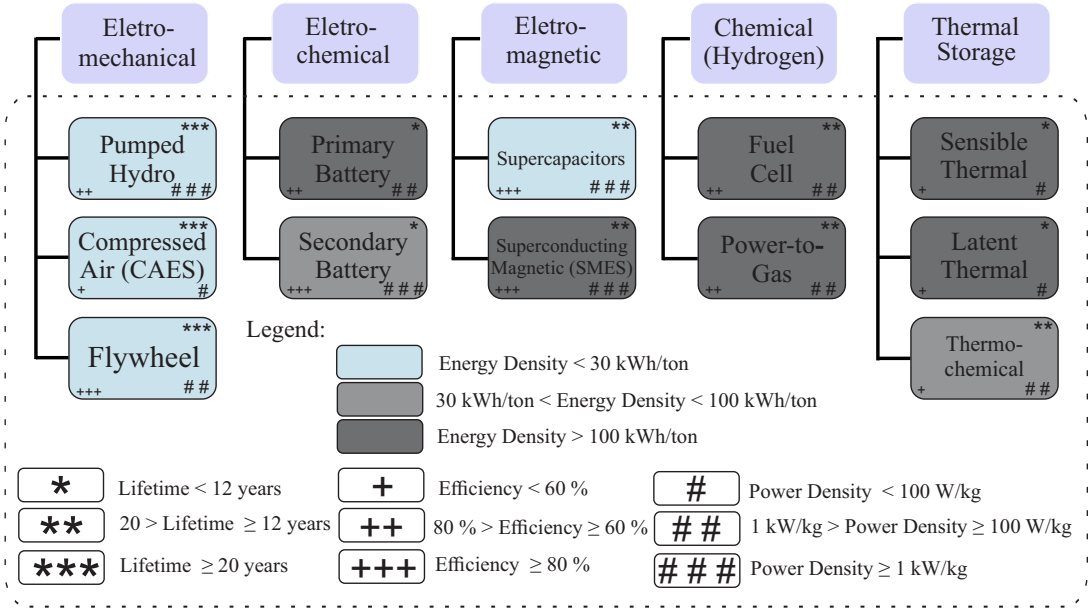
1.1 Energy Storage Systems

Energy storage systems (ESS) have become, in recent decades, an important solution to support the processes of generation and consumption of electricity (Saqib; Saleem, 2015; Babatunde; Munda; Hamam, 2019). Guaranteeing the improvement of the power systems at different levels of production through ESS, enabled a revolution in human activities, whether in industry, in the generation of electrical energy, or even in electro-portable equipment (Twidell, 2021). In this sense, numerous forms of storage have been developed based on natural phenomena, such as gravitational force, chemical reactions, thermal reactions, and magnetic field, among others (Chen et al., 2009; Silva, 2018). One of the first ways was the water storage in dams and hydroelectric plants, which allowed the control of electricity generation by controlling the water flow (Babatunde; Munda; Hamam, 2019; Díaz-González; Sumper; Gomis-Bellmunt, 2016). Despite the operational and financial advantages, these systems depend on the climatic conditions that regulate the flow of water in the region (Babatunde; Munda; Hamam, 2019; Posso Rivera et al., 2022). Other storage solutions were developed based on mechanical interactions and chemical, thermal, and electrical reactions.

Fig. 1 presents the main energy storage technologies for integration into the grid and provision of ancillary services. (Chen et al., 2009). ESS technologies are particularly interesting in dealing with a high energy density, which is the amount of energy that can be stored in a defined mass or volume. Fig. 1 highlights, among the types of ESS, technologies with emphasis on high energy density (above 100 kWh/ton), such as technologies based on thermal storage, chemical reactions of hydrogen gas, Superconducting Magnetic Energy Storage (SMES), and electrochemical technologies (especially the primary batteries and some secondary battery technologies) (Rebours et al., 2007). In addition, power density aspects are also evaluated, highlighting ESS such as pumped hydro, secondary batteries, supercapacitors, and SMES, which have power density greater than 1 kW/kg. The high value of energy and power density is essential for all mobility applications, stationary systems, and electro-portable devices, among others (Rufer, 2018). Finally, the lifetime and efficiency aspects are compared for the different types of ESS, where the flywheel, secondary battery, supercapacitors, and SMES technologies stand out with system efficiency greater than 80 % and the pumped hydro ESS technologies and flywheel stand out for their long lifetime of more than 20 years.

Despite the operational characteristics of ESS, it is worth noting that the ESS integrated into the grid can offer so-called ancillary services to the power system, to

Figure 1 – Energy storage technologies detailed according to the typical energy density.



Source: Adapted from (Hossain et al., 2020).

improve aspects of power quality and enable the flow of excess power (or lack) in the system, especially when applied in Renewable Energy Systems (RES) (Denholm et al., 2010; Rebours et al., 2007). This central role of energy intermediary reveals the growing application of ESS in power systems, which can substantially increase the reliability of these systems (Rebours et al., 2007; Rufer, 2018).

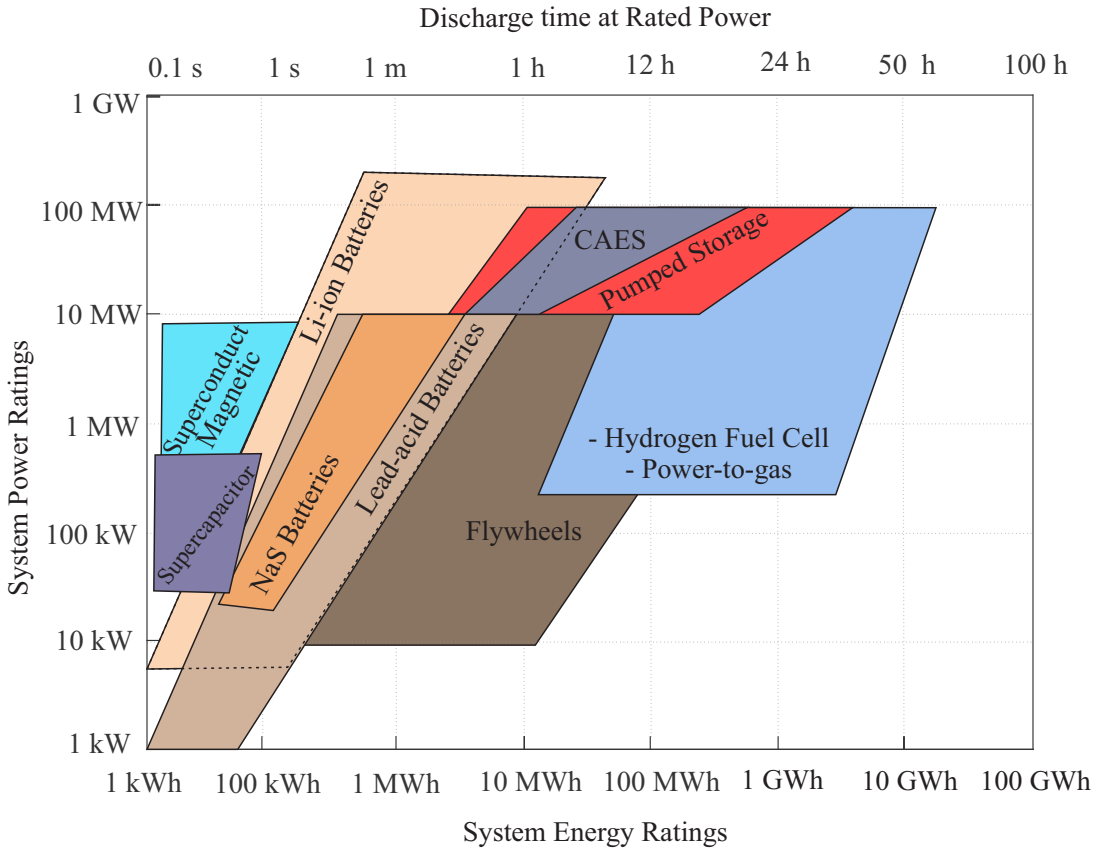
The choice of storage technologies has advantages and disadvantages in terms of their type of application. In this way, the use of a certain technology as a storage solution for a system requires the evaluation of several variables to be analyzed in a project. Factors such as system power level, autonomy time, costs, and performance are crucial for decision-making for a given technology (Argyrou; Christodoulides; Kalogirou, 2018; Barros et al., 2024). In summary, these factors can be listed in the following items:

- Investment costs (Capital expenditure (CAPEX) and operational expenditure (OPEX));
- Application (mobility, stationary systems, RES, among others.);
- Power, energy, and discharge time;
- Lifetime and reliability;
- Weight and volume.

Once the desirable characteristics of the system have been defined, the next step would be to evaluate the storage technology to be used. Fig. 2 illustrates some

of the technologies used in storage systems about their applicability in low, medium, and high-power electrical systems, in addition to evaluating their applicability as a function of discharge time at rated power.

Figure 2 – Application ranges of energy storage technologies based on discharge time at rated power and system power ratings.



Source: Adapted from (ITRE, 2015; Hossain et al., 2020).

Among the storage technologies presented in Fig. 2, batteries stand out as a storage solution, due to their wide application range in terms of application from low to medium power, as well as the complete discharge time of some hours, which comprises most typical grid-connected systems, such as renewable generation sources and residential and industrial loads (Díaz-González; Sumper; Gomis-Bellmunt, 2016). As verified, the pumped storage and Compressed Air Energy Storage (CAES) technologies stand out with high operating power and discharge time values, despite dealing with energy density problems, which require large spaces for installation, as well as aspects of security and environment.

In addition, the battery technologies have considerable system autonomy (verified by the discharge time). Among the operational advantages of batteries in ESS, nominated as Battery Energy Storage System (BESS), is the high energy density, high efficiency, low operating response time, quick installation, and no emission of pollutants during operation (Baker; Collinson, 1999). In this sense, the modularity, customization, and portability of batteries reveal the wide application of batteries in electrical systems (Rufer, 2018;

BLOOMBERGNEF, 2023). In addition, BESS offers some attractive advantages regarding other ESS, such as one of the fastest response times (generally, in the order of tenths of a second), making the BESS able to offer important services in the power system (transmission, distribution, and consumer) (Twidell, 2021; IEA, 2023; Horiba, 2014).

An ESS technology highlighted in recent years refers to the use of hydrogen fuel cells. Niaz et al. (2024) discusses the scenario of reducing the use of renewable energy (wind and solar) through three cases: Case 1 - BESS, Case 2 - alkaline water electrolyzer (AWE) for hydrogen energy, and Case 3 - a hybrid system (BESS and AWE). Sensitivity analysis highlights the crucial role of technology costs, suggesting ways to reduce expenses. The study guides effective energy reuse, considering the evolution of technology costs, having the best operating scenario and payback in case study 2, and average performance in case study 3.

Despite the relatively positive aspects of BESS, compared to most ESS, batteries present certain characteristics that reveal operational challenges. Firstly, a significant disadvantage of batteries lies in their relatively limited lifetime. Over time, batteries gradually lose their ability to store energy, resulting in reduced performance and shorter usage times (Hossain et al., 2020). This decline is explained by the phenomenon of "chemical aging", which is associated both with the charging and discharging process and with the battery idle operation. Furthermore, the materials used in batteries, such as lithium-ion (Li-ion), are harmful to the environment (Chen et al., 2009). Improper disposal can lead to the release of toxic substances, such as heavy metals, into the environment, posing a threat to human health and the ecosystem.

A sensitive issue concerning Li-ion batteries refers to the disposal and recycling of waste arising from batteries that have reached the end of their lifetime. The International Energy Agency, for example, estimates that electric vehicles produced in 2019 alone will generate 500,000 tons of waste, and the total amount of waste generated by 2040 could reach 8 million tons (Baum et al., 2022).

Due to the complex structure and number of materials in Li-ion batteries, they must be subjected to a variety of processes before reuse/recycling. Batteries must first be sorted and, most often, treated through discharge or inactivation, disassembly, and separation, after which they can be subjected to direct recycling, pyrometallurgy, hydrometallurgy, or a combination of methods (Baum et al., 2022; Hu et al., 2022).

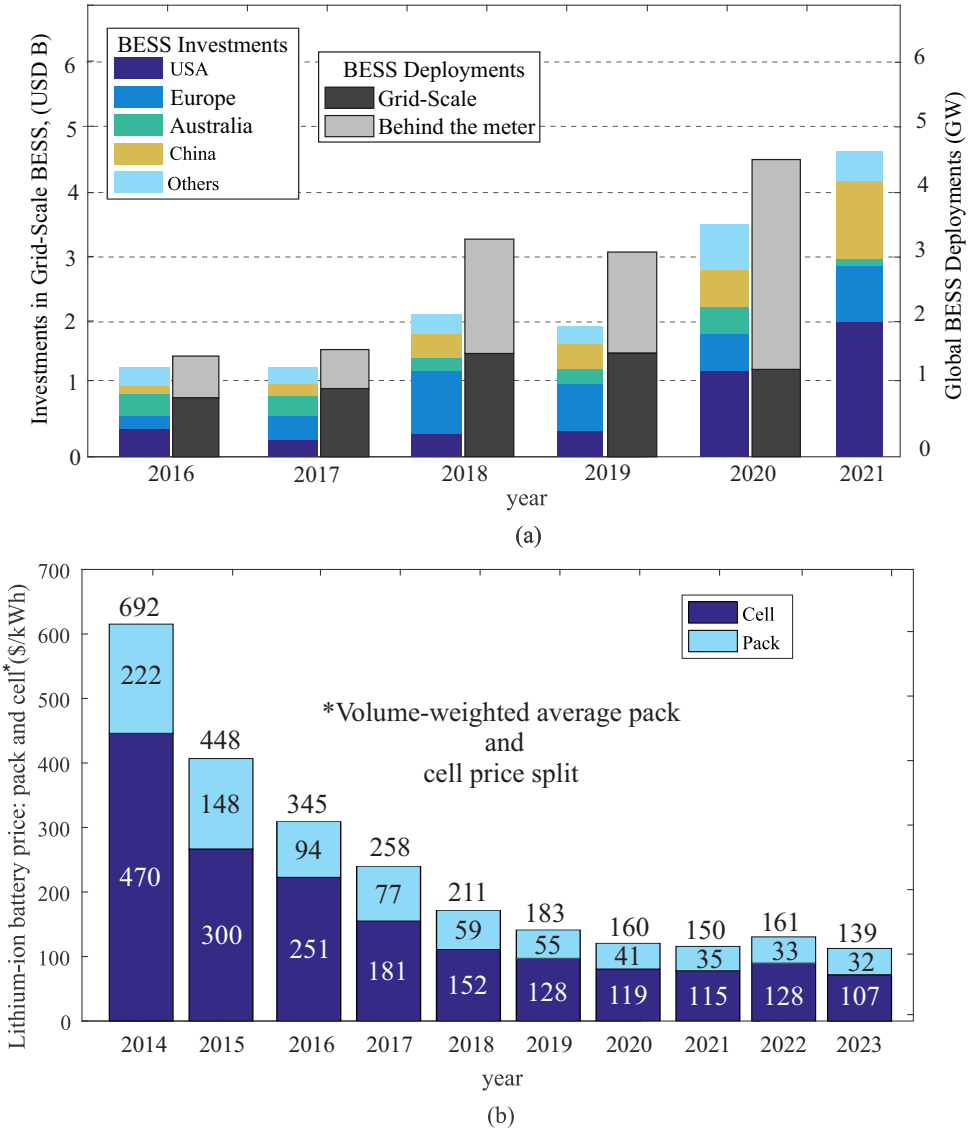
Lithium is the most frequently recovered element, followed by metals in the following order: Co, Ni, Mn and Fe. The trend is in line with the price differences between metals. In addition to economic motivations, the high publication volume of papers regarding Lithium recovery can likely be attributed to the prevalence of Li technology (Baum et al., 2022).

Finally, it is worth highlighting the cooling requirement. Battery conditioning rooms rely on air conditioning systems to maintain batteries at an ideal operating temperature of 20°C-25°C (ITRE, 2015). Typically, for every 10°C above this operating temperature, battery lifetime is halved (ITRE, 2015).

1.1.1 Battery Energy Storage Systems

BESS has the potential to become a key part of modern electrical power systems. This fact is evident by the growing investments of electrical system operators, electric vehicle assemblers, and large electrochemical cell manufacturing companies (Denholm et al., 2010). Fig. 3 (a) presents data referring to investments in storage systems for grid-scale stationary applications (BNEF, 2023; IEA, 2023).

Figure 3 – BESS increasing in terms of installation and price. (a) Utility-scale energy storage capacity in last years (b) Li-ion battery price in last years.



Source: Adapted from (BNEF, 2023; IEA, 2023).

The scenario for the year 2021 reveals a global investment of more than 4 billion dollars, with highlights for initiatives from the USA, European countries, China and Australia. Compared with the investment in BESS in 2016, there is an increase of more than 300% in a 5-year window. Additionally, regarding the BESS deployment, in 2020, more than 4 GW of installed power was verified among grid-scale and behind-the-meter (power that is produced and consumed on-site) applications. The latter stands out due to the large mobility market for electric vehicles in recent years, responsible for increasing the popularization of secondary batteries in the market, favoring aspects such as price (Loganathan et al., 2019), shown in Fig. 3 (b).

In this sense, the price composition of the lithium-ion (Li-ion) battery shown in Fig. 3 (b) is given for the electrochemical pack and cell. In the nine-year window, a reduction of more than 79% in the total price of a Li-ion battery is observed, totaling a value in the year 2023 equal to 139 $/kWh. The significant reduction presented in the price of this technology, with the new challenges of modern electrical systems, led to the first initiatives to diffuse BESS in power systems (Lawder et al., 2014). This fact can be explained in the scenario of high penetration of RES, where BESS plays a key role in the efforts to combine a sustainable energy source with reliable dispatched loads and to mitigate the impacts of the intermittent sources (Chatzinikolaou; Rogers, 2017; Lawder et al., 2014; REN23, 2023).

It is worth mentioning that in the period between 2021 and 2022, there was a change in the scenario about the price of batteries. Rising prices for raw materials and battery components (after more than a decade of declines) have seen volume-weighted average prices for lithium-ion batteries across all sectors rise to $151/kWh in 2022, an increase of 7% compared to 2021 (BLOOMBERGNEF, 2023). Rising pressure on battery costs has outpaced the increased adoption of low-cost chemicals such as lithium iron phosphate (LFP) (BLOOMBERGNEF, 2023). After unprecedented price increases in 2022, Li-ion battery prices have fallen again in 2023. The price of Li-ion batteries has fallen 14% to a record low of $139/kWh. This was driven by falling raw material and component prices as production capacity increased across all parts of the battery value chain, while demand growth fell short of expectations in some industries.

Many companies that deal with the manufacture and execution of BESS have been specializing and commercializing this storage technology in several countries around the world (Xavier; Cupertino; Pereira, 2018; Xavier et al., 2019). For example, companies like Tesla, ABB, Samsung, AES, Hyundai, Moura, Unicoba, WEG, and Siemens offer BESS solutions for sale. Tab. 1 summarizes some of the main grid-scale BESS among the largest in terms of power capacity and installed energy in the world. The largest battery bank is located in the state of California, USA, and comprises a system of more than 400 MW and 1.6 GWh, installed by the manufacturer Tesla (DOE, 2022).

Table 1 – Examples of BESS projects in operation providing power systems services (Based on (DOE, 2022)).

BESS Project	Ancillary Service	Rated Power and Energy	Manufacturer
California, USA	Transmission Relief and Backup Power	400 MW and 1.6 GWh	Tesla
Florida, USA	Time-shift and Backup Power	8.5 MW and 14.2 MWh	Tesla
California, USA	Power Reliability and Ramp Control	140 MW and 561 MWh	Tesla
Moorabool, Australia	Time-shift and Backup Power	300 MW and 450 MWh	Tesla
Wiltshire, UK	Ramp Support and Backup Power	150 MW and 266 MWh	Samsung
Ulsan, Korea	Backup Power	32.5 MW and 150 MWh	Hyundai
Hawaii, USA	Frequency Regulation and Ramp Support	203 MW and 203 MWh	AES

In particular, the state of California connected several BESS in the power system with significant installed power and energy, due to the high penetration of RES in the state power generation matrix, which caused frequent blackouts in the last decade (IEEE Spectrum, 2018; DOE, 2022). For example, manufacturer Tesla was responsible for the installation of different BESS in California state and other states of the USA, and countries around the world, such as Australia. This can be explained due to the great efforts of the company and well-known commercial lines, such as the Tesla PowerPack (Tesla, 2018), which facilitates the construction of a large-scale system for BESS.

The examples presented in Tab. 1 include BESS which employs Li-ion battery technology, being one of the most promising and currently applied, especially in the electric vehicle market and stationary applications (Horiba, 2014). Out of curiosity, in 2019, the Nobel Prize in chemistry was awarded to three scientists: John B. Goodenough (American), M. Stanley Wittingham (British), and Akira Yoshino (Japanese) for the development of the Li-ion battery, which is widely used in portable electronic equipment, electric vehicles, and BESS, among others (Nobel Prize, 2019). On the other hand, other technologies are applied with a similar degree of maturity, such as Lead-Acid (Pb-acid), Sodium sulfur (NaS), flow batteries, and Nickel Cadmium (NiCd) (Nwaigwe; Mutabilwa; Dintwa, 2019). The difference between these technologies is in terms of charging and discharging efficiency, cost per cycle, lifetime, and energy density (Barnes; Levine, 2017).

In the Brazilian context, some companies that deal with the manufacture and execution of BESS have been specializing and commercializing this storage technology around the country. For example, companies like Tesla, WEG, ISA CTEEP, with the

support of some Chinese manufacturers offer BESS solutions for the market. Tab. 2 summarizes some of the main grid-scale BESS among the largest in terms of power capacity and installed energy in Brazil. A limitation of installed capacities is perceived, compared with the projects in the Tab. 1, but with great prospects for increasing scale in terms of power and energy for new projects (Lima; Rabello, 2023).

Table 2 – Examples of BESS projects in operation providing power systems services in Brazil (Based on (Lima; Rabello, 2023)).

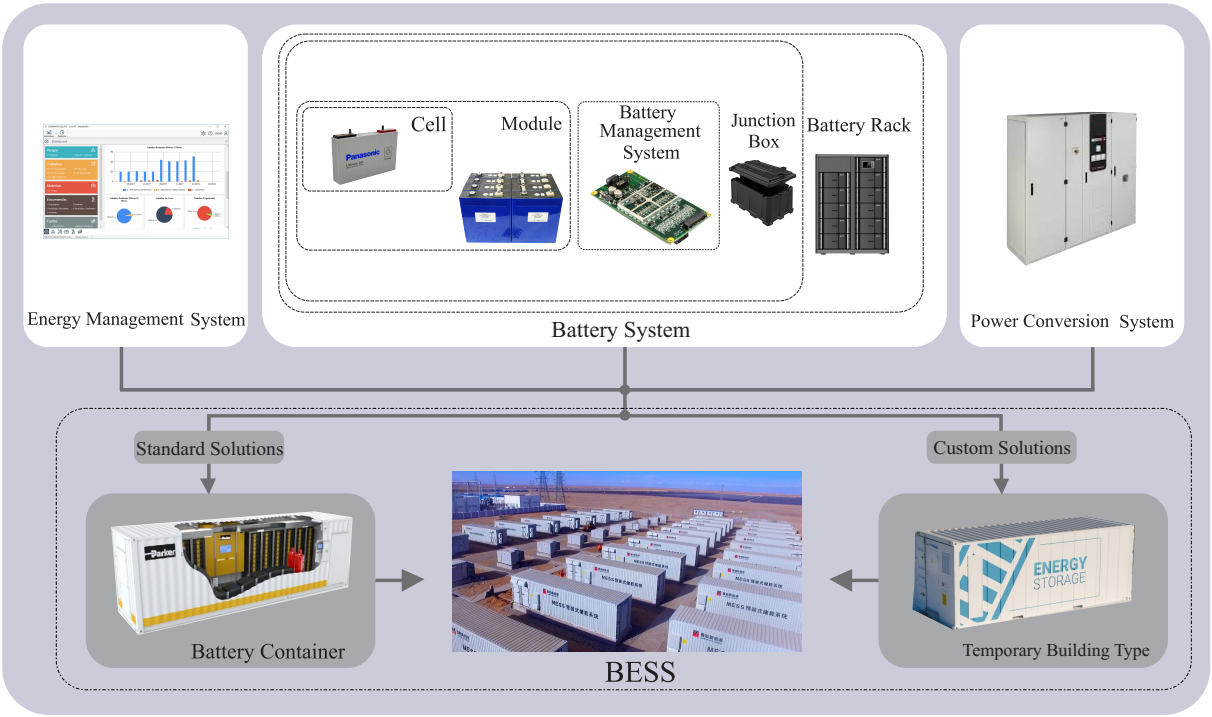
BESS Project	Ancillary Service	Rated Power and Energy	Manufacturer
Registro, SP	Peak Shaving	30 MW and 60 MWh	You.On Energia
Ilha Guaíba, RJ	Peak Shaving	10 MWh	Tesla
Ipiranga, PR	Voltage Support and Ancillary Services	500 kW and 2 MWh	WEG
Tubarão, SC	Frequency Regulation and Ramp Support	1 MW and 1.096 MWh	WEG
Curitiba, PR	Grid Support and Backup Power	1 MW and 1 MWh	WEG
Alcântara, MA	Microgrid and Rocket Launch Support	1 MW and 1 MWh	WEG
Belo Horizonte, MG	Support Volt/Var and Peak Shaving	750 kW and 1.1 MWh	WEG
Belo Horizonte, MG[1]	Support Volt/Var and Peak Shaving	400 kW and 750 kWh	Moura
Fernando de Noronha PE	PV Support and Electric Mobility	100 kW and 215 kWh	WEG
Ilha das Cobras, PR	Off-grid Microgrid	75 kW and 150 kWh	WEG

The Li-ion battery stands out among the others, which has led to its wide application in current BESS grid-scale projects (Argyrou; Christodoulides; Kalogirou, 2018). It is worth noting a central feature of these battery technologies mentioned, which fall into the category of secondary batteries, guaranteeing the ability to recharge the battery with the circulation of reverse electrical current in its terminals (as opposed to the primary batteries that are not rechargeable) (Argyrou; Christodoulides; Kalogirou, 2018). In this sense, the recharging capacity is fundamental for the wide expansion and operation of current BESS systems.

Fig. 4 presents a typical schematic of a BESS, emphasizing the constituent parts, from the electrochemical cell to the final composition of the BESS (ADB, 2018). The basic storage unit is formed by the electrochemical cell and is associated with several units in

[1] The battery technology of this project is lead carbon (PbC). For other projects, Lithium-ion technology was adopted.

Figure 4 – Schematic of a Battery Energy Storage Systems.



Source: Adapted from (ADB, 2018).

series (increasing the operating voltage) and rows in parallel (increasing the capacity of power and energy), forming the so-called battery module. This last unit is controlled by the battery management system (BMS), which controls the module electrical and thermal quantities, such as State-of-Charge (SOC), current, temperature, and voltage, to ensure operation in a safe region (Silva, 2018). For mechanical and thermal protection purposes, the BMS and module are terminated by the junction box. The set formed is then called a battery, which consists of a larger unit with well-defined electrical characteristics, such as current, voltage, and stored energy.

In power systems that deal with greater power and energy needs, it is necessary to increase the capacity range of a single battery. In this sense, these batteries are combined into a larger unit, called a battery rack. The latter is formed by the association of batteries in series and strings of batteries in parallel, increasing the terminal voltage and stored energy. To connect the battery system to the power system, a Power Converter System (PCS) is required to ensure the integration of voltage levels as well as the conversion of direct current (dc[1]) to alternating current (ac). Furthermore, an Energy Management System (EMS) is also used to ensure the mentioned electrical and thermal characteristics for each battery rack in a safe operating region indicated by the manufacturer (Lawder et al., 2014).

[1] The acronyms used in this work follow standards provide the recommended abbreviations, symbols, and units for IEEE publications.

The battery systems, EMS, and PCS are installed in a larger footprint, such as a container, for the allocation of other systems, such as the Heating, Ventilating, and Air Conditioning (HVAC) system, for thermal management purpose (Rufer, 2018). Finally, in a power system, the set formed by several battery containers makes up the so-called BESS, which can be a standard solution or custom solution, according to the manufacturer catalog.

1.2 Ancillary Services provided by BESS

BESS can be sited at three different levels of the power system: behind the meter, at the distribution level, or the transmission level (Krishnamoorthy et al., 2014; Fitzgerald et al., 2015). Energy storage deployed at all levels of the electricity system can add significant grid improvements (Velasco de la Fuente et al., 2013; Chivukula; Maiti, 2019). For example, the customer can benefit from the services, such as backup power and demand charge reduction, even though the BESS deployed behind the meter is not always the lowest cost option among ESS or other technical solutions (Farivar et al., 2023; Zhang et al., 2024).

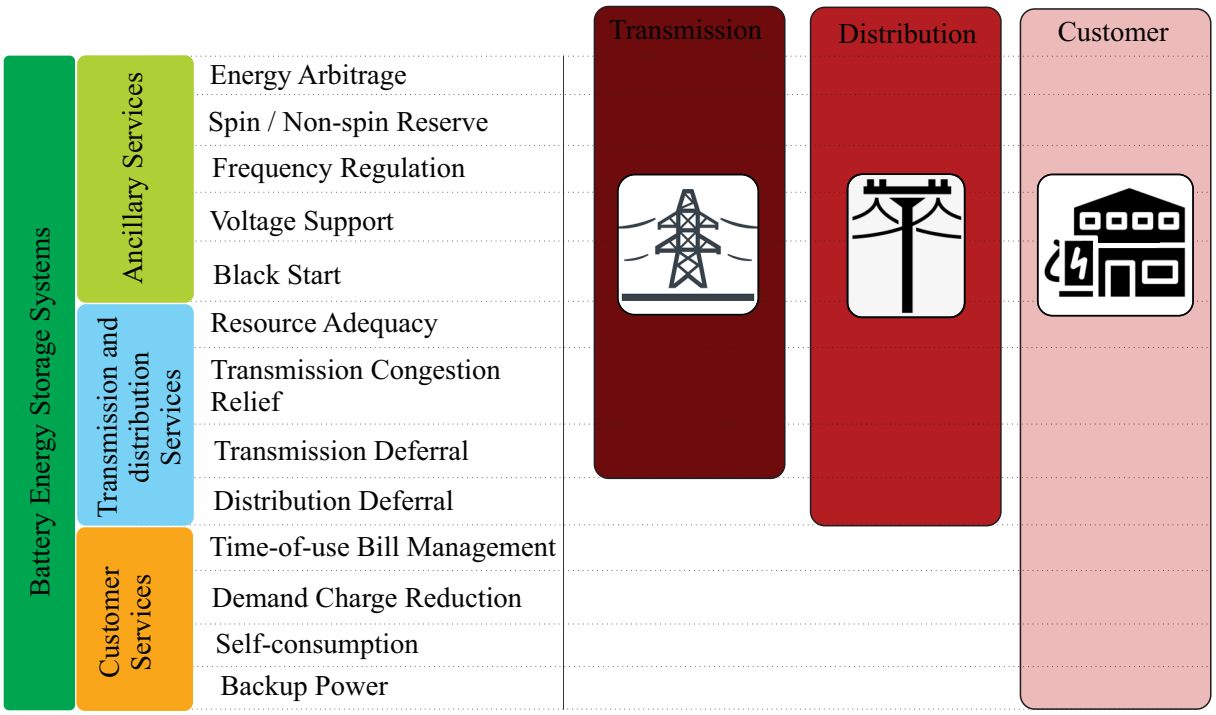
Furthermore, customer-sited storage is optimally located to provide an important energy storage service: backup power, ensuring system autonomy in situations of grid failure (Xu et al., 2015; Soong; Lehn, 2016; Krata; Saha, 2019). Accordingly, regulators, utilities, and operators should look into the power system when examining the economics of BESS and analyzing how those economics change depending on where energy storage is deployed on the grid, such as at the distribution or the transmission level. (Serban; Marinescu, 2014; Arifujjaman, 2015).

Several studies have been conducted on the different services that BESS can provide to the grid. The number of BESS services that can be provided and the definitions of those services vary across literature (Fitzgerald et al., 2015; Sigrist; Lobato; Rouco, 2013). Fitzgerald et al. (2015) proposes to divide the thirteen services that BESS can provide according to the power system segment that receives the service performed by the BESS. The segments are the transmission system, distribution system, and customers.

Fig. 5 presents some of the typical services performed by BESS in the power systems, noting that some services can benefit more than one group. Since BESS can be sited at three different levels: behind the meter, at the distribution level, or at the transmission level, a listing of typical services at each of these levels is presented:

- Transmission level: BESS is capable of providing a suite of services that largely benefit independent system operators (ISOs) and regional transmission organizations (RTOs). These services, outlined in Fig. 5, involve all typical ancillary services such as voltage support, frequency regulation, black start, energy arbitrage, and

Figure 5 – Typical BESS services in power system.



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spinning/non-spinning reserve. In addition, it can offer support in congested transmission lines, adequacy of resources, and its implementation deferral (Knap et al., 2016; Saqib; Saleem, 2015);

- Distribution level: The services that involve the power distribution system cover all the typical services applied in transmission lines. As an additional service, there is the possibility of deferral distribution lines. The typical distribution infrastructure upgrades are driven by peak demand events that occur on predictable occasions each year. On the distribution side, using incremental BESS to deal with limited time duration events can defer large investments and avoid oversizing the distribution system in the face of uncertain demand growth (Prasatsap; Kiravittaya; Polprasert, 2017; Garcia-Garcia; Paaso; Avendano-Mora, 2017; Walawalkar; Apt; Mancini, 2007);

- Customer level: Typical services employed in the transmission and distribution stages are directly reflected by customers. In addition, there are typical services employed behind the meter, such as backup power, self-consumption, and consumption aspects, such as time-of-use bill management and demand charge reduction. Furthermore, the provision of these services creates benefits for ISOs/RTOs and distribution levels, as well. When BESS maximizes the on-site consumption of local customers it reduces the building's peak demand charge, and smooths the peak load profile at distribution and transmission levels (Xavier et al., 2019; Fitzgerald et al., 2015).

In the following section, a summary of the types of power converters for BESS realization is summarized, according to the PCS function mentioned.

1.3 Power Converters for BESS Realization

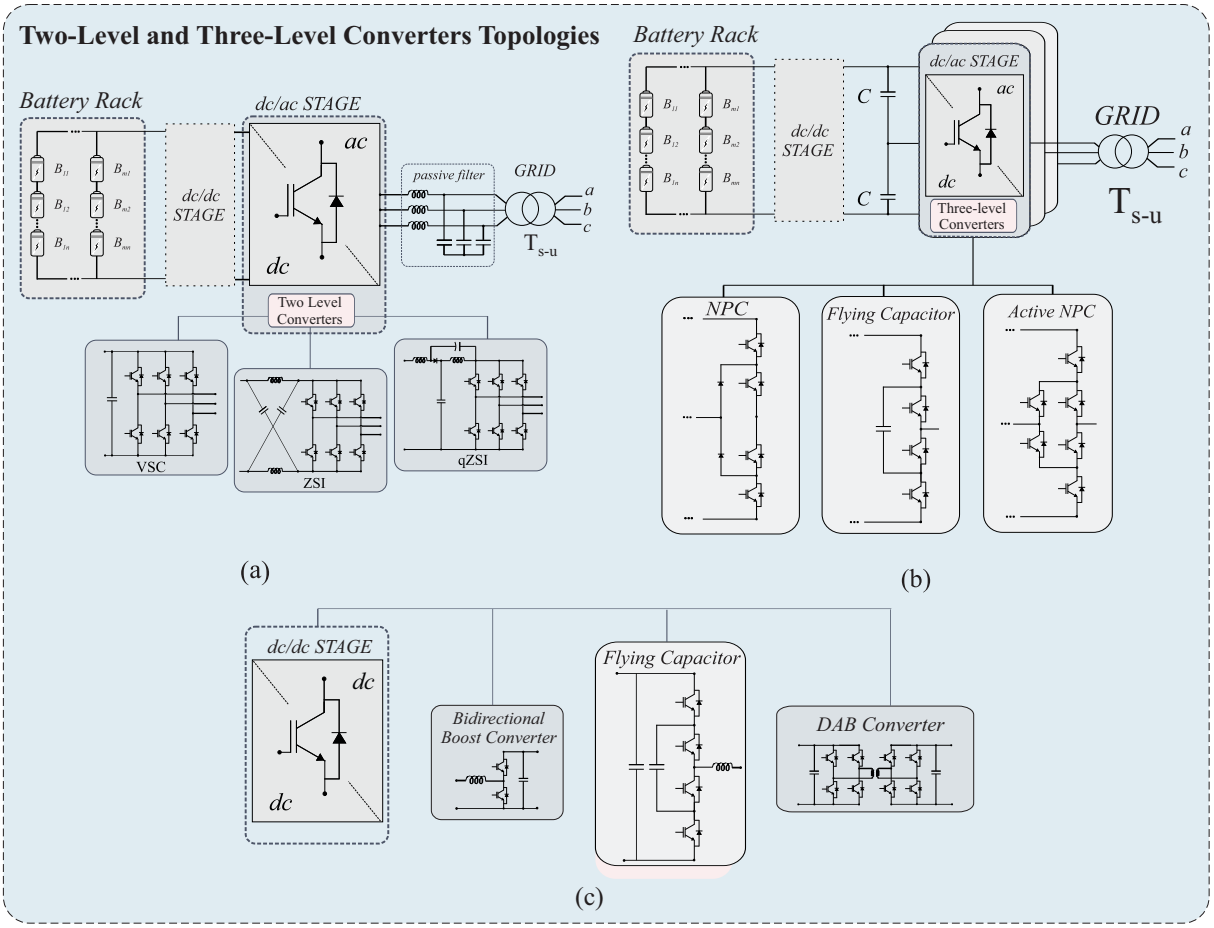
The major challenge for BESS integration with the power system is to design a converter topology that must handle high power and high voltages with standard semiconductor devices (Leon; Vazquez; Franquelo, 2017; Silva et al., 2010). Commercial semiconductor devices are limited in terms of the blocking voltage available, with values up to 6.5 kV for silicon-based devices (Chatzinikolaou; Rogers, 2017). Furthermore, the batteries provide dc voltage, which reveals the need for a PCS to carry out the energy conversion from dc to ac stage, enabling its connection to the grid. For these reasons, different PCS topologies applied in BESS have been developed and commercialized over the years, incorporating the classic topologies. Furthermore, recent research has made efforts in the realization of PCS applied in BESS, aiming for efficient and reliable topologies for low to high-voltage power systems. Therefore, this section aims to discuss the developments in the realization of PCS applied in BESS.

1.3.1 Two-level and Three-level Converters

The first applications of BESS were implemented using two-level voltage source converters for connection to the ac grid. The topology of the three-phase two-level converter with a step-up transformer is illustrated in Fig. 6 (a). As these converters have a limited number of output voltage levels, they require a relatively high switching frequency in their operation to handle the harmonic distortion requirements (Islam; Guo; Zhu, 2014). In this way, the high switching frequency results in high energy losses, which affects the efficiency of the converter (depending on the power level of the converter) and the heatsink requirement (Liu et al., 2013). Another impacting factor refers to the slope of the voltage derivative (dv/dt), which, due to the high value of the operating voltage, imposes significant stress on the insulation of any equipment connected to the ac terminal (Islam; Guo; Zhu, 2014). As an advantage of this topology, we can mention the simplicity of construction and operation of the converter, being mostly designed for low voltage applications (Islam; Guo; Zhu, 2014; Liu et al., 2013).

The VSC (Voltage Source Converter), ZSI (Z-Source Converter), and qZSI (quasi-Z-Source Converter), shown in Fig. 6 (a), are some of the traditional two-level converters for the dc/ac stage of PCS (Liu et al., 2013). In addition, for the grid connection, the use of a low-pass filter to attenuate the injected harmonics is generally adopted as LC or LCL filter configurations (Silva, 2018; Bellinaso et al., 2019). The transformer (T_{s-u}) is used to step up the low voltage (LV) from the inverter side to the medium or high voltage

Figure 6 – PCS technologies for BESS realization: (a) typical two-level converters: VSC, ZSI, and qZSI (b) typical three-level converters: NPC, Active NPC, and flying capacitor (c) typical dc/dc converter topologies: boost, DAB and FC converter.



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of the ac grid.

In the VSC configuration, the battery system can be connected directly to the dc/ac stage capacitor or connected through an intermediate dc/dc stage. The advantage of connecting the dc/dc stage is to ensure a smaller variation of the dc-link voltage, since current Li-ion battery technologies present typical voltage variations of the order of 30 % in their Open Circuit Voltage (OCV), depending on the maximum and minimum values of SOC (Gherard et al., 2020). In this way, the dc stage has the role of accommodating these voltage variations, consequently reducing the harmonics of the output voltage, ensuring a constantly high modulation index of the inverter, and reducing costs due to the oversizing of the battery bank (Gherard et al., 2020; Pinto et al., 2022).

The disadvantage of VSC topology is the possibility of operating only as a buck converter (Xavier et al., 2019). Therefore, the output voltage must be lower than the dc voltage. In this sense, the ZSI and qZSI topologies were designed to overcome these inherent disadvantages of the VSC topology (Peng, 2003). These converters can operate in

boost mode, because of the additional network with capacitors and inductors in the dc-link (Xavier et al., 2019). Despite the advantages of ZSI and qZSI, VSC is more commonly used due to its simplicity.

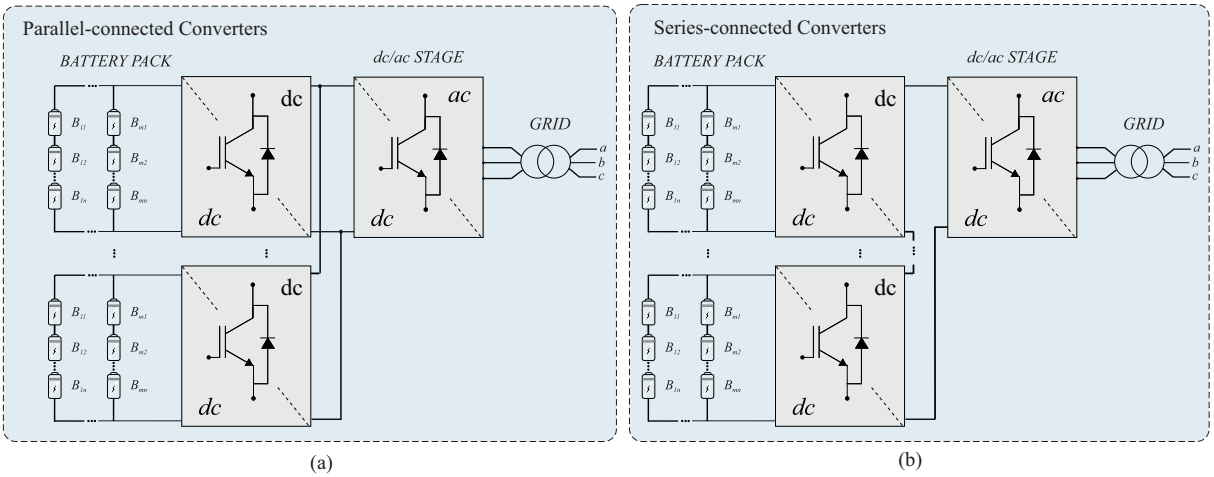
An alternative to overcome the limitations of two-level topologies in medium-voltage systems is the three-level converters, shown in Fig. 6 (b). These converters can employ current semiconductor device technologies to achieve high voltage capability on the converter output (Pou et al., 2005). Moreover, the multilevel converters have several advantages over the conventional two-level converters, such as lower switching frequency, lower voltage steps (dv/dt), a higher number of levels in the output voltage, and high power density, and low common-mode voltage (Pou et al., 2005; Xavier et al., 2019). On the other hand, these converters deal with a greater number of switching devices, dealing with the increase in switching and conduction losses (it is worth noting that this condition may change depending on the power, voltage, current, frequency, technology and manufacturer selected), as well as with the cost and complexity of the implementation (Mohamad; Teh, 2018). The NPC, Flying capacitor, and Active NPC topologies are some of the most used in the three-level converters category.

Fig. 6 (c) presents some typical topologies used in dc/dc converters to integrate the battery bank with the dc/ac converter. The bidirectional boost converter is one of the most traditional in the literature, due to its ease of implementation and operation (Pinto et al., 2022). The dual active-bridge converter (DAB) presents two full-bridge converters connected by a transformer that provides galvanic isolation between the two dc sides (Bragard et al., 2010; Pinto et al., 2022). In addition, it involves greater operating efficiency and output voltage gain. Finally, the flying capacitor converter handles high output voltage gain and lower energy losses (Bragard et al., 2010).

Despite the advantages presented for the two-level and three-level topologies, the semiconductor switches used in these converters present voltage and current limitations. In addition, BESS deals with the need to work at high levels of stored energy, which requires increasing the system current and voltage capacity. In this sense, the parallel association of a battery bank is adopted to increase the energy and power storage capacity of BESS, connecting each battery bank to a dc/dc converter and, in turn, all connected to a central dc/ac converter, as presented in Fig. 7 (a).

Furthermore, it is also possible to increase the voltage level of the dc-link of the central dc/ac converter to increase the output voltage, using switches with lower blocking voltage. Again, each battery bank is connected to a dc/dc converter which connects to the central dc/ac converter by connecting the output terminals of the dc/dc converters in series, as shown in Fig. 7 (b). On the other hand, although the dc/dc stages allow flexibility in adjusting the power and voltage of the dc-link, the blocking voltage of the semiconductors of the dc/ac converter still limits the level of ac voltage generated, forcing

Figure 7 – Association of dc-dc converters in two-level or three-level topology to improve BESS voltage and power: (a) parallel-connected converters (increase BESS power). (b) series-connected converters (increase output voltage).



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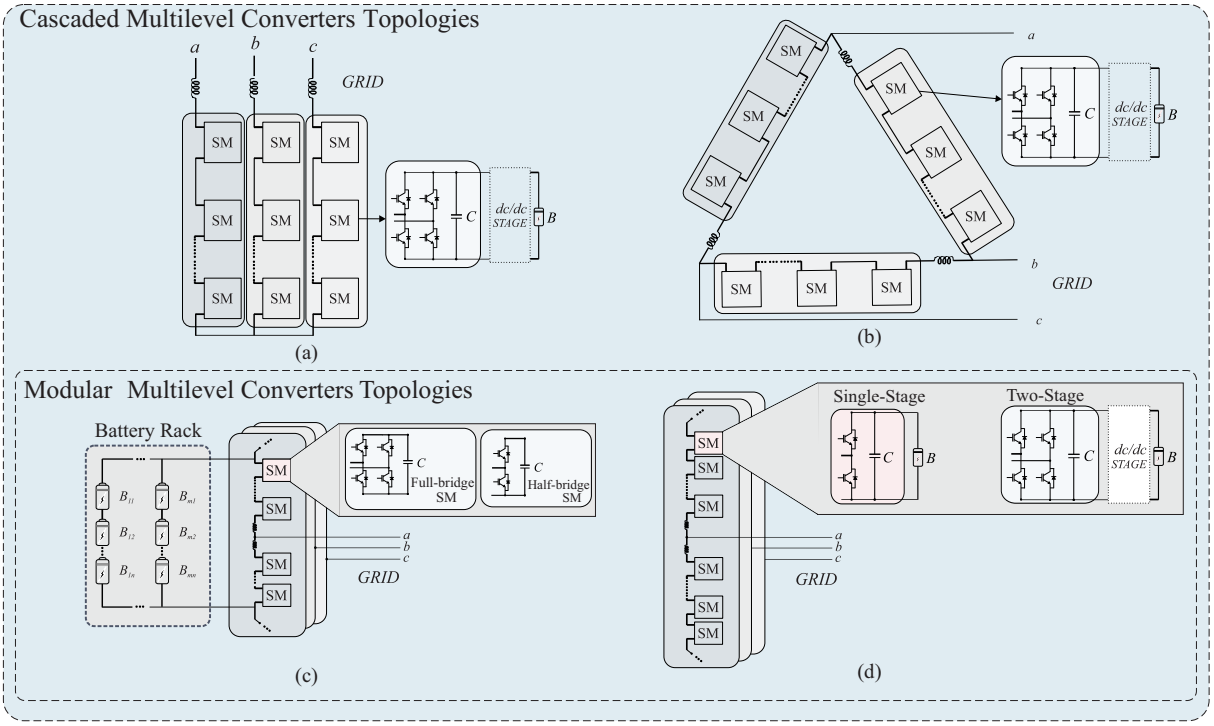
the BESS to connect to a low-voltage network or requiring the use of transformers with low frequency. In this sense, cascaded multilevel converter topologies are adopted as a solution, being the subject of discussion in the next subsection.

1.3.2 Cascaded Multilevel Converters

The cascaded multilevel converters are an alternative solution to overcome the limitations found in the two-level and three-level topologies, mainly to deal with the SOC unbalance of the batteries and to improve features like power losses (Cheng et al., 2006; Akagi; Maharjan, 2009). This alternative is based on the cascade connection of submodules (SMs), also called cells, to raise the output voltage by the individual contribution of each SM (Bharadwaj; Maiti, 2017a). Cascaded multilevel converters have several constructive and operational advantages, which can be listed as a greater number of ac voltage levels, modularity, fault-tolerance, redundancy, and low switching frequency (Bharadwaj; Maiti, 2017a; Chivukula; Maiti, 2019). This last one reduces the switching losses, improving efficiency. In addition, cascade multilevel converters have flexibility since the rated voltage can be increased by installing more SMs or even modifying the rated operating voltage of each SM (Chivukula; Maiti, 2019; Cupertino et al., 2019).

Among the cascaded multilevel converter topologies, three stand out among the most traditional and usually applied in commercial projects: star-connected cascaded multilevel converter, delta-connected cascaded multilevel converter, and modular multilevel converter (Cupertino et al., 2019). The multilevel topologies have been demonstrated to be prominent technologies in recent research on BESS, due to the possibility of connecting BESS directly to the medium voltage (MV) grid without the step-up transformer (Ch;

Figure 8 – PCS technologies for BESS realization: (a) Star-connected cascaded multilevel converter (b) Delta-connected cascaded multilevel converter (c) DSHB or DSFB with BESS centralized (d) DSHB or DSFB with BESS decentralized.



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Maiti, 2016; Chivukula; Maiti, 2019).

The star-connected and delta-connected cascaded converter is formed by the series connections of SM, of the full-bridge (FB) topology, in each converter phase, as shown in Fig. 8 (a) and (b), respectively. The implementation of the star-connected cascaded converter is less expensive, while the delta-connected cascaded converter dynamics are better in situations of an unbalanced grid (Cupertino et al., 2019). Furthermore, for the delta-connected cascaded converter, the insertion of a zero-sequence current between each phase of the converter is used for energy balancing (Sochor; Akagi, 2016). Each phase of the cascaded converter regulates the charging and discharging flow of each battery bank (Gherard et al., 2020). The inclusion of the dc/dc stage can be applied to improve the lifetime of the batteries and reduce BESS project costs (Pinto et al., 2022; Uddin et al., 2016).

Another cascaded converter alternative is the topology patented by Marquadt (2001), called Modular Multilevel Converter (MMC). The construction of the MMC is analogous to the use of SM, what differs is the arrangement of these converters in each phase (Ch; Maiti, 2016). In this topology, each converter phase is formed by two arms, where each arm is arranged with SM in series (Hillers; Stojadinovic; Biela, 2015). Fig. 8 (c) shows the structure of the MMC for the Double-Star Half-Bridge (DSHB) and Double-Star

Full-Bridge (DSFB) topology (nomenclature defined in Akagi (2010)), according to the type of SM applied (half-bridge or full-bridge) (Cupertino et al., 2018a; Sochor; Akagi, 2016). Furthermore, it emphasizes the distribution of the battery bank entirely in the dc-link of MMC, called centralized configuration. This arrangement of the batteries in a single battery bank limits the operational advantages of this converter due to numerous batteries in series reaching a significant voltage level (Vasiladiotis; Rufer, 2015).

Another proposal for the distribution of BESS batteries is among the SM of the converter, characterizing the decentralized configuration, as shown in Fig. 8 (d). In addition, it is possible to include a dc/dc stage between the SM and the batteries, to mitigate undesirable harmonic components and the OCV variation of the batteries. The configuration without including the dc/dc stage is called single-stage, while with the inclusion of the dc/dc stage, it is called two-stage (Pinto et al., 2022).

MMC is a promising technology for the next generations of medium/high-power VSC (Debnath et al., 2015; Xuan; Yang, 2017). Especially, MMC has favorable characteristics for application in BESS, called MMC-based BESS, due to the reduced switching frequency, low harmonic distortion level, reduced passive filters, and ease of SOC balancing (Bharadwaj; Maiti, 2017b; Wang et al., 2016). The operating reliability of the MMC is important for high-voltage direct current (HVDC), static synchronous compensators (STATCOM), and BESS, among others (Sharifabadi et al., 2016; Cupertino et al., 2018b; Gherard et al., 2020).

However, the significant number of SM poses challenges to the reliability of capacitors, IGBT modules, and batteries. These components are the most vulnerable in power electronics systems according to industry-based surveys (Mohamad; Teh, 2018), (Wang; Liserre; Blaabjerg, 2013). Electrothermal stress is one of the main mechanisms resulting in SM fatigue and failure (Zhang et al., 2017; Zhu; Ma; Cai, 2019). Thus, the validation of the MMC reliability before its operation in the field is crucial (Hahn et al., 2017).

1.4 Mission Profile Emulators

Despite the technical advantages, the MMC-based BESS implementation is challenging, since the converter contains hundreds or thousands of switching devices, capacitors, and batteries (Ahmed et al., 2014; Tang et al., 2016b). Thus, studies on the reliability, electrical, and thermal aspects of MMC can be extremely costly and require high implementation complexity in a full MMC construction (Tang et al., 2016a; Yang et al., 2019a). This is particularly important when the BESS application is taken into account. Therefore, mission profile emulators (MPE) play an important role in the simulation of SM, since the MPE can emulate similar voltage and current profiles (Jiang; Ma; Cai, 2020;

Yang; Wang; Ma, 2020a), with the advantage of a significant reduction of component number for implementation (Tang et al., 2017; Wang et al., 2019b; Yang; Ma; Wang, 2019).

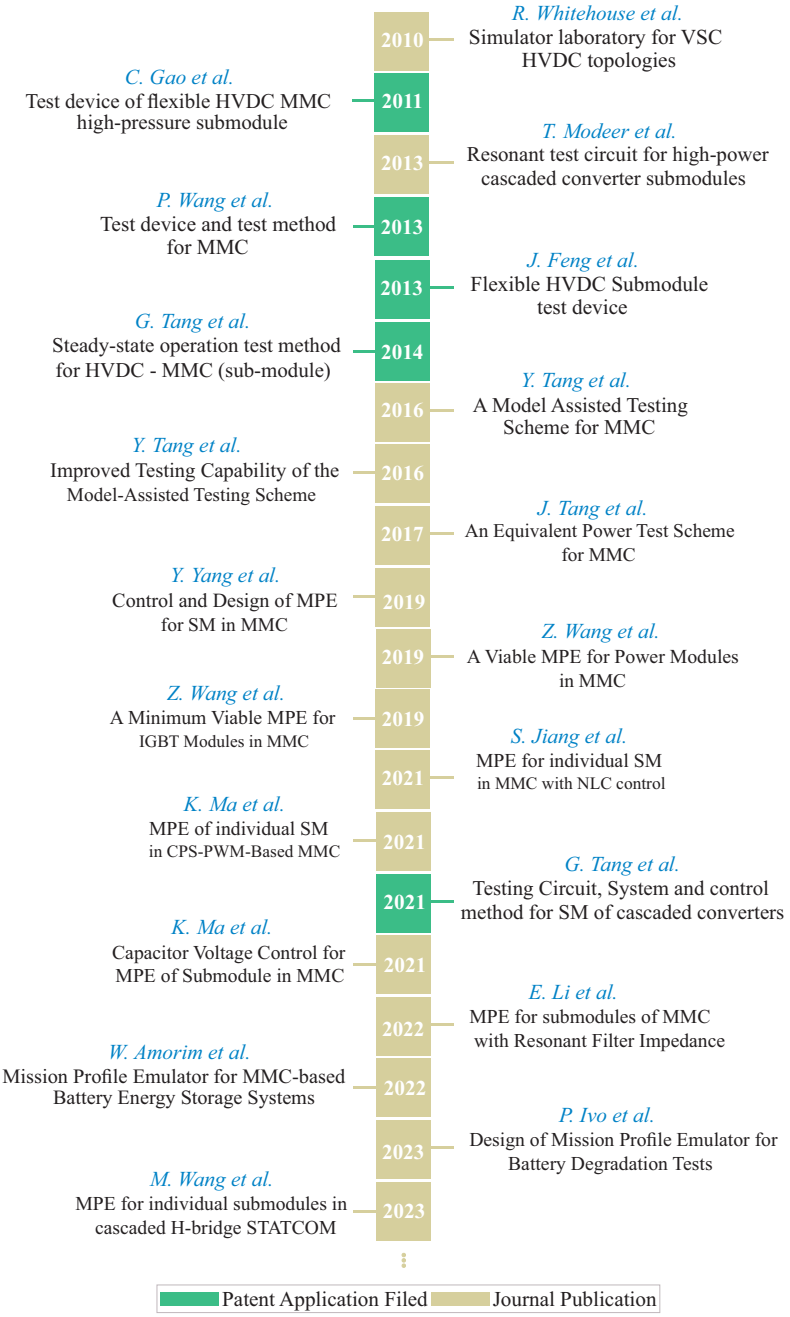
The MPE consists of a power converter controlled in current mode to guarantee the current and voltage verified in the SM of the MMC (Wang et al., 2019b). In this sense, with this emulator, it is possible to test one or more SMs of an MMC arm, without the need for complete implementation of the MMC. The aspects of reliability, electrical, and thermal evaluation mentioned above can be carried out in the MPE, through individual analysis of the effect of current and voltage on an SM of the MMC, or even on a single or more battery, capacitors, among others, connected to the SM (Tang et al., 2017). It is worth mentioning that the MPE proposal can be extended to other converter topologies, which further covers its application (Ma; Jiang; LI, 2021).

Fig. 9 summarizes some of the main scientific contributions, measured in terms of patents and journal paper citations, to developing MPE employed in cascaded multilevel converters, especially the MMC topologies. These MPE topologies are briefly described in the next paragraphs.

Tang et al. (2016b) proposes a model-assisted SM test scheme for evaluating the MMC operation in HVDC, STATCOM, among other applications with a full-bridge converter, as presented in Fig. 10 (a). Tang et al. (2016a) presents the new submodule testing scheme that builds on a recent development to improve the testing capability, as presented in Fig. 10 (b). The improved structure is introduced along with design and control techniques, with the voltage testing capability increased by more than five times when compared with the original scheme. In addition, simulation results show that the proposed method can offer better current tracking accuracy than the original with the same parameter settings. Modeer, Norrga and Nee (2013) proposes a test circuit and methodology suitable for testing high-power half-bridge SM used in cascaded converters, as presented in Fig. 10 (c). The circuit has a series resonant tank and two half-bridge submodules with voltage and impedance cancellation to minimize hardware requirements. Finally, Tang et al. (2017) presents an MPE for SM with high flexibility and low cost, based on a half-bridge converter, as presented in Fig. 10 (d).

Tab. 3 presents an operational comparison between the four MPE and testing scheme topologies presented in Fig. 10. The dc power supply voltage requirements are highlighted for the MPE based on a full-bridge converter with auxiliary SM, with a reduction close to 72.75% compared to the other topologies. In addition, it features high switching frequency operation, along with MPE based on full-bridge. For low switching frequency applications, MPE based on a half-bridge and testing scheme with a resonant circuit is not suitable. This last one, in turn, also does not have the ideal characteristics to emulate the applicable current profile for dc and second-order harmonic current. In contrast, the other topologies have these possibilities.

Figure 9 – Timeline of the main patents and journal papers related to MPE development.



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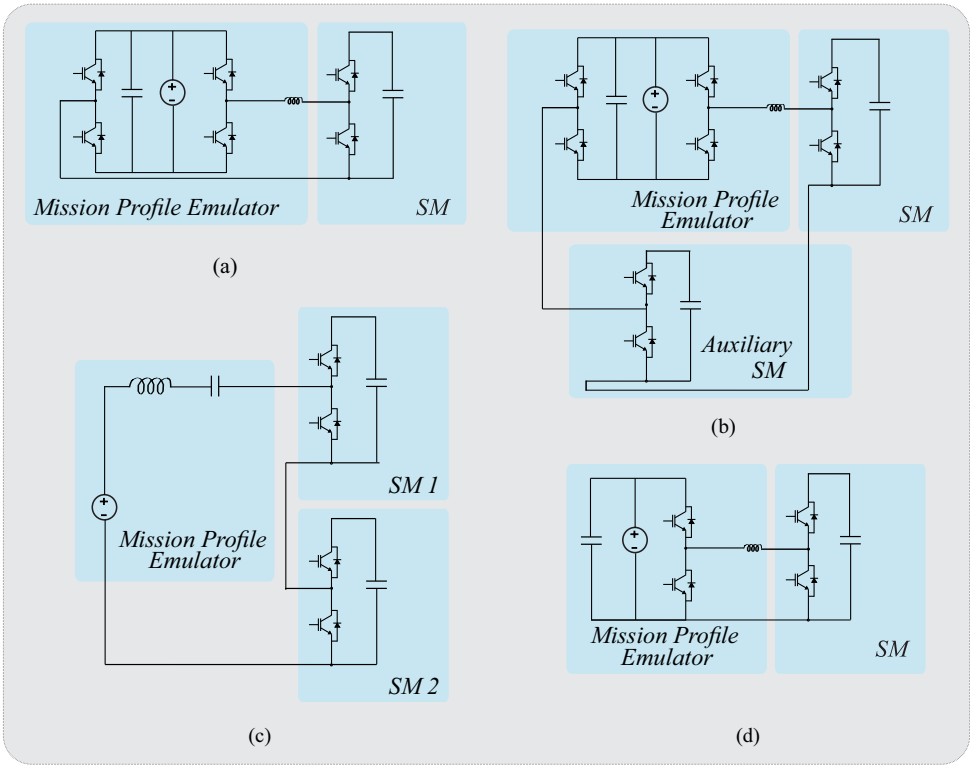
In addition to building different MPE topologies, authors in the literature address control strategies to optimize aspects of reliability, thermal behavior, and losses. Reference Yang, Wang and Ma (2020a) employs a full-bridge converter to emulate the arm current profile with a circulating current suppression method. In this study, a circulating current suppression method is proposed and evaluated for the emulator operation in inverting and rectifying mode. Authors of Wang et al. (2019a) develop an MPE with two full-bridge converters to assess the thermal behavior and the reliability of the power modules in the MMC. Reference Jiang et al. (2021) proposes the use of a novel control scheme for MPE

Figure 10 – Examples of MPE and testing scheme developed in the literature (a) MPE based on full-bridge converter (b) MPE based on full-bridge converter with SM auxiliary (c) Testing scheme for SM with resonant circuit (d) MPE based on half-bridge converter. (Resonant Circuit MPE is proposed by Modeer, Norrga and Nee (2013), Full-bridge MPE with SM auxiliary is proposed by Tang et al. (2016a), Full-bridge MPE is proposed by Tang et al. (2016b) and Half-bridge MPE is proposed by Tang et al. (2017).



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with nearest level control.

Reference Ma et al. (2021) employs a three-phase MPE for multiple SM in MMC. In addition, the authors published a patent, Ma, Jiang and LI (2021), with an MPE test bench for several SMs of a cascade converter. The current generator supplies a test current to a group of tested modules, with the ability to perform the simulation of the operating condition of the SMs of the cascade converter. The proposed current generator operates in both rectifier and inverter modes and can perform the simultaneous test of several SMs.

Although MPE is a more recent concept, as presented in the timeline of Fig. 9, the idea of designing a converter to emulate any electrical system is something older. The example of grid emulators (Jia; Averous; De Doncker, 2021), and load emulators (Vijay; Chandorkar; Doolla, 2019), among others, can be cited. According to the proposals for MPE topologies found in the literature, most of the solutions were inspired by these older solutions and adapted to the needs of the MPE. Therefore, they also served as inspiration for the development of this work.

Table 3 – Comparison among proposed MPE topologies and testing scheme. The dc power supply voltage range is considered for a nominal SM voltage equal to 2 kV. (Adapted from (Wang et al., 2019b)).

MPE capabilities	Full-bridge (Fig. 10 (a))	Half-bridge (Fig. 10 (d))	Full-bridge w/ SM auxiliary (Fig. 10 (b))	Resonant Circuit (Fig. 10 (c))
dc power supply voltage requirements	> 2 kV	< 2 kV	> 545 V	not applicable (ac voltage)
High switching frequency in MPE	√	√	√	√
Low switching frequency in MPE	√	χ	√	χ
Applicable Current profile: dc current	√	√	√	χ
Applicable Current profile: second-order current	√	√	√	χ

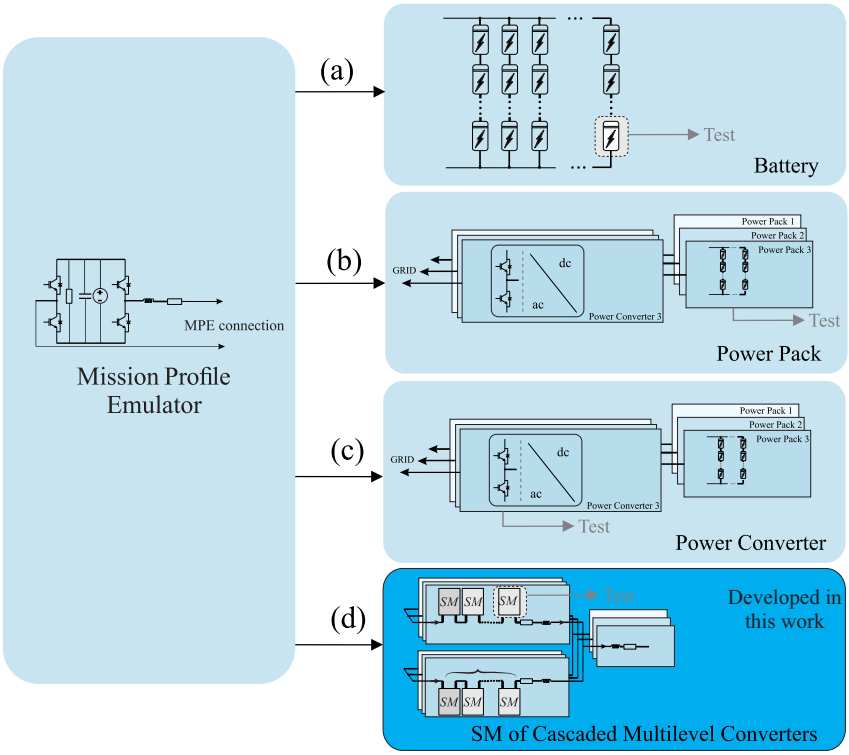
The MPE can be used to obtain battery current and arm current spectrum similar to those obtained in MMC. Thus, thermal and degradation studies on the batteries connected to the SM can be performed, without the implementation of the full MMC-based BESS. Aspects of the inclusion of batteries in the MPE design, operation during the batteries discharging process, and validation of typical battery current spectrum in MMC-based BESS, among others, are not evaluated in the literature. Indeed, to the best of the author's knowledge, MPE design and operation for MMC-based BESS has not been investigated.

1.5 MPE - Usage Possibilities

Despite the great application that the SM test can facilitate in reliability studies of the MMC in HVDC, STATCOM, and BESS, among other applications, it is worth highlighting that this application is not unique to the MPE structure presented in this work. Fig. 11 demonstrates the possibilities of using MPE beyond the SM test.

Power converters are made up of dozens of electrical components, such as inductors, capacitors, semiconductor switches, and batteries, among others. Battery-based storage systems are developed using these power converters. However, battery current models present operational implementation challenges, mainly associated with SOC balancing of the batteries. The challenge is even greater when applied in operational scenarios of high voltage and large power/energy capacity. Therefore, the continuous improvement of the

Figure 11 – MPE application possibilities: (a) test of battery (b) test of power pack (c) test of power converter (d) test of SM in Cascaded Multilevel Converters Topologies.



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capacity and voltage level of power converters is currently the focus of development and innovation. In this sense, the MPE can offer flexibility to overcome the voltage and current limits for the required BESS reliability studies, analyzing a battery or electrochemical cell, as indicated in Fig. 11 (a). In situations of steady and balanced operation of the BESS, there is an equal distribution of voltage and current in the battery strings. This way, studies carried out on a battery can be transferred to the battery bank.

It is worth mentioning that it is also important to develop equipment and processes to evaluate and test the reliability of low, medium, or high power during operation. Especially in the high power and energy scenario of BESS, it is common to use the power pack concept, in which each unit receives an equal proportional amount of full battery bank. For the aforementioned conditions of steady-state and balanced operation between power packs, the MPE can allow reliability studies of a power pack, as illustrated in Fig. 11 (b). Subsequently, the scaling process can be carried out for the battery bank as a whole, respecting the voltage and current limits of the proposed MPE.

In the initial stage, to evaluate and test the reliability of power converters applied in BESS, it is often necessary to build a complete system of the converter. In this sense, polyphase converters can be used to integrate the dc side of the battery bank with the ac side of the grid. The main focus of MPE is the emulation of ac or dc current with different

harmonic contents, where this flexibility makes it possible to test one of the n-phases of the converters, without necessarily having to implement the complete converter, as illustrated in Fig. 11 (c). Furthermore, the MPE construction structure does not necessarily need to be the same topology as a phase of the converter under study, it can have a different structure as long as it is capable of emulating a similar harmonic content in the output current.

Finally, Fig. 11 (d) illustrates the application under study in this work, emphasizing the SM test of MMC-based BESS, which can be extended to other categories of cascaded multilevel converters topologies.

1.6 Evaluation and Mitigation of Current Ripple on Li-ion Batteries

Despite the operational advantages of MMC-based BESS, this converter has the characteristic of harmonic components in the battery current, with significant first, second, and fourth-order components (Pinto et al., 2022). These current harmonic components impact battery lifetime (Uddin et al., 2016; Puranik; Zhang; Qin, 2018). The harmonics components increase the RMS value (since only the dc component is desired for the battery charging and discharging process) of the battery current and consequently increase the battery temperature. Thus, it increases battery losses and reduces its lifetime (Bragard et al., 2010; Uno; Tanaka, 2011).

Reference Uddin et al. (2016) carried out the evaluation of real-world measurements of the current on the high voltage bus of a series of hybrid electric vehicles (HEV) that exhibited significant current perturbations ranging from 10 Hz to 10 kHz. The work carried out the experimental investigation of studies of the long-term impact of current ripple on battery performance degradation. The results concluded that capacity fade and impedance rise progressively increase as the frequency of the superimposed ac increases. Furthermore, the spread of degradation for batteries cycled with a coupled ac and dc signal increases for batteries with a single dc component. The fact was verified by the expressive rise of the battery temperature according to the increment of the ac components in the battery current (Uddin et al., 2016; Puranik; Zhang; Qin, 2018).

Reference Bessman et al. (2019) evaluated the harmonics in battery current arising from switching of power electronics and harmonics in electric machinery. The results were considered for commercial Nickel Manganese Cobalt (NMC)/graphite prismatic Li-ion battery cells, which were subjected to frequencies of 1 Hz, 100 Hz, and 1 kHz, with operating temperatures, held constant by thermal conditioning systems. The conclusions led to the verification of no interference on cycled cells and calendar-aged cells under test, for tests with dc component exclusively and with dc and ac components. The study

in question presents the true impact on the battery lifetime, referring to the operating temperature. In this sense, the technical effort to maintain a battery constant temperature in the system with ac and dc components was significantly higher, due to the higher RMS component verified in the battery current.

Authors of Brand et al. (2018) evaluated the effect of the denominated corner frequency, which is defined by the local maximum of the impedance spectrum at the Nyquist plot as revealed by electrochemical impedance spectroscopy (EIS), concerning the battery degradation. The paper has proven that accelerated aging rather occurs at ac frequencies below a certain corner frequency, where mostly slower electrochemical processes are activated inside a lithium-ion battery cell. It is worth noting that the corner frequency value is entirely dependent on the typical SOC value. The work demonstrates that the diameter of the impedance semicircle in the Nyquist plot steadily increases with decreasing SOC. This is mainly attributed to the increase of the impedances of the cathode at low SOCs.

References Puranik, Zhang and Qin (2018), Puranik (2018) evaluated in an MMC-based BESS system the direct connection of the battery integrated into SM without dc/dc interfaced converters, which corresponds to the configuration provided the highest system efficiency and lowest cost. The experimental results show that the low-frequency ripple causes accelerated degradation of the battery during charging and discharging processes, which leads to a significant reduction in the battery lifetime, with a state-of-health (SOH) reduction greater than 40%. Despite verifying the impact of the typical MMC current on the lifetime battery, the work does not analyze the effect of including the dc/dc stage on battery degradation and the use of passive strategies to mitigate ripple in the battery current.

It is worth highlighting that the need to mitigate ripple in batteries is a problem faced in other types of applications and systems. It is possible to check several articles in the literature focused on ripple mitigation techniques in electric vehicle batteries and battery chargers (Goldammer et al., 2022), ripple mitigation demanded by fuel cells (Zhu; Zhan, 2020), and ripple mitigation produced by dc/dc and dc/ac converters that perform MPPT in photovoltaic series (Lin et al., 2012), among others. Therefore, they are applications that require ripple suppression similar to the problem of BESS based on MMC, and which served as inspiration for most of the solutions found in the literature on this problem, also being the inspiration for the development of this work.

In this sense, there is a gap in the academic literature about the potential effect on batteries in systems that deal with dc and ac exposure, especially on the effect of battery lifetime in MMC-based BESS. The points listed below are related to the gaps still found in the literature:

- Design of passive filters and dc/dc converters to mitigate typical harmonic components in the battery current verified in the SM of the MMC-based BESS;
- Evaluation of operation with passive and active strategies to mitigate current ripple in the batteries of an MMC-based BESS;
- MPE design including passive and active strategies to evaluate the mitigation of typical current harmonic components of an SM in an MMC-based BESS.

1.7 Purpose and Contributions

The MPE presents interesting operation features. As discussed in previous sections, the most recent research efforts in MPE aim to improve the efficiency and reliability of these converters, based on studies implemented in these emulators. Therefore, the MMC-based BESS efficiency and reliability are important aspects to be analyzed. Consequently, the stress on the SM's batteries can be reduced, improving the lifetime.

The operating reliability of the MMC is important for BESS. However, the significant number of SM poses challenges to the reliability of capacitors, IGBT modules, and batteries. These components are the most vulnerable in power electronics systems according to industry-based surveys. Electrothermal stress is one of the main mechanisms resulting in SM fatigue and failure and is underexplored in the literature, due to the high cost of validation with full-MMC.

In addition, the battery lifetime is influenced by the mechanisms of cycling aging and calendar aging, which are related to the cycling operation or idle operation, respectively. In applications of BESS with considerable battery cycling, factors such as depth-of-discharge (DOD), SOC, number of cycles, and temperature, significantly affect the cycling aging. The dependence on battery degradation according to the service provided to the power system is underexplored.

Regarding the harmonic current components, some research efforts focused on the effect of low harmonic contents in the battery lifetime. The harmonic current content in the batteries can affect the losses and lifetime. Especially, when the batteries are submitted to low-frequency harmonic current, the degradation rate increases. Thus, strategies such as the use of passive filters, dc/dc converters, or current injection control must be employed to increase the battery lifetime.

However, the use of harmonic attenuation strategies deals with the trade-off between the filter design and battery lifetime: if the current ripple is fully absorbed by the filtering methods, the system can not be profitable due to more filtering requirements. On the other hand, if the current ripple is fully absorbed by the battery, its lifetime can be severely

affected by the battery. In this way, these strategies for harmonic attenuation must be carefully analyzed, to optimize aspects such as efficiency, volume, costs, and lifetime.

This Ph.D. thesis intends to design and evaluate an MPE based on a full-bridge converter for analyzing the typical operation of an MMC-based BESS. Moreover, different methods of ripple suppression in battery current will be analyzed to improve the battery lifetime.

Based on the general purpose, the following topics are approached in this work:

- *Design and control tuning of MPE*: this topic presents the MPE control strategy and design adopted in this work. Besides, the modeling of MPE based on the MMC parameters is discussed;
- *Evaluation of MPE based on full-bridge converter for experimental and simulation results*: this topic fills the aforementioned void about the evaluation of MPE in an MMC-based BESS. Thus, an MPE based on a full-bridge converter is used to emulate the arm current MMC in a steady state. The SM under test is switched in such a way that the battery current harmonic spectra are similar to that observed in MMC-based BESS. The proposal is verified through simulations and using a reduced-scale prototype which validates the proposal experimentally. In addition, the validation of ripple current and operation under different operating power factors of the MPE is evaluated;
- *Use of passive filters for current ripple suppression*: this topic proposes the design of different passive filter topologies suitable for mitigating harmonic components of the battery current in an MMC-based BESS. In this sense, the use of the harmonic attenuation transfer function of the battery current and voltage is adopted to find the optimal design point of the passive filter. Simulation and experimental results from MMC-based BESS systems are evaluated to validate, the reduction of the harmonic content of the battery current;
- *Use of active methods for current ripple suppression*: this topic addresses the dc/dc converter design methodology to suppress the current ripple. The challenge is the definition of parameters considered appropriate for the design of the passive and active strategies analyzed, avoiding oversizing the components and enabling the comparison between them. Simulation and experimental results from MMC-based BESS systems are evaluated to validate the reduction of the harmonic content of the battery current.

The present research has been developed at Universidade Federal de Minas Gerais (UFMG) in the Laboratory of Energy Conversion and Control (LCCE) in cooperation with

the Gerência de Especialistas em Sistemas Elétricos de Potência (GESEP-UFV). In addition, the present research is grateful for the financial support provided by the P&D project ANEEL/CEMIG D722 e D727, CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico) - projects 408059/2021-4, 307172/2022-8, 407926/2023-2, 443170/2023-1, 313868/2023-9 and FAPEMIG (Fundação de Amparo à Pesquisa do Estado de Minas Gerais) - projects APQ-01187-18, APQ-02556-21 and RED-00216-23. Finally, this work was carried out with the support of the CAPES (Coordenação de Aperfeiçoamento de Pessoal de Nível Superior) - Financing Code 001.

1.8 Organization of the Ph.D Thesis

This Ph.D. thesis is organized into 5 chapters, as follows:

- Chapter 1 presents the motivations and objectives;
- Chapter 2 describes the modeling, basic dynamic equations, and design of the MMC-based BESS. Besides, the converter topology, control strategy, and components design are introduced;
- Chapter 3 describes the modeling, control, and design of the MPE. Besides, the converter topology, basic dynamic equations, and components design are introduced. In addition, introduces the experimental and simulation results for the MPE based on full-bridge converter evaluation;
- Chapter 4 presents the use of passive filters for current ripple suppression in batteries, based on LC filter and CL-LC filter. Experimental and simulation results are discussed;
- Chapter 5 presents the use of active filters for current ripple suppression in batteries, based on dc-dc converter. Experimental and simulation results are discussed;
- Finally, Chapter 6 presents the conclusions and the future developments of this work.

1.9 List of Publications and Contest Result

The results produced in this work originated the following papers, filed patent and contest results.

1.9.1 Award

- J. V. G. França, **W. C. S. Amorim**, A. F. Cupertino and H. A. Pereira. "ReliaBat: Reducing the cost and time to market of full modular battery energy storage system". IAS Zucker Design Contest Results (2022). IEEE.

1.9.2 Filed Patent (under review)

- **W. C. S. Amorim**, A. F. Cupertino, V. F. Mendes, H. A. Pereira, J. V. G. França. "Aparato e método de teste de degradação de baterias". INPI. 2024.

1.9.3 Published Journal Papers

- **W. C. S. Amorim**, J. V. G. França, A. F. Cupertino, V. F. Mendes and H. A. Pereira (2022). "Mission Profile Emulator for MMC-based Battery Energy Storage Systems". Eletrônica de Potência. vol. 27, no. 2, pp. 1-9.
- **W. C. S. Amorim**, A. F. Cupertino, H. A. Pereira and V. F. Mendes (2024). "On Sizing of Battery Energy Storage Systems for PV Plants Power Smoothing". Electric Power Systems Research. vol. 229, pp. 110-119.

1.9.4 Published Journal Papers: In cooperation with the research group

- R. C. de Barros, **W. C. S. Amorim**, W. do C. Boaventura, A. F. Cupertino, V. F. Mendes, and H. A. Pereira, "Methodology for BESS Design Assisted by Choice Matrix Approach", Eletrônica de Potência, vol. 29, p. e202412, Jun. 2024.
- J. H. D. G. Pinto, **W. C. S. Amorim**, A. F. Cupertino, H. A. Pereira, S. I. S. Junior and R. Teodorescu (2021), "Optimum Design of MMC-Based ES-STATCOM Systems: The Role of the Submodule Reference Voltage," in IEEE Transactions on Industry Applications, vol. 57, no. 3, pp. 3064-3076.
- J. H. D. G. Pinto, **W. C. S. Amorim**, A. F. Cupertino, H. A. Pereira, S. I. S. Junior (2022). "Benchmarking of Single-Stage and Two-Stage Approaches for an MMC-Based BESS." Energies 2022, 15, 3598.
- J. M. Callegari, L. S. Gusman, D. C. Mendonça, **W. C. S. Amorim**, I. Alves, H. A. Pereira and F. Pinto (2021). "Detection of Stressed Electronic Components in PV Inverter using Thermal Imaging." IEEE Latin America Transactions, 18(10), 1760–1767.

1.9.5 Submitted Journal Papers (under review):

- **W. C. S. Amorim**, A. F. Cupertino, V. F. Mendes, J. V. G. França, H. A. Pereira, "Evaluation of Battery Current Harmonic Suppression Schemes for MMC-Based Energy Storage Systems Through Mission Profile Emulator". IEEE Transactions on Industry Applications. September (2024).
- J. M. S. Callegari, **W. C. S. Amorim**, D. I. Brandao, B. J. C. Filho, "On Sizing of Battery Energy Storage Systems for Independent Multi-Ancillary Services in AC Grids". Advances in Electrical Engineering, Electronics and Energy. February (2024).
- R. O. de Sousa, R. C. de Barros, **W. C. S. Amorim**, A. F. Cupertino, H. A. Pereira and L. M. F. Morais, "Modified rainflow algorithm for temperature-time-dependent counting in lifetime estimation of power devices", Eletrônica de Potência. September (2024).

1.9.6 Published Conference Papers

- **W. C. S. Amorim**, A. F. Cupertino, V. F. Mendes, H. A. Pereira, R. C. Barros, R. O. Sousa. "On Reliability Assessment of a Battery Energy Storage Systems Supporting PV Plants". In: 17th Brazilian Power Electronics Conference and 8th Southern Power Electronics Conference, 2023, Florianópolis, SC. COBEP/SPEC 2023, 2023.

1.9.7 Published Conference Papers: In cooperation with the research group

- R. O. Sousa, R. C. Barros, **W. C. S. Amorim**, A. F. Cupertino, H. A. Pereira. "Modified Rainflow for Lifetime Estimation of Semiconductors Devices". In: 17th Brazilian Power Electronics Conference and 8th Southern Power Electronics Conference, 2023, Florianópolis, SC. COBEP/SPEC 2023, 2023.
- R. C. Barros, R. O. Sousa, **W. C. S. Amorim**, Allan F. Cupertino, H. A. Pereira. "The Effect of the Harmonic Current Compensation on the dc-link Capacitor of a Three-phase Photovoltaic Inverter". In: 17th Brazilian Power Electronics Conference and 8th Southern Power Electronics Conference, 2023, Florianópolis, SC. COBEP/SPEC 2023, 2023.
- E. J. Araujo, F. E. Silva, C. R. Mesquita, **W. C. S. Amorim**. "Modelagem da Proteção Direcional de Sobrecorrente de uma Linha de Transmissão". In: XVI Simpósio Brasileiro de Automação Inteligente e X Simpósio Brasileiro de Sistemas Elétricos, 2023, Manaus, AM. SBAI-SBSE, 2023.

- A. A. A. Barreto, R. S. F. Zeferino, R. C. de Barros, **W. C. S. Amorim**, H. A. Pereira, A. F. Cupertino. "Análise do Efeito do Tempo de Descarga na Vida Útil de Baterias de Ion-Lítio em Aplicações de Sistemas Fotovoltaicos com Fluxo Reverso". In: Congresso Brasileiro de Automática. 2024.

- R. L. S. Cruz, R. C. Barros, V. P. Dardengo, H. A. Pereira, **W. C. S. Amorim**. "Dimensionamento de Banco de Bateria de BESS para aplicação de Peak Shaving, baseado no perfil de carga". In: Congresso Brasileiro de Automática. 2024.

1.9.8 Published Conference Papers invited for Publication in Journal

- **W. C. S. Amorim**, A. F. Cupertino, V. F. Mendes, H. A. Pereira, R. C. Barros, R. O. Sousa. "On Reliability Assessment of a Battery Energy Storage Systems Supporting PV Plants". In: Eletrônica de Potência. 2024.

2 MMC-based BESS: Control Strategy and Design

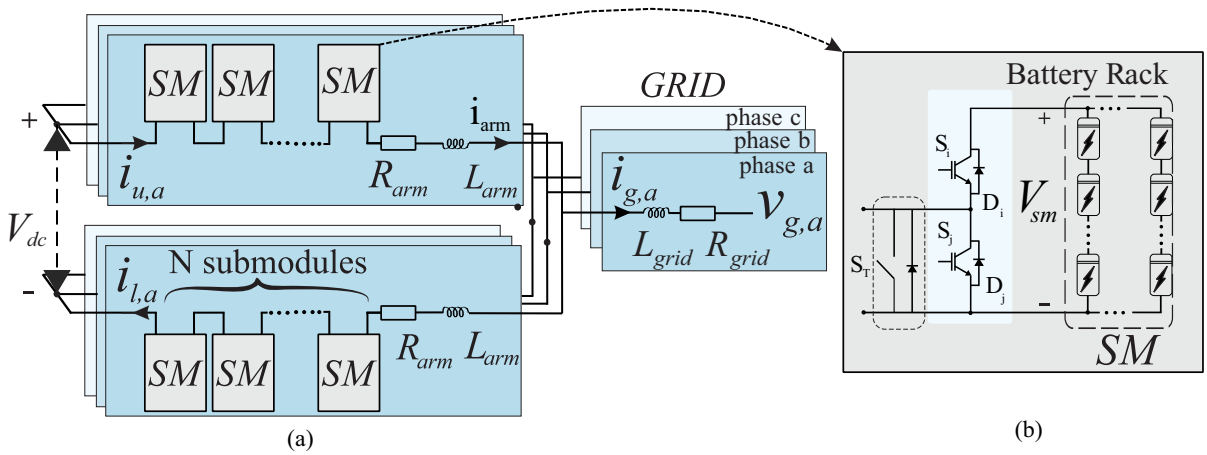
This chapter begins with a presentation of the architecture of the MMC-based BESS. This presentation analyzes the mathematical model of the converter as well as the equations for modeling and design. In this sense, the basic dynamic equations are introduced. In addition, the control strategies, control tuning, and modulation strategies are presented.

Furthermore, the MMC dynamics for a DSHB topology are evaluated for BESS application to quantify the main harmonic content of battery current in SM. Aspects involving BESS arrangement are evaluated for MMC-based BESS, as well as passive components design of this converter. Finally, the possibilities of integrating batteries into MMC SM using active and passive current ripple mitigation strategies are addressed.

2.1 MMC-based BESS

Fig. 12 (a) presents the MMC-based BESS topology studied in this work. The SM structure, presented in Fig. 12 (b), is a half-bridge topology. The battery rack is connected to the SM, with series and parallel associations to fulfill the application power and energy requirements.

Figure 12 – Basic structure of an MMC-based BESS: (a) converter structure (b) SM structure.



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In the DSHB converter, there are N SMs per arm and each SM contains four semiconductor devices (represented by S_i, S_j, D_i, and D_j) and a battery rack. There is

a switch S_T in parallel with the SM that bypasses it in case of failures (Cupertino et al., 2018b). The arm inductance is represented by L_{arm}, which reduces the high-order harmonics in the circulating current and limits the fault currents (Chaudhary et al., 2020). The intrinsic resistance of L_{arm} is represented by R_{arm}.

The converter is connected to the main grid through a three-phase isolation transformer with inductance L_{grid} and resistance R_{grid} (which corresponds to the Thévenin equivalent circuit). Moreover, $i_{u,n}$ and $i_{l,n}$ are the upper and lower arm currents in the n-phase (where n belongs to a, b, and c converter phase), respectively. Finally, $v_{g,n}$ is the grid voltage in the n-phase, V_{dc} is the dc-link voltage of the MMC, and $i_{g,n}$ is the output current in the converter n-phase.

2.1.1 Control Strategy for MMC-based BESS

Fig. 13 shows the control strategy of an MMC-based BESS providing a typical ancillary service (Cupertino et al., 2020). The control can be divided into:

1. Grid current control (Fig. 13 (a));
2. Circulating current control (Fig. 13 (a));
3. Converter control mode (Fig. 13 (a) and (b)).

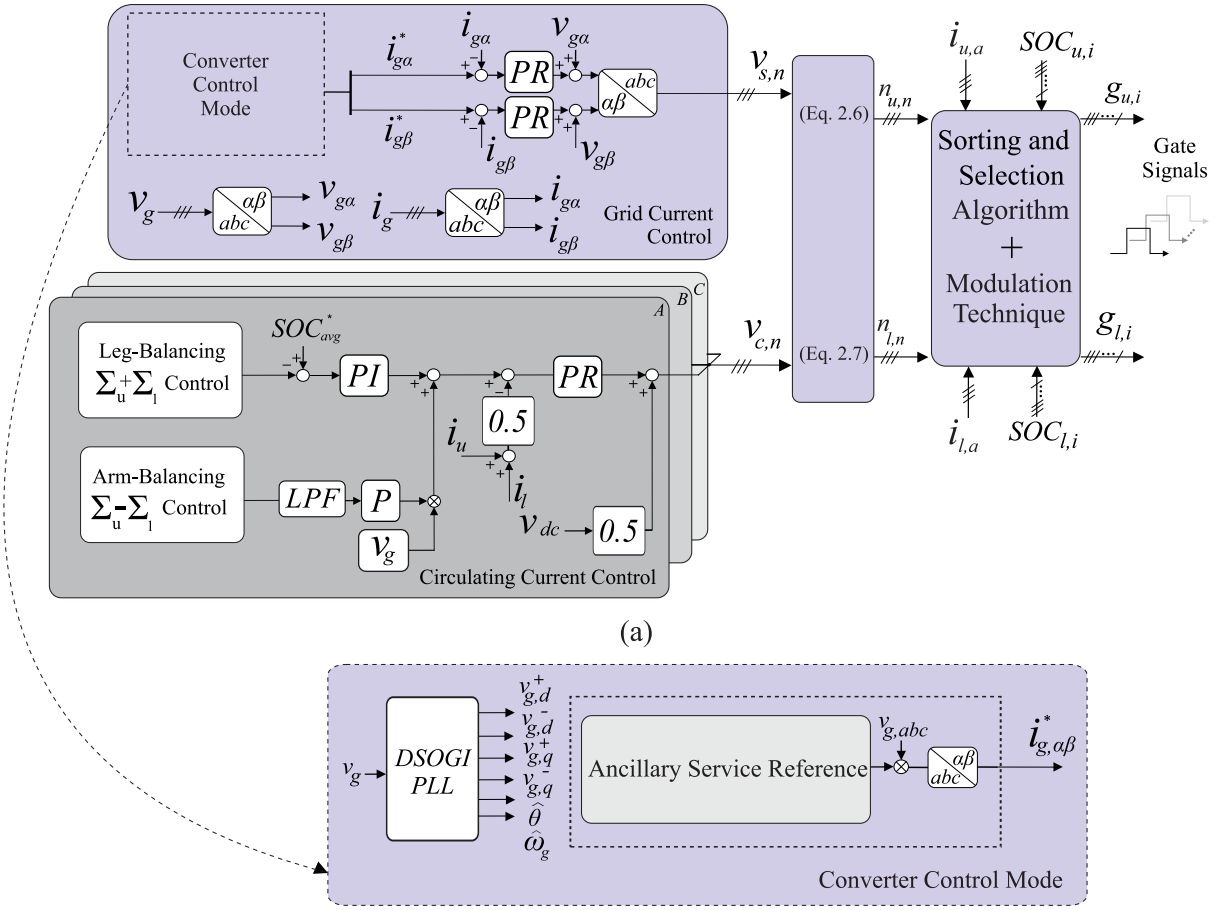
The grid current control is implemented in the stationary reference frame ($\alpha\beta$), presented in Fig. 13 (a), where proportional resonant (PR) controllers are employed. This control is responsible for the active and reactive power exchange with the grid. The grid current reference is given by:

$$i^*_{g,\alpha\beta} = i^*_{gp,\alpha\beta} + i^*_{gq,\alpha\beta}, \tag{2.1}$$

where $i^*_{gq,\alpha\beta}$ is the reference current component related to the reactive power transfer (this reference can be computed based on the reactive power or voltage support demand (Sharifabadi et al., 2016)), and $i^*_{gp,\alpha\beta}$ is the component of the reference current related to the active power transfer. This variable depends on the MMC-based BESS control mode.

Under steady-state grid conditions (where BESS is not providing an ancillary service), $i^*_{gp,\alpha\beta}$ is computed by the global SOC control, which calculates the amount of active power to charge the batteries until SOC^* (reference of SOC). The global SOC control is implemented in each phase of the converter and is performed using proportional-integral (PI) controllers. For some ancillary services, these controllers can be saturated in a fraction of the rated current, such as in frequency regulation and deferral transmission applications.

Figure 13 – (a) MMC-based BESS control strategy for promoting a typical ancillary service (b) Converter control mode.



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(Cupertino et al., 2020). Thus, the charging and discharging process of the batteries might not affect the grid.

The ancillary service reference is obtained in the converter control mode, presented in Fig. 13 (b). In this sense, the objective of this block is to generate a reference $i^*_{gq,\alpha\beta}$ or $i^*_{gp,\alpha\beta}$ (reactive or active power injection depends on the type of ancillary service performed). Obtaining this reference depends exclusively on the characteristics of the intended ancillary service, and is generally associated with the determinations of the grid code (Rebours et al., 2007). It is worth mentioning that the BESS can operate by performing global SOC control or by performing the ancillary service reference, thus acting exclusively in one of the two operating modes.

The circulating current control is implemented to insert damping in the converter dynamic response. This control is responsible for suppressing the second harmonic and achieving the SOC individual control per SM (Li et al., 2018). The circulating current $i_{c,n}$ is calculated for each phase n:

$$i_{c,n} = \frac{i_{u,n} + i_{l,n}}{2}, \tag{2.2}$$

The circulating current control is implemented based on a PR controller that derives the MMC internal voltage $v_{c,n}$. According to Tsolaridis et al. (2017), a dc circulating current can exchange power among the converter phases, while a fundamental frequency circulating current can exchange power between the upper and lower arms (Cupertino et al., 2020). Thus, the circulating current control is used for SOC balancing in batteries without affecting the converter output current.

The leg-balancing control is realized using PI controllers that compute the dc component of the circulating current. This control is necessary to guarantee that all legs present the same average SOC. Thus, the average SOC in phase n is given by:

$$SOC_{n,avg} = \frac{1}{2N}\left(\sum_{i=1}^{N} SOC_{u,i} + \sum_{i=1}^{N} SOC_{l,i}\right), \tag{2.3}$$

The reference of the leg-balancing control is given by:

$$SOC^{*}_{avg} = \frac{1}{3}\sum_{j=1}^{3} SOC_{j,avg}. \tag{2.4}$$

where N is the number of submodules per arm. For the arm-balancing control, the difference between the average SOC of the upper and the lower arms, SOC_{diff}, is computed for each phase using a low pass filter (LPF), as follows:

$$SOC_{n,diff} = \frac{1}{N}\left(\sum_{i=1}^{N} SOC_{u,i} - \sum_{i=1}^{N} SOC_{l,i}\right). \tag{2.5}$$

For an MMC-balanced operation, the reference of the arm-balancing control is zero. A proportional controller is used to compute the amplitude of the fundamental frequency circulating current. This signal is multiplied by the grid voltage, as presented in Fig. 13 (b).

Finally, the insertion indexes for upper and lower arms, in the *n-th* phase, are given by:

$$n_{u,n} = \frac{v_{c,n} - v_{s,n}}{N v^{*}_{sm}}, \tag{2.6}$$

$$n_{l,n} = \frac{v_{c,n} + v_{s,n}}{N v^{*}_{sm}}, \tag{2.7}$$

where v^{*}_{sm} is the SM voltage reference. $v_{s,n}$ is the voltage synthesized in the MMC output, which drives $i_{g,n}$ and $v_{c,n}$ is the MMC internal voltage, which drives $i_{c,n}$. Regarding the

modulation strategy, the injection of 1/6 of the third harmonic can be considered to increase the linear region of the modulator (Sharifabadi et al., 2016).

2.2 MMC-based BESS Mathematical Modelling

The dc-link current (i_{dc}) is defined by the sum of the upper arm currents or lower arm currents. For the decentralized configuration, i_{dc} is equal to zero. Therefore,

$$\sum_{n=1}^{3} i_{u,n} = \sum_{n=1}^{3} i_{l,n} = 0. \tag{2.8}$$

where $i_{u,n}$ is the n-phase upper arm current and $i_{l,n}$ is the n-phase lower arm current. In addition, in the centralized or decentralized configuration is assumed a dc-link is balanced among the arms of each phase, which results in:

$$V_{dc,u} = V_{dc,l} = \frac{V_{dc}}{2}, \tag{2.9}$$

where $V_{dc,u}$ and $V_{dc,l}$ are the value of dc-link concentrated in the upper and lower arm, respectively.

The instantaneous arm voltage synthesized for each arm can be obtained from the modulation index and the instantaneous value of the battery voltage in series per SM. The inserted voltage ($v_{u,n}$) in the upper arm of n-phase can be expressed as:

$$v_{u,n} = \sum_{i=1}^{N} m_{u,n} v_{sm,n}^{i}. \tag{2.10}$$

where $m_{u,n}$ is the n-phase upper modulation index and $v_{sm,n}^{i}$ is the n-phase SM voltage of the i-th submodule. The MMC output current ($i_{g,n}$) is referred to as grid current since the output of the converter is connected directly to the ac grid through a three-phase isolation transformer. Based on the arm currents direction present in Fig. 20 (a), the n-phase output current is derived:

$$i_{g,n} = i_{u,n} - i_{l,n}. \tag{2.11}$$

The circulating current ($i_{c,n}$) in MMC is responsible for exchanging energy between the arms, and consequently carrying out an equalizing process of the battery racks. However, to keep the power losses and the arm currents at a minimum, the circulating current should be a purely harmonic-free dc signal. The circulating current is calculated for each phase and given by:

$$i_{c,n} = \frac{i_{u,n} + i_{l,n}}{2}. \tag{2.12}$$

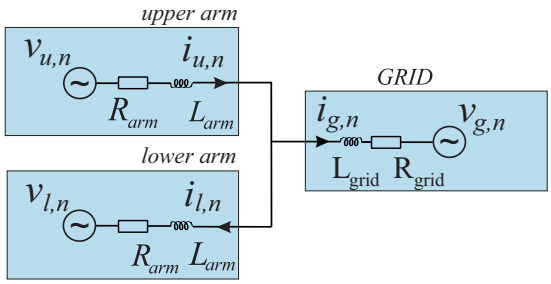
Thus, the upper and lower arm currents ($i_{u,n}$ and $i_{l,n}$, respectively), in n-phase, can be expressed in terms of circulating current and grid current, respectively:

$$i_{u,n} = \frac{i_{g,n}}{2} + i_{c,n}, \tag{2.13}$$

$$i_{l,n} = -\frac{i_{g,n}}{2} + i_{c,n}. \tag{2.14}$$

Fig. 14 shows the equivalent circuit of the MMC arms and output converter.

Figure 14 – Equivalent circuit of the MMC arms and output converter.



Source: own representation.

In this sense, the output voltage ($v_{g,n}$) and output current ($i_{g,n}$) dynamics can be obtained by the following equation:

$$v_{s,n} - \left(\frac{L_{arm}}{2} + L_{grid}\right)\frac{di_{g,n}}{dt} - \left(\frac{R_{arm}}{2} + R_{grid}\right)i_{g,n} = v_{g,n}. \tag{2.15}$$

where $v_{s,n}$ is the line-to-neutral voltage synthesized by the MMC, that can be expressed by [1]:

$$v_{s,n} = \frac{v_{l,n} - v_{u,n}}{2}. \tag{2.16}$$

The dynamics of the circulating current per phase are analyzed from the MMC internal voltage ($v_{c,n}$), which is responsible for the circulating current control, being expressed by:

$$v_{c,n} = L_{arm}\frac{di_{c,n}}{dt} + R_{arm}i_{c,n}. \tag{2.17}$$

Thus, the upper arm voltage ($v_{u,n}$) and lower arm voltage ($v_{l,n}$) is given by, respectively:

[1] According to Millman (1940) the association voltage sources connected in parallel can be reduced to one equivalent voltage source. It is worth highlighting that the same conclusion can be obtained through Thevenin's theorem.

$$v_{u,n} = v_{c,n} - v_{s,n} + \frac{V_{dc}}{2}. \tag{2.18}$$

$$v_{l,n} = v_{c,n} + v_{s,n} + \frac{V_{dc}}{2}. \tag{2.19}$$

The instantaneous active power exchange by MMC-based BESS is derived from the instantaneous active power exchange by the upper and lower arms (it is worth noting that it is considered that the same power is synthesized by all SMs). Thus, the instantaneous active power delivered by each upper and lower arm is given by:

$$p_{u,n} = v_{u,n} i_{u,n} = \left(v_{c,n} - v_{s,n} + \frac{V_{dc}}{2}\right)\left(\frac{i_{g,n}}{2} + i_{c,n}\right), \tag{2.20}$$

$$p_{l,n} = v_{l,n} i_{l,n} = \left(v_{c,n} + v_{s,n} + \frac{V_{dc}}{2}\right)\left(-\frac{i_{g,n}}{2} + i_{c,n}\right), \tag{2.21}$$

where $v_{c,n}$ is the n-phase circulating voltage and $v_{s,n}$ is the n-phase MMC output voltage. Equations (2.20) and (2.21) results in, respectively:

$$p_{u,n} = v_{c,n}\frac{i_{g,n}}{2} + v_{c,n} i_{c,n} - v_{s,n}\frac{i_{g,n}}{2} - v_{s,n} i_{c,n} + V_{dc}\frac{i_{g,n}}{4} + V_{dc}\frac{i_{c,n}}{2}, \tag{2.22}$$

$$p_{l,n} = -v_{c,n}\frac{i_{g,n}}{2} + v_{c,n} i_{c,n} - v_{s,n}\frac{i_{g,n}}{2} + v_{s,n} i_{c,n} - V_{dc}\frac{i_{g,n}}{4} + V_{dc}\frac{i_{c,n}}{2}. \tag{2.23}$$

For DSHB decentralized configuration, the circulating current ($i_{c,n}$) is approximately zero since it is assumed that the circulating current control can reject the ac component. In addition, the internal voltage ($v_{c,n}$) is approximately zero to keep the circulating current at zero. From these approximations, the instantaneous active power can be simplified to, respectively:

$$p_{u,n} = \underbrace{v_{c,n}\frac{i_{g,n}}{2} + v_{c,n} i_{c,n} + V_{dc}\frac{i_{c,n}}{2} - v_{s,n} i_{c,n}}_{\approx 0} - \underbrace{v_{s,n}\frac{i_{g,n}}{2}}_{dc+ac\ comp.} + \underbrace{V_{dc}\frac{i_{g,n}}{4}}_{ac\ comp.}, \tag{2.24}$$

$$p_{l,n} = \underbrace{-v_{c,n}\frac{i_{g,n}}{2} + v_{c,n} i_{c,n} + V_{dc}\frac{i_{c,n}}{2} + v_{s,n} i_{c,n}}_{\approx 0} - \underbrace{v_{s,n}\frac{i_{g,n}}{2}}_{dc+ac\ comp.} - \underbrace{V_{dc}\frac{i_{g,n}}{4}}_{ac\ comp.}. \tag{2.25}$$

The different power terms have different physical meanings. At this point, the following conclusions can be stated:

- The product $v_{s,n}\frac{i_{g,n}}{2}$ leads to a fundamental ac component and dc component. Assuming that $v_{s,n}$ and $i_{g,n}$ are sinusoidal waves, the average value represents the active power transferred from the SM to the grid. In addition, the oscillating component leads to a second harmonic ripple in the battery current;
- The oscillating component $V_{dc}\frac{i_{g,n}}{4}$ leads to a fundamental frequency oscillating power. This term results in a fundamental frequency ripple in the battery current. As observed, this term presents opposite signals in the lower and upper arms. Thus, this power oscillation is not observed at the MMC output terminals.

The sum of equations (2.24) and (2.25) results in:

$$p_{u,n} + p_{l,n} = -v_{s,n} i_{g,n}. \tag{2.26}$$

In this sense, the power delivered to the grid ($p_{g,n}$) is equal to the sum of power delivered by each arm in the n-phase. It is worth noting that half of the power is processed by each arm, based on equations (2.24) and (2.25), which leads to an equal distribution between the arms. Conversely, the ac output voltage in DSHB can be expressed as:

$$v_{s,n} \approx v_{g,n} = \widehat{V}\cos(\omega_g t + \theta_v + \delta), \tag{2.27}$$

where $\widehat{V}$ is the peak of grid voltage, ω_g is the nominal grid angular frequency, θ_v is the phase angle of each grid phase ($\theta_v \in \left\{-\frac{2\pi}{3}, 0, \frac{2\pi}{3}\right\}$) and δ is the grid voltage angle.

Alternatively, the grid current can be expressed as:

$$i_{g,n} = \widehat{I}\cos(\omega_g t + \theta_v + \phi_g), \tag{2.28}$$

where $\widehat{I}$ is the peak of grid current and ϕ_g is the grid current angle. From the equations (2.27) and (2.28), the instantaneous active power delivered by each phase can be expressed as:

$$p_{g,n} = v_{g,n} i_{g,n} \approx v_{s,n} i_{g,n}. \tag{2.29}$$

Replacing equation (2.26) in (2.29), the instantaneous active power delivery by each phase is given by:

$$p_{g,n} = -(p_{u,n} + p_{l,n}) = \underbrace{\frac{\widehat{V}\widehat{I}}{2}\cos(\delta - \phi_g)}_{\overline{p}_{g,n}} + \underbrace{\frac{\widehat{V}\widehat{I}}{2}\cos(2\omega_g t + 2\theta_v + \phi_g + \delta)}_{\widetilde{p}_{g,n}}. \tag{2.30}$$

From the equation of instantaneous active power obtained, the dc power term ($\overline{p}_{g,n}$) exchanges effective active power between the grid and batteries in SM. In addition, the instantaneous active power equation can be formulated in terms of modulation index (m), which for DSHB-MMC topology is given by:

$$m = 2\frac{\widehat{V}}{V_{dc}}, \tag{2.31}$$

which results in

$$p_{g,n} = \frac{mV_{dc}\widehat{I}}{4}\cos(\delta - \phi_g) + \frac{mV_{dc}\widehat{I}}{4}\cos(2\omega_g t + 2\theta_v + \phi_g + \delta). \tag{2.32}$$

2.3 Evaluation of Battery Current in SM

The upper arm voltage ($v_{u,n}$) can be expressed based on the value of the maximum modulation index, dc-link voltage, angular grid frequency, and phase displacement (Cupertino et al., 2018b):

$$v_{u,n} = \frac{V_{dc}}{2} - \frac{mV_{dc}}{2}\cos(\omega_g t + \theta_v) + \frac{mV_{dc}}{12}\cos(3\omega_g t + \theta_v). \tag{2.33}$$

Furthermore, the upper arm current ($i_{u,n}$) can be expressed based on the value of the amplitude of grid current, converter angle, angular grid frequency, and phase displacement:

$$i_{u,n} = \frac{\widehat{I}_{g,n}}{2}\cos(\omega_g t + \theta_v + \phi_g). \tag{2.34}$$

In this sense, assuming negligible power losses in SM and that the power is evenly distributed between the SM, the current flowing through the batteries present in each SM can be estimated by the following approximation:

$$i_{bat}(t) \approx \frac{p_{u,n}}{NV_{SM}} \approx \frac{v_{u,n}i_{u,n}}{NV_{SM}}. \tag{2.35}$$

The same analysis can be performed considering the power of the lower arm and the power for other converter phases. Multiplying equations (2.33) and (2.34), substituting in the equation (2.35), and rearranging the second harmonic terms using trigonometric identity[2], the following expression is obtained for the current flowing through the batteries in each SM:

[2] $A\cos(\omega t) + B\sin(\omega t) = \sqrt{A^2 + B^2}\cos(\omega t - \phi)$ and $\phi = \text{tg}^{-1}(\frac{B}{A})$.

$$i_{bat}(t) = \underbrace{-\frac{m\widehat{I}_g}{8}\cos(\phi_g)}_{\text{dc component}} + \underbrace{\frac{\widehat{I}_g}{4}\cos(\omega_g t + 2\theta_v + \phi_g)}_{1^{st}\text{harmonic}} + \underbrace{\frac{m\widehat{I}_g}{48}\cos(4\omega_g t + 2\theta_v + \phi_g)}_{4^{th}\text{harmonic}} + \underbrace{\frac{m\widehat{I}_g}{48}\sqrt{37 - 12\cos(2\phi)}\cos(2\omega_g t + \theta_v + \phi_g + \beta)}_{2^{nd}\text{harmonic}}; \tag{2.36}$$

where β is expressed by:

$$\beta = \sin^{-1}\left(\frac{\sin(2\phi_g)}{\sqrt{37 - 12\cos(2\phi_g)}}\right). \tag{2.37}$$

According to equation (2.36), the battery current has a significant portion of the dc component, being directly responsible for charging and discharging the batteries in each SM. Furthermore, the presence of first, second, and fourth harmonic components, which can generate a significant ripple in the battery (especially the first and second-order components) is verified. In this sense, if no filter is applied, the fundamental, second, and fourth harmonic components flow through the battery. Under such conditions, those harmonics increase the Root Mean Square (RMS) value of the battery current and the losses in the batteries.

The effective RMS value of the battery current in the case with and without ripple suppression can be calculated as follows, respectively (Pinto, 2022):

$$\begin{cases} i_{bat,w/sup} = \frac{m\widehat{I}_g}{8}\left|\cos(\phi_g)\right|, \\ i_{bat,w/osup} = \frac{m\widehat{I}_g}{8}\sqrt{\cos^2(\phi_g) + \frac{67}{36}}, \end{cases} \tag{2.38}$$

where $i_{bat,w/sup}$ is the RMS value of battery current with complete harmonic suppression and $i_{bat,w/osup}$ is the RMS value of battery current without harmonic suppression.

Fig. 16 presents an analysis of the RMS value of the battery current in the case with ($i_{bat,w/sup}$) and without ($i_{bat,w/osup}$) battery current ripple suppression (based on the equations in (2.38)).

Fig. 16 (a) depicts the influence of grid current angle and modulation index in the pu value of the RMS value of battery current. It can be seen that the largest current amplitudes are reached under conditions of unity power factor ($\phi_g = 0$, $-\pi$ or π). Furthermore, the higher the modulation index, the higher the expected battery current value, as example for m = 1.15 and grid current angle equal to 0 rad, a maximum RMS current value is obtained around 0.14375 pu. Under operating conditions with non-unitary power factor, theoretically, a dc portion of the current circulating in the batteries is not expected, with two points with a value close to zero ($\phi_g = \frac{-\pi}{2}$ or $\frac{\pi}{2}$) (Cupertino et al., 2018b).

Figure 15 – Analysis of effective RMS value of the battery current in the case (a) with and (b) without ripple suppression.

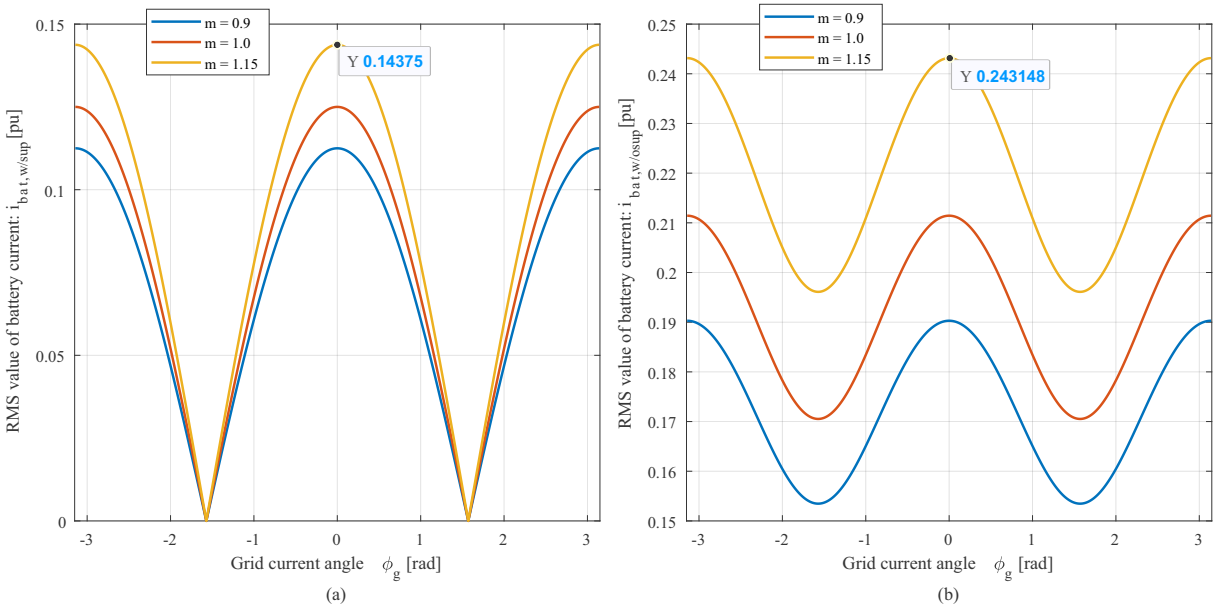


Figure 16 – Source: own representation.

Fig. 16 (b) presents an analog analysis, for the influence of grid current angle and modulation index in the pu value of the RMS value of battery current. Again, it can be seen that the largest current amplitudes are reached under conditions of unity power factor ($\phi_g = 0$, $-\pi$ or π). Furthermore, the higher the modulation index, the higher the expected battery current value. Under operating conditions with non-unitary power factor, theoretically, dc components do not appear, but ac components are present, which reflect a non-zero RMS value. In Fig. 16 (b) is possible to verify two points with a minimum value of RMS battery current ($\phi_g = \frac{-\pi}{2}$ or $\frac{\pi}{2}$).

Based on the equation (2.38), the battery temperature variation (directly related to the ohmic power dissipated in the battery resistance) in the case with and without battery current ripple suppression can be calculated as follows, respectively:

$$\begin{cases} \Delta T_{bat,w/sup} = R_{th,bat} R_{bat} \left(i_{bat,w/sup}\right)^2, \\ \Delta T_{bat,w/osup} = R_{th,bat} R_{bat} \left(i_{bat,w/osup}\right)^2, \end{cases} \tag{2.39}$$

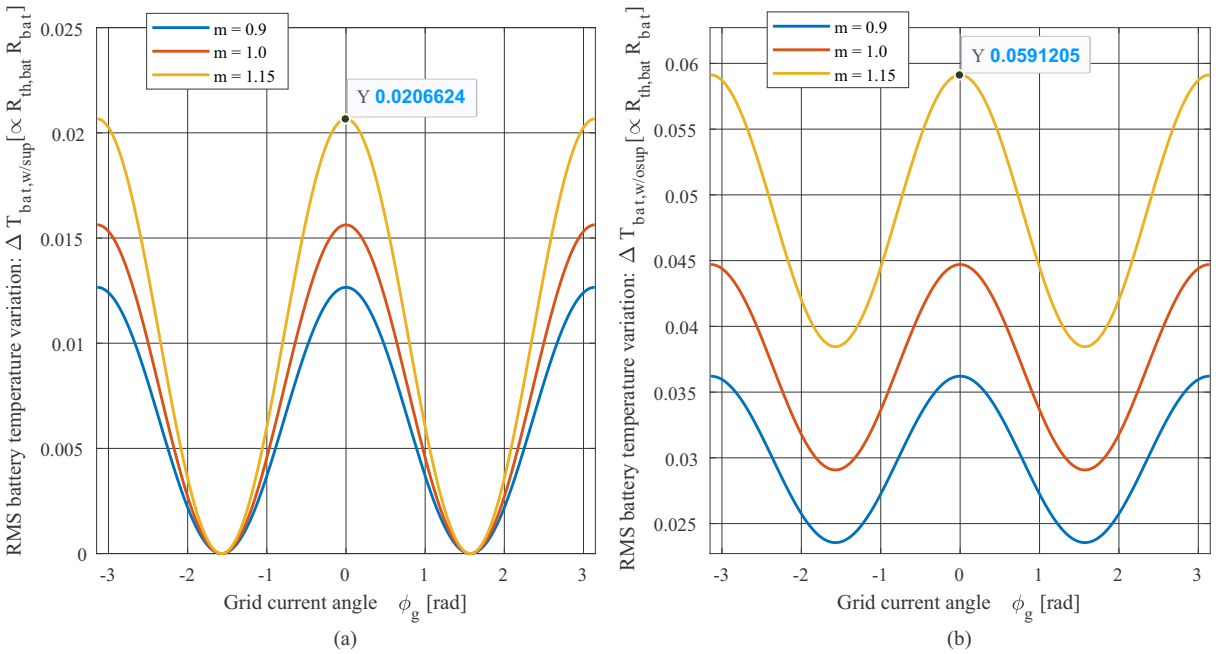
where $R_{th,bat}$ is a battery thermal resistance determined in laboratory tests, in K/W, and R_{bat}, is the battery ohmic resistance.

Fig. 17 presents an analysis of battery temperature variation in the case with ($i_{bat,w/sup}$) and without ($i_{bat,w/osup}$) battery current ripple suppression.

Fig. 17 (a) demonstrated the influence of grid current angle and modulation index in the average battery temperature variation. As there is a proportion with the square

of the average battery current, the relative characteristics are preserved in the largest battery temperature variation under conditions of unity power factor ($\phi_g = 0$, $-\pi$ or π). Furthermore, the higher the modulation index, the higher the expected battery current value. Under operating conditions with non-unitary power factor, theoretically, a dc portion of the current circulating in the batteries is not expected, with two points with a zero variation in battery temperature ($\phi_g = \frac{-\pi}{2}$ or $\frac{\pi}{2}$).

Figure 17 – Analysis of battery temperature variation in the case (a) with and (b) without battery current ripple suppression.



Source: own representation.

Fig. 17 (b) presents an analog analysis, for the influence of grid current angle and modulation index in the RMS battery temperature variation. Again, it can be seen that the largest variations are reached under conditions of unity power factor ($\phi_g = 0$, $-\pi$ or π). Furthermore, the higher the modulation index, the higher the expected battery current value. Under operating conditions with a reactive power factor, a non-zero RMS value is obtained. In Fig. 17 (b) is possible to verify two points with a minimum value of battery temperature variation ($\phi_g = \frac{-\pi}{2}$ or $\frac{\pi}{2}$).

Based on the maximum values of battery temperature variation, expressed in the Fig. 17, a minimum relationship between $\Delta T_{bat,w/sup}$ and $\Delta T_{bat,w/osup}$ can be obtained as follows:

$$\frac{\Delta T_{bat,w/osup}}{\Delta T_{bat,w/sup}} = \frac{0.0591205}{0.0206624} = 2.86 \tag{2.40}$$

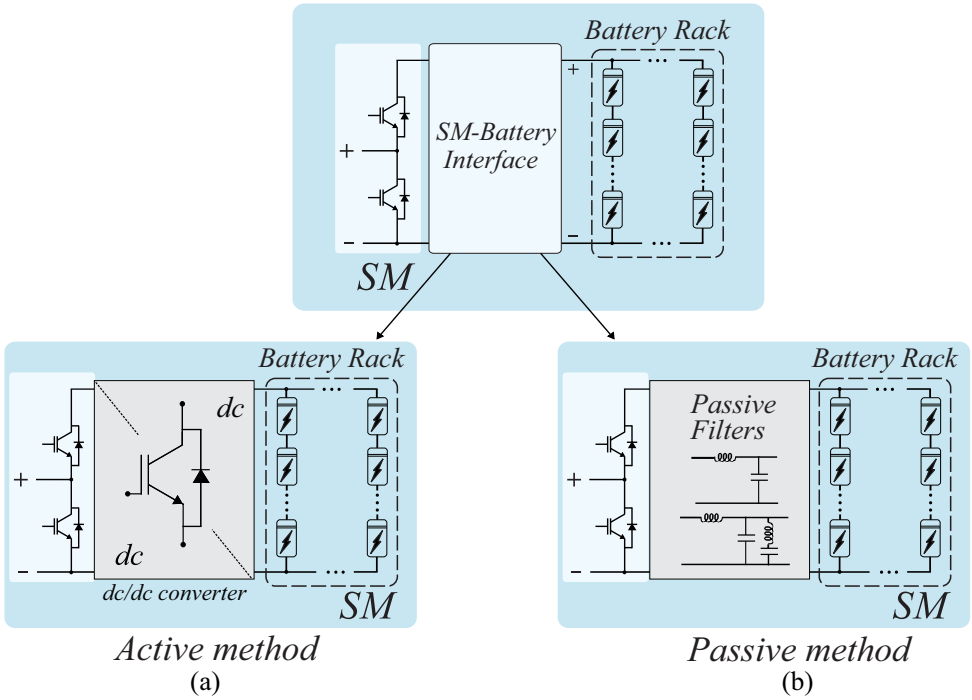
It is worth noting that the condition expressed previously occurs when $\phi_g = 0$ rad, as discussed in Pinto (2022). For other conditions, the relationship between $\Delta T_{bat,w/sup}$ and

$\Delta T_{bat,w/osup}$ will be equal or greater, revealing a greater problem. It is also worth mentioning that in terms of charging and discharging the batteries, the ac components verified have no role in this process. In this sense, passive strategies are introduced, employing passive filters, and active strategies, employing dc/dc converters, to improve aspects of the reliability of the MMC-based BESS.

2.4 Integrating Battery into MMC SM

In most literature, the harmonic suppression in battery current is solved using dc/dc converts as active interfaces between battery and SM, as presented in Fig. 18(a). This work also investigates a passive filter arrangement as an alternative solution to the dc/dc converters, as shown in Fig. 18(b).

Figure 18 – Analysis of battery integration in SM with suppression technique: (a) active method with dc/dc converter; (b) passive method with passive filter.



Source: own representation.

In this sense, the batteries are interfaced with the SM using a passive filter with a low-pass filter that attenuates the first component and its harmonics. Similar works in literature, (Novakovic; Nasiri, 2017; Saari; Ryynänen; Lindfors, 2012; Wersland; Acharya; Norum, 2017) concluded that this passive technique could be an attractive solution, especially where high reliability is of concern.

2.4.1 BESS Arrangement

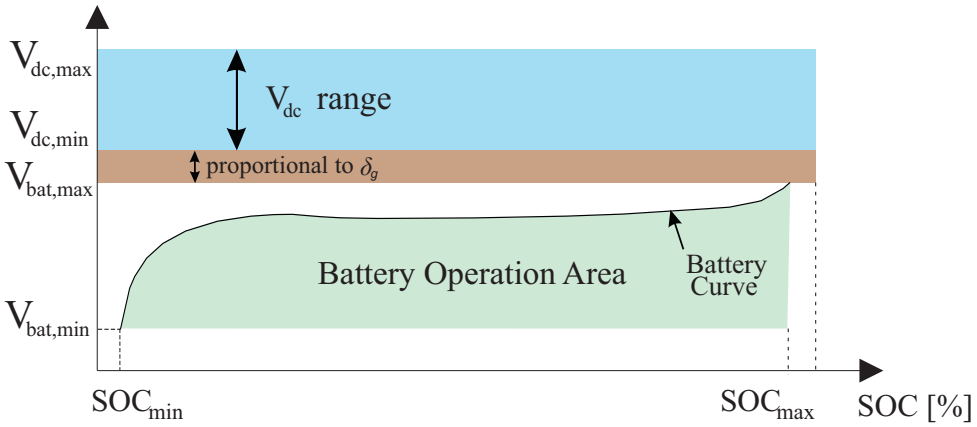
The battery operates between the minimum and maximum voltage defined by the minimum and maximum SOC specifications (SOC_{min} and SOC_{max}, respectively). In addition, the output voltage of the MMC also presents a range of operations. The minimum required output voltage which guarantees the connection to the grid is chosen based on the methodology proposed by Cupertino et al. (2020):

$$V_s = 1.05\hat{V}_g(1 + \Delta V_g + x_{pu} I_{g,pu}), \tag{2.41}$$

where $\hat{V}_g$ is the peak of the line-to-line neutral voltage, ΔV_g is the maximum ac grid voltage variation (in pu), $I_{g,pu}$ is the maximum ac grid current (in pu), and x_{pu} is the unit equivalent output impedance of the MMC. The minimum dc-link voltage is adopted with a margin of 5% (1.05 factor), according to (ABB, 2013; Lima; Rabello, 2023).

The inclusion of the voltage margin (δ_g) between the maximum battery voltage and minimum dc-link voltage of the SM can be adopted in the case of the use of a dc/dc converter between SM and batteries. The voltage range of the battery bank and the dc-link voltage of the SM are presented in Fig. 19. This margin guarantees a better performance during the battery charging and discharging processes.

Figure 19 – Voltage limits of the MMC dc-link and battery bank.



Source: adapted from (Amorim et al., 2024).

The number of batteries in series per string is given by [3]:

$$N_{s,bat} = \text{floor}\left(\frac{V^*_{SM}}{V_{bat,max}\delta_g}\right). \tag{2.42}$$

where V^*_{SM} is the reference SM voltage that must be higher than the battery voltage and lower than the power module maximum voltage (recommended by the manufacturer). It is

[3] where δ_g is equal to 1 if the dc/dc stage is not included and is greater than 1 if the dc/dc stage is included. In this work, $\delta_g = 1.05$ is considered according to (Pinto, 2022).

worth highlighting that the number of battery racks in series is computed using the floor function to avoid the maximum battery rack voltage exceeding V_{100FIT}[4].

The MMC must be able to synthesize V_s in the limit region of the modulator. The sum of the capacitor voltages ($\sum v_C$) is obtained from V_s. This relationship depends on the topology and the modulation strategy used. In this way, the sum of the capacitor voltages of each arm when using the Sinusoidal Pulse Width Modulation (SPWM) is $2V_s$ (Pinto, 2022). Another interesting approach that makes it possible to extend the linear region of the modulator is to consider 1/6 third harmonic injection (Pinto, 2022). Thus, the sum of the capacitors is equal to $\sum v_C = \sqrt{3}V_s$. In this sense, the number of SM per arm, N, is computed by:

$$N = \text{ceil}\left(\frac{\sum v_C}{N_{s,bat}V_{b,min}}\right), \tag{2.43}$$

The number of parallel battery strings must fulfill two requirements. The first criterion assumes that the batteries must have the capacity to inject the rated power into the grid. Accordingly:

$$N_{p,1} = \text{ceil}\left(\frac{P_{B,n}}{6NV_{b,min}C_rC_n}\right), \tag{2.44}$$

where $P_{B,n}$ is the nominal battery bank power, C_r is the recommended discharging rate and C_n is the battery nominal capacity. The second criterion assumes that the batteries must fulfill the energy storage requirements for the ancillary service application. Accordingly

$$N_{p,2} = \text{ceil}\left(\frac{100E_{B,n}}{6NE_{bat}N_s(SOC_{max} - SOC_{min})}\right), \tag{2.45}$$

where $E_{B,n}$ is the battery bank energy storage, E_{bat} is the unit battery energy storage, SOC_{max} is the maximum SOC value of batteries and SOC_{min} is the minimum SOC value of batteries. Finally, the number of battery strings is given by:

$$N_p = \max\left(N_{p,1}; N_{p,2}\right), \tag{2.46}$$

Comparing the value of the battery C-rate with the C-rate requirement, it is possible to obtain the following condition for evaluating which criterion (power or energy) will prevail for decision-making in the N_p calculation:

$$N_p = \begin{cases} N_{p,1}, \text{ if } C_{r,apl} > C_{r,bat}, \\ N_{p,2}, \text{ if } C_{r,apl} < C_{r,bat}, \end{cases} \tag{2.47}$$

[4] FIT (Failure In Time) is a unit that represents failure rates and how many failures occur every 10^9 hours.

where $C_{r,bat}$ is the maximum battery discharging rate and $C_{r,apl}$ is the C-rate application requirement.

In this sense, according to Amorim et al. (2024) the power criterion defines the number of strings in cases where the batteries adopted in BESS have a discharging rate lower than the C-rate requirement (due to the increase of strings to obtain the BESS nominal power). On the other hand, if the battery discharging rate is higher than the C-rate requirement, the energy criterion defines the number of strings (due to the increase of strings to obtain the BESS nominal energy). Finally, if the battery discharging rate is equal to the C-rate requirement, the definition of the number of strings is given by the highest value between the power and energy criterion.

2.4.2 SM Components Design

After developing the battery rack design, the next step is to perform calculations related to passive components, such as SM capacitance, arm inductance, and semiconductors (IGBT and diodes). The SM capacitance is defined as follows:

$$C = \frac{W_{conv} S_n}{3000 N (V_{SM}^*)^2} \tag{2.48}$$

where W_{conv} is the MMC energy storage requirements given in kJ/MVA and S_n is the MMC nominal power. According to Harnefors et al. (2013), the value of 40 kJ/MVA guarantees a maximum capacitor voltage ripple equal to 10%, which is typical for MMC topology. It should be noted that the SM capacitance selection is performed considering that the system can operate as STATCOM even if batteries are not available (Pinto, 2022).

According to Soong and Lehn (2016), in the MMC-based BESS, shorter battery strings are preferable to increase the system's reliability. Therefore, the authors concluded that in an MMC-based BESS the battery bank can be turned off up to 33% of batteries without affecting the energy exchange of the MMC with the grid.

The L_{arm} attenuates the high-frequency components in the arm current and smooths the circulating current. Thus, the L_{arm} can be expressed by:

$$L_{arm} = x_{arm} \frac{\hat{V_g}^2}{\omega_g S_n} \tag{2.49}$$

where x_{arm} is the per unit value of arm reactance and ω_g is the grid angular frequency. According to Sharifabadi et al. (2016), the typical values of arm inductance can vary in the range of 0.05 to 0.15 per unit (up), where in this work 0.15 pu is adopted.

The determination of maximum arm current value is important to select the MMC semiconductor devices and inductor devices (Cupertino et al., 2018b). As previously

discussed, at balanced conditions of MMC operation, the circulating current can be neglected. Based on this consideration, the maximum value of arm current is expressed by (Cupertino et al., 2018b):

$$\max(i_{u,n}) = \max(i_{l,n}) = \frac{\max(i_{g,n})}{2} = \frac{S_n}{\sqrt{6}\hat{V}_g} \tag{2.50}$$

It is worth mentioning that the equation (2.50) reflects a simplification for operation with only reactive power factor, as in a STATCOM. In situations of active power applications, such as in MMC-based BESS, the maximum current values are directly dependent on the value of the operating power factor.

Finally, the RMS current value in semiconductor devices can be calculated as follows (where the current stresses in semiconductor devices do not depend on the MMC modulation index - m) (Cupertino et al., 2018b):

$$i_{IGBT,rms} = i_{Diode,rms} = \frac{\hat{I}_g}{4\sqrt{2}}. \tag{2.51}$$

2.5 Chapter Summary

In this chapter, the MMC topology, modeling, control strategy, and design for the MMC-based BESS are presented. The MMC-based BESS control strategy was discussed, emphasizing the need to control the grid, circulating current, and SOC balancing. The ancillary service performed by BESS is directly inserted into the SOC balancing control, through the requirements established by the grid code. It has been demonstrated that several variables can influence the MMC design, demonstrating aspects of batteries and passive components such as inductors and capacitors. Furthermore, an analytical evaluation of the battery current is demonstrated, emphasizing undesirable first, second, and fourth harmonic components. Strategies for integrating batteries into SMs are discussed as active and passive methods to mitigate such harmonics.

Based on the presentation of the MMC-based BESS topology, modeling, control strategy, and design, the development of MPE is presented in Chapter 3. In this sense, in the next chapter concepts of the topology, modeling, control strategy, and design for the MPE are explored. The results of a small-scale prototype will be discussed, with simulation and experimental results, highlighting its requirements and operating limits for implementing the MPE experimentally.

3 MPE for MMC-based BESS: Control Strategy and Design

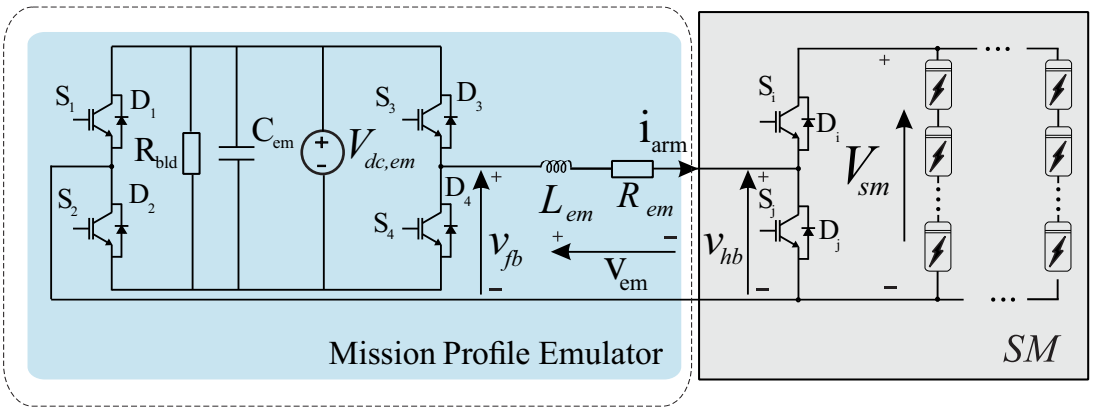
This chapter describes the modeling, control, and design of the MPE based on a full-bridge converter. Initially, the MPE structure, parameters, and current control parameters selection are presented. Then, MPE inductance design and basic dynamic equations are introduced. In addition, the control tuning and modulation strategies are presented.

A small-scale prototype is developed and presented in terms of technical discussion of module design. Considerations about the dc-link voltage, and components design are presented. Discussions on simulated results of a full-scale MMC system are compared with an MPE with equivalent parameters. Furthermore, the typical voltage and current waveforms verified in the MPE on a low scale are validated, also analyzing the typical spectrum. Finally, the effects of the switching frequency of the MPE and SM converters are analyzed and the approximations of the MPE empirical equations are compared.

3.1 MPE Structure and Parameters

An MPE based on a full-bridge converter is used to emulate the MMC arm current in steady-state, as shown in Fig. 20.

Figure 20 – Basic structure of a mission profile emulator connected to the SM under test.



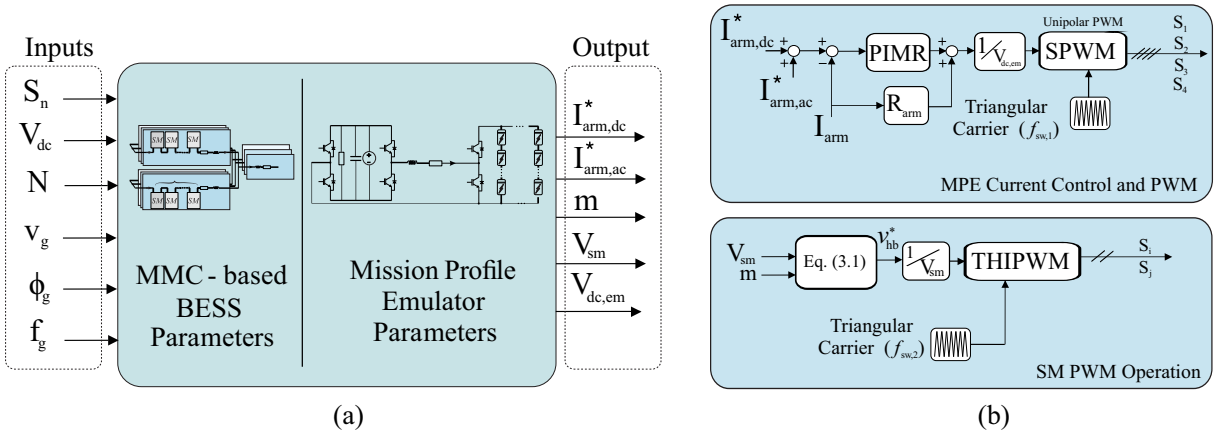
Source: own representation.

The MPE is composed of a current-controlled full-bridge converter and an inductor. The MPE components are defined in terms of the dc supply voltage source ($V_{dc,em}$), the output capacitance of the supply voltage source (C_{em}), and the bleeder resistor for battery discharge test (R_{bld}) - if the supply voltage source is not bidirectional. The full-bridge

converter switches are identified by (S_1, S_2, S_3, S_4, D_1, D_2, D_3 and D_4). Finally, the SM is connected to the SM through the MPE inductance (L_{em}) and the inductor resistance (R_{em}).

The MMC-based BESS parameters and operational conditions are the input variables used to derive the MPE parameters, as shown in Fig. 21 (a).

Figure 21 – Control scheme of the proposed MPE: (a) representation of input variables based on MMC-based BESS parameters and output variables based on MPE parameters (b) MPE current control and SM PWM operation.



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The MMC-based BESS parameters, such as nominal power (S_n), dc-link voltage (V_{dc}), number of SM (N), and operational conditions, such as power factor ($\cos(\phi_g)$), grid frequency (f_g) and grid voltage (v_g) are converted to the MPE parameters: dc arm current reference ($I^*_{arm,dc}$), ac arm current reference ($I^*_{arm,ac}$), modulation index (m), SM voltage reference (V_{sm}), and dc supply voltage ($V_{dc,em}$). It is worth mentioning that the outputs indicated in Fig. 21 (a) are valid to emulate the steady-state behavior of the MMC-based BESS and can be obtained separately as discussed in Yang, Wang and Ma (2020b).

It is important to note that the arm reference current is divided into two components (dc and ac). This division is justified by the fact that the arm current may present dc components in the situation where the MMC has the connection of batteries into the dc-link, such as the HVDC application, and may present ac components in situations where the batteries are arranged in the SM (Sharifabadi et al., 2016). In this sense, the MPE could emulate this type of application as well, increasing its flexibility in terms of reliability studies for other applications.

The MPE current control and SM PWM operation are presented in Fig. 21 (b). The MPE output current is regulated by a proportional-integral multi-resonant (PIMR) controller. Regarding the modulation strategy, sinusoidal pulse width modulation (SPWM) with unipolar switching is employed. The triangular carrier frequency of the full-bridge converter is denoted by $f_{sw,1}$. In addition, the SM voltage control is performed with the

third harmonic injection to increase the linear region of the modulator (Cupertino et al., 2018b). This approach is known as the third harmonic injection pulse-width-modulation (THIPWM) (Pinto et al., 2022). The triangular carrier frequency of the SM is denoted by $f_{sw,2}$. In the simulation of the full-scale MMC-based BESS, the classic equations of the MMC in steady-state are implemented, as presented in Cap. 2.

The half-bridge output voltage reference (v_{hb}^{*}) is obtained from the equation that relates the arm voltage (v_{arm}) synthesized in the MMC. In this sense, the half-bridge output voltage is given as a function of the full-scale MMC-BESS parameters. Without loss of generality, the upper arm of phase a is considered in the mathematical modeling. Accordingly (Cupertino et al., 2018b):

$$v_{hb}^{*} = \frac{V_{sm}}{2} - m\frac{V_{sm}}{2}\cos(\omega_g t) + m\frac{V_{sm}}{12}\cos(3\omega_g t), \tag{3.1}$$

where V_{sm} is the SM nominal voltage, m is the modulation index, and ω_g is the angular grid frequency. The analyses performed are referred to as the converter phase a, which results in angular displacement equal to zero degrees in the v_{hb}^{*}. The same analysis can be applied to the other phases.

The circulating current in an MMC-based BESS application has a significant second harmonic component that affects the SM voltage ripple and semiconductor losses (Cupertino et al., 2018b). The MMC circulating current control inserts damping in the converter dynamic response through a proportional and resonant controller tuned in the second harmonic. In this sense, the second harmonic current suppression is implemented only in the MMC simulation. The MPE design approach assumes that the circulating current control works properly, i.e., the second harmonic component is suppressed. Thus, the arm current reference in MPE is based on the analytical expression for an arm current in full MMC-based BESS (Cupertino et al., 2018b). Accordingly:

$$i_{arm}^{*} = \frac{i_{dc}}{3} + \frac{\hat{I}_{g,n}}{2}\cos(\omega_g t - \phi_n), \tag{3.2}$$

where i_{dc} is the dc-link current, $\hat{I}_{g,n}$ is the amplitude of grid current in the n-th converter phase and ϕ_n is the power angle in the n-th converter phase. For the decentralized connection of batteries in the SM of the MMC, as presented in Fig. 8 (d), the i_{dc} is equal to 0, during MMC balanced operation (Chaudhary et al., 2020).

3.2 Current Control Parameters Selection

The transfer function that relates the output voltage of the full bridge (v_{fb}) with the arm current (I_{arm}) that flows through the MPE inductor is given by:

$$\frac{I_{arm}(s)}{v_{fb}(s)} = \frac{1}{L_{em}s + R_{em}}, \tag{3.3}$$

where L_{em} is the MPE inductance and R_{em} its resistance. Therefore, the open-loop transfer function ($G_i(s)$) is given by:

$$G_i(s) = \left(k_p + \frac{k_i}{s} + \frac{k_{r,1}}{s^2 + \omega_{r,1}^2} + \frac{k_{r,3}}{s^2 + \omega_{r,3}^2}\right)\left(\frac{1}{sT_{sw,MPE} + 1}\right)\left(\frac{1}{sL_{em} + R_{em}}\right), \tag{3.4}$$

where k_p, k_i and k_r are the proportional, integral and resonant gains, respectively, $T_{sw,MPE}$ is the switching period of the MPE, $\omega_{r,1}$ is the resonant frequency at ω_g and $\omega_{r,3}$ is the resonant frequency at $3\omega_g$. The resonant module in the third harmonic is explained by the single-phase topology of the MPE that does not cancel this harmonic in the arm current, as is verified in the three-phase implementation of the MMC-based BESS.

The implementation delay caused by the modulator and sampling of the arm current is approximated by the first-order transfer function, for a double-updated acquisition, $\tau = T_{sw,MPE}$[1] (Pinto, 2022).

The proportional, integral, and resonant gains are computed based on Holmes et al. (2009), Peña-Alzola et al. (2014), which proposes to maximize the control bandwidth based on a given phase margin (ϕ_{pm}). This methodology leads to the following tuning formulas:

$$k_p = \frac{L_{em}(\frac{\pi}{2} - \phi_{pm})}{T_{sw,MPE}}, \tag{3.5}$$

$$k_i = \frac{10R_{em}f_{sw,MPE}}{3}, \tag{3.6}$$

$$k_{r,1} = k_{r,3} = \frac{k_p(\frac{\pi}{2} - \phi_{pm})}{20T_{sw,MPE}}. \tag{3.7}$$

A phase margin of (ϕ_{pm}) approximately 60 degrees is assumed for the implementation of arm current control in simulation results and approximately 30 degrees in experimental results (Amorim et al., 2022).

Assuming that the typical frequency of switching devices in SM is in the range of 150-2000 Hz (Sharifabadi et al., 2016; Wang et al., 2019a), for the pulse-width modulation (PWM) methods, the MPE can require switching frequencies in the order of 1.5 kHz to 20 kHz (i.e., at least ten times greater than the typical range observed in the SM of the MMC). However, little has been discussed and explored in the literature about the order

[1] as the operating frequency of the control loop is 2 times that of the PWM, then the delay is 1/2 $T_{sw,MPE}$ of the microcontroller + 1/2 $T_{sw,MPE}$ of PWM = $T_{sw,MPE}$.

of magnitude of this proportion and the operational limitations of these frequencies to obtain a good arm current emulated in the MPE. At the end of this chapter, experimental observations will be made in this sense, to analyze the operating limits of the SM and MPE switching frequencies.

To equate and simplify the design of the MPE inductance, initially, an MPE switching frequency of ten times the SM switching frequency is adopted. The condition of the MPE switching at a higher frequency than that typically found in the MMC's SM can be explained to reduce the MPE inductance, as discussed in Tang et al. (2016b), Tang et al. (2016a). In this way, the maximum value found in the typical frequency of the MMC is adopted. Thus, the disturbances caused by the commutation of the SM converter do not affect the control of the average arm current. In the next section, the MPE inductance design is discussed based on the considerations presented.

3.3 MPE Inductor Design

The design of the MPE inductor is based on the maximum current ripple present in the arm current emulated by the full-bridge converter. In this sense, a relationship between the time that the semiconductor devices are turned on in the full-bridge converter ($t_{on,1}$ and $t_{on,3}$) and the SM under test ($t_{on,i}$) can be derived to estimate the maximum ripple magnitude.

Fig. 22 shows the estimated arm current ripple obtained for the instants where the SM is bypassed (S_i OFF), as presented in Fig. 22 (a) and (c), and the instants where the SM is inserted (S_i ON), as presented in Fig. 22 (b) and (d). Additionally, the Fig. 22 details the situation where $d_1 > d_3$, as presented in Fig. 22 (a) and (b), and $d_1 < d_3$, as presented in Fig. 22 (c) and (d).

Fig. 23 shows the equivalent circuit for different switch states of full-bridge and half-bridge converter and generated arm current, where the lines highlighted in red represent the direction of conduction of the arm current in the MPE. The four cases presented are given by:

- SM bypassed and $d_1 > d_3$, Fig. 23 (a);
- SM inserted and $d_1 > d_3$, Fig. 23 (b);
- SM bypassed and $d_1 < d_3$, Fig. 23 (c);
- SM inserted and $d_1 < d_3$, Fig. 23 (d);

According to Fig. 22 (a) and (c), the arm current derivative is negligible in the situation where the state of switches S_1 and S_3 are both high or low. Furthermore, the

Figure 22 – Switch state of full-bridge and half-bridge converter and generated arm current: (a) SM bypassed and $d_1 > d_3$ (b) SM inserted and $d_1 > d_3$ (c) SM bypassed and $d_1 < d_3$ (d) SM inserted and $d_1 < d_3$.

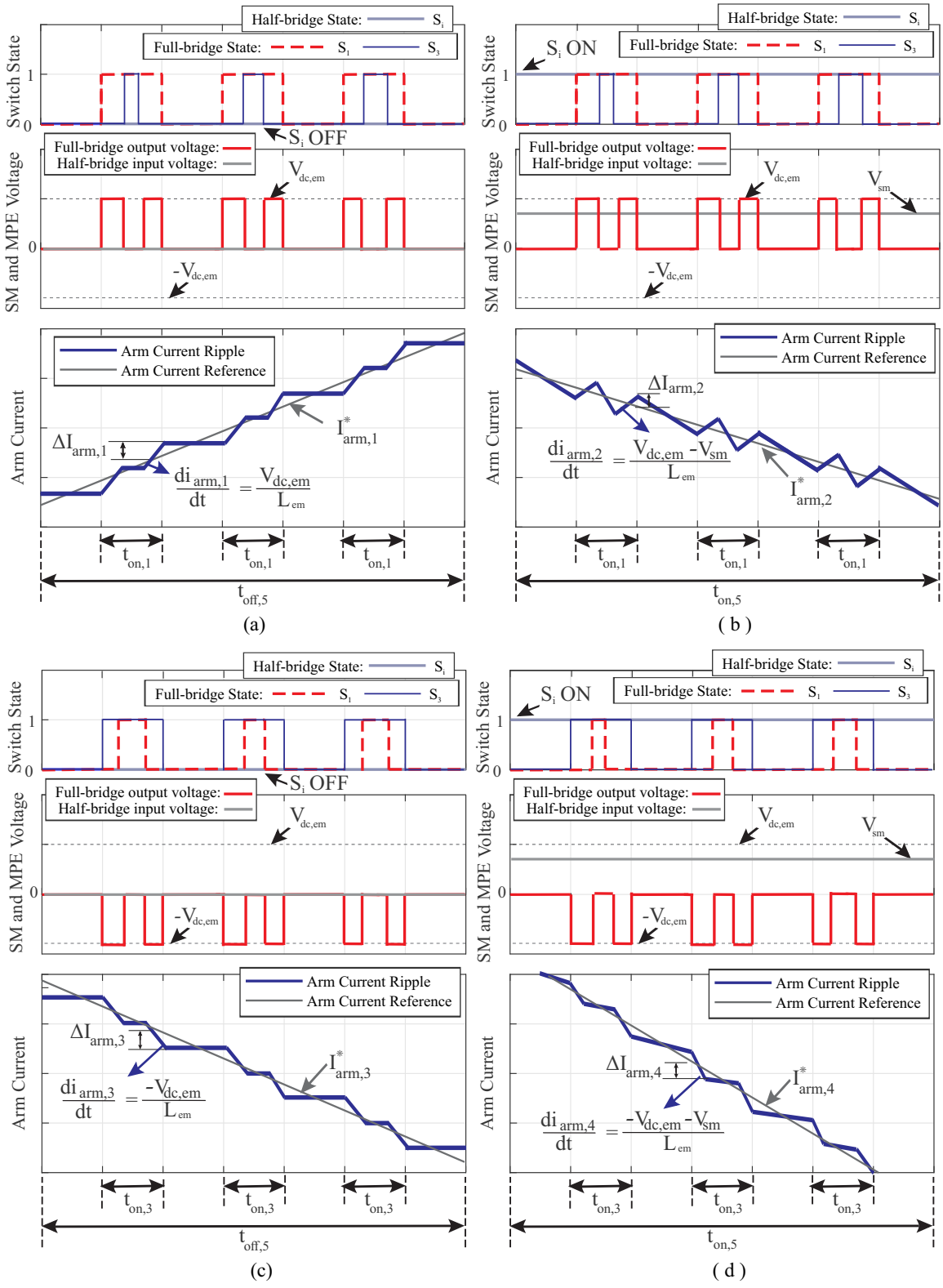

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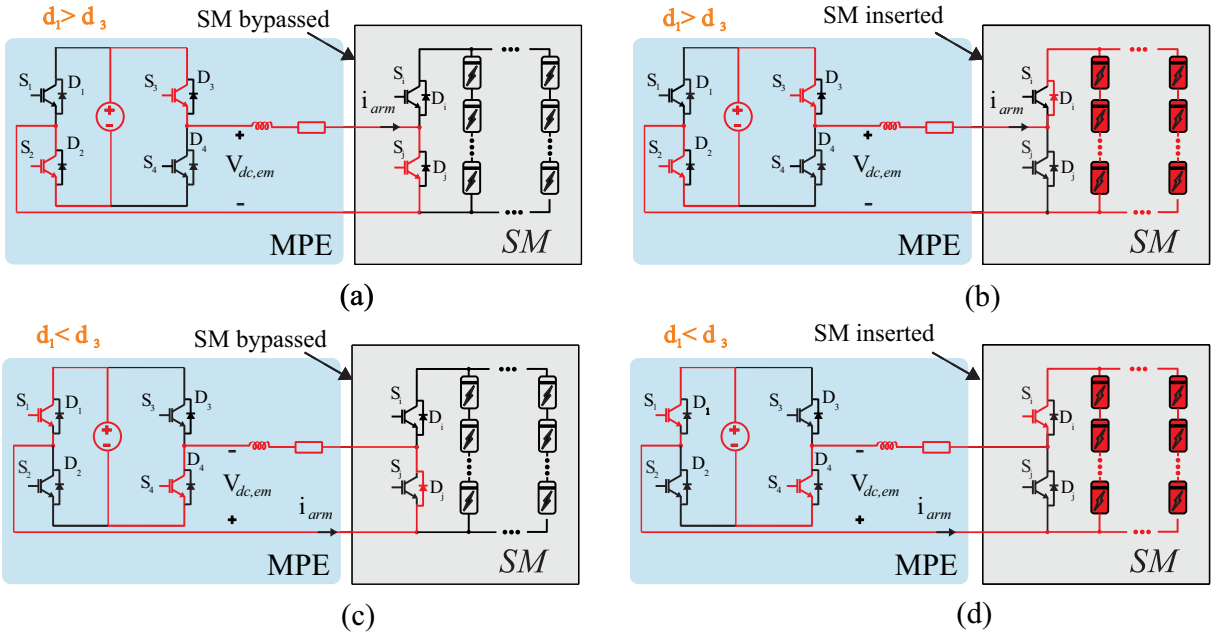
Figure 23 – Equivalent circuit for different switch state of full-bridge and half-bridge converter and generated arm current: (a) SM bypassed and $d_1 > d_3$ (b) SM inserted and $d_1 > d_3$ (c) SM bypassed and $d_1 < d_3$ (d) SM inserted and $d_1 < d_3$.



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considerable inductor current ripple is defined for the instant where the emulator dc-link is applied on the ac side, being submitted to the emulator dc-link voltage and limited by the MPE inductor.

Similarly, the analysis can be performed for the instances where the SM is inserted. In this situation, zero current variation does not occur due to the voltage difference between the emulator output voltage and SM voltage. The maximum derivative is defined for the instant when the SM and the dc-link emulator are inserted, leading to the maximum ripple magnitude (Jiang et al., 2021; Yang et al., 2019b).

The duty cycle of full-bridge converter (d_1 and d_3, related with switch S_1 and S_3, respectively) and SM under test (d_i, related with switch S_i) can be defined by:

$$d_1 = \frac{t_{on,1}}{T_{sw,MPE}} \ , \ d_3 = \frac{t_{on,3}}{T_{sw,MPE}} \ \text{ and } \ d_i = \frac{t_{on,i}}{T_{sw,SM}}, \tag{3.8}$$

where $t_{on,3}$ is the time that the switch S_3 are turned on, $t_{on,i}$ is the time that the switch S_i are turned on, $T_{sw,MPE}$ is the switching period of the switches S_1 and S_3 and $T_{sw,SM}$ is the switching period of the switch S_i. Additionally, the MPE global duty cycle (d_{em}) can be defined as the relationship between emulator dc-link and SM voltage:

$$d_{em} = \frac{V_{dc,em}}{V_{sm}}. \tag{3.9}$$

The relationship between the MPE global duty cycle and the duty cycle of the full-bridge converter can be given as a function of the derivative of the arm current, the SM voltage, and the emulator dc-link voltage. Accordingly:

$$d_1 - d_3 = \left(V_{sm} + L_{arm}\frac{di_{arm}}{dt}\right)\frac{1}{V_{dc,em}} = d_{em} + \frac{L_{arm}}{V_{dc,em}}\frac{di_{arm}}{dt}. \tag{3.10}$$

The maximum ripple magnitude is defined as the maximum difference between the reference arm current and the arm current generated due to inserting/bypassing the emulator dc-link. Thus, based on Fig. 22, four situations of maximum ripple magnitude can de be considered:

$$\Delta I_{arm} = \max\left(\Delta I_{arm,1}, \Delta I_{arm,2}, \Delta I_{arm,3}, \Delta I_{arm,4}\right). \tag{3.11}$$

Once the switching frequency of the full-bridge converter is assumed to be higher than the SM under test ($f_{sw,MPE} \gg f_{sw,SM}$), the maximum arm current ripple can be computed considering the instant where the SM and the dc-link emulator are inserted, leading to a greater deviation of the arm current, concerning the reference arm current (Jiang et al., 2021), as shown in Fig. 22 (b). In addition, the maximum current ripple (illustrated by $\Delta I_{arm,2}$) occurs at approximately half of the switching period of the full-bridge converter, as discussed in (Jiang et al., 2021). Accordingly:

$$\Delta I_{arm} = \Delta I_{arm,2} \approx \left(\frac{V_{dc,em} - V_{sm}}{L_{arm}} - \frac{di_{arm}}{dt}\right)\frac{d_1 - d_3}{2f_{sw,MPE}}. \tag{3.12}$$

Rearranging the terms of (3.12) and replacing the relation (3.10) in (3.12), the following relation is obtained:

$$\Delta I_{arm} \approx \left[1 - (d_1 - d_3)\right](d_1 - d_3)\frac{V_{dc,em}}{2L_{em}f_{sw,MPE}}. \tag{3.13}$$

In this sense, the emulator inductance (L_{em}) is obtained by rearranging the terms in (3.13):

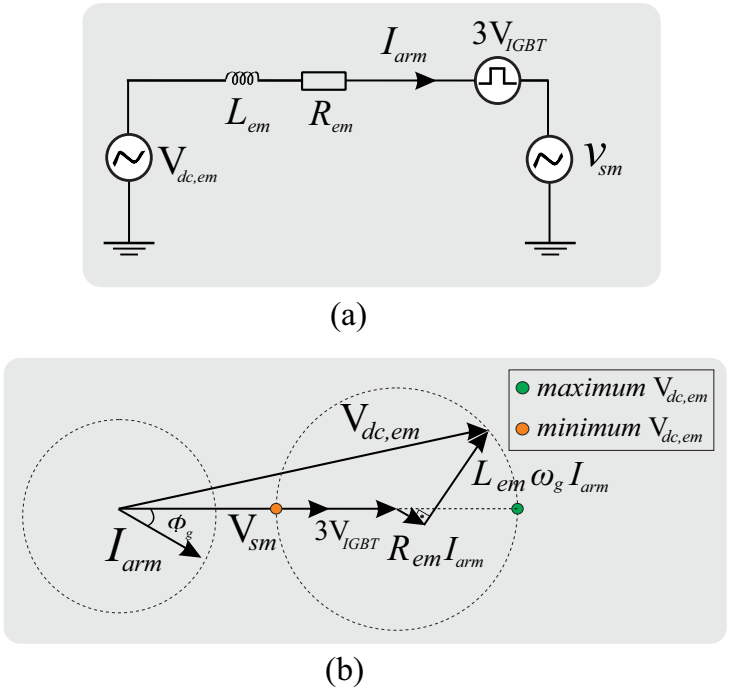
$$L_{em} \approx \left[1 - (d_1 - d_3)\right](d_1 - d_3)\frac{V_{dc,em}}{2\Delta I_{arm}f_{sw,MPE}}. \tag{3.14}$$

In addition, it is noteworthy that the other cases of arm current variations ($\Delta I_{arm,1}$, $\Delta I_{arm,3}$ and $\Delta I_{arm,4}$), despite imposing a higher rate in nominal terms, occur in events with times shorter than the situation presented in $\Delta I_{arm,2}$, according to Jiang et al. (2021).

The maximum current ripple is defined for the instant where the derivative of the equation obtained in (3.14), concerning $d_1 - d_3$, is equal to zero. Thus, for the instants where $d_1 - d_3 = 0.5$, the L_{em} is defined.

The MPE for the MMC-based BESS average model and the phasor diagram are illustrated in Fig. 24 (a) and (b), respectively. As observed, $v_{dc,em}$ varies according to the operating angle of the MMC (ϕ_g). The dc-link voltage emulator must be set considering the voltage level of the SM, as well as the voltage drop in the semiconductor devices and the maximum values of di/dt values imposed by the MPE (Tang et al., 2016b; Wang et al., 2019b).

Figure 24 – MPE for MMC-based BESS: (a) average model; (b) phasor diagram.



Source: own representation.

Since the MPE can operate with several converter angles, such as in the charging and discharging process, $\phi_g = 0°$ and $\phi_g = 180°$, respectively, and injecting reactive power ($\phi_g = 90°$ or $\phi_g = -90°$), the dc-link voltage emulator must comply with all possible operations. In this sense, the maximum voltage value is adopted for MPE development. According to Fig. 24 (b), the maximum voltage of $V_{dc,em}$ is given at the point highlighted in green, where the phasors of the SM voltage, IGBT voltage, and voltage drop across the arm inductor and its resistance are in phase (that is, a converter angle equal to zero $\phi_g = -90°$). Also, it is worth noting that the lowest value of the dc-link voltage emulator is given for operation with a converter angle equal to $\phi_g = 90°$. Accordingly:

$$V_{dc,em} \geq V_{sm} + L_{em}\omega_g I_{arm} + 3V_{IGBT}, \tag{3.15}$$

where I_{arm} is the peak of arm current and V_{IGBT} is the collector-emitter conduction voltage of IGBTs. The IGBT voltage value is adopted as a reference because it has a greater voltage drop than the diode in the ON state, for the semiconductors devices adopted in the

case study. Also, the multiplicative value equal to 3 refers to the state in which two IGBTs of the full-bridge conductor are conducting and one IGBT of the half-bridge converter is conducting.

3.4 Simulation Analysis - MMC-based BESS and MPE

The performance of the MPE is compared with a full-scale MMC system simulation of 10.9 MVA/13.8 kV and 12.6 MWh of BESS, similar to the MMC-based BESS implemented in Pinto (2022). The grid frequency is equal to 60 Hz and the MMC is considered an arm inductance of 7.6 mH (0.15 pu). The nearest level control (NLC) for SM voltage balancing is implemented in the full-scale MMC-based BESS simulation (Sharifabadi et al., 2016). For the SM capacitor design, an energy requirement of 40 kJ/MVA is considered [2] (Gherard et al., 2020), leading to a SM capacitance of 15 mF. The simulation results are developed in the PLECS platform. The main parameters for the MMC-BESS simulation are shown in Table 4.

Table 4 – Main System Parameters of the MMC-based BESS Simulation.

Parameters	Symbol	Value
Rated apparent power [MVA]	S_n	10.9
Rated reactive power [Mvar]	Q_n	10.9
Rated active power [MW]	P_n	10.9
Total energy storage [MWh]	E_n	12.6
rms Output voltage (line to line) [kV]	$V_{g,l-l}$	13.8
dc-link voltage [kV]	V_{dc}	28
Grid frequency [Hz]	f_g	60
Arm inductance [mH]	L_{arm}	7.6
SM capacitance [mF]	C	15
Number of SMs per arm	N	15
Nominal SM voltage [kV]	V_{sm}^*	1.87
Number of battery rack in series per SM	$N_{s,bat}$	2
Number of battery rack strings per SM	N_p	1

The battery rack P3-R070 manufactured by Samsung was considered in the MMC-based BESS implementation (SAMSUNG, 2018). The battery rack parameters are presented in Table 5.

In addition, the main system parameters used in the MPE simulation are shown in Table 6, considering the same ratings of the SM voltage, grid frequency, arm current, and arm inductance observed in the full MMC-BESS system simulation.

The values obtained for the MPE arm inductance and the dc-link voltage emulator are calculated based on the parameters in Tab. 6 applied in equations (3.14) and (3.15), respectively. Based on the MPE parameters presented in Tab. 4 and Tab. 6, the PIMR

[2] It is worth noting that the proposed requirement increases the costs related to the SM capacitance, however, this approach aims to increase the flexibility of the MMC operation in the event of a battery bank failure in SM, thus maintaining the quality of the MMC output voltage (Pinto, 2022).

Table 5 – Parameters of the Battery Rack P3-R070.

Parameters	Symbol	Value
Power capacity [Ah]	C_n	78
Discharging rate	C_r	0.5
Total energy storage [kWh]	E_n	70
Battery rack voltage at SOC = 100 % [V]	$V_{bat,max}$	992
Battery rack voltage at SOC = 0 % [V]	$V_{bat,min}$	750

Table 6 – Main System Parameters of the MPE Simulation (based on full MMC-BESS simulation).

Parameters	Symbol	Value
Peak ac arm current [A]	$I_{arm,ac}$	309.28
Maximum arm current ripple [%]	$\Delta I_{arm,\%}$	10
MPE arm inductance [mH]	L_{em}	15.11
Switching frequency of the MPE [kHz]	$f_{sw,MPE}$	10
Switching frequency of the SM [kHz]	$f_{sw,SM}$	1
Grid frequency [Hz]	f_g	60
Nominal SM voltage [kV]	V_{sm}^*	1.87
Emulator dc-link voltage [kV]	$V_{dc,em}$	3.5

controller parameters are calculated for the MPE emulating the full MMC-based BESS parameters and testing scheme, as presented in Tab. 7.

Table 7 – PIMR Controllers Parameters.

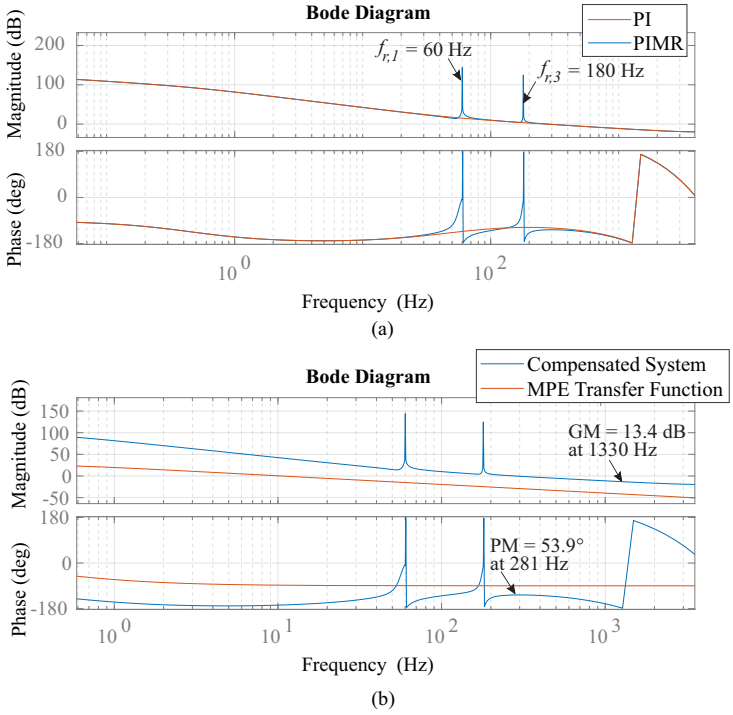
Gains for MPE emulating the MMC-based BESS simulation	Value	Units
Proportional gain (k_p)	25.4	Ω
Integral gain (k_i)	7.8×10^3	Ω/s
Resonant gain ($k_{r,1}$ and $k_{r,3}$)	2.33×10^3	Ω/s
Gains for MPE in testing scheme	**Value**	**Units**
Proportional gain (k_p)	38.6	Ω
Integral gain (k_i)	3.475×10^3	Ω/s
Resonant gain ($k_{r,1}$ and $k_{r,3}$)	2.7×10^4	Ω/s

Fig. 25 (a) shows the Bode diagram for the traditional PI controller and the employed PIMR controller (equation (3.4)) for the full MMC-based BESS simulation gains.

It is possible to check the frequencies tuned to the PIMR controller (1-*st* and 3-*rd* harmonics). In addition, the Bode diagram for the open-loop MPE transfer function and the resulting compensated system (equation (3.3) and (3.3)×(3.4), respectively) is presented in Fig. 25 (b). The control features a gain margin (GM) of 13.4 dB at 1.33 kHz and a phase margin (PM) of 53.9° at 281 Hz. Again it is possible to check the frequencies tuned to the PIMR controller (1-*st* and 3-*rd* harmonics) appearing in the compensated system, which includes the effect of the PIMR controller.

Fig. 26 (a) shows the arm current obtained from the complete simulation of a full MMC-based BESS and MPE simulation. The arm current reference is set to 309.2 A, in both simulations. Fig. 26 (b) shows that the maximum value of the MPE inductor current

Figure 25 – (a) Bode diagram of a traditional PI controller and the employed PIMR controller (b) Bode diagram of the open-loop MPE system and the compensated system.



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ripple is equal to 28.6 A, which corresponds to 9.25% (which is following the maximum limit of 10 % set for the MPE design) of the arm current reference peak.

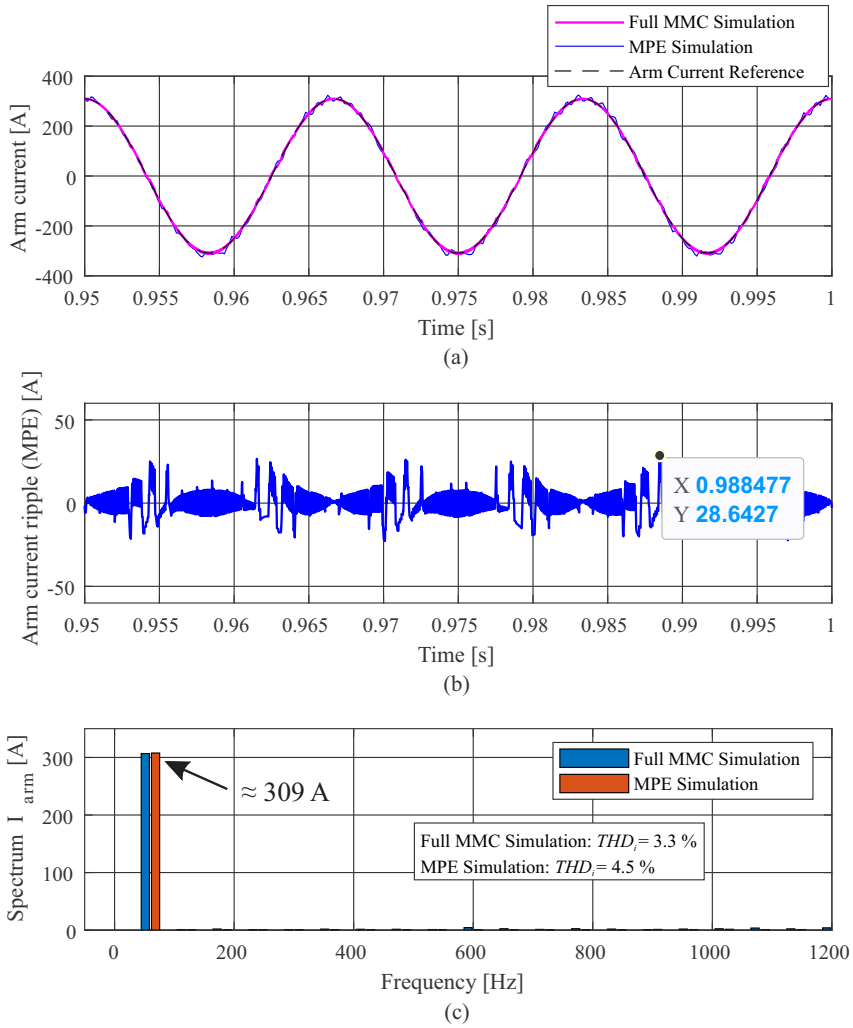
Based on the frequency spectrum of the arm current, shown in Fig. 26 (c), it is observed that the harmonic contents of both currents are similar, evidencing an ac signal (with emphasis on the fundamental component). In addition, a low level of total harmonic distortion (THD) is observed in both simulations. The THD definition adopted in this work for the current (THD_i) is given by (IEEE Std 519, 2014):

$$THD_i = \frac{\sqrt{\sum_{n=2}^{200} I_{n,RMS}^2}}{I_{1,RMS}} \tag{3.16}$$

where $I_{n,RMS}$ is the *n-th* RMS battery harmonic current component and $I_{1,RMS}$ is the first RMS battery harmonic current component. It is worth noting that according to the recommendation of (IEEE Std 519, 2014), the THD value is typically calculated up to the 50-th harmonic, however, the standard allows harmonic components of order greater than 50-th harmonic to be included when necessary. In this situation, the increase of harmonic components in the THD calculation was extended up to the 200-th harmonic to compute the influence of the maximum switching frequency of the MPE.

Based on the definition of THD_i and the values obtained in Fig. 26 (c) there is

Figure 26 – (a) Arm current (b) arm current ripple (c) spectrum of arm current.



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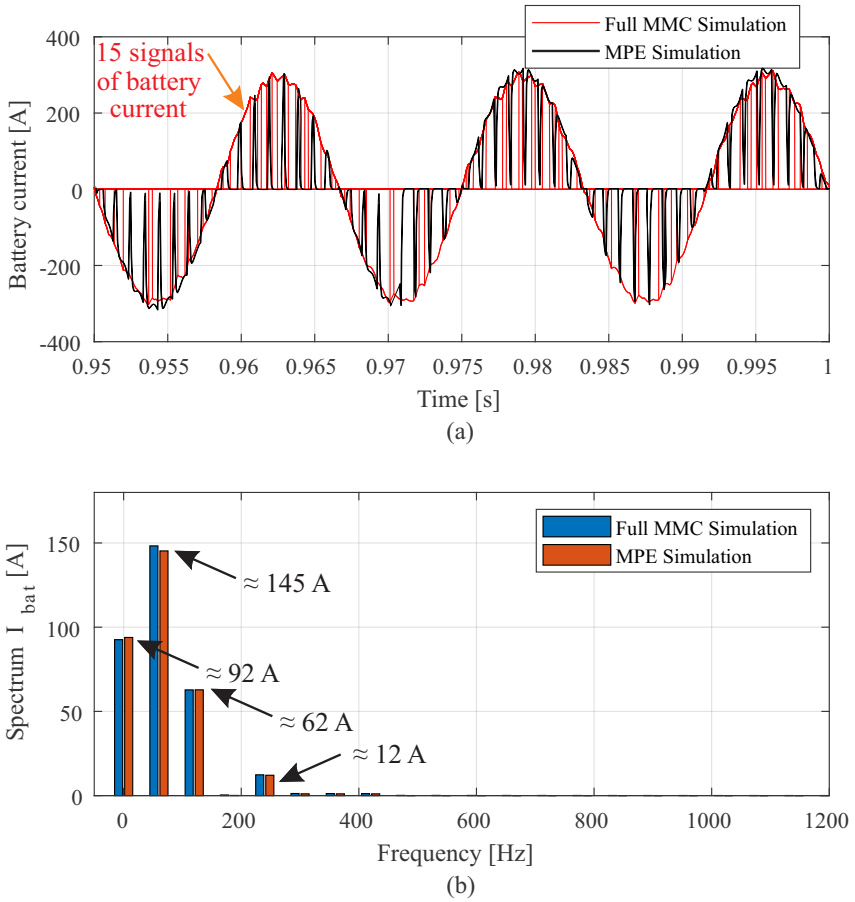
relative proximity between the two values (difference of 1.2%), with the THD_i value of the MMC simulation having a lower value concerning the MPE, which can be explained by the difference in the modulation strategy and of the modularity of the MMC, favoring the harmonic content of the output voltage and consequently the in the arm current.

Fig. 27 (a) shows the current in the SMs of the MMC upper arm, as well as the battery current measured in the MPE. Once the full MMC-BESS simulation implements all the SMs of the MMC, the 15 signals of battery current in the upper arm of phase a are presented.

Fig. 27 (b) shows the average current spectrum of the 15 battery current signals obtained in the complete simulation of MMC. The harmonic contents of the battery current for both models are similar, especially for the most significant components dc, 1^{st}, 2^{nd}, and 4^{th} order. Furthermore, the result shows that even using different modulation techniques (Nearest Level Control - NLC, for full MMC simulation and PWM, for the MPE), the

Figure 27 – (a) Battery current in SM (b) spectrum of battery current.



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low-frequency spectral content is well represented by the emulator.

3.5 MPE Test-Bench Validation

Once validation has been carried out through the simulation of the full MMC-based BESS simulation, an evaluation of the MPE setup is carried out considering values of low arm current and low power supply voltage for reproducibility in a laboratory environment. It is worth highlighting that in this study, the main intention is to validate the harmonic components and typical waveforms of the MPE currents and voltages concerning those verified in the MMC-based BESS.

3.5.1 MPE Test-Bench Parameters

The main full-bridge module parameters of the experimental test bench are presented in Tab. 8. The technical discussion of full-bridge module development is presented in detail in Appendix A.1, based on the work developed by França et al. (2022).

Table 8 – Main Full-bridge Module Parameters.

Parameters	Value	Unit
Output current ($I_{out,RMS}$)	20	[A]
Output voltage (line) ($V_{out,RMS}$)	220	[V]
dc-link voltage ($V_{dc,mod}$)	450	[V]
dc-link capacitors parallel	4 x 680	[μF]
IGBT - IKP20N60H3 (V_{CE},I_C)	600/20	[V]/[A]

The MPE test bench results are obtained considering the same SM nominal voltage, grid frequency, battery arrangement, and nominal arm current, for experimental and simulated results. The results, for the experimental and simulated analysis, consider a reduced scale prototype with the main parameters presented in Table 9. The validations for the arm current and battery current are based on the current spectrum and the maximum arm current ripple.

Table 9 – Main System Parameters of the MPE in Experimental and Simulation Results.

Parameters	Symbol	Value
Peak ac arm current [A]	$I_{arm,ac}$	5
Arm inductance [mH]	L_{em}	5.53
Arm induc. internal resistance [Ω]	R_{em}	0.13
MPE Switching frequency [kHz]	$f_{sw,MPE}$	10
SM Switching frequency [kHz]	$f_{sw,SM}$	1
Sampling frequency [kHz]	f_s	20
Grid frequency [Hz]	f_g	60
Power devices (IKP20N60H3)[A/V]	S_{1-4}, D_{1-4}	40/600
Nominal SM voltage [V]	V_{sm}^*	24
Emulator dc-link voltage [V]	$V_{dc,em}$	30
Battery (UP1270E) voltage [V]	V_{bat}	12
Battery (UP1270E) capacity [Ah]	C_{Ah}	7
Battery internal resistance [mΩ]	$R_{bat,em}$	5

3.5.2 MPE Test-Bench

Fig. 28 presents the experimental test bench developed in this work, highlighting the connection between MPE (full-bridge converter), SM, dc source, DSP, MPE inductance, battery bank, and bleeder resistor (R_{bld}, used to discharge the output capacitor of MPE unidirectional power supply). Also highlighted are the current probe and current sensor. The battery arrangement consists of two 12V/7 Ah batteries in series, with two string connections in parallel, totaling 4 batteries and a 24 V/14 Ah battery storage system. The laptop is used to program, through Simulink/Matlab, the arm current control and SM PWM operation, loading the program into the DSP.

The control algorithm is programmed in the Texas Instruments TMS320F28379D digital signal processor. The dc power supplier FA-3050 supplies the voltage of the full-bridge dc-side. The voltage and current measurements are obtained from a Tektronix DPO 2014B oscilloscope equipped with TCPA300 Tektronix ac/dc Current Probe and P5200A 50 MHz

Figure 28 – Experimental test bench.

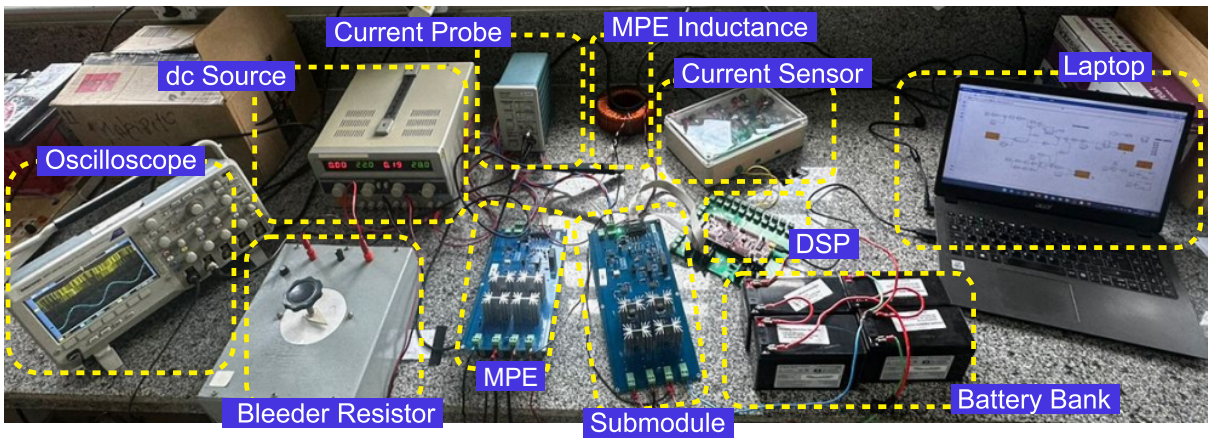

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Table 10 – Voltage and Current Probes Parameters.

TCPA300 Tektronix ac/dc Current Probe Parameters	Value
dc Gain Accuracy	1%
Bandwidth (-3 dB)	dc to 100 MHz
Ranges, nominal	5 A/V, 10 A/V
Signal Delay, typical	approximately 19 ns
Lowest Measurable Current	5 mA
P5200A 50 MHz High Voltage Differential Probe Parameters	**Value**
Attenuation	50X / 500X
Differential Voltage	50X: ±150 V
Bandwidth	200 MHz
Rise Time	< 1.8 ns

High Voltage Differential Probe, with the main characteristics presented in Tab. 10. In turn, the voltage measurement for the DSP supply (range of 0 - 3.3 V) is described in Appendix A.1.

The measurement circuit, responsible for obtaining the arm current, and battery current and sending it to the DSP, is named Gbox, which has two versions, one for voltage measurement and the other for current measurement (which was adopted in this work). Appendix A.2 details the principal points of Gbox design.

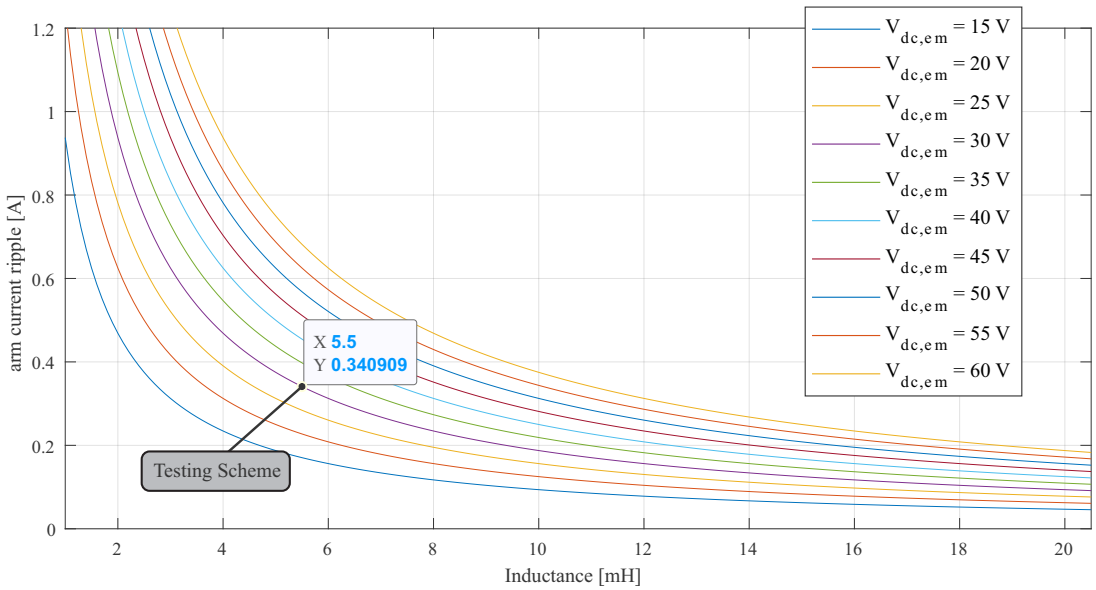
3.5.3 MPE Inductor Design

The design of the MPE inductor considers a limit of maximum arm current ripple according to the MPE supply voltage. In this sense, the testing scheme employed in this work adopted an inductance of 5.5 mH (with a 0.13 Ω of intrinsic resistance) leading to a maximum arm current ripple of approximately 0.34 A (for $V_{dc,em} = 30V$), according to (3.14).

Fig. 29 shows the maximum arm current ripple derived from (3.14) for different

values of emulator dc-link voltage and arm inductance, highlighting the design point employed in the testing scheme. An inversely proportional relationship can be seen between the arm current ripple and the inductance value. Furthermore, for the same arm inductance value, the higher the MPE supply dc voltage value, the greater the ripple, as expected according to the discussion of the equation (3.14).

Figure 29 – Maximum arm current ripple for different arm inductance and emulator dc-link voltage.



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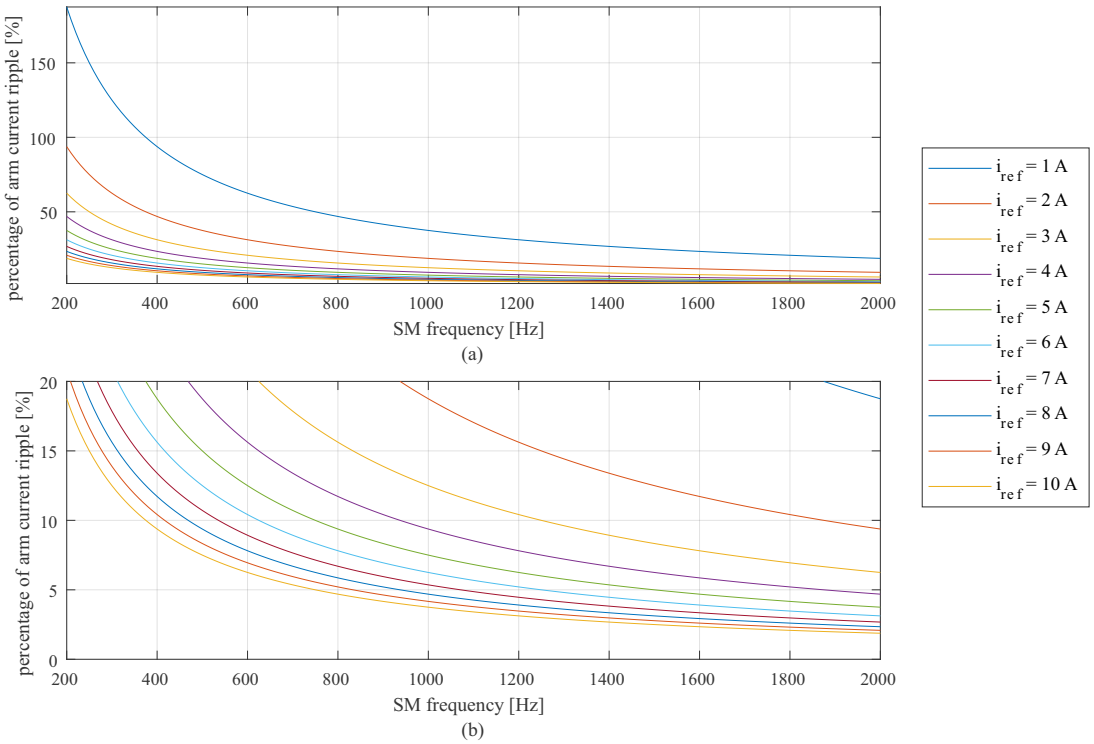
It can be seen that the maximum arm current ripple obtained may or may not be significant compared to the value of the arm reference current. Another effect to be considered is the switching frequency of the SM (which is related to MPE frequency, as discussed previously). Fig. 30 (a) presents an analysis of these two variables, representing the percentage of the maximum ripple of the arm current for an SM frequency range between 200 Hz and 2 kHz.

Very significant values of ripple percentages above 20% are observed for the arm current of the emulator. This design region makes it unfeasible to emulate a reasonable sinusoidal current in the MPE. In this sense, Fig. 30 (b) presents the curves of different reference values for the emulator current, emphasizing the possible regions of switching frequency of the SM under test to obtain a maximum ripple in the arm current equal to 20%.

Another possibility for evaluating the combinations of inductances and switching frequencies of the SM under test is shown in Fig. 31 (a). It can be seen how the value of the MPE inductance impacts different values of maximum ripple in the arm current. For the same value of arm inductance, the lower the switching frequency, the greater the ripple expected in the MPE arm current. Fig. 31 (b) presents a zoom on the y-axis emphasizing

Figure 30 – Percentage of maximum arm current ripple for different SM frequency and arm current reference (a) y-axis limited between 0% to 180% (b) y-axis limited between 0% to 20%.



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the combinations of arm inductance and switching frequencies of the SM under test that generate arm current ripple lower than 1 A. It can be seen that certain inductance values cannot generate the limit of 1 A in the arm current ripple due to the low frequency of the SM under test.

The previous discussion based on Fig. 30 and Fig. 31 can be synthesized in a maximum arm current ripple surface, as shown in Fig. 32. The testing scheme point is highlighted on the curve for an inductance of 5.5 mH, a maximum arm ripple equivalent to 0.34 A.

It is worth mentioning that the MPE inductance evaluation in this subsection considered typical values of inductance and switching frequency to be applied to the devices available in the testing scheme. In a scenario of evaluating a typical SM voltage, at a fixed kV, the scaling procedure for the study presented in this work should be performed (Ma et al., 2021).

3.5.4 MPE Control Design

Based on the MPE parameters presented in Tab. 9, the PIMR controller parameters are calculated for the MPE testing scheme, as presented in Tab. 11.

Figure 31 – Maximum arm current ripple for different SM frequency and MPE arm inductance (a) y-axis limited between 0 to 9 A (b) y-axis limited between 0 A to 1 A.

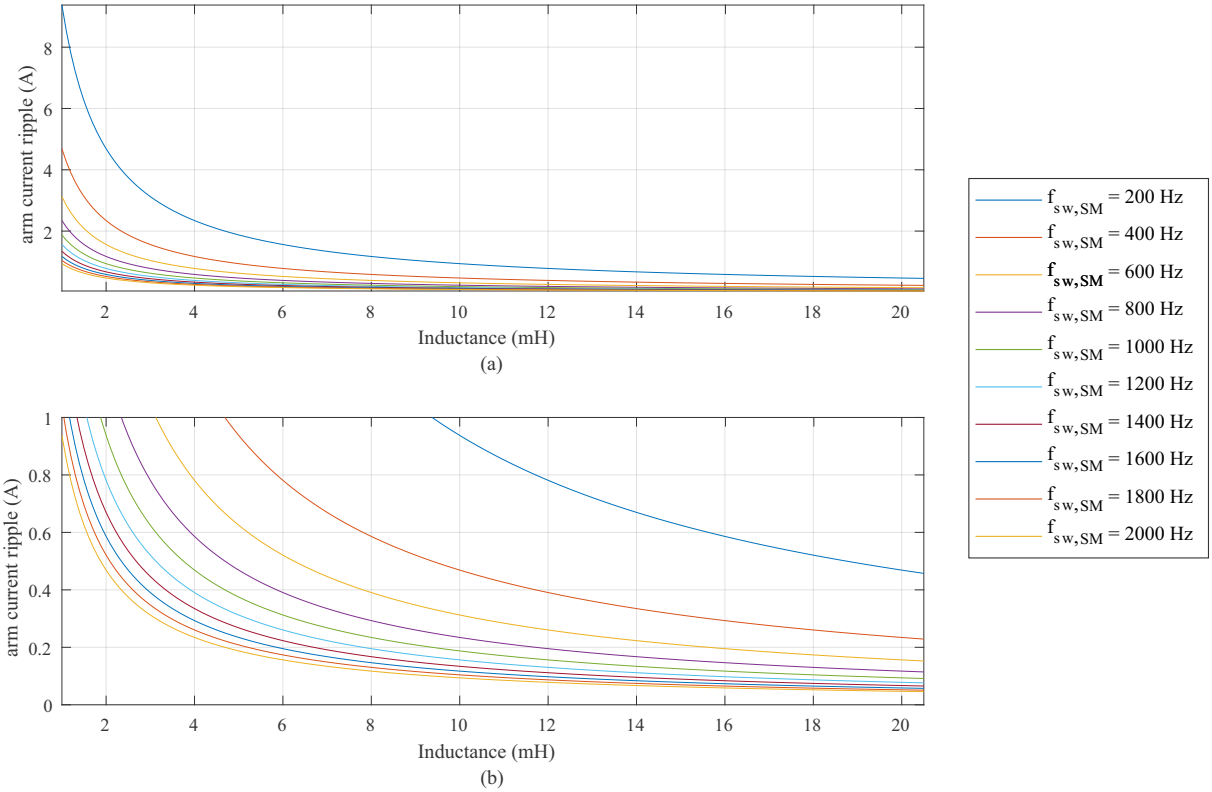

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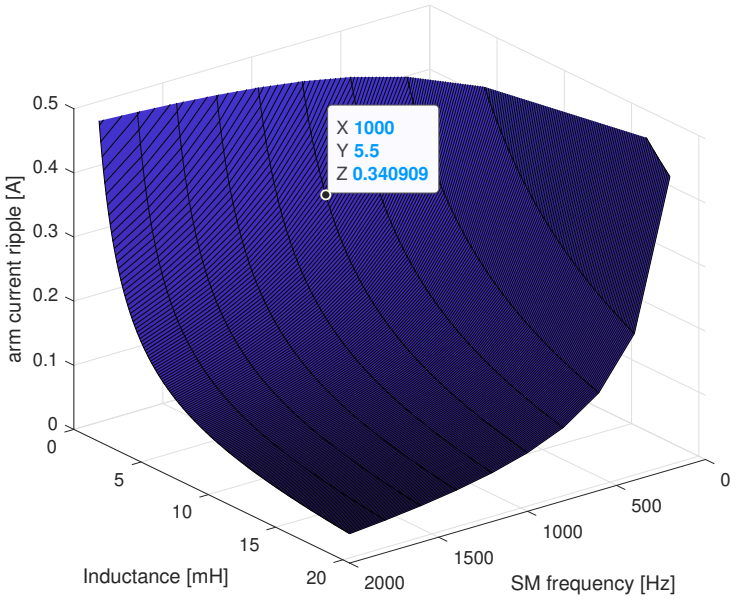
Figure 32 – Maximum arm current ripple surface for different arm inductance and SM frequency.



Source: own representation.

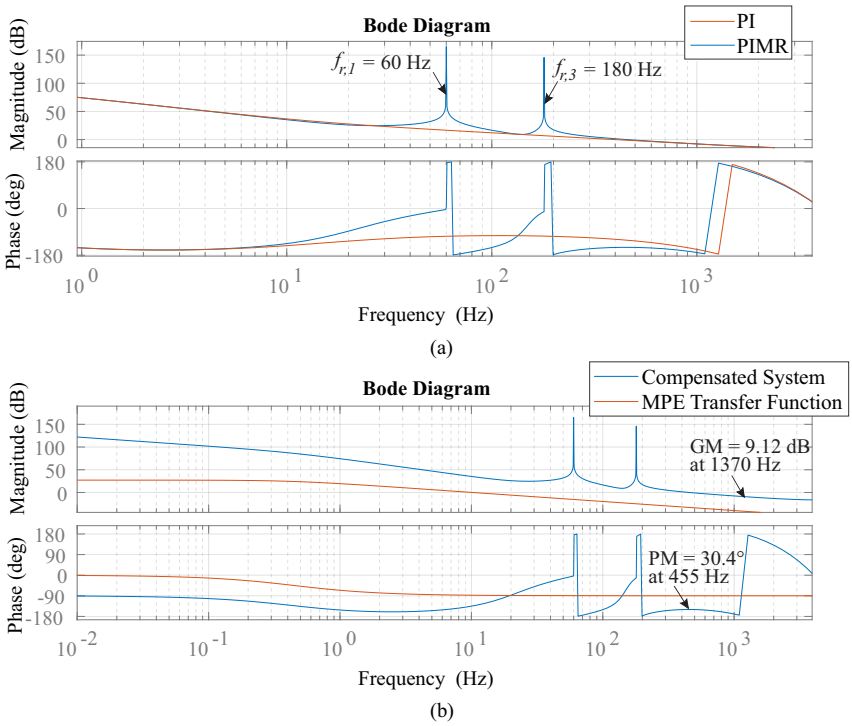
Table 11 – PIMR Controllers Parameters.

Gains for MPE in testing scheme	Value	Units
Proportional gain (k_p)	77.2	Ω
Integral gain (k_i)	3.5×10^3	Ω/s
Resonant gain ($k_{r,1}$ and $k_{r,3}$)	5.3×10^4	Ω/s

For the MPE test bench development, the switching frequency of the MPE and SM adopted is equal to 10 kHz and 1 kHz, respectively.

Fig. 33 (a) shows the Bode diagram for the traditional PI controller and the employed PIMR controller (equation (3.4)) for the MPE testing scheme gains. It is possible to check the frequencies tuned to the PIMR controller (1-*st* and 3-*rd* harmonics).

Figure 33 – (a) Bode diagram of a traditional PI controller and the employed PIMR controller (b) Bode diagram of the open-loop MPE system and the compensated system.



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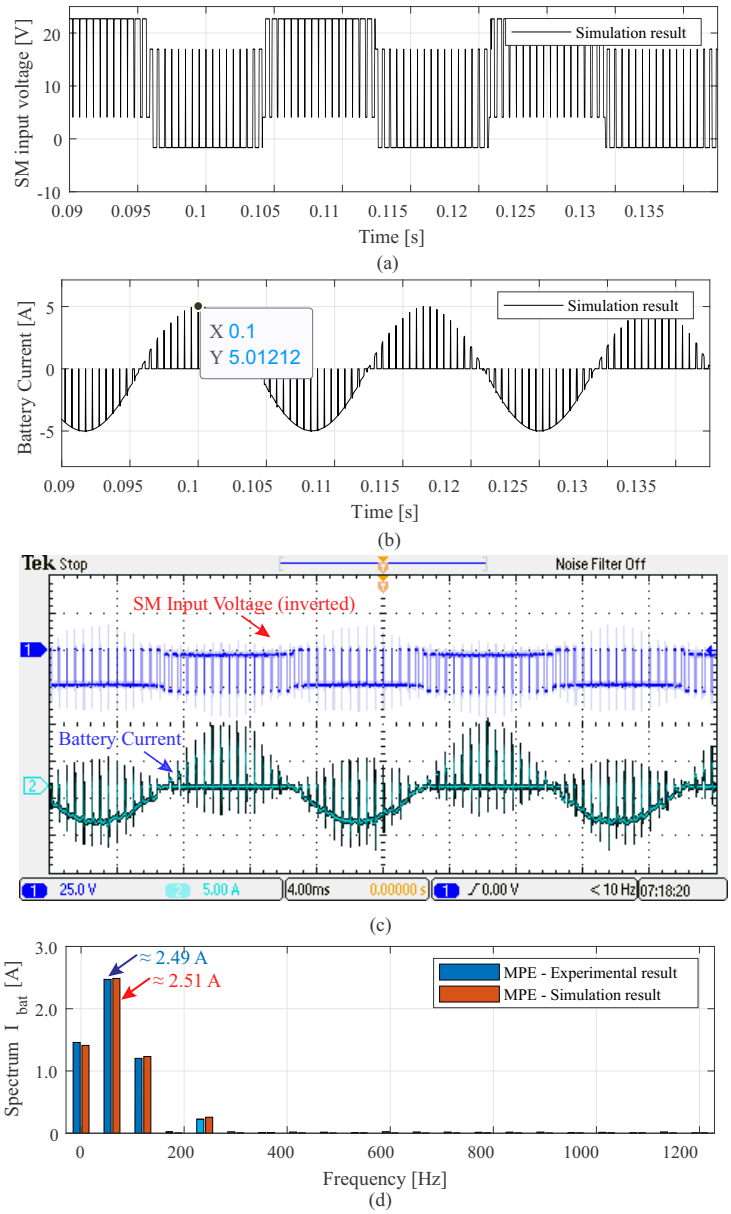
In addition, the Bode diagram for the open-loop MPE transfer function and the resulting compensated system (equation (3.3) and (3.3)×(3.4), respectively) is presented in Fig. 33 (b). The control features a gain margin (GM) of 9.12 dB at 1.37 kHz and a phase margin (PM) of 30.4° at 455 Hz. Again it is possible to check the frequencies tuned to the PIMR controller (1-*st* and 3-*rd* harmonics) appearing in the compensated system, which includes the effect of the PIMR controller.

3.5.5 Experimental Results - Proof of Concept

Fig. 34 (a) and (b) present the SM input voltage and battery current, respectively, during the battery discharging process for an arm peak current of 5 A, from the MPE simulation with the same parameters of the experimental test bench.

Figure 34 – (a) SM input voltage from simulation (b) battery current from simulation (c) experimental waveforms of the SM input voltage [25 V/div], arm current [5 A/div], and time division of 4 ms/div (d) the spectrum of experimental and simulation battery current.



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The difference observed between the upper and lower level in the SM input voltage is due to the collector-emitter saturation voltage in the IGBT ($V_{CEsat} \approx 1.95V$) and diode forward voltage ($V_F \approx 1.65V$). A similar effect is observed for the MPE output voltage.

Fig. 34 (c) shows the experimental waveforms of the SM input voltage and battery current during the discharging process for the arm current peak of 5 A. Fig. 34 (d) presents the battery current frequency spectrum for the simulated and experimental system. The harmonic content of the battery currents for the two models are similar, especially for the most significant components of dc, 1^{st}, 2^{nd}, and 4^{th} order, with amplitude error lower than 5%.

Figure 35 – (a) Arm current from simulation. (b) MPE output voltage from simulation. (c) experimental waveforms of the MPE output voltage [25 V/div], arm current [5 A/div], and time division of 4 ms/div (d) the spectrum of experimental and simulation arm current.

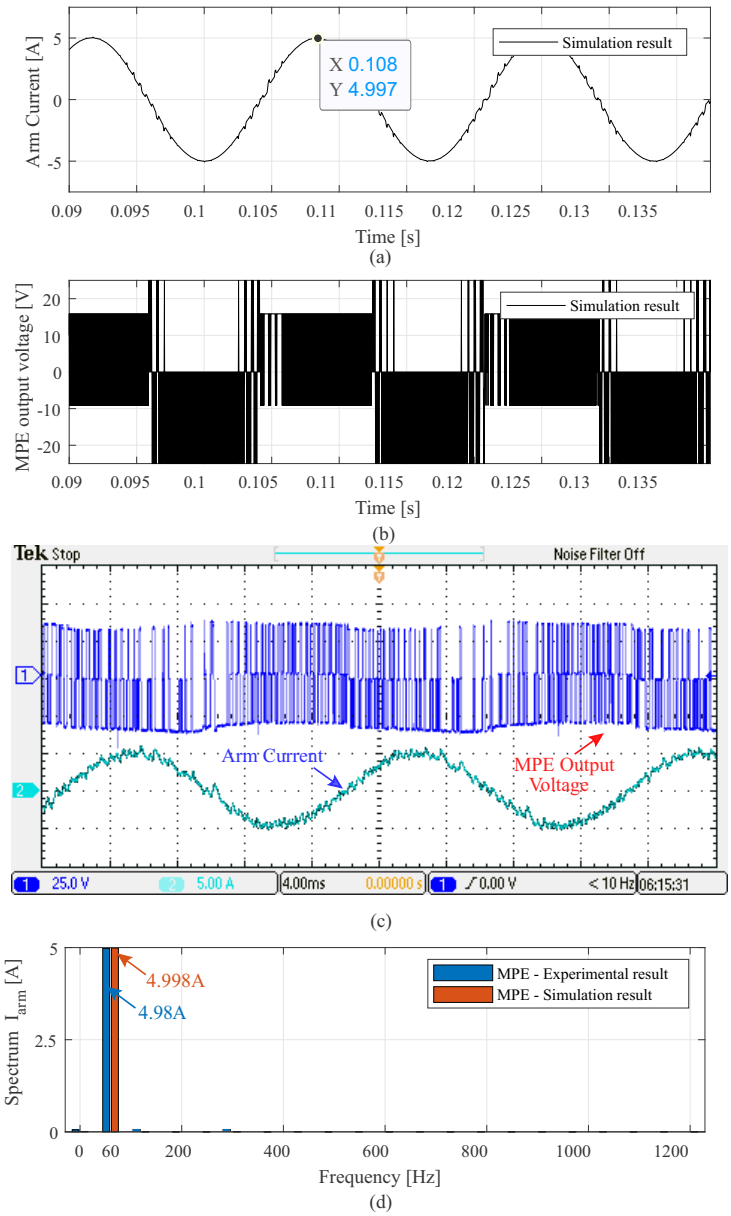

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Fig. 35 (a) and (b) present the arm current and MPE output voltage, respectively, during the battery discharging process for an arm peak current of 5 A, from the MPE

simulation. Fig. 35 (c) shows the experimental waveforms of the MPE output voltage and arm current during the discharging process for an arm current peak of 5 A. Fig. 35 (d) presents the arm current spectrum for the simulated and experimental system. The harmonic contents of the battery current for the two models are similar, especially for the fundamental component, where the 1^{st} amplitude is equal to 4.98 A in the testing scheme and equal to 4.998 A for the simulation result, resulting in an error lower than 1%. Some high-order components, in the range of 200 - 1200 Hz, are verified in the experimental signal spectrum, but with negligible amplitudes.

Fig. 36 (a) and (b) present the arm current and MPE output voltage, respectively, for a variation of arm current peak of 1 A to 5 A. Fig. 36 (c) shows the arm current control dynamic behavior for a step in the arm current amplitude from 1 A to 5 A. The waveforms presented are the MPE output voltage and the MPE output current. As verified, the peak of the output current ranges from 1 A to 5 A, for a 60 Hz sinusoidal reference current. Fig. 36 (d) shows the arm current ripple with a maximum peak value of 0.203 A, for the experimental result, and 0.158 A, for the simulation result.

The maximum arm current ripple is computed by nulling the fundamental component of the Fourier transform of the measured current of the arm and checking the maximum peak value of the resulting signal. Thus, to obtain the ripple signal of the arm current, the inverse Fourier transform is performed.

Tab. 12 presents a summary of the obtained maximum arm current ripple values and their respective errors. The experimental arm current ripple shows an error of 7.96% and the simulated arm current ripple, an error of -3.4%.

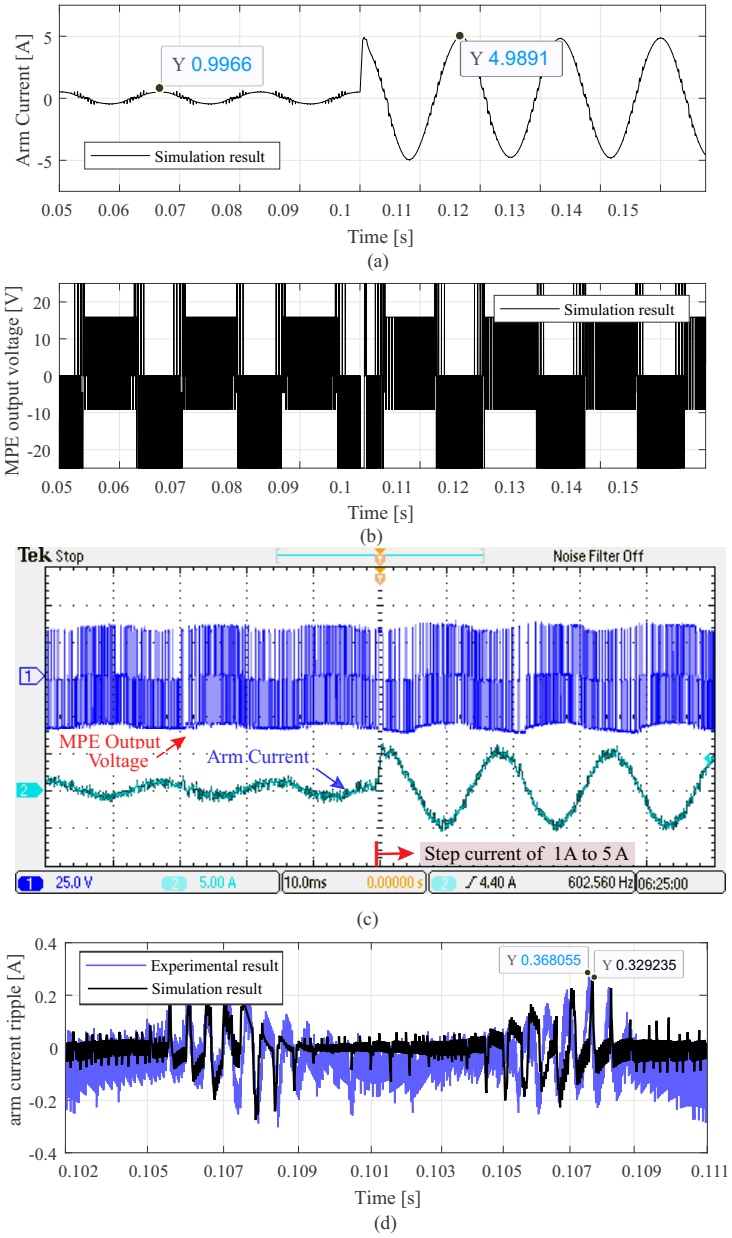
Table 12 – Maximum Arm Current Ripple Results.

Method	Current Ripple [A]	Error [%]
Theoretical Analysis - Eq. (3.13)	0.3409	not applicable
Simulation Result	0.3292	-3.4
Experimental Result	0.3680	7.96

Fig. 37 presents the MPE current and battery current for the operation of the MPE processing only reactive power (without charging and discharging the batteries).

The results presented are evaluated for the experimental test bench and simulation. Fig. 37 (a) shows the operation for reactive power process with $\phi_n = \pi/2$, for simulation results. Fig. 37 (b) shows the operation for the reactive power process with $\phi_n = \pi/2$, highlighting the battery current and SM input voltage for experimental results. In addition, Fig. 37 (c) shows the operation for the reactive power process with $\phi_n = \pi/2$, highlighting the arm current and MPE output voltage for experimental results. It is possible to verify a continuous component in the battery current signal that becomes evident at moments of decrease from the maximum current amplitude to the minimum amplitude. High-frequency

Figure 36 – (a) Arm current from simulation. (b) MPE output voltage from simulation. (c) Experimental waveforms of the MPE output voltage [25 V/div], arm current [5 A/div] (for the step of arm current), and time division of 10 ms/div. (d) arm current ripple for experimental test bench for one fundamental cycle.



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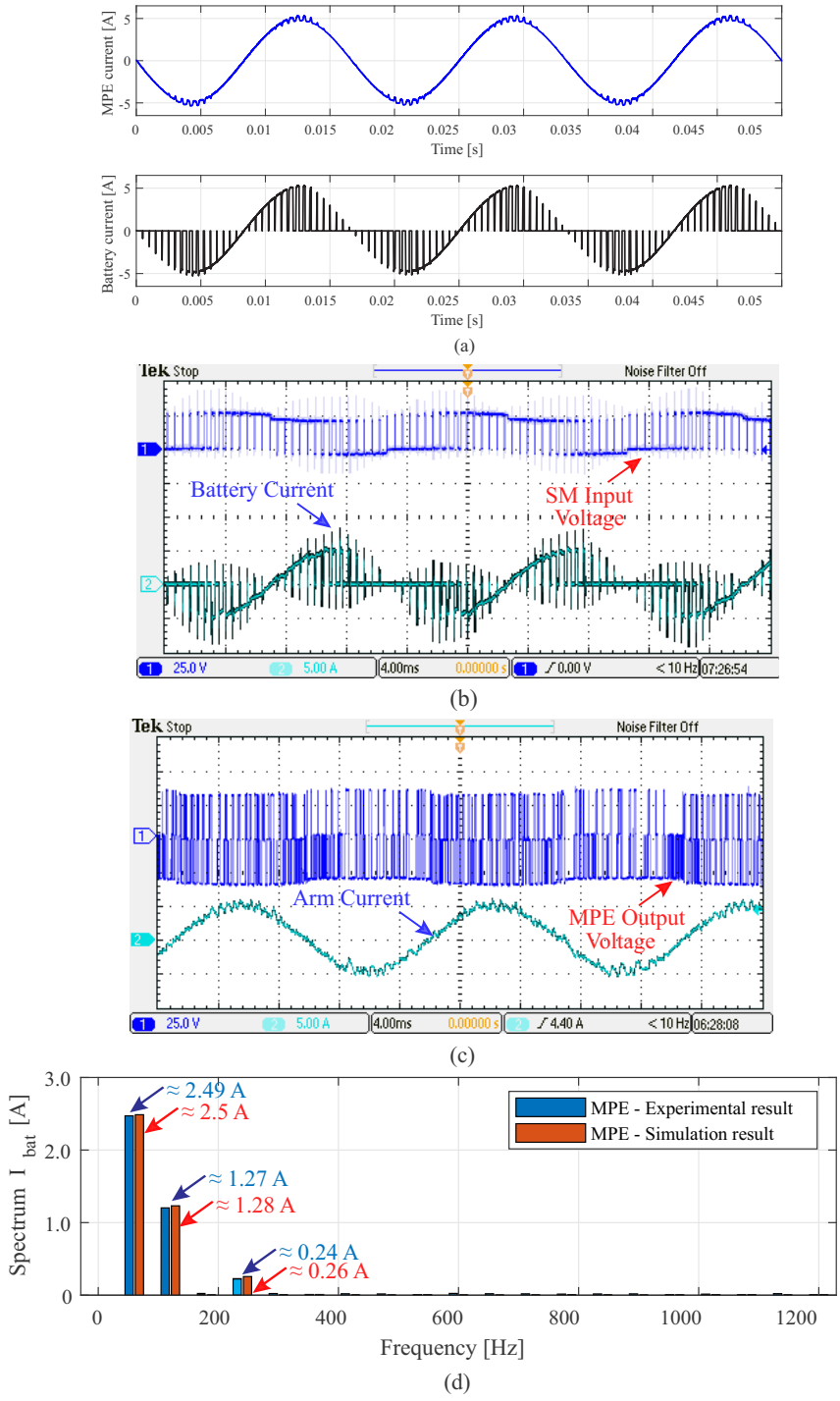
components are verified in the experimental result, a phenomenon not presented in the simulation which does not consider the non-idealities of the test bench.

The experimental and simulation battery current spectrum is shown in Fig. 37 (d). It is possible to verify the presence of the first, second, and fourth harmonic ac components, as observed in the unitary power factor, without having the dc component, due to the operation in the reactive power factor.

Fig. 38 (a) shows the operation for reactive power process with $\phi_n = -\pi/2$, for

Figure 37 – Steady-state behavior of the arm current and battery current for (a) $\phi_n = \pi/2$ (Simulation waveforms - battery and arm current) (b) $\phi_n = \pi/2$ (Experimental waveforms - battery current and SM input voltage) (c) $\phi_n = \pi/2$ (Experimental waveforms - arm current and MPE output voltage) (d) the spectrum of experimental and simulation battery current.



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simulation results. Fig. 38 (b) shows the operation for the reactive power process with $\phi_n = \pi/2$, highlighting the battery current and SM input voltage for experimental results. In addition, Fig. 38 (c) shows the operation for the reactive power process with $\phi_n = \pi/2$,

highlighting the arm current and MPE output voltage for experimental results. Again, the experimental and simulation battery current frequency spectrum is shown in Fig. 38 (d). It is possible to verify the presence of the first, second, and fourth harmonic ac components, as observed in the unitary power factor, without having the dc component.

Results for operating conditions with $\phi_n = \pi/2$ and $\phi_n = -\pi/2$ show similarities between current waveforms. In this operation, it is worth noting that the dc-link voltage emulator presents the maximum operation value. Again, verifying a continuous portion in the battery current signal is possible, but that becomes evident at moments of increases from the minimum current amplitude to the maximum amplitude. High-frequency components with values close to ten amps are verified again in the experimental result. In both operating situations with reactive power factor, it can be seen that the maximum current ripple occurs at the valley and peak of the arm current signal. For all situations evaluated, the ripple was limited to the expected value of approximately 0.34 A, with a maximum verified error equal to 8.5%.

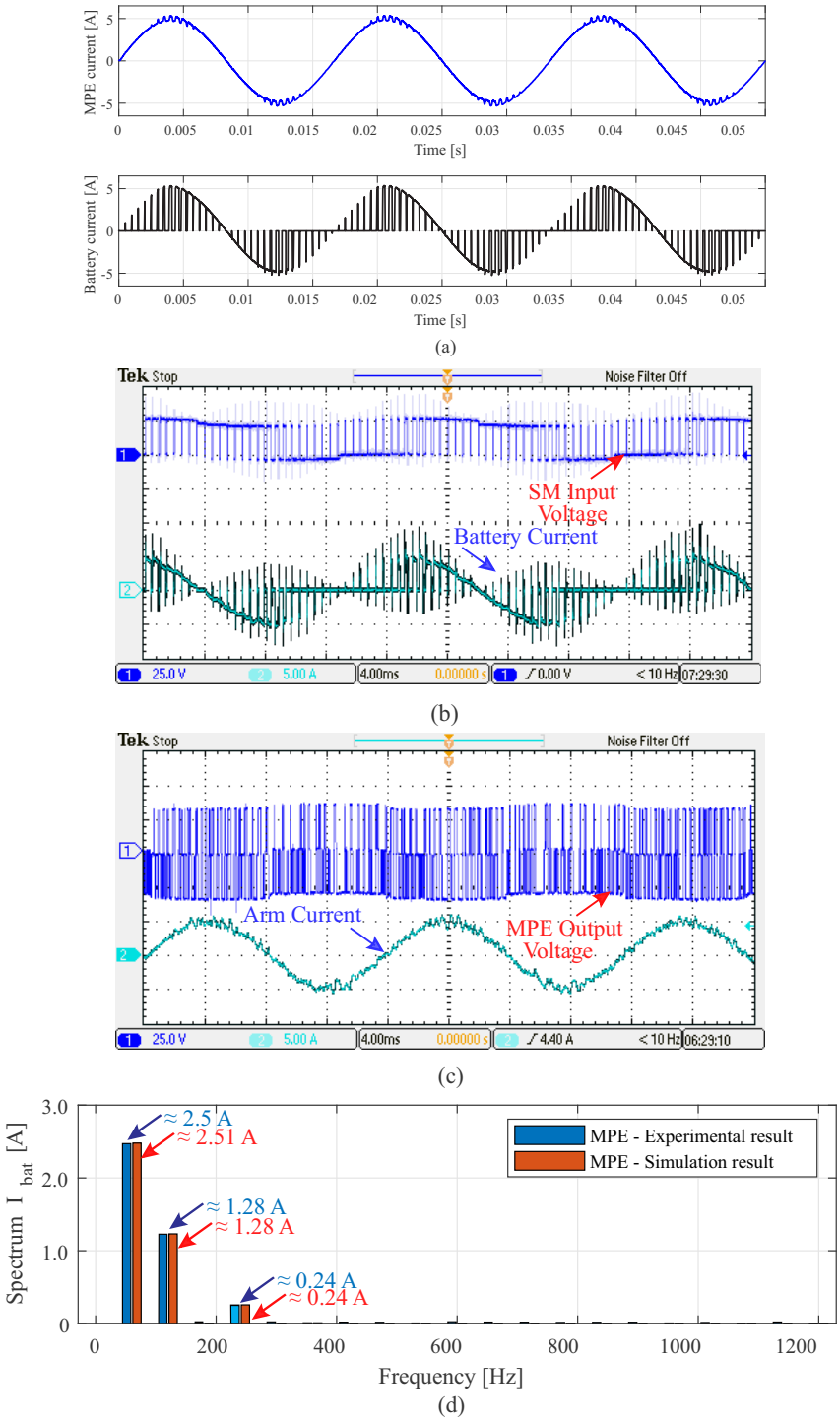
3.5.6 Experimental Results - Analysis of SM and MPE frequency

As discussed previously, the SM and the MPE (full-bridge converter) switching frequency determines the value of the emulator arm current ripple. In this sense, the consideration made that $f_{sw,MPE} >> f_{sw,SM}$ is adopted.

An experimental evaluation carried out concerns the concept of operating the SM and the MPE with the same switching frequency ($f_{sw,MPE} = f_{sw,SM}$). This analysis is performed to evaluate the approximation limit between the switching frequencies of the MPE converter and SM converter, as well as to reduce the switching losses of the MPE. Although the analytical equations for calculating the maximum ripple consider that $f_{sw,MPE} >> f_{sw,SM}$, an experimental study is made considering that the switching frequencies between the two converters are equal and how the arm current waveform, the maximum arm current ripple and the ability to emulate the forms typical waveform behaves. In this sense, in Fig. 39 (a) the behavior of the MPE was analyzed in the condition where $f_{sw,MPE} = f_{sw,SM} = 5$ kHz, in terms of the MPE output voltage and arm current.

In turn, Fig. 39 (b) presents the behavior of the MPE in the condition where $f_{sw,MPE} = f_{sw,SM} = 2$ kHz, in terms of the MPE output voltage and arm current. In this condition, there is no longer good harmonic content in the arm current and MPE output voltage, highlighting a limitation for practical validation as MMC-based BESS. These findings can be seen in Tab. 13, showing the high value of the maximum current ripple in the condition of SM frequency equal to 2 kHz, in addition to the high value of THD_i. It is verified that switching frequency values close to the controller passband (455 Hz) have already begun to affect its harmonic content, as presented in Tab. 13. It is worth noting that values above 5 kHz in the SM frequency demonstrated good harmonic content and

Figure 38 – Steady-state behavior of the arm current and battery current for (a) $\phi_n = -\pi/2$ (Simulation waveforms - battery and arm current) (b) $\phi_n = -\pi/2$ (Experimental waveforms - battery current and SM input voltage) (c) $\phi_n = -\pi/2$ (Experimental waveforms - arm current and MPE output voltage) (d) the spectrum of experimental and simulation battery current.



Source: own representation.

validity for applying MPE in emulating typical MMC-based BESS profiles.

One possibility to improve the harmonic content and current ripple to work with

Figure 39 – Experimental waveforms of the MPE output voltage [25 V/div], arm current [5 A/div], and time division of 4 ms/div (a) for the $f_{sw,MPE} = 5$ kHz and $f_{sw,SM} = 5$ kHz (b) for the $f_{sw,MPE} = 2$ kHz and $f_{sw,SM} = 2$ kHz.

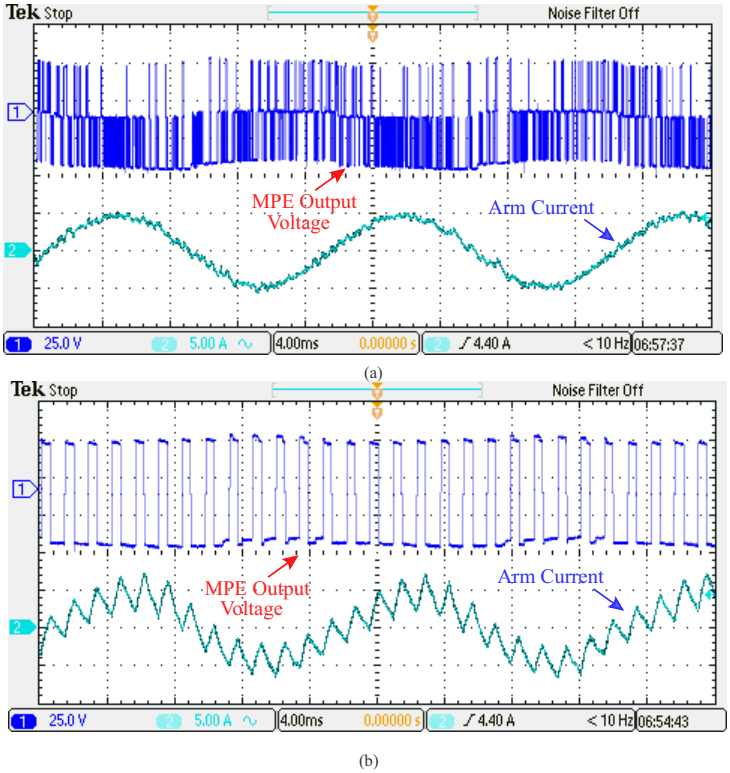


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Table 13 – Maximum Arm Current Ripple and THD_i Results for different MPE frequencies.

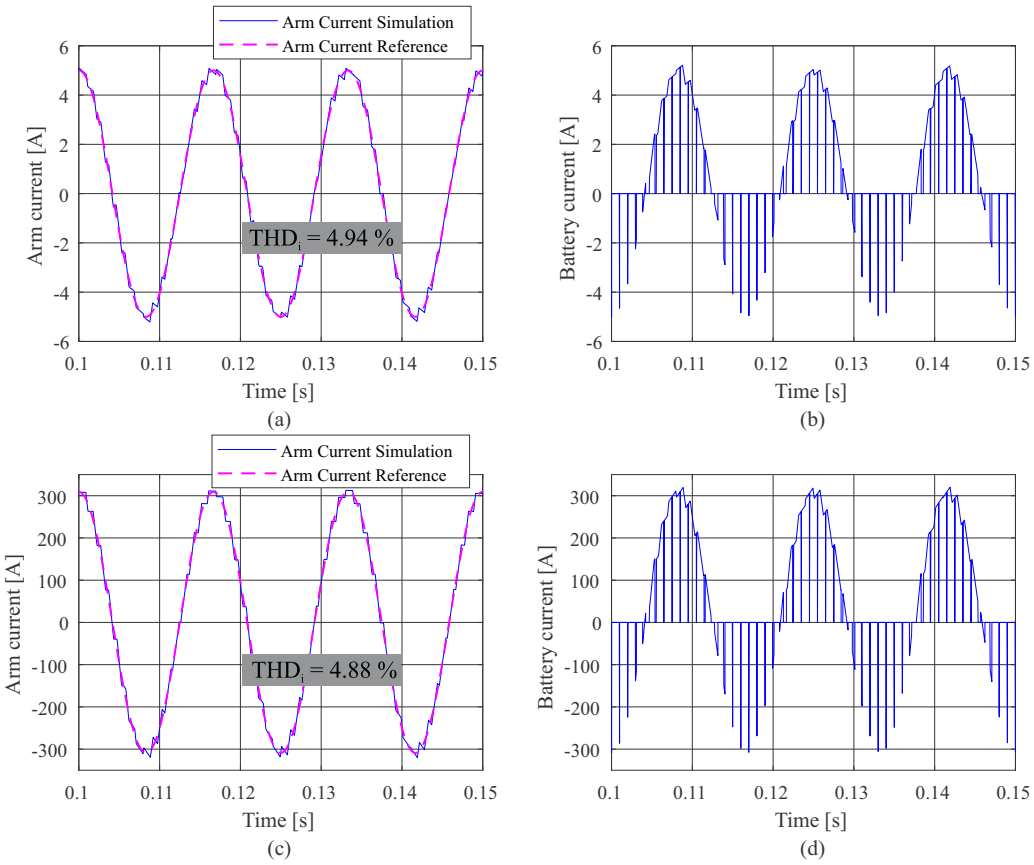
MPE and SM Frequency	Current Ripple [A]	THD_i [%]
$f_{sw,MPE} = f_{sw,SM} = 5$ kHz	0.3009	4.7
$f_{sw,MPE} = f_{sw,SM} = 2$ kHz	2.2580	12.7

lower switching frequencies in the MPE and SM would be to increase the value of the MPE inductance. Due to limitations in the inductance values available in the laboratory, it was not possible to evaluate switching frequencies lower than 2 kHz in the MPE and SM.

Laboratory tests showed the limitation of the MPE dc-link voltage and MPE inductance for an operating frequency. To evaluate the operating limits of the MPE for low switching frequencies and maintain the equality of the switching frequency between the SM and the MPE ($f_{sw,MPE} = f_{sw,SM}$), simulations were carried out to obtain the best combinations of $V_{dc,em}$ and L_{em} that would result in an arm current synthesized with a THD_i limit equal to 5% (IEEE Std 519, 2014) (it is worth noting that the limit imposed by IEEE Std 519 (2014) is for the grid current, however, as the arm current affects the converter output/grid current, the limit presented was considered in the arm current). Thus, the analysis was made in simulations due to the laboratory limitations in dealing with high values of inductance and voltage.

In this sense, in Fig. 40 the behavior of the MPE was analyzed in the condition where $f_{sw,MPE} = f_{sw,SM} = 1$ kHz, in terms of the arm current and battery current for full MMC simulation and low scale in the testing scheme. A high similarity can be seen with the curves obtained in Fig. 40 (a), highlighting the arm current reference.

Figure 40 – Simulation waveforms of the (a) arm current and (b) battery current for the $f_{sw,MPE} = f_{sw,SM} = 1$ kHz with arm current peak equal to 5 A and simulation waveforms of the (c) arm current and (d) battery current for the $f_{sw,MPE} = f_{sw,SM} = 1$ kHz with arm current peak equal to 309 A.



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The THD$_i$ value obtained is equal to 4.94%. Fig. 40 (b) presents the result for the battery current, emphasizing a similarity with the previously verified harmonic content and the peak value. To obtain this result, the values of $V_{dc,em}$ and L_{em} were combined according to Tab. 14 in the simulation condition of the testing scheme (the peak value in the arm current around 5 A).

It is worth noting that when the L_{em} value increases, there is a reduction in the switching frequency to close to 0 dB of the control, so a lower switching frequency becomes acceptable. On the other hand, the control will become very slow in transients (Jiang et al., 2021).

For the full MMC simulation level, the arm current and battery current waveforms

are shown in Fig. 40 (c) and (d), respectively. At this current level, there is a THD_i of around 4.88 % for the arm current, with the maintenance of the harmonic content of the battery current. The combination of $V_{dc,em}$ and L_{em} were combined according to Tab. 14 in the simulation condition of the full MMC simulation (the peak value in the arm current around 309 A).

Table 14 – MPE dc-link voltage and THD_i results for Full MMC Simulation and Testing Scheme.

MPE and SM Frequency	$V_{dc,em}$ [V]	THD_i [%]	L_{em} [mH]
$f_{sw,MPE} = f_{sw,SM} = 1$ kHz (Full MMC Simulation)	8000	4.88	45
$f_{sw,MPE} = f_{sw,SM} = 1$ kHz (Testing Scheme)	50	4.94	18

Due to the relatively good performance of the MPE for the previous case study, a final test was carried out to evaluate the performance of the MPE for the scenario of a more critical switching frequency in which $f_{sw,MPE} = f_{sw,SM} = 500$ Hz. In this sense, in Fig. 41 the behavior of the MPE in terms of the arm current and battery current for full MMC simulation and low scale in the testing scheme. A similarity can be seen with the curves obtained in Fig. 41 (a), highlighting the arm current reference. However, there is a greater distortion in the arm current in this situation, with a best THD_i scenario obtained equal to 7.02 %.

Fig. 41 (b) presents the result for the battery current, emphasizing a loss of current harmonic content and peak amplitude. To obtain this result, the values of $V_{dc,em}$ and L_{em} were combined according to Tab. 15 in the simulation condition of the testing scheme (the peak value in the arm current around 5 A).

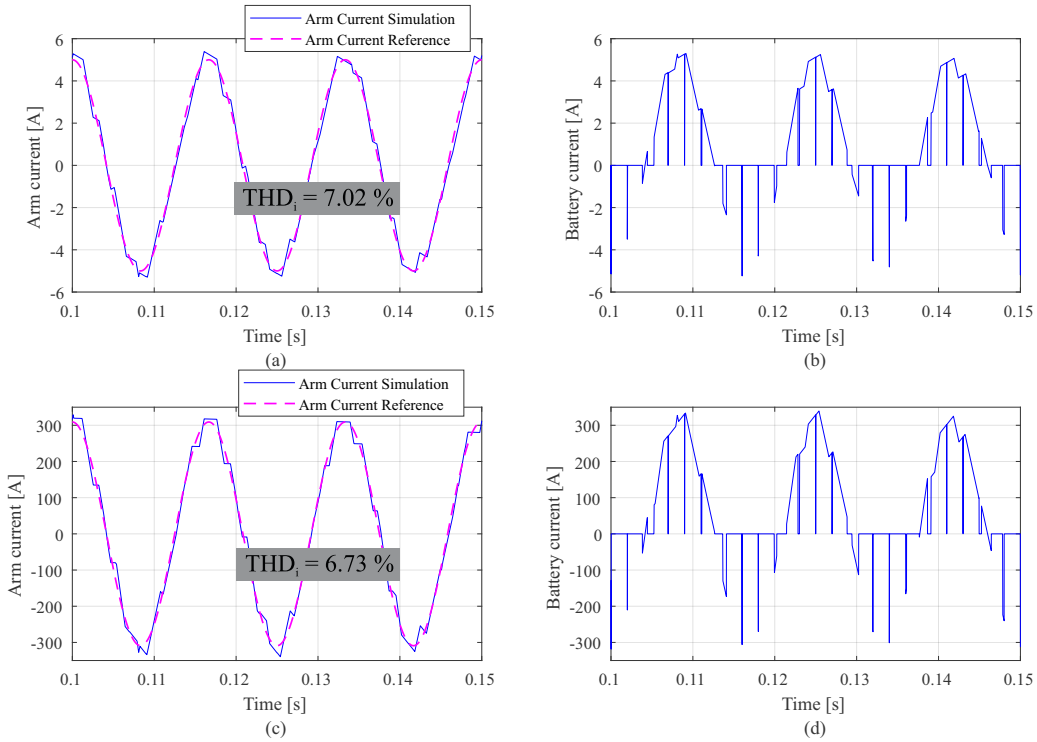
For the full MMC simulation level, the arm current and battery current waveforms are shown in Fig. 41 (c) and (d), respectively. At this current level, there is a THD_i of around 4.94 % for the arm current, with the maintenance of the harmonic content of the battery current. The combination of $V_{dc,em}$ and L_{em} were combined according to Tab. 15 in the simulation condition of the full MMC simulation (the peak value in the arm current around 309 A).

Table 15 – MPE dc-link voltage and THD_i results for Full MMC Simulation and Testing Scheme.

MPE and SM Frequency	$\text{V}_{dc,em}$ [V]	THD_i [%]	L_{em} [mH]
$f_{sw,MPE} = f_{sw,SM} = 500$ Hz (Full MMC Simulation)	8000	6.73	60
$f_{sw,MPE} = f_{sw,SM} = 500$ Hz (Testing Scheme)	50	7.02	25

For the full MMC simulation level, the arm current and battery current waveforms are shown in Fig. 41 (c) and (d), respectively. At this current level, there is a THD_i of around 6.73 % for the arm current, with the maintenance of the harmonic content of the battery current. The combination of $V_{dc,em}$ and L_{em} were combined according to Tab. 15

Figure 41 – Simulation waveforms of the (a) arm current and (b) battery current for the $f_{sw,MPE} = f_{sw,SM} = 500$ Hz with arm current peak equal to 5 A and simulation waveforms of the (c) arm current and (d) battery current for the $f_{sw,MPE} = f_{sw,SM} = 500$ Hz with arm current peak equal to 309 A.



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in the simulation condition of the full MMC simulation (the peak value in the arm current around 309 A).

Based on the results obtained for the conditions of $f_{sw,MPE} = f_{sw,SM} = 1$ kHz and $f_{sw,MPE} = f_{sw,SM} = 500$ Hz, it can be seen that the transition to frequencies below 1 kHz already leads to a worse ability to use the MPE to emulate typical arm and battery currents, aiming to analyze an application MMC-based BESS. Even though the dc-link voltage of MPE and MPE inductance requirements are varied, considerable values of these variables are necessary to obtain THD_i indices close to reasonable, with losses in the harmonic content of the battery current. In this sense, the study revealed the need for a cost and operational feasibility study aimed at reducing the switching frequency requirements and the consequent reduction of MPE and SM switching losses.

The experimental analysis obtained can be extended to a mathematical analysis, based on the type of current waveform to be synthesized with well-defined amplitude and phase. For example, for a signal with full control of a 60 Hz component in the arm current and considering the insertion of the resonant module in the third harmonic, probably to mitigate interference from the submodule control, at least a 600 Hz control bandwidth would be necessary. Thus, based on the desired current ripple value for the arm inductor,

an analysis can be made of which combinations of bus voltage, switching frequency and inductance will meet the MPE design premises. Finally, if this minimum frequency limit can be applied in a full-bridge converter, this topology is adopted, otherwise, the study for an alternative topology is evaluated.

3.6 Chapter Summary

In this chapter, the proposed methodology for the model and design of an MPE was evaluated in terms of control dynamics and maximum arm current ripple with a full-bridge converter. The experimental results indicated that the converter dynamics with the design implemented are suitable for emulating SM steady-state waveforms of MMC-based BESS during the battery discharging and charging process. Furthermore, the reactive power injection or absorption operation was validated, also proving suitable for emulating the MMC-based BESS.

The arm current transient is smooth and does not significantly affect the converter dynamics. Furthermore, the results showed that the estimated maximum arm current ripple shows good agreement with the approximation to design an MPE inductor. In addition, the spectrum of arm and battery current showed that the harmonic contents of these signals are similar to the experimental and simulation results, according to the typical current spectrum observed in the MMC-BESS.

The studies referring to the effect of the MPE and SM switching frequency demonstrated that the relationship between these two variables is fundamental to obtaining results consistent with emulating the typical current and voltage profiles of the MMC-based BESS. The approach proved to be valid, improving the aspects of ripple in the battery current and THD_i. Furthermore, it was experimentally verified that the equal relationship between the two frequencies makes good emulation possible in the frequency range of up to 5 kHz in the two converters (for the MPE inductance analyzed). In addition, the lower the SM frequency concerning the MPE frequency, the better the content of the waveform synthesized by the MPE, also evidenced by the maximum arm current and THD_i values.

Based on the presented evaluation of the MPE operation and the experimental verification of critical harmonic components in the battery current, Chapter 4 will address the first method to mitigate these components, through passive filters. An approach to the design methodology will be carried out, with validation through simulation and test bench of the designed filter.

4 Integrating Battery into SM Using Passive Filters

This chapter introduces the harmonic suppression methods for attenuating the harmonic components of the current flowing through the battery integrated into MMC submodules. The methodology is focused on designing two passive filter topologies, considering a low-pass LC filter, denominated as LC filter, and a tuned LC filter combined with an LC low-pass filter, denominated as CL-LC filter.

The filter design results are evaluated in terms of frequency response. For the implemented LC filter, the influence of damping ratio and attenuation are evaluated. In turn, the impact of the damping resistor and resonance frequency are evaluated for the CL-LC filter. Discussions about the minimum and maximum capacitance and inductance values for the filters are addressed. Besides, the design points of passive filters are determined. Finally, the simulation results for the LC and CL-LC filters are presented, proving the expected attenuation. The experimental result is presented considering the implementation of the LC filter on an experimental bench, validating the expected attenuation according to the empirical equations and simulation results.

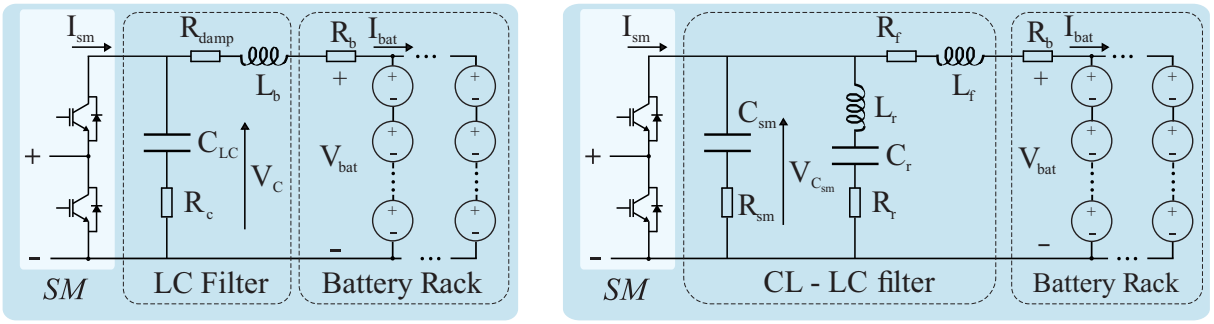
4.1 Passive Filters Design

Section 2.3 and the results in Chapter 3 showed that the passive filter needs to attenuate one relatively large first-order harmonic, a significant second-order harmonic, and a considerable fourth-order harmonic. A low-pass filter could be designed to do this, but to attenuate such low frequencies, very bulky components would be required. In this sense, this work proposes to analyze a typical low-pass LC filter, presented in Fig. 42(a), and a filter with a lower requirement for inductance and capacitance. The chosen filter is a tuned LC filter combined with an LC low-pass filter (CL-LC filter), shown in Fig. 42(b). In both topologies, the battery bank is modeled as an equivalent resistance (R_b), and the connection in series and parallel of batteries open circuit voltage.

All these filters can be tuned to attenuate a specific frequency. The direct advantage of applying a first-order low-pass filter at the 60 Hz frequency is to eliminate the other undesirable harmonic components, due to the natural response of the filter. However, the filtering requirements, in terms of capacitance and inductance, are considerable.

In turn, the CL-LC filter can attenuate the 60 Hz frequency, but with the possibility of not suppressing the other harmonics, depending on the type of frequency response of the designed filter. Therefore, combining two filters is an interesting strategy in the sense

Figure 42 – Topologies of passive filters for harmonic suppression in battery current (a) low-pass LC filter (b) tuned LC filter combined with an LC low-pass filter (CL-LC filter).



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of using the advantage of both filters and consequently suppressing the desired harmonics. As a disadvantage of this proposal, there is an increase in the filter design effort, since it works with the design of more than two reactive components, in addition to dealing with resonance frequencies.

4.2 LC Filter Design

The transfer function from the input current of SM to the batteries using the LC filter, presented in Fig. 42(a), is given by:

$$G_1(s) = \frac{I_{bat}(s)}{I_{SM}(s)} = -\frac{R_c C_{LC} s + 1}{L_b C_{LC} s^2 + (R_{damp} + R_b + R_c) C_{LC} s + 1}. \tag{4.1}$$

where R_c is the capacitor intrinsic resistance, C_{LC} is the capacitance of LC filter, L_b is the series inductance, R_{damp} is the damp resistor of LC filter and R_b is the battery resistance. In addition, the transfer function of capacitor SM voltage and input current of SM is given by:

$$G_{1,v}(s) = \frac{V_C(s)}{I_{SM}(s)} = \frac{C_{LC} L_b R_c s^2 + (R_b R_c C_{LC} + L_b) s + R_b}{L_b C_{LC} s^2 + (R_{damp} + R_b + R_c) C_{LC} s + 1}. \tag{4.2}$$

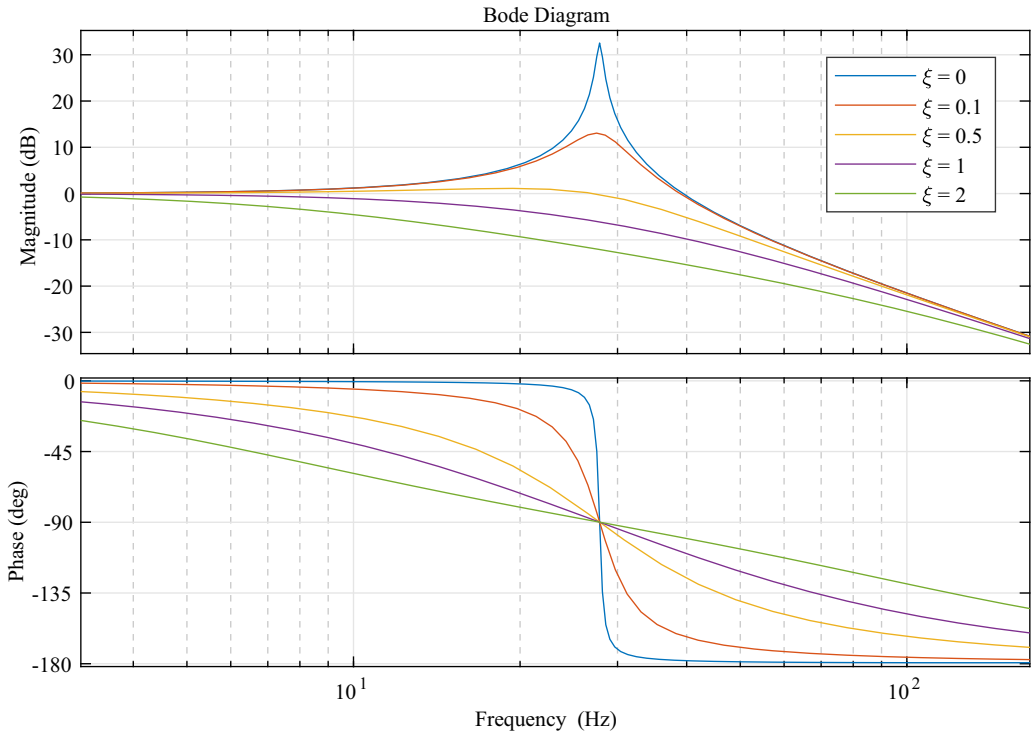
Based on the equations (4.1) and (4.2) the goal is to find parameters for the filter inductor and filter capacitor that will suppress the first, second, and fourth harmonic of the battery current and capacitor voltage ripple caused by the SM input current.

The analysis can be done for the 60 Hz frequency since the analyzed filter is a low-pass filter. Thus, higher harmonics will be also suppressed. For this study, the minimum attenuation of battery current in the 60 Hz component is adopted equal to -15 dB, which corresponds to a reduction of approximately 82.21%. In turn, the voltage attenuation of the

capacitor is adopted as equal to -7.5 dB, which corresponds to a reduction of approximately 57.83%.

The LC filter has a typical range without typical attenuation of the filter (magnitude in positive dB), which corresponds to a region of no interest to the project since it can attenuate the 60 Hz frequency and increase the neighboring frequencies. This effect can be seen in Fig. 43 for the curve where the damping ratio, ξ, is varied in equation (4.1). In this sense, a damping resistor is adopted in series with the filter inductor to reduce the resonant peak.

Figure 43 – Bode diagram of the LC low-pass filter highlighting the frequency response for different damping ratios - zoomed view with frequency range from 3 Hz to 200 Hz.



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Values of ξ above 0.5 are adequate to suppress the resonant effect, with the counterpart of increasing the ohmic losses in the inserted damping resistor. The characteristic equation of the $G_1(s)$ transfer function presents the determination of the damping resistance (R_{damp}) as a function of the LC filter parameters:

$$L_b C_{LC} s^2 + (R_{damp} + R_b + R_c) C_{LC} s + 1 = 0 \Rightarrow s^2 + \frac{(R_{damp} + R_b + R_c)}{L_b} s + \frac{1}{L_b C_{LC}} = 0. \quad (4.3)$$

The equation (4.3) can be formally expressed by the damping ratio (ξ) and the natural frequency (ω_n) as shown:

$$s^2 + (2\xi\omega_n)s + \omega_n^2 = 0 \Rightarrow s^2 + \frac{(R_{damp} + R_b + R_c)}{L_b}s + \frac{1}{L_b C_{LC}} = 0. \tag{4.4}$$

In this sense, considering that $R_{damp} \gg (R_b + R_c)$, the damping ratio can be expressed by:

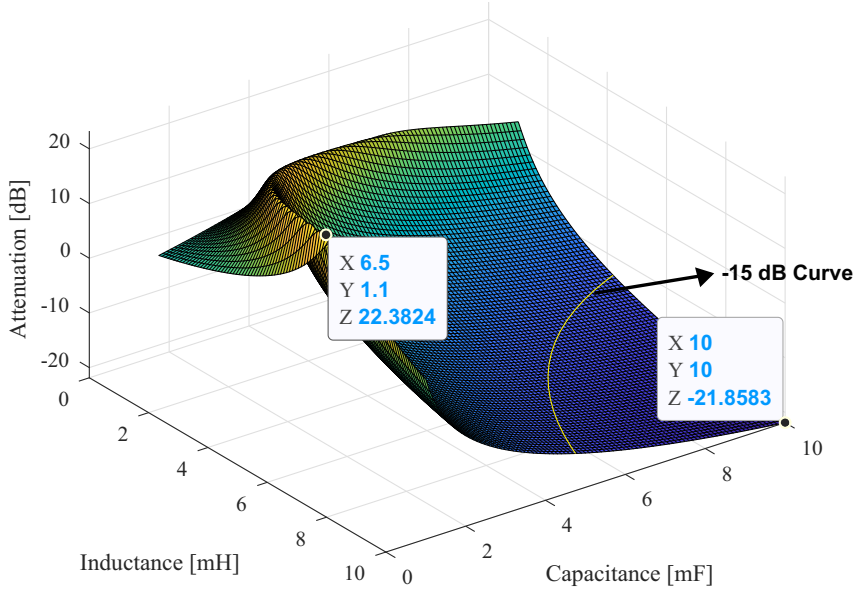
$$\xi = \frac{R_{damp}}{2\omega_n L_b} \Rightarrow R_{damp} \approx 2\xi\sqrt{\frac{L_b}{C_{LC}}}. \tag{4.5}$$

In addition, the equivalent series resistance (ESR) of the filter inductor is assumed to be (Puranik; Zhang; Qin, 2018):

$$\frac{X_{L_b}}{R_{damp}} = \frac{2\pi L_b f_g}{R_{damp}} = 40. \tag{4.6}$$

Fig. 44 presents a 3D surface indicating the combinations of inductance and capacitance filter requirements with their maximum attenuation values, in dB, for the desired 60 Hz frequency, for L_b ranging from 1 to 10 mH, and C_{LC} ranging from 1 to 10 mF.

Figure 44 – 3D surface for the attenuation, in dB, of the LC low-pass filter as a function of the inductance and capacitance filter requirements.



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It can be seen that the ideal range (attenuation values lower than -15 dB) is limited by the curve indicated in yellow, which presents all combinations of L_b and C_{LC} that result in such attenuation. For the analyzed capacitance and inductance range, expressed in Fig. 44, the maximum attenuation is obtained at -21.85 dB.

4.3 CL-LC Filter Design

Similarly, the CL-LC filter is analyzed. In this sense, the transfer function from the input current of SM to the batteries is given by:

$$G_2(s) = -\frac{n_2(s)}{d_2(s)}. \tag{4.7}$$

where the numerator $n_2(s)$ is expressed by:

$$n_2(s) = C_{sm}R_{sm}C_rL_rs^3 + (C_{sm}R_{sm}C_rR_r + C_rL_r)s^2 + (C_{sm}R_{sm} + C_rR_r)s + 1 \tag{4.8}$$

and the denominator $d_2(s)$ is given by:

$$\begin{aligned} d_2(s) = \; & C_rC_{sm}L_fL_rs^4 + [C_rC_{sm}L_r(R_{bat} + R_f) + C_rC_{sm}R_{sm}(L_f + L_r)\,]s^3 + \\ & [C_rC_{sm}R_r(R_{bat} + R_f) + C_rC_{sm}R_{sm}(R_{bat} + R_f) + \\ & C_rC_{sm}R_rR_{sm} + C_{sm}L_f + C_r(L_f + L_r)\,]s^2 + \\ & [(C_r + C_{sm})(R_{bat} + R_f) + C_rR_r + C_{sm}R_{sm}\,]s + 1 \end{aligned} \tag{4.9}$$

The numerator $n_2(s)$ and denominator $d_2(s)$ of the equation (4.7) are given as a function of the capacitance, inductance and resistance parameters of the filter. In this sense, the C_{sm} is the SM capacitance of CL-LC filter, R_{sm} is the intrinsic resistance of SM capacitance, L_r is the trap filter inductance, C_r is the trap filter capacitor, R_r is the equivalent resistance of series combination of C_r and L_r, L_f is the series inductance of CL-LC filter and R_f is the intrinsic resistance of L_f.

In addition, the transfer function of capacitor SM voltage and input current of SM is given by:

$$G_{2,v}(s) = \frac{V_{C_{sm}}(s)}{I_{SM}(s)} = \frac{2(R_b + R_f + L_fs)n_2(s)}{d_2(s)}. \tag{4.10}$$

In the resonance frequency, the resonant branch impedance is zero. Thus, the values of L_r and C_r are defined as:

$$j\omega_rL_r + \frac{1}{j\omega_rC_r} = 0. \tag{4.11}$$

Since $j^2 = -1$ and $\omega_r = 2\pi f_r$, the capacitance of the LC tuned filter can be expressed as:

$$C_r = \frac{1}{2\pi\sqrt{L_r f_r}}. \tag{4.12}$$

Since the filter has four degrees of freedom for design, this work adopts the definition of the capacitance of the tuned LC filter as a percentage of the capacitance of the LC filter (Zhang; Li, 2015):

$$C_r = \alpha_C C_{sm}. \tag{4.13}$$

where α_C is the percentual value of C_{sm}. This design strategy is discussed in Zhang and Li (2015). Since the LC trap frequency is designed much higher than the 60 Hz frequency, fewer power losses are generated by the ESR of the LC-tuned filter. Thus, the value of α_C is expected to be less than 1.

In this way, based on the equations (4.12) and (4.13), it is possible to reduce the design variables of the LC filter from a fourth-order problem to a second-order problem, in which the inductances and capacitances are related.

The ESR of the series inductor (L_f) and tuned inductor (L_r) are assumed to be a function of the X/R ratio, respectively (Puranik; Zhang; Qin, 2018):

$$\frac{X_f}{R_f} = \frac{2\pi L_f f_r}{R_f} = 40, \tag{4.14}$$

$$\frac{X_r}{R_r} = \frac{2\pi L_r f_r}{R_r} = 40. \tag{4.15}$$

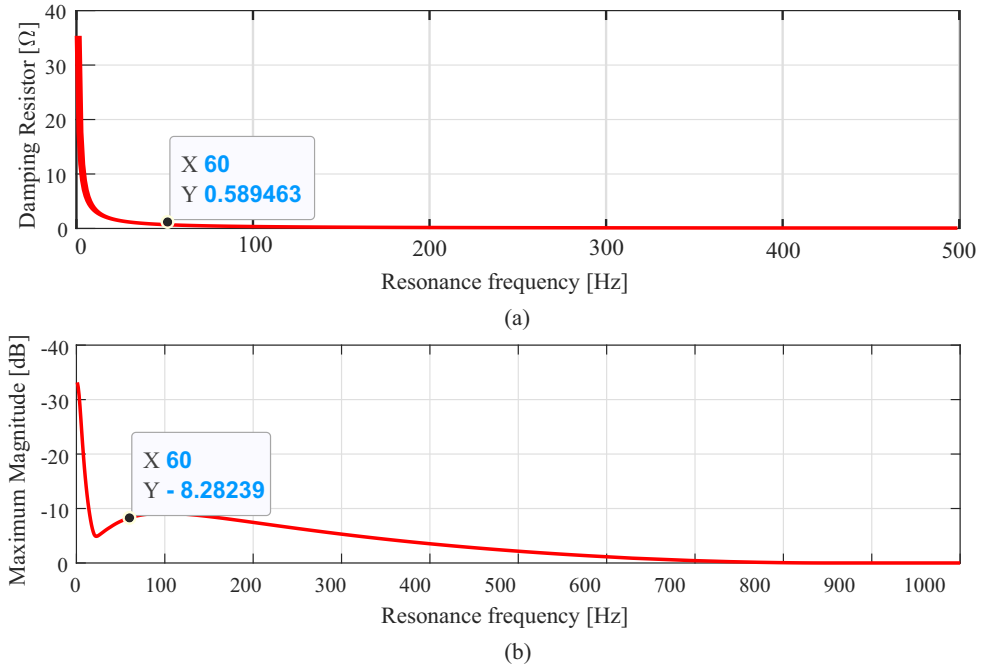
As a solution to reduce the resonant frequencies present in the analyzed CL-LC filter, a damping resistance is adopted in series with the inductor of the tuned LC component. The idea is to reduce the two resonant peaks characteristic of this filter topology by smoothing the filter frequency response (Calzo et al., 2013; Zhang; Li, 2015).

In this sense, for an LC trap frequency equal to 60 Hz, the maximum attenuation in dB and damping resistor is evaluated, as presented in Fig. 45.

Fig. 45 (a) presents the values of the damping resistance for the underdamped type response condition ($\xi = 0.5$), which presents the minimum condition to reduce the values of the typical resonances of the CL-LC filter. The damping resistance ($R_{damp,CL-LC}$) is computed by:

$$R_{damp,CL-LC} \approx \sqrt{\frac{L_r}{C_r}} \text{ (for } \xi = 0.5), \tag{4.16}$$

Figure 45 – Analysis of the effect of inserting a damping resistor in the tuned LC filter combined with an LC low-pass filter (a) damping resistor for $\xi = 0.5$ (b) maximum attenuation in dB.



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In addition, Fig. 45 (b) shows the maximum attenuation value, in dB, provided by inserting the damping resistance in the battery current, at different values of the LC trap frequency.

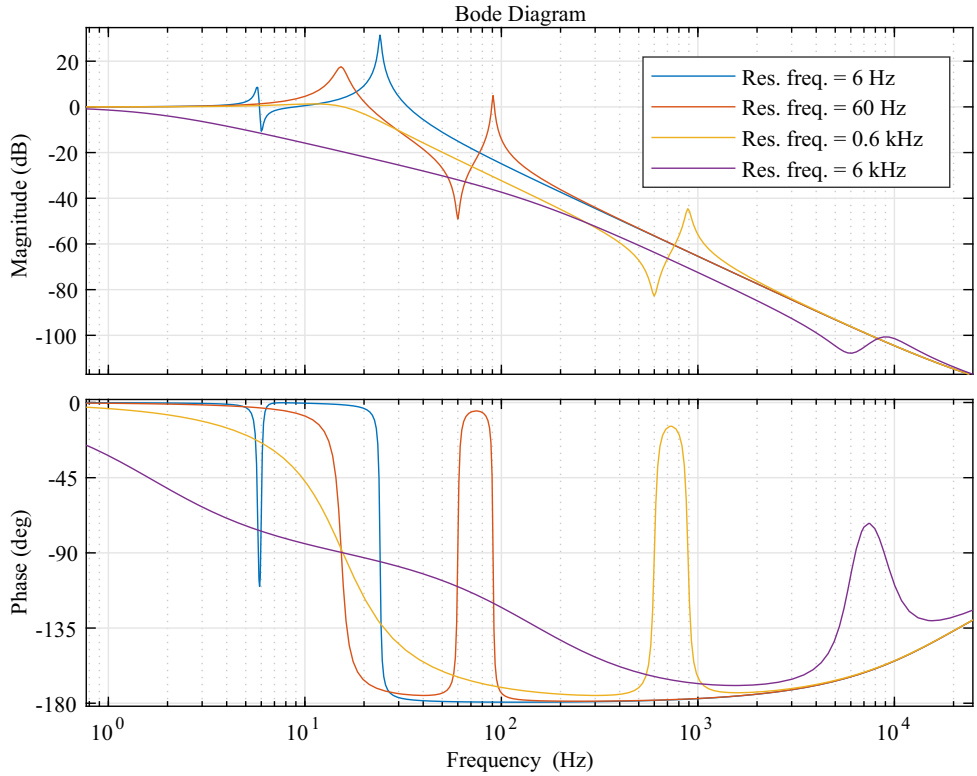
In this sense, it is verified that for the 60 Hz frequency of interest, the attenuation of the battery current does not reach the minimum stipulated value of -15 dB, in addition to requiring a significant damping resistance of 0.584 Ω that would lead to the addition of considerable losses in the CL-LC filter.

As an alternative solution to insert damping resistance, the variation of the LC trap frequency, outside the value of the 60 Hz frequency, is performed. Fig. 46 shows the Bode diagram for different combinations of resonant frequencies of the CL-LC filter with a percentage of the capacitance of the tuned LC filter equal to 30% of the capacitance of the LC low-pass filter.

As shown in Fig. 46, the resonance effect is reduced as the resonance frequency increases, which is attractive for the desired low harmonic suppression. As verified, despite the effectiveness of tuning the filter to the 60 Hz frequency significantly reducing the highest harmonic component, components neighboring this frequency can be enhanced, returning to the problem of increasing battery degradation.

In this sense, a possible solution would be to work with a higher tuned frequency, which leads to the response of the CL-LC filter to low-pass characteristics, with the

Figure 46 – Bode diagram of the CL-LC filter highlighting the frequency response for the different resonant frequencies with $\alpha_C = 0.3$ - zoomed view with a frequency range from 1 Hz to 20 kHz.



Source: own representation.

presence of characteristic peaks in the attenuation region, which is no longer a problem for neighboring frequencies. Thus, as an advantage, there is a reduction in the need for the L and C components characteristic of the LC low-pass filter previously presented, with analogous frequency response.

Based on the analyses carried out to suppress the resonance effect of the CL-LC filter and the damping resistance insertion strategies, as well as the resonance frequency variation (LC trap frequency), the considerations during their design are summarized as (Zhang; Li, 2015):

- Damping resistor ($R_{damp,CL-LC}$): a tradeoff between the damping of resonance and the trapping performance of the LC trap branch is verified;
- Capacitance of the LC low-pass filter component in CL-LC filter: The decrease of C_{sm} can contribute to the improvement of the filter power factor, but such a reduction should be proper with the considerations of the absorption of high-order battery current harmonics (above LC trap frequency);
- Inductance (L_r) and capacitance (C_r) of the LC trap branch: The LC trap frequency needs to be carefully designed to guarantee that the LC trap branch can effectively

absorb the dominant harmonics in battery current. The type of damping resistor and trap frequency adopted is 600 Hz to reach the desired attenuation criterion in dB.

The three considerations presented are adopted for the design of the CL-LC filter, as presented in the next section.

4.4 Evaluation of LC and CL-LC Filter Design

The filter design point to define the capacitance and inductance values of the LC and CL-LC filters is given based on the transfer functions that relate the ripple attenuation in the battery current and the SM input voltage. In this sense, based on the definition of the minimum attenuation of -15 dB for the battery current ripple and - 7.5 dB for the voltage ripple on the SM input capacitor, the intersection between the two curves is defined as the design point of the filter.

To limit the inductance and capacitance values of the two presented filter topologies, the maximum and minimum values are defined based on the maximum and minimum values of voltage and current ripple.

In this sense, the maximum and minimum capacitance values of the LC filter and CL-LC filter can be defined based on the voltage ripple on the SM input capacitor (defined as C_{LC} for the LC low-pass filter and C_{sm} for the CL-LC filter), respectively (Cupertino et al., 2019):

$$C_{min} = \frac{24(\sqrt{3}+13)}{144\sqrt{3}} \frac{Q_n}{\omega_g \hat{V}_g \Delta V_{C,min} V_{sm}}, \tag{4.17}$$

$$C_{max} = \frac{24(\sqrt{3}+13)}{144\sqrt{3}} \frac{Q_n}{\omega_g \hat{V}_g \Delta V_{C,max} V_{sm}}. \tag{4.18}$$

Furthermore, the maximum and minimum values of the inductance of the LC low-pass filter and CL-LC filter can be set based on the voltage drop in the filter inductor in series with the SM battery (set to L_b for the LC low-pass filter and L_f for the CL-LC filter), respectively:

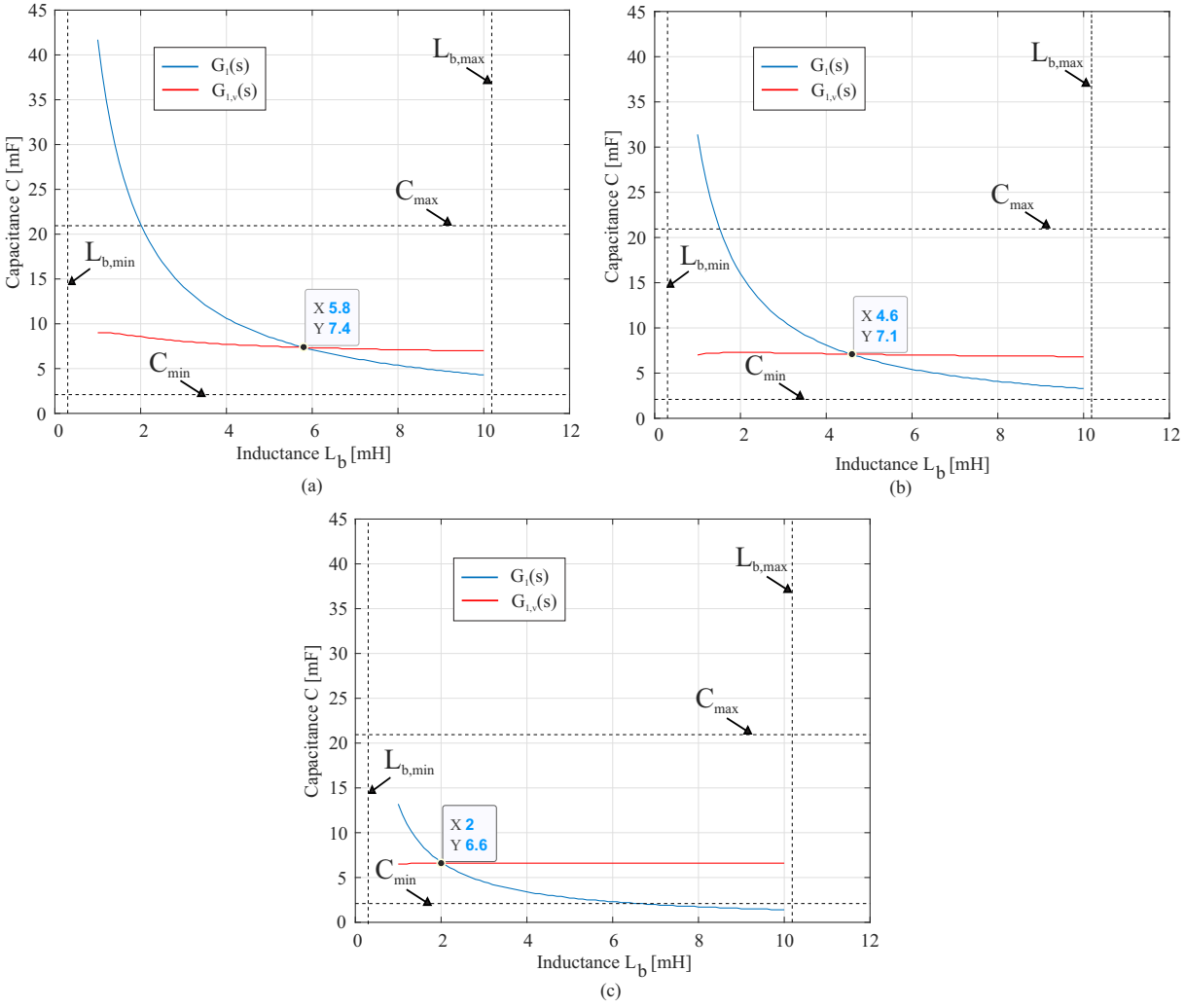
$$L_{min} = \frac{\frac{X_L}{R_L} \Delta V_{L,min} V_{sm}}{\pi f_g \hat{I}_b}; \tag{4.19}$$

$$L_{max} = \frac{\frac{X_L}{R_L} \Delta V_{L,max} V_{sm}}{\pi f_g \hat{I}_b}. \tag{4.20}$$

4.4.1 Determining the Design Points of Passive Filters

First, the design points for the LC filter are evaluated. Fig. 47 (a) presents the contour plot for the damping factor (ξ) equal to 0.5 (underdamped response). The critically damped response and overdamped response ($\xi = 1$ and $\xi = 2$, respectively) are presented in Fig. 47 (b) and (c), respectively.

Figure 47 – Contour plot for G_1(s) = -15 dB and $G_{1,v}$(s) = -7.5 dB as a function of capacitance and inductance components. Contour plot for (a) $\xi = 0.5$ (b) $\xi = 1$ and (c) $\xi = 2$.



Source: own representation.

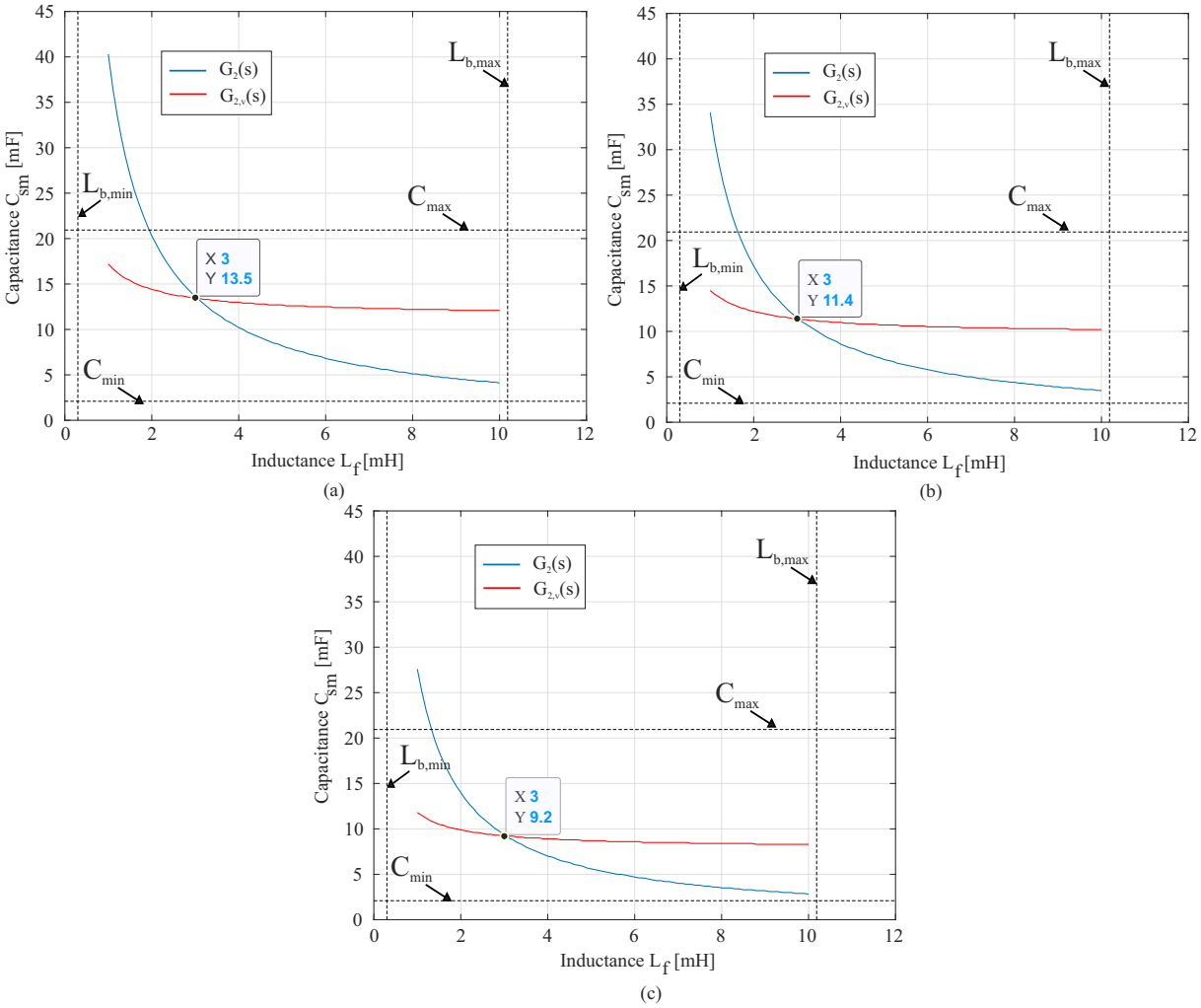
As shown in Fig. 47, the points highlighted in black, the intersection of the attenuation curves, are given as the filter design points. In addition, the dashed curves limit the design region of the filter based on the limits of current and voltage ripples discussed previously.

In this sense, for the LC filter, it is verified that the increase in the damping factor leads to a significant reduction in the filter inductance, with a reduction of approximately 65.5 % in the scenario from $\xi = 0.5$ to $\xi = 2$. On the other hand, the variation of the

capacitance of the LC filter is subtle (approximately 10.81% reduction), due to the small effect of the insertion of the damping resistor on the voltage ripple of the SM capacitor. Despite the advantage of reducing filter requirements, mainly impacting cost and volume, it is worth mentioning that there is an impact on filter ohmic losses, due to the increase in damping resistance, characterizing a trade-off.

Analogously, the filter design point analysis can be applied to the CL-LC filter topology. Fig. 48 presents the contour plot for a percentage of the capacitance of the low-pass LC filter included in CL-LC filter (α_C) equal to 0.1, in Fig. 48 (a), $\alpha_C = 0.3$, in Fig. 48 (b) and $\alpha_C = 0.6$, in Fig. 48 (c).

Figure 48 – Contour plot for G_2(s) = -15 dB and $G_{2,v}$(s) = -7.5 dB as a function of capacitance and inductance components for $f_r = 600$ Hz. Contour plot for (a) $C_r = 0.1\ C_{sm}$ (b) $C_r = 0.3\ C_{sm}$ and (c) $C_r = 0.6\ C_{sm}$.



Source: own representation.

For the CL-LC filter, there is a small influence on the value of the series inductance with the battery, located in the LC low-pass component. In all cases of the reduced capacitance of the tuned LC filter, the value of the design inductance (L_f) remained

constant, due to the maintenance of the value of the resonance frequency at 600 Hz. Furthermore, the variation of the capacitance of the tuned LC filter has a direct effect on the ripple of the SM input capacitor voltage (C_{sm}).

On the other hand, the SM input capacitance has a reduction in its value with the increase of the percentage ratio, due to the contribution in the attenuation of the voltage ripple verified in the voltage capacitance of the input of the SM. Therefore, a reduction of 31.82 % of C_{sm} is observed, in the $\alpha_C = 0.1$ to $\alpha_C = 0.6$.

Comparing the values obtained for series inductance with the battery, for the analyzed LC and CL-LC filter topologies, there is a reduction in the filter inductance requirement, directly responsible for limiting the cost and volume values of the filter. The reduction of the series inductance with the battery from the most realistic scenario of the low-pass LC filter ($\xi = 1$) to the best scenario of the CL-LC filter ($\alpha_C = 0.6$) is approximately 34.78 %. In turn, the value of the input capacitance of the SM presents an increase of 29.57 %, as a counterpart of the gain in terms of attenuation of the battery current.

4.5 Filter Analysis - Simulation and Experimental Results

Tab. 16 presents the main system parameters adopted to evaluate the proposed design of the LC and CL-LC filters.

Table 16 – Main system parameters for the evaluation of LC and CL-LC filter design.

Parameters	Symbol	Value
Maximum arm inductor voltage ripple [%]	$V_{L,max}$	10
Minimum arm inductor voltage ripple [%]	$V_{L,min}$	1
Maximum SM capacitor voltage ripple [%]	$V_{C,max}$	10
Minimum SM capacitor voltage ripple [%]	$V_{C,min}$	1
Grid frequency [Hz]	f_g	60

Based on the values of the main system parameters for the LC and CL-LC filter, the following design points for the two passive filter topologies are employed:

- LC low-pass filter: $\xi = 1$;
- CL-LC filter: $\alpha_C = 0.6$ and $f_r = 600$ Hz.

These parameters are adopted for validation both in the full MMC system simulation and in the experimental results.

Firstly, the simulation results for the full MMC system and the MPE simulation will be evaluated, with the same typical values of SM voltage and arm current in both simulations.

In sequence, as the idea is to validate this approach in the laboratory, the design values for low voltage, current, and power were adopted too. Thus, the MPE parameters are set on a peak of arm current of 5 A, battery bank of 24 V, and limited to a 150 W bench source (emulator dc-link voltage).

4.5.1 Simulation Analysis - MMC-based BESS and MPE

The performance of the MPE is compared with the full MMC system simulation of 10.9 MVA/13.8 kV and 12.6 MWh of BESS, equal to the MMC-based BESS implemented in Chapter 3 (the main parameters for the MMC-based BESS simulation are shown in Table 4). The simulation results are developed on the PLECS platform. In this simulation analysis, the LC low-pass and CL-LC filters are evaluated, according to the parameters presented in Table 17.

Table 17 – Main Parameters of the LC low-pass and CL-LC Filter in Full MMC System Simulation and MPE Simulation.

Parameters	Symbol	Value
Capacitance of LC filter [mF]	C_{LC}	7.1
Series Inductance of LC filter [mH]	L_b	4.6
Damp Resistance of LC filter [Ω]	R_{damp}	1.6
SM capacitance of CL-LC filter [mF]	C_{sm}	9.2
Trap filter inductance [mH]	L_r	0.14
Trap filter capacitance [mF]	C_r	5.52
Series inductance of CL-LC filter [mH]	L_f	3

4.5.1.1 Simulation Analysis: LC filter

Firstly, the results of the LC filter are evaluated. Fig. 49(a) shows the arm current obtained from the full MMC-based BESS and MPE simulation. In both simulations, the arm current reference is set to an amplitude of approximately 309 A. Fig. 49(b) shows that the maximum value of the MPE inductor current ripple is approximately 30.68 A, which corresponds to 9.92% (which is following the maximum limit of 10 % set for the MPE design) of the arm current reference peak.

Based on the spectrum of the arm current, shown in Fig. 49(c), it is observed that the harmonic contents of both currents are similar, evidencing an ac signal with negligible harmonic distortions.

Fig. 50(a) shows the current measurements in the batteries of the SMs in the MMC upper arm, as well as the battery current measured in the MPE. Once the full MMC-BESS simulation implements all the SMs of the MMC, the 15 signals of battery current in the upper arm of phase A are presented. It is also possible to check that all batteries are charging, with slightly different battery current values. This can be explained by the NLC modulation process and the performance of SOC control.

Figure 49 – (a) Arm current with LC filter in the SM (b) arm current ripple (c) frequency spectrum of arm current.

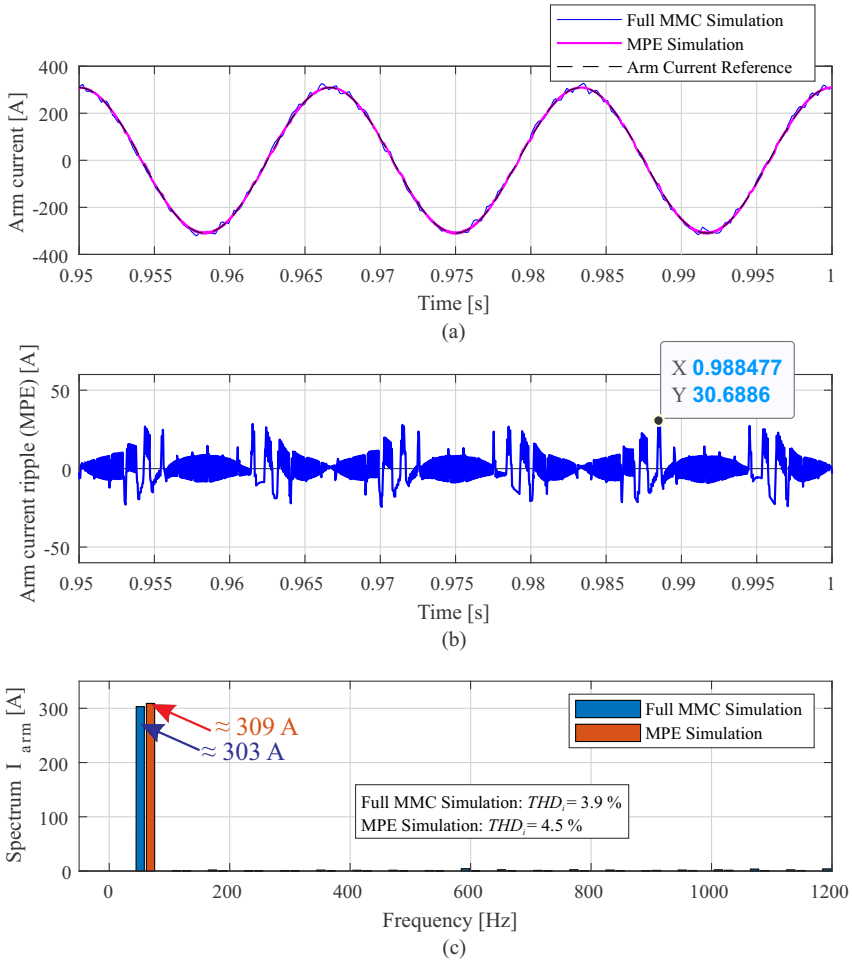


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Figure 50 – (a) Battery current in SM with LC filter (b) spectrum of battery current.

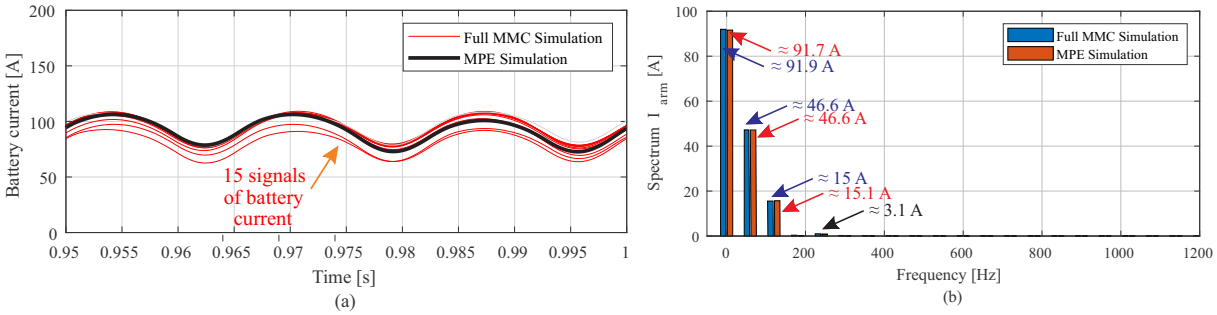

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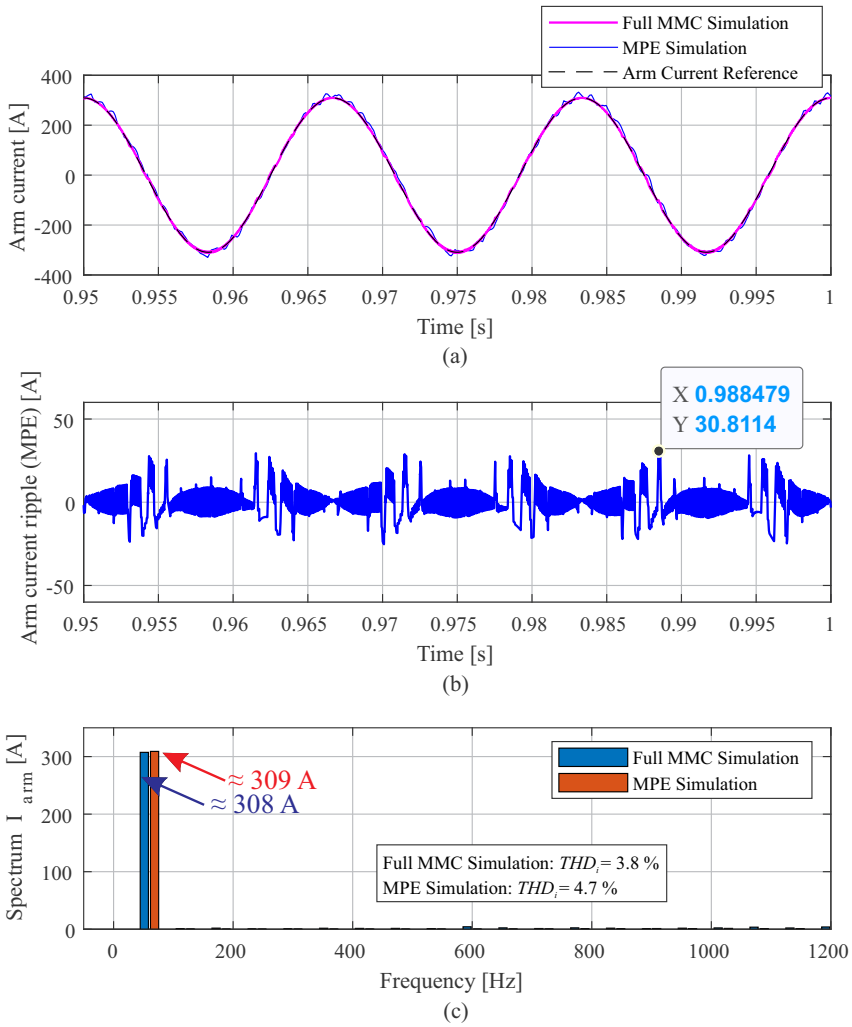
Fig. 50(b) shows the average current spectrum of the 15 battery current signals obtained in the simulation of MMC. The harmonic contents of the battery current for both models are similar, especially for the most significant components dc, 1^{st}, 2^{nd}, and 4^{th} order. Furthermore, the result shows that even using different modulation techniques (NLC, for full MMC simulation, and PWM, for the MPE), the emulator low-frequency spectral

content is well represented. In addition, it is possible to verify that the dc component in Fig. 27(b) is practically preserved, with a substantial reduction in the first, second, and fourth harmonic components.

4.5.1.2 Simulation Analysis: CL-LC filter

Once the results of the LC filter have been evaluated, the same study is conducted for the CL-LC filter. Fig. 51 (a) shows the arm current obtained from the full MMC-based BESS and MPE simulation. Again, in both simulations, the arm current reference is set to an amplitude of approximately 309 A.

Figure 51 – (a) Arm current with CL-LC filter in the SM (b) arm current ripple (c) spectrum of arm current.



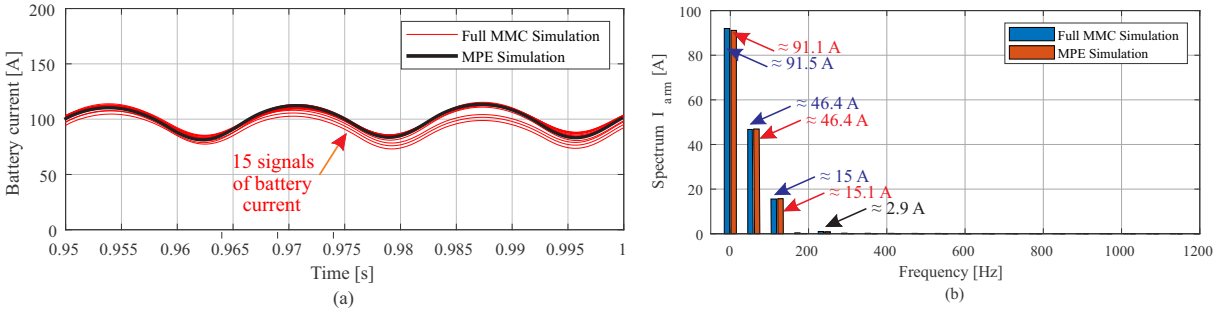
Source: own representation.

Fig. 51 (b) shows that the maximum value of the MPE inductor current ripple is approximately 30.81 A, which corresponds to 9.97% (which is following the maximum limit of 10 % set for the MPE design) of the arm current reference peak.

Based on the frequency spectrum of the arm current, shown in Fig. 51 (c), it is observed that the harmonic contents of both currents are similar. Again, the frequency spectrum evidences an ac signal (with emphasis on the fundamental component) and proximity between the THD_i values, which are less than 5 %.

Fig. 52 (a) shows the current measurements in the batteries of the SMs in the MMC upper arm, as well as the battery current measured in the MPE. Once the full MMC-BESS simulation implements all the SMs of the MMC, the 15 signals of battery current in the upper arm of phase a are presented. Again, it is also possible to check that the batteries are charging with a different level of current, for the same reason discussed previously.

Figure 52 – (a) Battery current in SM with CL-LC filter (b) spectrum of battery current.



Source: own representation.

Fig. 52 (b) shows the average current spectrum of the 15 battery current signals obtained in the simulation of MMC. The harmonic contents of the battery current for both models are similar, especially for the most significant components dc, 1^{st}, 2^{nd}, and 4^{th} order. Furthermore, the result shows that even using different modulation techniques (NLC, for full MMC simulation, and PWM, for the MPE), the emulator low-frequency spectral content is well represented.

4.6 Comparison of LC and CL-LC filter

The attenuation results for the 60Hz, 120Hz, and 240 Hz components in the battery current of the LC filter simulations are summarized in Tab. 18. It is possible to verify a high similarity in the attenuation results in the analyzed frequency range. The largest differences in attenuation (as seen in the bode diagram) occur at frequencies above 500 Hz. Furthermore, the proposed reduction of -15 db in the 60 Hz component of the current in the batteries is highlighted, with a consequent reduction in the other components.

In addition, the attenuation results for the 60Hz, 120Hz, and 240 Hz components in the battery current of the CL-LC filter simulations are summarized in Tab. 19. Again,

Table 18 – Harmonic Current Attenuation Analysis: LC Filter.

Harmonic Current Component	MMC-based BESS Simulation	MPE Simulation
60 Hz	82.9 % (-15.3 dB)	82.3 % (-15.04 dB)
120 Hz	95.1 % (-26.1 dB)	95.5 % (-26.9 dB)
240 Hz	98.9 % (-39.2 dB)	99 % (-40 dB)

it is possible to verify a high similarity in the attenuation results in the analyzed frequency range.

Table 19 – Harmonic Current Attenuation Analysis: CL-LC Filter.

Harmonic Current Component	MMC-based BESS Simulation	MPE Simulation
60 Hz	82.8 % (-15.3 dB)	82.2 % (-14.9 dB)
120 Hz	95.2 % (-26.4 dB)	95.1 % (-26.2 dB)
240 Hz	98.9 % (-39.1 dB)	98.7 % (-37.7 dB)

In terms of attenuation capacity, the two filter designs, LC and CL-LC, proved to be quite effective, with high similarity between the attenuations in the 60 Hz, 120 Hz, and 240 Hz components. These results demonstrate the effectiveness of the proposed methodology for the design of these filters. However, aspects of comparison and selection between different filters are necessary for decision-making regarding which type of filter to apply for a given application.

One of the aspects used to compare passive filters involves an estimate of the size of the filter. This variable is directly related to the energy stored in the nominal operating condition of these filters. In this sense, to quantify the energy stored in these filters, the following energy definitions are adopted.

To evaluate the volume of LC filter, the value of the total energy stored in the inductor (L_b) and capacitor (C_{LC}) can be estimated as, respectively:

$$E_{ind,LC} = \frac{6N}{2} L_b I_{bat}^2, \tag{4.21}$$

$$E_{cap,LC} = \frac{6N}{2} C_{LC} V_c^2. \tag{4.22}$$

It is worth highlighting that the multiplicative factor is defined by the presence of a total of 6N SMs in the three-phase MMC studied in this work.

On the other hand, to evaluate the CL-LC filter, the value of the total energy stored in the inductors (L_f and L_r) and capacitors (C_{SM} and C_r) can be estimated as, respectively:

$$E_{ind,CL-LC} = \frac{6N}{2} L_f I_{bat}^2 + \frac{6N}{2} L_r I_{L_r}^2, \tag{4.23}$$

$$E_{cap,CL-LC} = \frac{6N}{2} C_{SM} V_{c_{sm}}^2 + \frac{6N}{2} C_r V_{c_r}^2. \tag{4.24}$$

Tab. 20 presents an analysis of inductive and capacitive energy stored when using the LC and CL-LC filter in the MMC-based BESS. It is possible to verify that the LC filter has an inductive energy 53.3 % higher than the CL-LC filter. In turn, the LC filter has a capacitive energy lower than 42.5 % of the energy of the CL-LC filter losses and cost. The final aim would be to choose the best filter, among some initially defined topology possibilities.

Table 20 – Analysis of inductive and capacitive energy in LC and CL-LC filter for the full MMC-based BESS.

Filter type	Inductive energy [kJ]	Capacitive energy [kJ]
LC Filter	1.740	1.118
CL-LC Filter	1.135	1.946

These results show that the proposed filters can perform better depending on the type of volume limitation that is aimed at. Furthermore, a multi-objective optimization strategy can be combined with the proposed design methodology to improve aspects of the filter in terms of volume, and even other variables such as ohmic and magnetic losses.

As discussed, the attenuation results in the LC and CL-LC filters present similarities in the ability to mitigate the harmonic components in the battery current. The positive effect of reducing inductances in the CL-LC filter can be questioned due to the increase in capacitances when compared to the LC filter. In this sense, mainly due to the high attenuation similarity for the 60 Hz, 120 Hz, and 240 Hz components, only the LC filter will be evaluated in the experimental results. Furthermore, it is worth highlighting that the purpose of this work involves the comparison of passive and active current mitigation strategies from batteries present in the SM of an MMC-based BESS.

4.6.1 LC Filter Experimental Results - Proof of Concept

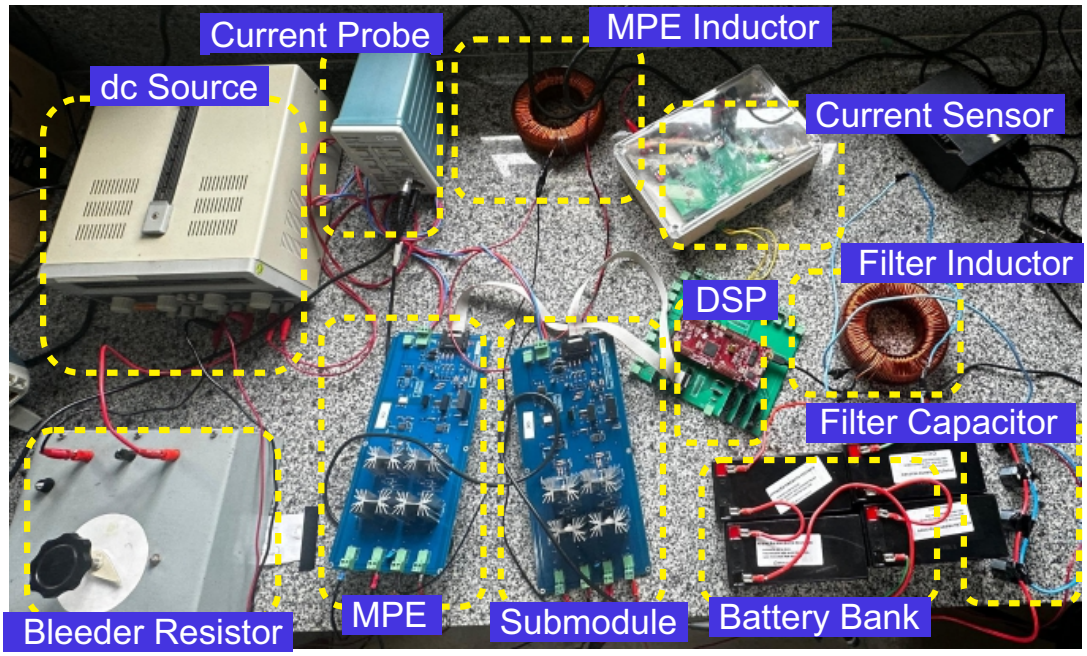
The experimental results consider a reduced scale prototype with the main parameters presented in Table 9. The arm current and battery current validations are based on the frequency spectrum current and the maximum arm current ripple. In this analysis, the LC filter is evaluated, according to the parameters presented in Table 21.

Table 21 – Main Parameters of the LC Filter in Small-scale Prototype.

Parameters	Symbol	Value
Capacitance of LC filter [mF]	C_{LC}	8.8
Series Inductance of LC filter [mH]	L_b	5.53
Damp Resistance of LC filter [Ω]	R_{damp}	1.5

Fig. 53 presents the experimental setup to validate the LC filter attenuation. As shown, it is possible to check the connection between MPE, SM, dc source, DSP, MPE inductance, battery bank, bleeder resistor, and LC filter (with connection between the filter capacitor and filter inductor, according to Fig. 42(a)).

Figure 53 – Experimental setup for LC filter implementation.



Source: own representation.

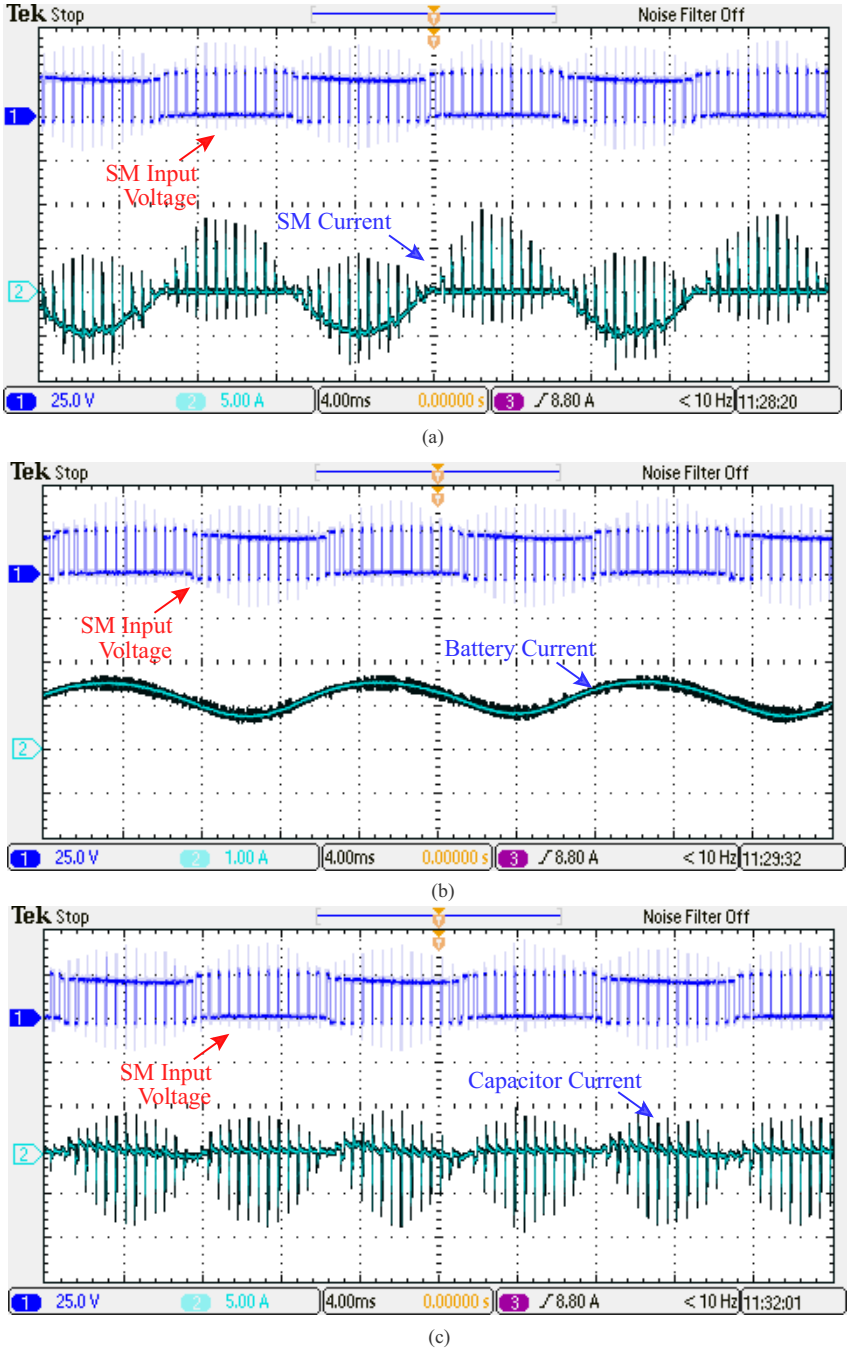
The LC filter implementation in the experimental setup considers a combination of 4 x 2.2 mF capacitors (connected in parallel) and an inductance of 5.53 mH, according to the components available in the laboratory and commercially (combined to produce an attenuation close to -15dB, following the initial proposal presented). Also highlighted are the current probe and current sensor for observing and implementing the arm current control. Again, the battery arrangement consists of two 12V/7 Ah batteries in series, with two string connections in parallel, totaling 4 batteries and a 24 V/14 Ah battery storage system.

The waveforms of the SM input voltage and typical currents in the LC filter and batteries are evaluated in Fig. 54. The waveforms of the SM current and the SM input voltage are presented in Fig. 54 (a), emphasizing the dc component and first harmonic. This measurement is carried out in the input battery terminals.

In turn, the battery current is evaluated in Fig. 54 (b), where it is possible to verify a significant dc component with a low amplitude sinusoidal component. A large difference in this current can be seen concerning the battery current analyzed in Fig. 34 (a) without the presence of a passive filter in SM.

Fig. 54 (c) shows the current that circulates in the capacitor of the LC filter,

Figure 54 – Experimental waveforms of SM input voltage [25 V/div] and currents with time division of 4 ms/div and [5 A/div] for (a) SM current (b) battery current (c) capacitor current.



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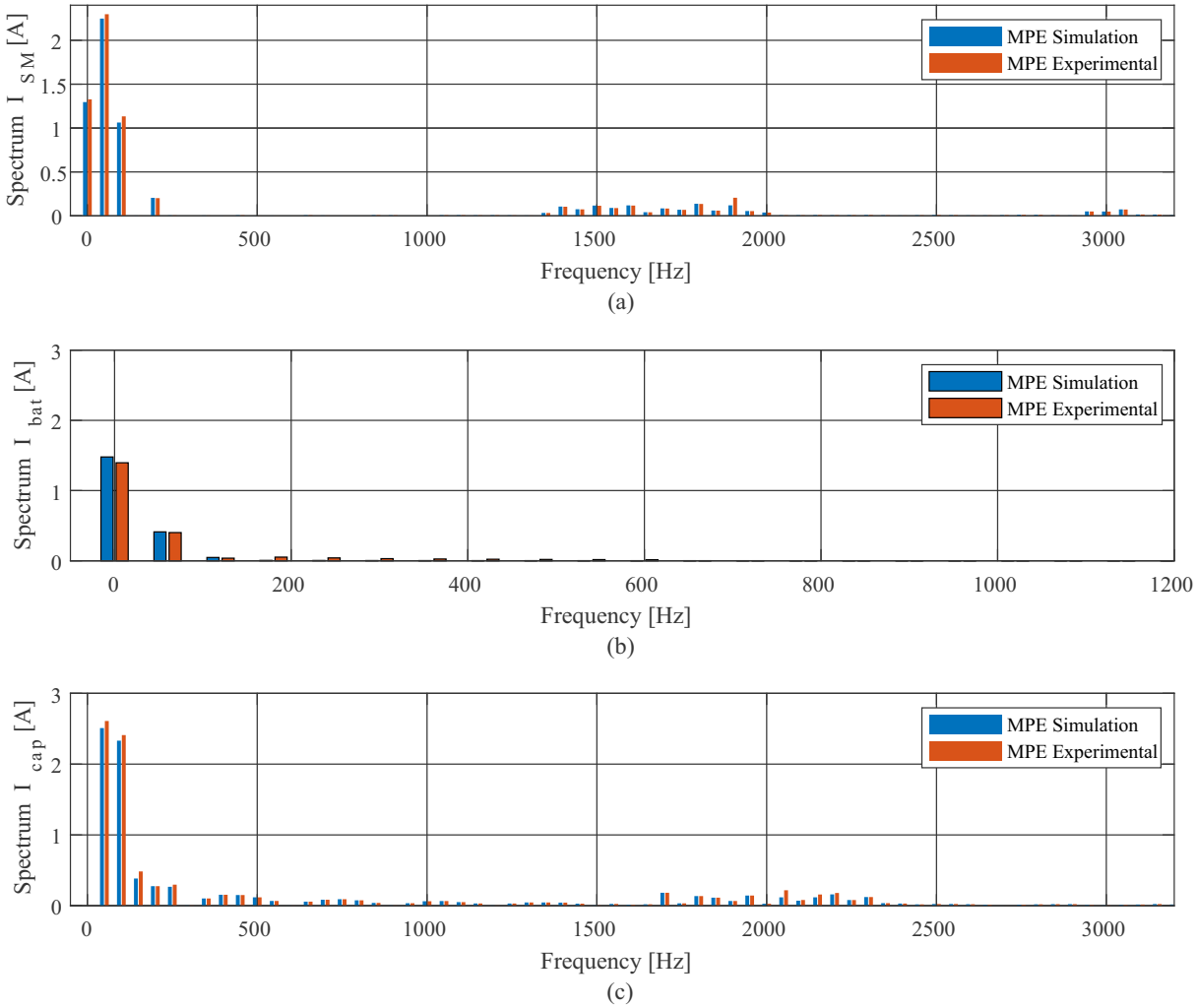
highlighting the high-frequency portion absorbed by the capacitor branch, explaining the attenuation observed in the battery current, in Fig. 54 (b).

The frequency spectrum of the currents presented in Fig. 54 are analyzed in Fig. 55. A comparison of the experimental result is made with the result simulated considering the same parameters of the test bench.

Figure 55 – Currents analysis with LC filter: (a) spectrum of SM current (b) spectrum of battery current (c) spectrum of capacitor (LC filter) current.



Source: own representation.

Fig. 55 (a) presents the frequency spectrum of the SM input current, emphasizing the previously discussed components of dc, first, second, and fourth harmonic components. There is a high similarity between the simulated and experimental results, with current amplitude errors less than 5%. In Fig. 55 (b) the current spectrum in the battery is presented, already emphasizing the filtering procedure, maintaining the dc portion of the SM input current, and significantly attenuating the first, second, and fourth harmonic portions. The maximum amplitude error of current is approximately to 6% in the dc component. The portion of the first harmonic, which used to be twice the dc component, now has a value of around a quarter of the dc component. Finally, the spectrum of the LC filter capacitor current is presented in Fig. 55 (c), where the presence of the most significant low-order components is verified, except for the dc component.

Finally, the attenuation results for the 60Hz, 120Hz, and 240 Hz components in the battery current of the LC filter in simulation and experimental setup are summarized in Tab.

22. Verifying a high similarity in the attenuation results in the analyzed frequency range is possible. It can be seen that although the combination of inductance and capacitance values in the simulated and experimental results were little different, both were designed to obtain the same typical attenuation in the 60 Hz component (next to -15 dB) and consequently in the other current harmonic components.

Table 22 – Harmonic Current Attenuation Analysis.

Battery Harmonic Current Component	LC filter: Simulation	LC filter: Experimental
60 Hz	82.5 % (-15.2 dB)	82.6 % (-15.2 dB)
120 Hz	95 % (-26 dB)	95.2 % (-26.4 dB)
240 Hz	98.9 % (-39.1 dB)	98.4 % (-35.9 dB)

4.7 Chapter Summary

This chapter presented the harmonic suppression methods for attenuating the harmonic components of the current flowing through the battery integrated into an SM of an MMC-based BESS. The methodology for designing two passive filter topologies, considering a LC filter and a CL-LC filter showed effectiveness in terms of the proposed attenuation for the battery current ripple. The simulation results through the MPE, proposed in Chapter 3, validated the suppression of critical harmonics in the SM battery current, eliminating the desired components with the expected values in dB. The methodology for surveying the capacitance and inductance curves, based on the definition of attenuation in dB, proved to be adequate for a comparison between passive filter topologies.

It is worth highlighting that the experimental results were able to validate the methodology for attenuating harmonic components in the battery current. The LC filters implemented in the simulation and testing scheme were able to obtain the attenuation level in the desired component of 60 Hz in the battery current, around -15 dB, demonstrating the flexibility of the methodology to implement the passive filter according to the availability of components present. Furthermore, the current spectrum of the SM, filter capacitor, and battery showed high similarity with the simulated results and values obtained in the empirical equations, validating the proposed methodology. The same idea could be applied to the CL-LC filter experimentally, but the focus of the work is the comparison of the passive strategy (passive filter) with the active strategy (dc/dc converter), as presented in the next Chapter.

5 Integrating Battery into SM Using Active Filters

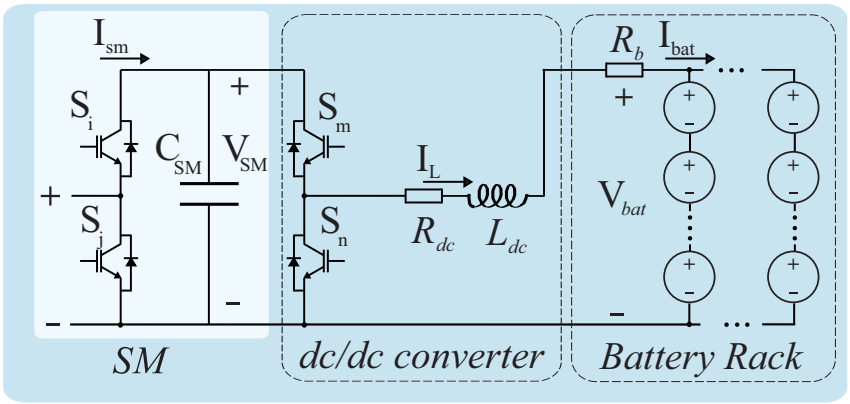
This chapter introduces the harmonic active suppression method for attenuating the harmonic components of the current flowing through the battery integrated into MMC submodules. The methodology is focused on designing an active filter based on a dc/dc bidirectional buck-boost converter topology. In addition, the active filter control strategy is discussed.

Discussions about the minimum capacitance and inductance values for the dc/dc converter are addressed. Besides, the design points of passive components are determined. Finally, the simulation results for the dc/dc converter are presented, proving the expected attenuation. Experimental results are presented validating the expected attenuation according to the empirical equations and simulation results.

5.1 Active Filter Design

Fig. 56 shows the SM configuration with the dc/dc converter proposed for the active filter method. In this work, the dc/dc converter employed is the buck-boost type, considering the batteries as the input terminals and the dc-link of SM as the output terminals. As a consequence, the total voltage of the battery rack varies according to the dc/dc converter voltage margin (δ_g).

Figure 56 – Schematic of SM with dc/dc converter for active filter approach in MMC-based BESS.

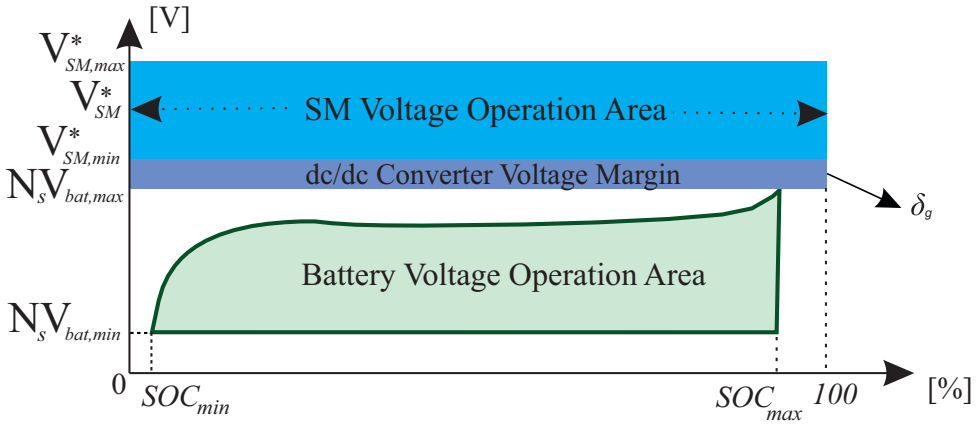


Source: own representation.

Fig. 57 presents the battery bank voltage, showing the range between the minimum and maximum values, which are defined by the voltage at the maximum and minimum

SOC of the battery. In addition, the SM voltage also presents a range of operations, which is defined by the maximum and minimum voltage. It is highlighted that the battery bank voltage is defined by the number of batteries in series per string, totaling a $N_s V_{bat}$ voltage.

Figure 57 – Operating intervals for the battery and SM reference voltage of the dc/dc converter.



Source: Adapted from Pinto (2022).

The maximum value of SM voltage ($V^*_{SM,max}$) is defined based on the safe voltage supported by the semiconductor device. Generally, the maximum value used is around 60 - 70 % of the blocking voltage provided by the semiconductor device manufacturer (Gherard et al., 2020). On the other hand, the minimum value of SM voltage ($V^*_{SM,min}$) is chosen based on the minimum voltage necessary to inject reactive power into the SM (Pinto, 2022). In this sense, the dc/dc converter voltage margin between the maximum battery voltage and minimum SM voltage of the dc/dc converter deserves special attention, since this margin guarantees a better performance of the dc/dc stage during the battery charging and discharging processes.

Indeed, the SM reference voltage V_{SM} has an important role in the sizing of MMC-based BESS, according to the discussion of Pinto (2022). Thus, some considerations are highlighted:

- For the adopted dc/dc converter topology, the SM reference voltage must be higher than the maximum battery voltage and lower than the maximum voltage of the dc power supply (recommended by the manufacturer);
- The minimum and maximum battery voltage range adopted in the MMC-based BESS operation depend on the minimum and maximum allowed SOC of the battery;
- SM power losses increase according to the SM reference voltage. This fact is justified by the increase in the switching losses with the blocking voltage and the increase of the dc/dc converter duty-cycle, which increases the conduction losses;

- For different operational SOC, the dc/dc converter duty-cycle is different. Thus, the MMC-based BESS global efficiency is a function of the converter mission profile;
- The value of SM reference voltage affects the MMC-based BESS total cost.

Regarding the passive components of the active filtering method, it is worth mentioning the sizing of the SM capacitor and the inductor of the dc/dc converter. The SM capacitance (C_{SM}) can be defined based on equation (2.48). According to Harnefors et al. (2013) and Cupertino et al. (2018b), 40 kJ/MVA guarantees a maximum capacitor voltage ripple equal to 10 % (typical for MMC applications).

The SM capacitance design is performed considering that the system can operate only with reactive power, as in the Static Synchronous Compensators (STATCOM) applications. According to Soong and Lehn (2016), shorter battery strings are preferable in MMC-based BESS to increase the reliability of batteries. In this work, it is considered that the MMC-based BESS up to 33 % of the battery banks can be turned off without affecting the energy exchange of the MMC with the grid, according to the discussion of Pinto (2022).

The minimum value of dc/dc converter inductance (L_{dc}) to operate in continuous conduction mode can be expressed by (Pinto, 2022):

$$L_{dc} = \frac{V_{bat,max}(V^*_{sm} - V_{bat,max})}{V^*_{SM} f_{sw,dc} \Delta I_{bat}}. \tag{5.1}$$

where $V_{bat,max}$ is the maximum value of the battery string voltage, $f_{sw,dc}$ is the dc/dc converter switching frequency and ΔI_{bat} is the maximum battery current ripple.

5.1.1 dc/dc Converter Control

The control strategy adopted for the dc/dc converter comprises an internal battery current loop and an external SM reference voltage loop. Fig. 58 shows the block diagram of the control of the dc/dc converter.

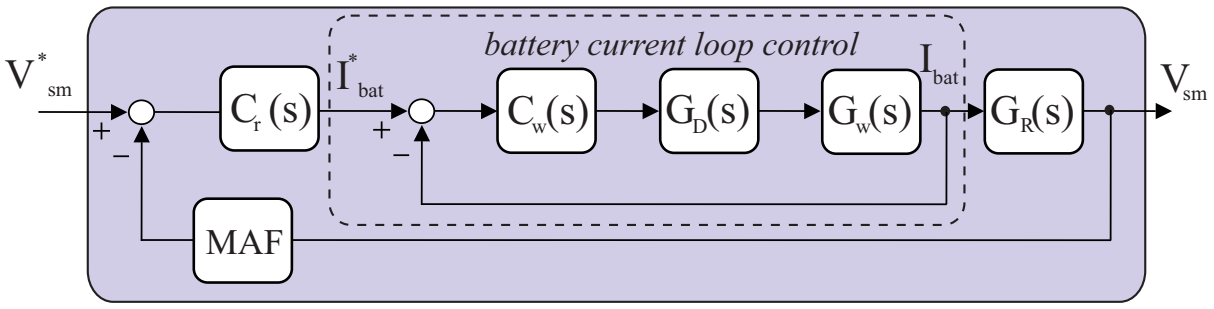
The internal battery current control is performed with a PIR controller ($C_w(s)$) defined as:

$$C_w(s) = k_{p,w} + \frac{k_{i,w}}{s} + \frac{k_{r,dc}s}{s^2 + \omega_g^2}. \tag{5.2}$$

where $k_{p,w}$ is the proportional gain, $k_{i,w}$ is the integral gain and $k_{r,dc}$ is the resonant gain. The plant transfer function of the dc/dc converter ($G_w(s)$) is given by:

$$G_w(s) = \frac{I_L(s)}{v_{SM}(s)} = \frac{1}{L_{dc}s + R_{dc}}. \tag{5.3}$$

Figure 58 – Block diagram of the dc/dc converter control.



Source: own representation.

where R_{dc} is the intrinsic resistance of the dc/dc converter inductance (L_{dc}). The plant transfer function due to the delay in the dc/dc converter ($G_D(s)$) is given by:

$$G_D(s) = \frac{1}{1.5T_{sw,dc}s + 1} \tag{5.4}$$

In this sense, the open-loop transfer function ($G_{w,OL}(s)$) for controlling the battery current of the dc/dc converter can be expressed by:

$$G_{w,OL}(s) = \left(k_{p,w} + \frac{k_{i,w}}{s} + \frac{k_{r,dc}s}{s^2 + \omega_g^2}\right)\left(\frac{1}{1.5T_{sw,dc}s + 1}\right)\left(\frac{1}{L_{dc} + R_{dc}}\right). \tag{5.5}$$

where $T_{sw,dc}$ is the dc/dc converter switching period. The proportional and integral gains are adjusted for the closed-loop poles allocated to the left semi-plane (Pinto, 2022). In this way, the gains of the PI are adjusted as follows:

$$\begin{cases} k_{p,w} = 2\pi f_i L_{dc}, \\ k_{i,w} = 2\pi f_i R_{dc}. \end{cases} \tag{5.6}$$

where f_i is the frequency relative to the closed-loop pole and is defined as a ratio of the dc/dc converter switching frequency ($f_{sw,dc}$). For this work, $f_i = \frac{1}{20} f_{sw,dc}$ is adopted (Pinto, 2022). The control tuning of the current loop follows the methodology discussed in (Sharifabadi et al., 2016). The objective is to maximize the current control bandwidth. Based on this methodology, the following tuning formula is obtained for the resonant gain ($k_{R,dc}$):

$$k_{r,dc} = 2\alpha_h k_{p,w}, \tag{5.7}$$

where α_h is computed as:

$$\alpha_h = \frac{1}{20T_{sw,dc}}. \tag{5.8}$$

In SM reference voltage control, the bandwidth must be lower than the battery current loop. Indeed, the transfer function of the PI controller ($C_r(s)$) is defined as:

$$C_r(s) = k_{p,r} + \frac{k_{i,r}}{s}. \tag{5.9}$$

where $k_{p,r}$ is the proportional gain and $k_{i,r}$ is the integral gain. The plant transfer function of the dc/dc converter capacitor ($G_R(s)$) is given by:

$$G_R(s) = \frac{V_{sm}(s)}{I_{SM}(s)} = \frac{1}{C_{SM}s}. \tag{5.10}$$

Furthermore, a filtering technique is employed to attenuate the ripples in the capacitor voltages. A Moving Average Filter (MAF) with a 1/60 window is used. However, as the voltage control poles are allocated below the cutoff frequency of the MAF, its dynamics can be disregarded for control tuning.

In this sense, the open-loop transfer function for the SM reference voltage control ($G_{r,OL}(s)$) of the dc/dc converter can be expressed by:

$$G_{r,OL}(s) = \left(k_{p,r} + \frac{k_{i,r}}{s}\right)\left(\frac{1}{C_{SM}s}\right)\left(\frac{V_{bat}N_s}{V_{sm}}\right). \tag{5.11}$$

The tuning of the controllers can be done by the following equations (Pinto, 2022):

$$\begin{cases} k_{p,r} = 2\pi\dfrac{(f_{c1,d} + f_{c2,d})}{K_k}, \\ k_{i,r} = 4\pi^2\dfrac{f_{c1,d}f_{c2,d}}{K_k}. \end{cases} \tag{5.12}$$

where the gain K_k is given by:

$$K_k = \frac{V_{bat}N_s}{V_{sm}}. \tag{5.13}$$

The $f_{c1,d}$ and $f_{c2,d}$ are the closed-loop poles, expressed by:

$$\begin{cases} f_{c1,d} = 0.12f_i, \\ f_{c2,d} = 0.12f_{c1,d}. \end{cases} \tag{5.14}$$

These poles are allocated at least 1 decade below the passband of the current control.

It is worth highlighting that the gains for all proposed controllers were calculated disregarding the sensor gains. It is important to consider these gains in the MMC-based BESS practical development and simulations.

5.1.2 Controllers - Frequency Analysis

To summarize the frequency analysis results of the proposed controllers, Tab. 23 presents the frequencies chosen for each control in the dc/dc converter.

Table 23 – Frequency bandwidth for the dc/dc converter control.

Frequencies	Value	Unit
f_i	50	Hz
$f_{c1,d}$	6	Hz
$f_{c1,d}$	0.72	Hz

The gains of the controllers used in the full MMC-based BESS simulation for the dc/dc converter are shown in Tab. 24.

Table 24 – dc/dc Converter Controllers Parameters in full MMC-based BESS Simulation.

Gains	Value	Units
Proportional Gain of Current Control ($k_{p,w}$)	0.1293	Ω
Integral Gain of Current Control ($k_{i,w}$)	0.9356	Ω/s
Resonant Gain of Current Control ($k_{r,dc}$)	172.8	Ω/s
Proportional Gain of Voltage Control ($k_{p,r}$)	0.2871	S
Integral Gain of Voltage Control ($k_{i,r}$)	2.8993	S/s

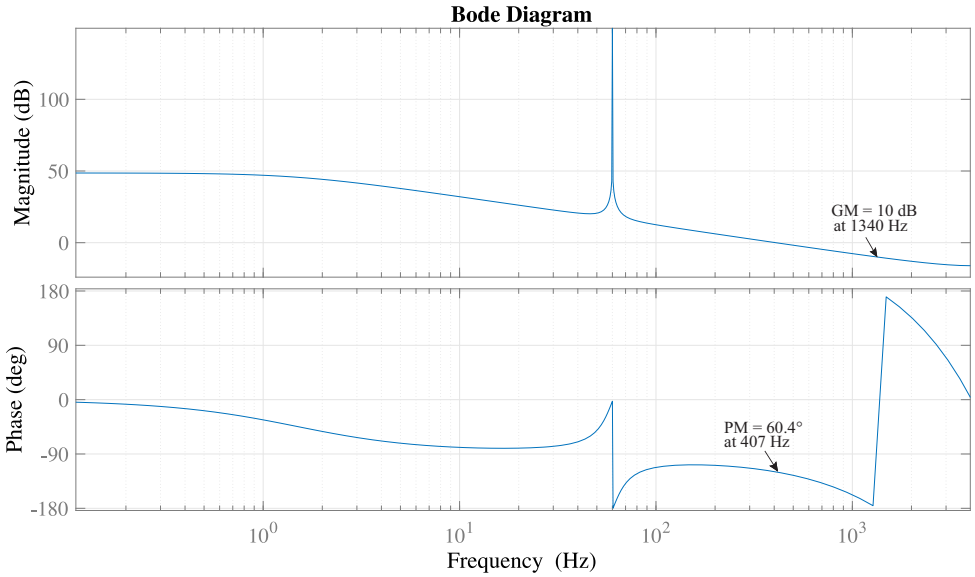
The control strategy implemented in the dc/dc converter is performed with an internal current loop and an external voltage loop. The switching frequency of the dc/dc converter is adopted equal to 1 kHz.

Fig. 59 shows the Bode plot for the internal current loop of the dc/dc converter, emphasizing the crossover frequency of the bandwidth approximately equal to 407 Hz (2557.26 rad/s).

In terms of stability analysis of the controllers, a phase margin equal to 60.4° is verified at a frequency of approximately 407 Hz, while the gain margin is equal to 10 dB at a frequency of 1340 Hz. Fig. 60 shows the step response for the battery current control of the dc/dc converter, due to the PI controller response. Note that the system needs 0.04 s approximately to reach the current reference.

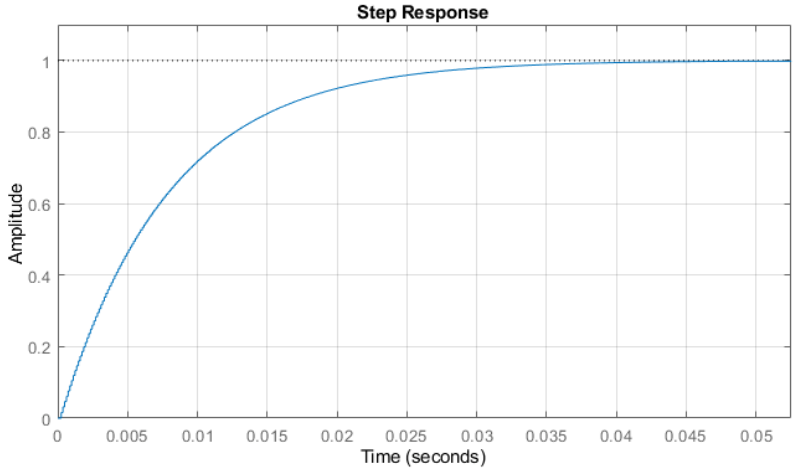
The external voltage loop of the dc/dc converter is designed for 6 Hz. This control loop must be slower dynamic than the battery current loop. Furthermore, to improve steady-state response, MAF is adopted. Fig. 61 presents the Bode plot for the dc-link voltage loop of the dc/dc converter, emphasizing the crossover frequency equal to 5.95 Hz (37.4 rad/s).

Figure 59 – Current controller open-loop Bode diagram.



Source: own representation.

Figure 60 – Battery current controller step response in dc/dc converter.



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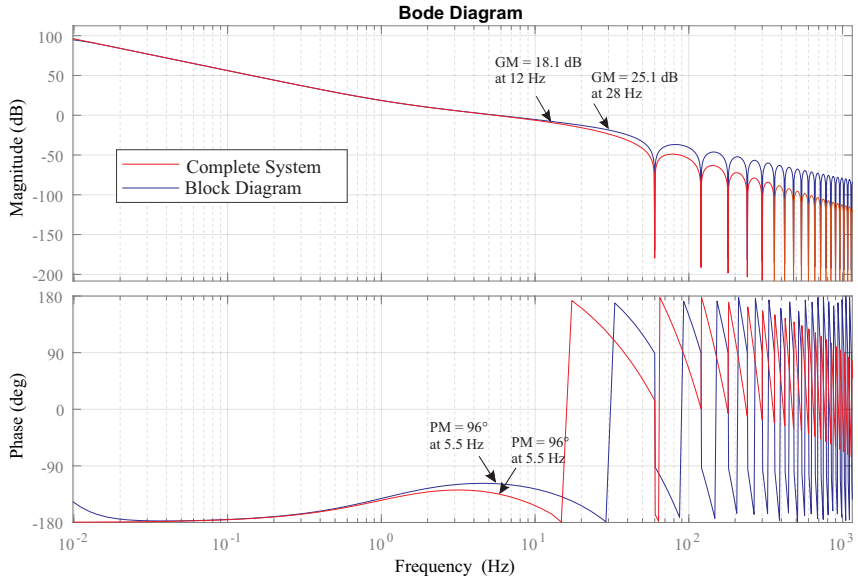
The Bode plot compares the frequency response of the system considering the simplified block diagram and complete system for the internal current loop. Note that for frequencies below 12 Hz, the systems have the same behavior. In terms of stability analysis of the controllers, a phase margin equal to 96° is verified at a frequency of approximately 5.5 Hz, while the gain margin is equal to 25.1 dB at the frequency of 28 Hz, for the complete system bode diagram. On the other hand, a phase margin equal to 96° is verified at a frequency of approximately 5.5 Hz, while the gain margin is equal to 18.1 dB at the frequency of 12 Hz, for the block diagram.

Fig. 62 shows the step response for the current control of the dc/dc converter. Note

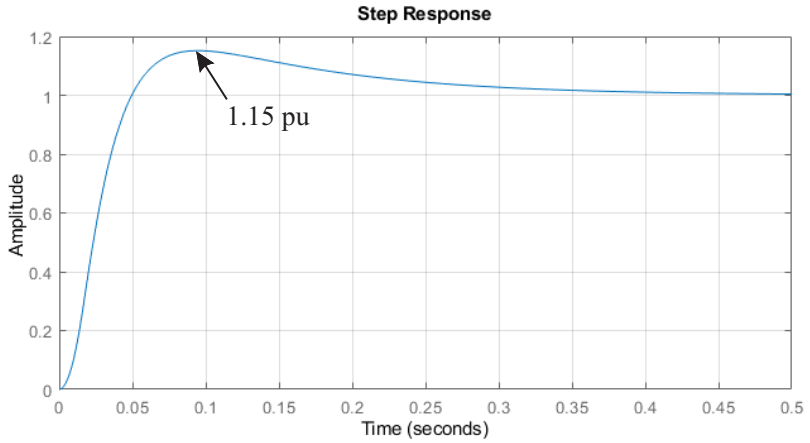
Figure 61 – Voltage controller open-loop Bode diagram.



Source: own representation.

that the system needs 0.4 s approximately to reach the dc voltage reference. Furthermore, an overshoot of 15 % of the steady-state value of the voltage is observed.

Figure 62 – Voltage controller step response in dc/dc converter.



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5.2 Experimental and Simulation Results - Proof of Concept

5.2.1 Simulation Results - Active Filter Results

The performance of the MPE is compared with the full MMC system simulation of 10.9 MVA/13.8 kV and 12.6 MWh of BESS, equal to the MMC-based BESS implemented in Chapter 3 (the main parameters for the MMC-based BESS simulation are shown in

Table 4). The simulation results are developed on the PLECS platform. In this simulation analysis, the dc/dc converter is evaluated, according to the parameters presented in Table 25.

Table 25 – Main System Parameters for the Evaluation of dc/dc Converter in MMC-based BESS and MPE.

Parameters	Symbol	Value
Emulator dc-link Voltage [kV]	$V_{dc,em}$	3.5
SM Capacitance [mF]	C_{SM}	15
SM Reference Voltage [kV]	V_{SM}^{*}	1.8
Switching frequency [kHz]	$f_{sw,dc}$	1
Battery Nominal Voltage [kV]	V_{bat}	1.5
Maximum dc/dc Inductor Ripple [%]	ΔI_{dc}	10
Peak ac Arm Current [A]	$I_{arm,ac}$	309
Minimum Inductance of dc/dc Converter [mH]	L_{dc}	8.09
Resistance of dc Inductance [mΩ]	R_{dc}	204

For experimental and simulated results, the MPE setup results are obtained considering the same SM nominal voltage, grid frequency, battery arrangement, and nominal arm current. The arm current and battery current validations are based on the frequency spectrum current and the maximum arm current ripple.

Fig. 63 (a) shows the arm current obtained from the full MMC-based BESS and MPE simulation. In both simulations, the arm current reference is set to an amplitude of approximately 309 A.

Fig. 63 (b) shows that the maximum value of the MPE inductor current ripple is approximately 27.67 A, which corresponds to 8.96 % (which is following the maximum limit of 10 % set for the MPE design) of the arm current reference peak, considering a maximum arm current of approximately 309 A.

Based on the spectrum of the arm current, shown in Fig. 63 (c), it is observed that the harmonic contents of both currents are similar, evidencing an ac signal (with emphasis on the fundamental component).

Fig. 64 (a) shows the current measurements in the batteries of the SMs in the MMC upper arm, as well as the battery current measured in the MPE. Once the full MMC-BESS simulation implements all the SMs of the MMC, the 15 signals of battery current in the upper arm of phase A are presented. It is also possible to check that the batteries are charging with slightly different current levels. This can be explained by the NLC modulation process and the performance of SOC control, as previously mentioned.

Fig. 64 (b) shows the average current spectrum of the 15 battery current signals obtained in the simulation of MMC. The harmonic contents of the battery current for both models are similar, especially for the most significant components dc, 1^{st}, 2^{nd}, and 4^{th} order. It is possible to verify that the dc component in Fig. 27(b) is practically preserved,

Figure 63 – (a) Arm current with dc/dc converter in the SM (b) arm current ripple (c) spectrum of arm current.

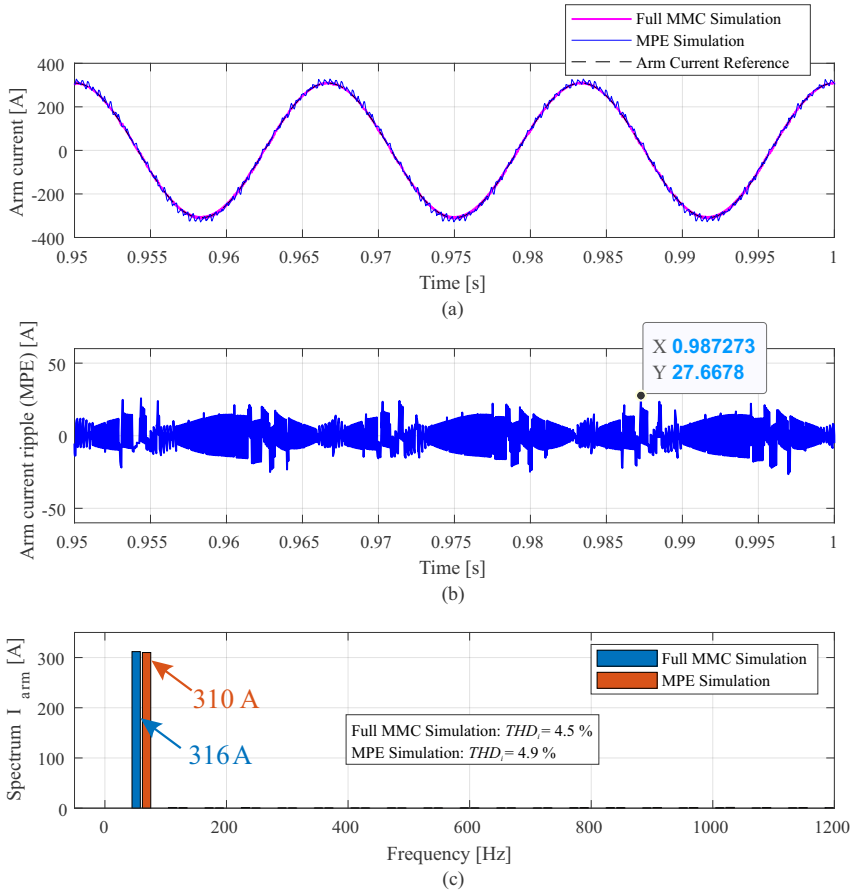

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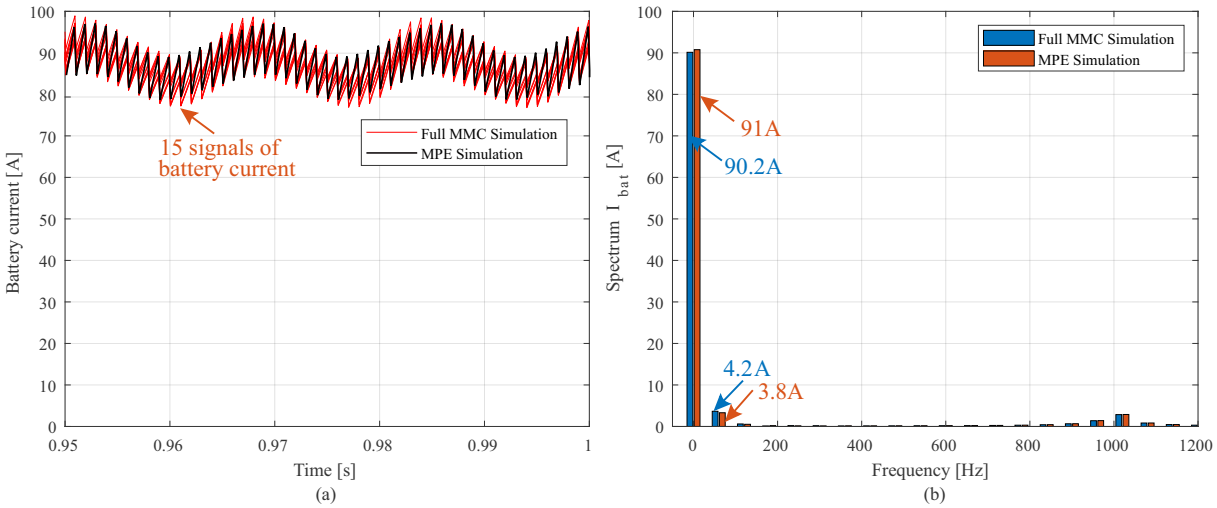
Figure 64 – (a) Battery current in SM with dc/dc converter (b) spectrum of battery current.



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with a substantial reduction in the first, second, and fourth harmonic components.

5.2.2 Experimental Results (Test Bench) - dc/dc Converter Results

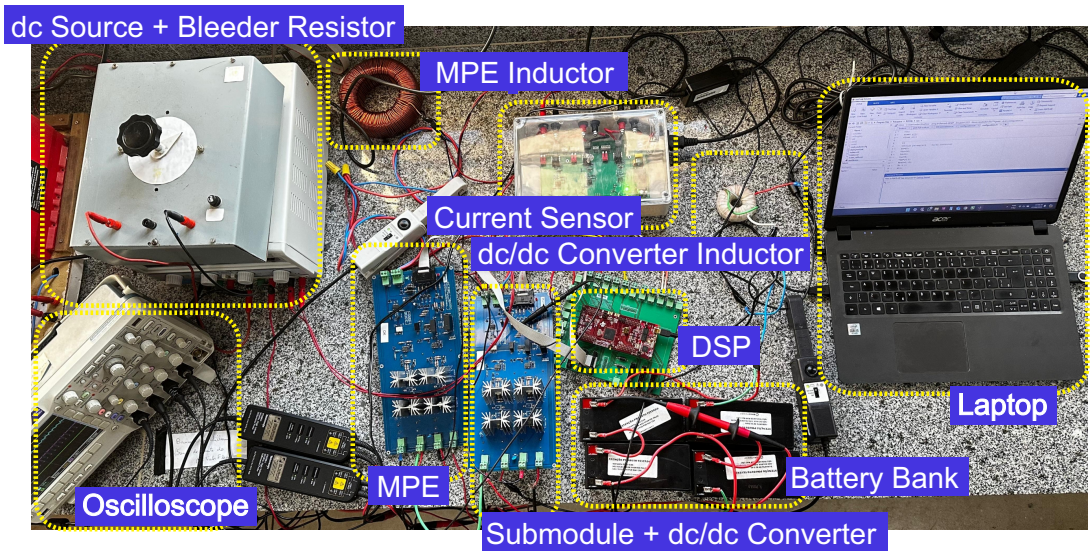
Tab. 26 presents the main system parameters adopted to evaluate the proposed design of the dc/dc converter in the test bench. As the idea is to validate this approach in the laboratory, the design values for low voltage, current, and power were adopted. Thus, the MPE parameters are set on a peak of arm current of 5 A, battery bank of 24 V, and limited to a 150 W dc bench source (emulator dc-link voltage).

Table 26 – Main System Parameters for the Evaluation of dc/dc Converter.

Parameters	Symbol	Value
Emulator dc-link Voltage [V]	$V_{dc,em}$	35
SM Capacitance [mF]	C	2.72
SM Reference Voltage [V]	V^*_{SM}	30
Battery Nominal Voltage [V]	V_{bat}	24
Maximum dc/dc Inductor Ripple [%]	ΔI_{dc}	10
Peak ac Arm Current [A]	$I_{arm,ac}$	5
Minimum Inductance of dc/dc Converter [mH]	L_{dc}	9.6
Resistance of dc Inductance [mΩ]	R_{dc}	104

Fig. 65 presents the experimental setup to validate the dc/dc converter implementation. As shown, it is possible to check the connection between MPE (full-bridge converter), SM, dc source, DSP, MPE inductance, battery bank, bleeder resistor, and dc/dc converter inductance (with the connection between the SM capacitor and dc/dc converter inductor, according to Fig. 56).

Figure 65 – Experimental setup for dc/dc converter implementation.



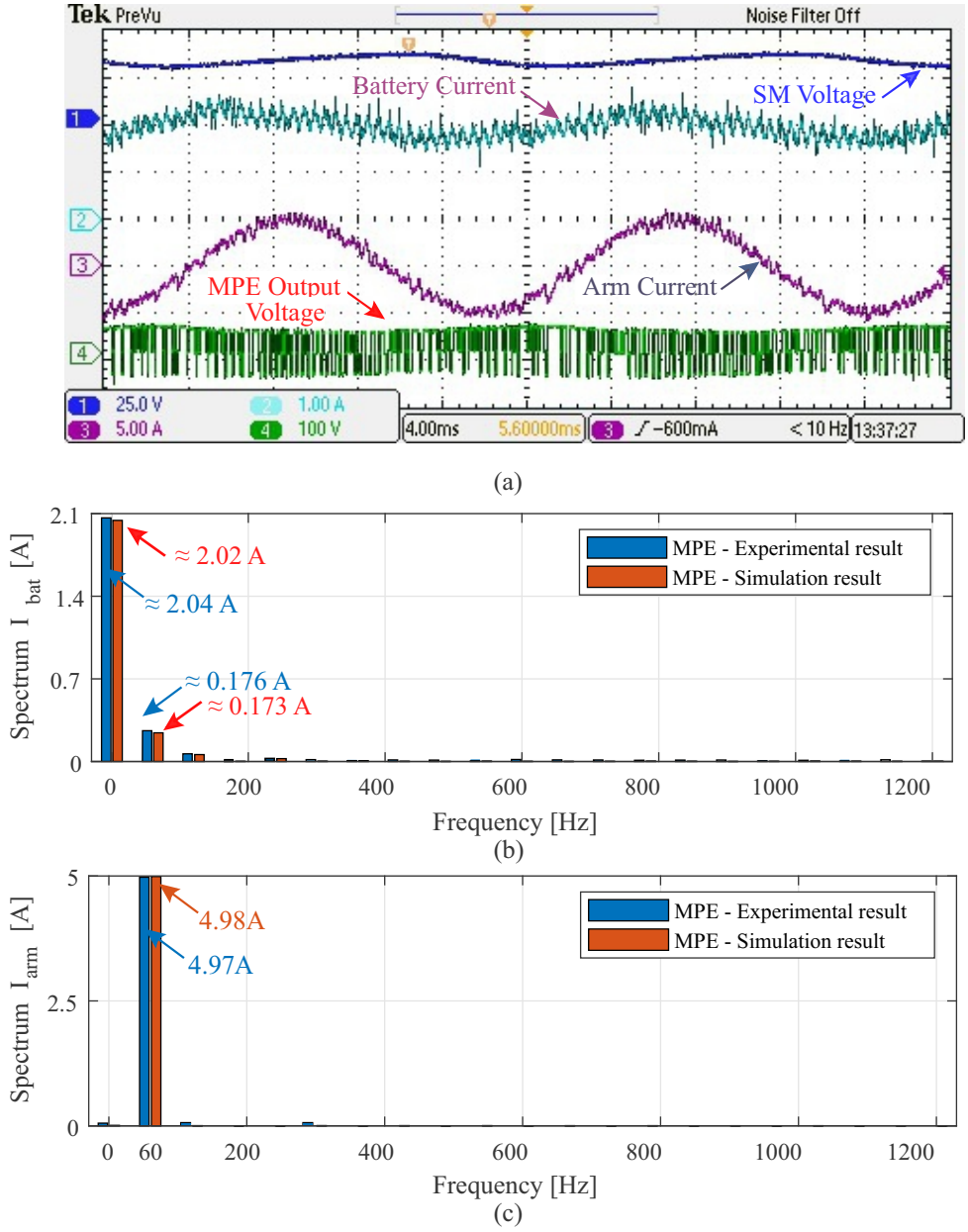
Source: own representation.

The dc/dc converter implementation in the experimental setup considers a dc-link with 4 x 2.2 mF capacitors (connected in parallel) and an inductance of 14.4 mH, according to the components available in the laboratory and commercially. Also highlighted are

the current probe and current sensor for observing and implementing the arm current control. Again, the battery arrangement consists of two 12V/7 Ah batteries in series, with two string connections in parallel, totaling 4 batteries and a 24 V/14 Ah battery storage system.

The waveforms of the SM voltage, MPE output voltage, battery current, and arm current in the MPE and dc/dc converter are evaluated in Fig. 66 (a).

Figure 66 – (a) Experimental waveforms of SM voltage and MPE output voltage [25 V/div and 100 V/div] and currents (measured in the arm and batteries) [5 A/div and 1 A/div] with time division of 4 ms/div (b) spectrum of battery current (c) spectrum of arm current.



Source: own representation.

It is possible to verify that the SM voltage is composed of a dc signal of around

25 V with a small oscillation of 60 Hz, due to the charging and discharging effect of the capacitances present in the dc-link. The battery current is also formed by a dc component, whose amplitude is an average value of around 1.4 A, in addition to the presence of high-frequency and reduced 60 Hz, 120 Hz, and 240 Hz harmonic components.

The MPE arm current has a sinusoidal characteristic with an amplitude of 5 A, showing a high-frequency ripple, already expected according to the discussions in Chapter 3. Furthermore, the output voltage of the full-bridge converter is evident on the last channel of the oscilloscope, with voltage waveform modulated between the maximum and minimum values of the MPE dc supply voltage.

In turn, the battery current frequency spectrum is evaluated in Fig. 66 (b), where verifying a significant dc component with a low amplitude sinusoidal component of first and second order is possible. A comparison of the experimental result is made with the result simulated in the current spectrum presented, in which both results show a similarity.

In Fig. 66 (c) the arm current spectrum is shown, highlighting the first harmonic amplitude with a maximum value close to 5 A approximately. The other harmonic components are negligible for the analyzed spectrum.

The attenuation results for the 60Hz, 120Hz, and 240 Hz components in the battery current of the dc/dc converter simulation and experimental setup are summarized in Tab. 27. Verifying a high similarity in the attenuation results in the analyzed frequency range is possible. The largest differences in attenuation occur at frequencies above 500 Hz.

Table 27 – Harmonic Current Attenuation Analysis in dc/dc Converter.

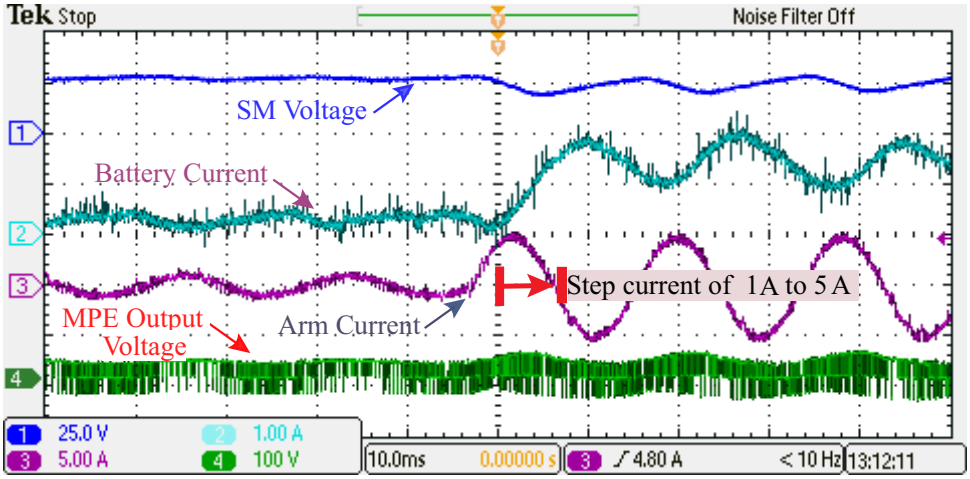
Harmonic Frequency	dc/dc Converter Simulation	dc/dc Converter Experimental
60 Hz	92.96 % (-23.05 dB)	92.94 % (-23.02 dB)
120 Hz	93.84 % (-25.7 dB)	93.55 % (-27.81 dB)
240 Hz	97.66 % (-38.4 dB)	98.73 % (-39.95 dB)

Fig. 67 presents the SM voltage, battery current, arm current, and MPE output voltage, respectively, for a variation of arm current peak of 1 A to 5 A of a 60 Hz sinusoidal reference current.

Again it is possible to verify that the SM voltage is composed of a dc signal of around 25 V with a small oscillation of 60 Hz. The oscillating component increases in the current transition from 1A to 5 A, explained by the greater voltage drop in the MPE inductor (since the portion of active power has been increased) and consequent reflection in the voltage of the dc-link capacitors.

The current in the battery is also formed by a dc component, whose amplitude is an average value of around 0.5 A, with an arm current of 1 A peak, and an average value of 1.4 A at the battery current for an arm current of peak arm equal to 5 A. Furthermore, in addition to the presence of high-frequency and reduced 60 Hz, 120 Hz, and 240 Hz

Figure 67 – Experimental waveforms of SM voltage and MPE output voltage [25 V/div and 100 V/div] and currents (measured in the arm and batteries) [5 A/div and 1 A/div] with time division of 4 ms/div.



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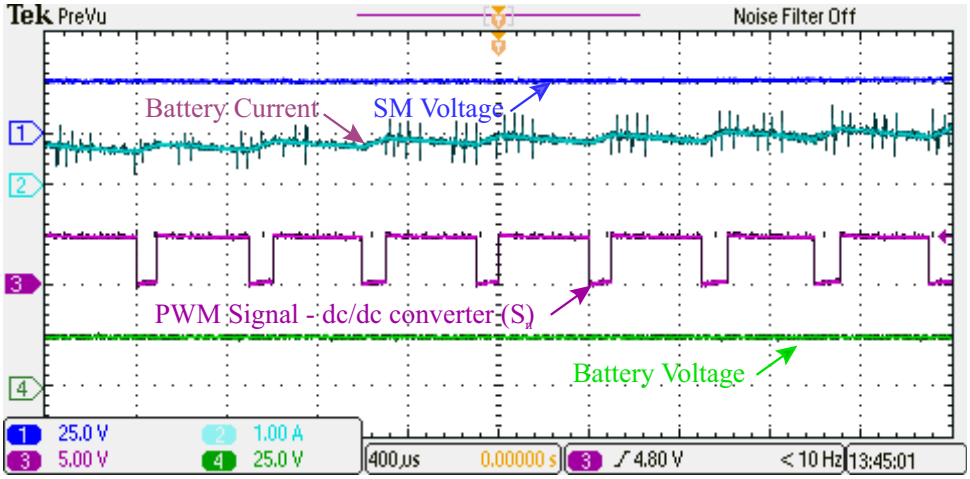
harmonic components. The MPE arm current has a sinusoidal characteristic with an amplitude transition of 1A to 5A, showing a high-frequency ripple.

The output voltage of the full-bridge converter is evident on the last channel of the oscilloscope, with voltage waveform modulated between the maximum and minimum values of the MPE dc supply voltage. At the instant of the arm current step transition, little change is seen in the amplitude of the MPE output voltage, modifying the width of the pulses, with a smaller duration window.

Finally, Fig. 68 presents the SM voltage, battery current, PWM signal of dc/dc converter, and battery voltage, respectively, during the transition of an arm current peak of 1 A to 5 A of a 60 Hz sinusoidal reference current.

On channel 1 of the oscilloscope, the voltage measured on the SM (or dc-link capacitors) is displayed. Little variation or oscillation is observed due to the time window being restricted to 400 μs, whose amplitude value is around 25 V. In channel 2, the current measured at the battery terminals is verified, with a slight increase in current due to the chosen arm current transition instant. Channel 3 presents the PWM signal from the Sn switch of the dc/dc converter, which is fed to the input of the gate driver circuit, as discussed in Appendix A. The signal is modulated between 0 V and 5 V. Finally, in the last channel the battery voltage signal is displayed, which also presents a practically constant value of around 24V, the nominal voltage of the batteries.

Figure 68 – Experimental waveforms of SM voltage and battery voltage [25 V/div and 100 V/div], PWM signal in dc/dc converter [5 V/div] and battery current [5 A/div and 1 A/div] with time division of 0.4 ms/div.



Source: own representation.

5.3 Comparison of LC Filter and Active Filter for Harmonic Mitigation in Battery Current

The attenuation results for the 60Hz, 120Hz, and 240 Hz components in the battery current of the LC filter and dc/dc converter simulations for the full MMC-based BESS are summarized in Tab. 28. It is possible to verify superiority in terms of attenuation in dB for the dc/dc converter concerning all harmonic components analyzed in the battery current. In particular, for the 60 Hz frequency, the attenuation was much more effective.

It is worth highlighting, that the active filter experimental result showed an attenuation of the 60 Hz component also superior to the experimental LC filter, even dealing with some limitations of practical implementation such as the control bandwidth, mainly due to current and voltage measurements, and noise, among others. In this sense, in terms of attenuation aspects, the dc/dc converter presents a slight superiority over the LC filter.

Table 28 – Harmonic Current Attenuation Analysis in MMC-based BESS: LC Filter and Active Filter.

Harmonic Current Component	LC Filter	Active Filter
60 Hz	82.9 % (-15.3 dB)	97.1 % (-30.8 dB)
120 Hz	95.1 % (-26.1 dB)	99.1 % (-40.9 dB)
240 Hz	98.9 % (-39.2 dB)	99.8 % (-54 dB)

Another aspect that can be evaluated between the two proposed mitigation strategies involves evaluating the volume of practical implementation. As previously described, for the LC filter an estimate of this volume can be made around the energy

stored by the passive components. The same analysis can be extended to the inductor present in the dc/dc converter. However, the volume of this converter is still associated with the volume occupied by the heatsinks and semiconductor devices. In this work, the volume metric is partially analyzed in terms of the energy stored in the passive components.

To evaluate the volume of dc/dc converter, the value of the total energy stored in the inductor (L_{dc}) and capacitor (C_{SM}) can be estimated as, respectively:

$$E_{ind,LC} = \frac{6N}{2} L_{dc} I_{bat}^2, \tag{5.15}$$

$$E_{cap,LC} = \frac{6N}{2} C_{SM} V_{SM}^2. \tag{5.16}$$

Tab. 29 presents an analysis of inductive and capacitive energy stored when using the LC filter and dc/dc converter in the full MMC-based BESS. It is possible to verify that the dc/dc converter has an inductive energy 69.4 % higher than the LC filter. Concerning capacitive energy, the comparison cannot be made since the capacitor present in the SM does not form a constituent element of the dc/dc converter.

Table 29 – Analysis of Inductive and Capacitive Energy in LC Filter and Active Filter for the Full MMC-based BESS.

Harmonic Mitigation Method	Inductive energy [kJ]	Capacitive energy [kJ]
LC Filter	1.740	1.118
Active Filter	2.948	not applicable

Based on the comparison results of inductive energy and capacitive energy for the LC filter and active filter, it can be concluded that in terms of inductive energy the active filter has a larger equivalent volume (69.42 % higher). In turn, for the analysis of capacitive energy, the comparison cannot be applied since the dc/dc converter does not present a capacitor in its topology.

The evaluated harmonic component mitigation methods present different dynamic behavior. To characterize this transient regime, for comparison purposes, it is considering the settling time (when the signal accommodates in a band of ± 10 % of the steady state signal value (Femmam, 2017)) and the maximum current overshoot percentage in the battery current for the simulations carried out using the nominal operation of MMC-based BESS defined in Tab. 4.

Tab. 30 presents a performance comparison for the two mitigation strategies using the two aforementioned figures of merit.

The results presented for the settling time and overshoot percentage value demonstrate that the LC filter loses in these figures of merit to the dc/dc converter,

Table 30 – Performance Comparison for the LC Filter and Active Filter during the Transient.

Figure of Merit	LC Filter	Active Filter
Settling Time [s]	0.26	0.09
Overshoot Percentage [%]	45	16

which stands out in both. It is worth highlighting that the significant value of the overshoot value of the LC filter can deal with more complex and expensive protection devices.

Based on the comparisons made between the LC filter and the dc/dc converter, it is worth highlighting the potential of the dc/dc converter, especially in terms of reducing losses in the batteries (due to the increase and flexibility of attenuation) and in dynamic behavior, quite attractive in high power scenarios as an application of an MMC-based BESS. However, optimization strategies can be implemented to quantify other aspects, such as costs and losses in the filters, for more accurate decision-making for a given application.

5.4 Chapter Summary

This chapter presented the harmonic suppression method with dc/dc converter for attenuating the harmonic components of the current flowing through the battery integrated into an SM of an MMC-based BESS. The methodology for designing the proposed dc/dc converter topology showed effectiveness in terms of the proposed attenuation for the battery current ripple. The simulation results through the MPE, proposed in Chapter 3, validated the suppression of critical harmonics in the SM battery current, eliminating the desired harmonic components.

It is worth highlighting that the experimental results were able to validate the methodology for attenuating harmonic components in the battery current. The dc/dc converter implemented in the simulation and testing scheme was able to obtain an attenuation level higher than the desired component of 60 Hz in the battery current, around -23 dB, demonstrating the flexibility of the methodology to attenuate. Furthermore, the current spectrum of the SM and battery showed high similarity with the simulated results and values obtained in the empirical equations, validating the proposed methodology. Finally, it highlights the potential of the dc/dc converter, especially in terms of reducing losses in the batteries and in dynamic behavior, which is attractive in high-power scenarios as an application of an MMC-based BESS, evaluated in this work. Although the dc/dc converter has operational advantages, when considering aspects such as weight, volume, cost, losses, and reliability, the passive solution may still have advantages (requiring multi-objective optimization studies). Interlaced solutions may be interesting.

6 Conclusions and Research Perspectives

MMC has been widely used in medium/high voltage applications and pointed out as a promising solution for BESS. However, these converters have important challenges related to the expensive implementation cost. For medium/high voltage applications, the MMC is based on tens or hundreds of SMs. Thus, the complete implementation of the MMC system can be expensive and complex for operational and reliability testing of batteries. In this sense, the MPE was developed in this work to emulate the typical voltage and current in an SM for low voltage and power, preserving the harmonic content. The previous chapters introduced and evaluated a proposal for an MPE design, modeling, and control methodology, in addition, to the evaluation of active and passive mitigation strategies for the reduction of harmonic components in the battery current. This chapter summarizes the main conclusions and contributions of this Ph.D. thesis and the possible future developments.

6.1 Conclusions

This work proposed a detailed design and implementation of the MPE for an MMC-based BESS. The MPE is validated in simulations and a reduced-scale prototype. In addition, with the designed MPE, passive and active filters are evaluated to eliminate harmonic components present in the battery current when using the MMC-based BESS. Thus, the conclusions obtained for this stage of the work can be divided into two parts:

- MPE design, modeling, and control methodology for MMC-based BESS;
- Harmonic mitigation methods for battery current in MMC-based BESS.

6.1.1 MMC-based BESS: Control Strategy and Design (Chapter 2)

- The MMC-based BESS control strategy discussed emphasizes the need to control the grid, circulating current, and SOC balancing. In particular, for the application of MMC in a BESS, SOC control and the ancillary service reference are crucial for correct battery SOC balancing;
- The evaluation of battery current in SM empirically demonstrated the presence of a significant dc component, and first, second, and fourth harmonics circulating in the

batteries of SMs. In this sense, to charge and discharge the batteries, only the dc component is necessary, taking into account the need to mitigate the other harmonic components;

- The battery temperature rise study demonstrated the direct dependence of this variable on the grid current angle and the modulation index. The study carried out revealed the least critical scenario of increasing battery temperature, in which an increase of 2.86 times greater is revealed in batteries that do not have complete elimination of current harmonics.

6.1.2 MPE Control Strategy and Design for MMC-based BESS (Chapter 3)

- The experimental results indicated that the MPE dynamics with the design implemented are suitable for emulating SM steady-state waveforms of MMC-based BESS during the battery charging and discharging process;
- The arm current transient is smooth and does not significantly affect the converter dynamics;
- The experimental results showed that the estimated maximum arm current ripple shows good agreement with the approximation to design an MPE inductance. All results obtained were within the arm current ripple limit set at 10 %;
- The frequency spectrum of arm and battery current showed that the harmonic content of these signals is similar to the experimental and simulation results, according to the typical current spectrum observed in the MMC-based BESS;
- The experimental results verified that the equal relationship between the MPE and SM frequencies makes reasonable emulation possible in the frequency range of up to 5 kHz in the two converters (for the MPE inductance analyzed in this work);
- Low-frequency operation is also made possible by validation in simulations, increasing the value of the MPE dc power supply and its inductance (the observed limit was around 500 Hz for the MPE and SM frequencies). In addition to the need to increase these characteristics, there were losses in the quality of reproduction of the harmonic content of the arm current and batteries and THD_i value.

6.1.3 Integrating Battery into SM Using Passive Filters (Chapter 4)

- The methodology for designing two passive filter topologies, considering a low-pass LC filter and a CL-LC filter showed effectiveness in terms of the proposed attenuation for the battery current ripple and voltage ripple of the SM input capacitor;

- The methodology for surveying the capacitance and inductance curves, based on the definition of attenuation in dB, proved to be adequate for a comparison between passive filter topologies;
- The simulation and experimental results through the MPE, proposed in Chapter 2, validated the mitigation of critical harmonics in the SM battery current, eliminating the undesired components with the expected values in dB.

6.1.4 Integrating Battery into SM Using Active Filters (Chapter 5)

- The methodology for designing the proposed dc/dc converter topology showed effectiveness in terms of the proposed attenuation for the battery current ripple;
- The simulation and experimental results through the MPE validated the suppression of critical harmonics in the SM battery current, eliminating the undesired harmonic components;
- The dc/dc converter implemented in the simulation and testing scheme was able to obtain a higher attenuation level in the desired component of 60 Hz in the battery current, around -23 dB, demonstrating the flexibility of the methodology to attenuate compared to the passive filters.

6.2 Research Perspectives

While the present Ph.D. thesis has explored and documented numerous aspects, there remains room for further enhancements and future research. From the author's perspective, the following topics could be considered for future work:

- Evaluation of the arm current ripple estimation methodology for other MPE topologies: The simplification condition for the MPE switching frequency to be much higher than the SM switching frequency can be evaluated in quantitative terms regarding its limits and region of validity of this condition, as the experimental and simulated results demonstrate a good approximation between the estimate arm current ripple for equal frequencies;
- Validation of the passive filter design proposal for other converter topologies: Aspects such as volume optimization, cost, and losses of these filters can be explored to generate a figure of merit that allows the selection of a certain type of filter, based on already defined topologies;

- Evaluation of the long-term mission profile operation in an MMC-based BESS: One of the main aspects raised about the MPE refers to reliability and lifetime studies, which can be facilitated by the use of this emulator;
- Evaluation of an optimization tool to compare passive and active filtering strategies for the harmonic components of batteries: Aspects such as volume, losses, cost, and lifetime of passive filters and dc/dc converter can be explored to select the best strategy aimed at applying MMC-based BESS;
- Experimental validation of the full MMC-based BESS with the MPE results: The validations carried out in this work in terms of simulations can be carried out experimentally in laboratories that can test the full MMC-based BESS.

As observed, the possibilities for future developments are many. The author expects this research project to have continuity after the present Ph.D thesis.

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Biography

William Caires Silva Amorim was born in Caetité-BA, Brazil in 1996. He is a professor at the Federal Institute of Education, Science, and Technology of Minas Gerais, a Ph.D. in Electrical Engineering at the Federal University of Minas Gerais, and a professor of the Lato Sensu Postgraduate Course in the Department of Engineering Electrical at the Federal University of Viçosa. Graduated in Electrical Engineering at the Federal University of Viçosa (UFV) and Master in Electrical Engineering at the Federal Center for Technological Education of Minas Gerais (CEFET-MG).

He was a substitute professor at the Department of Electrical Engineering at the UFV, a Scientific Initiation Scholarship (IC) in the area of Information Theory, with an emphasis on Coding Theory by the PICME (Scientific Initiation and Master's Program) and monitor of the Signals and Systems. He is currently an effective member of the Brazilian Society of Power Electronics (SOBRAEP), an associate member of the Institute of Electrical and Electronics Engineers (IEEE), and a member of GESEP - Gerência de Especialistas em Sistemas Elétricos de Potência, where he develops research in the area of Renewable Energy and Storage Systems. He won a medal at the Brazilian Mathematics Olympiad (Bronze Medal - National Level), Brazilian Physics Olympiad (Gold Medal - State Level and Bronze Medal - National Level) and Public School Highlight at the Bahia Chemistry Olympiad. He was highlighted for the excellent Academic Performance of the 2018.1 graduating class of the Electrical Engineering course at UFV and awarded second place in the IEEE IAS Zucker Design Contest Results 2022 award.

E-mail: william.amorim@ieee.org
Website: www.gesep.ufv.br
Research Gate: https://www.researchgate.net/profile/William-Amorim
LinkedIn: https://www.linkedin.com/in/william-caires-silva-amorim-108b68169/

APPENDIX A – Appendix

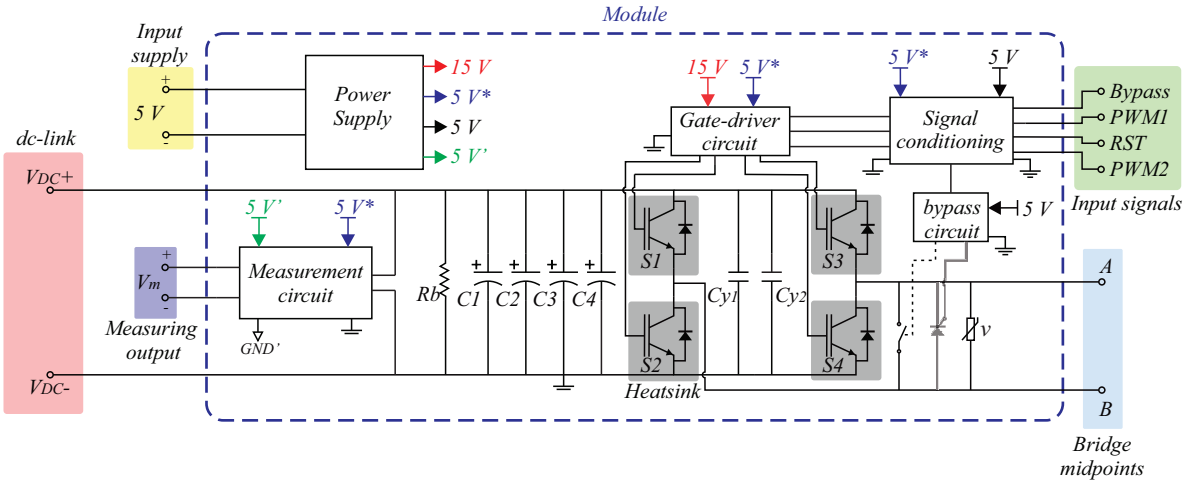
A.1 Small-scale prototype

A.1.1 Modules overview

To carry out experiments involving the MPE, at least two converter modules are needed. One of them must be a full-bridge converter, to operate as the MPE, and a second, to operate as the SM under test. The second module must be capable of operating as both full-bridge and half-bridge, depending on the SM type to be emulated. In the case discussed in this work, the SM is a half-bridge converter.

In this project, full-bridge modules were employed. The structure of the modules is shown in Fig. 69. One full-bridge module is used to implement the MPE, while another module is operated as a half-bridge converter to represent the SM under test. This configuration is obtained by blocking one of the IGBT arms of the full-bridge converter, that is, keeping the upper IGBT (S1) in the OFF state and the lower IGBT (S2) in the ON state. The other IGBT arm is modulated as a half-bridge converter. The designed full-bridge module is based on four layers of the printed circuit board (PCB) containing the power circuit, the gate drivers, dc-link voltage measurement, conditioning circuits, the bypass, and the power supply, as presented in Fig. 70. This circuit is responsible for receiving the signals coming from the DSP and generating the: PWM1*, PWM2*, RST* (reset signal - to turn off the IGBTs), and bypass (BP) signal.

Figure 69 – Proposed scheme for the converter modules.



Source: adapted from França et al. (2022).

Regarding power supplies and GND points, it is worth highlighting (França et al.,

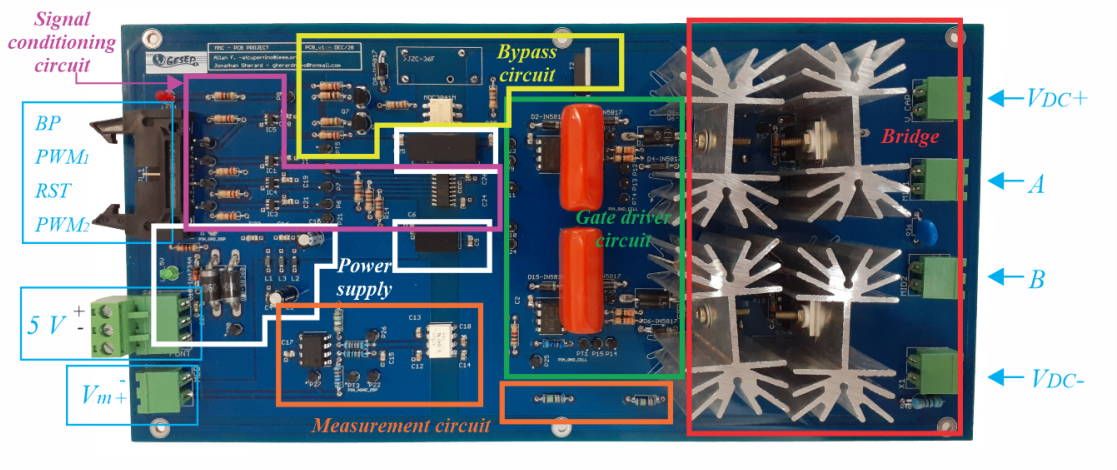
2022):

- The first one, called GND, is the digital circuit reference. The second, V_{DC-}, is the power circuit reference, and the third, GND', is the measurement circuit reference;
- 5 V^* refers to the isolated 5 V for the power circuit, and 5 V' refers to the filtered 5 V for the dc-link voltage measurement circuit;
- The first output level follows the protection scheme and supplies the isolated dc-dc converters, bypass circuits, LEDs, buffers, and the optocoupler from the signal circuit;
- After the π filter, the filtered voltage (5 V') supplies the voltage measurement circuit. The other two isolated voltage outputs (5V* and 15 V) are obtained by the dc-dc converters, supply the gate-driver, signal conditioning, and measurement circuits.

A.1.2 Technical Discussion of Module Design

Fig. 70 shows the top view of the full-bridge module. The board dimensions are 272 mm x 127 mm.

Figure 70 – Detailed view of the designed full-bridge module employed at the experimental results (the dc-link capacitors are not visible since they are installed at the bottom of the PCB).



Source: adapted from França et al. (2022).

In the full-bridge circuit, electrolytic capacitors $C1$, $C2$, $C3$, and $C4$ are used for ripple attenuation in the dc-link due to its higher energy density (compared with other capacitor technologies), in addition to the bleeder resistor R_b, to realize their discharge when the converter shuts down. There are also decoupling capacitors, C_{y1} and C_{y2}, installed near the IGBT legs to reduce the oscillations caused by IGBT switching.

The objective of the power supply scheme is to provide an isolated voltage supply to the integrated circuits (IC) and filtered voltage to the measurement circuit. In addition,

this circuit eliminates the need for pre-loading to start switching since the components are not powered by the dc-link. Isolated supplies are necessary since the same Digital Signal Processor (DSP) can be used to control different full-bridge modules. Therefore, a single DSP can measure several dc-link voltages that are about different electrical potentials. In this context, galvanic isolation is essential to prevent possible short circuits.

The digital conditioning circuit is responsible for galvanically isolating and adjusting the voltage value of the signals from the DSP and generating the isolated signals received in the gate-driver circuit. The gate-driver circuit is based on two half-bridge bootstrap drivers, each one responsible for triggering a pair of IGBTs. Furthermore, the IGBT and gate-driver connection is made as shown in Semikron (2016).

The dc-link voltage measurement circuit is composed of a voltage divider, an optocoupler, and an operational amplifier in a subtraction mode, which galvanically isolates and conditions the dc-link voltage to a range of values suitable for the DSP. Finally, the bypass circuit is composed of two activation circuits: the thyristor and the relay. Nevertheless, the thyristor is used just in HB applications, since the modules operating as full-bridge, could be accidentally triggered by an eventual dv/dt.

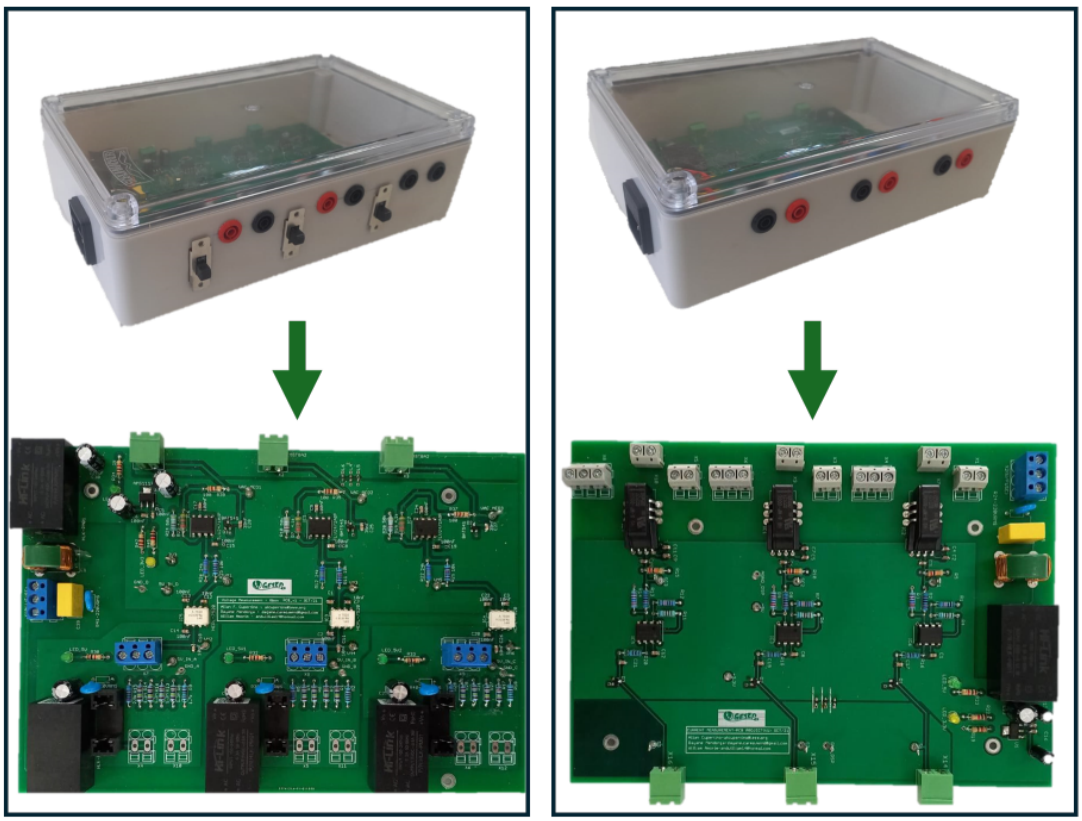
The bleed resistor adopted in this work is a rheostat in parallel with the unidirectional dc voltage source, with sufficient power to support charging and discharging current tests on batteries implemented in the results.

A.2 Measurement Circuit

The measurement circuit used to obtain the arm current, and battery current and send it to the DSP are presented in Figure 71. The measurement circuit, named Gbox, has two versions, one for voltage measurement and the other for current measurement (which was adopted in this work).

The voltage measurement circuit in Figure 71 (a), Gbox-V, is designed to read three independent ac voltage signals, with voltage levels defined in a scale of 127 Vrms or 220 Vrms, conditioning the outputs for reading a DSP with a range of 0-3.3V. The board features three connectors for the analog inputs, three selector switches to set the voltage level to be measured (127 Vrms or 220 Vrms), a three-terminal power supply connector, and three other connectors that provide the conditioned signals for the input of the DSP. The board supply voltage is realized by a bivolt power supply (127 Vrms or 220 Vrms), which through 4 ac/dc sources (Hi-link +5V), with isolation, obtains the +5V supply signals for the ICs. The output of the conditioning circuit results in three independent signals that are later taken to the DSP, via the 2-terminal MSTBA connector from manufacturer Phoenix Contact. Module inputs are provided via Phoenix connectors. It is worth remembering that despite the possibility of using the Gbox-V to measure the

Figure 71 – Measurement circuit: (a) Gbox-V; (b) Gbox-I.



(a) (b)

Source: own representation.

SM voltage, the measurement circuit on the full-bridge module, presented in Appendix A, already returns this value on the DSP input scale (range of 0-3.3V). This way, the full-bridge module dc-link voltage measurement circuit was used.

In turn, to measure arm and battery currents it was necessary to use the Gbox-I. The current measurement board in Figure 71 (b), Gbox-I, is designed to measure three individual current signals. The board features three 2-terminal connectors (Phoenix) for current measurement. The conditioned output from the board is via three 2-terminal connectors (MSTBA). The current sensor is the HO 8-NP-0000, and its operation is based on the Hall effect. This board power supply is performed similarly to the Gbox - Voltage circuit, with the difference that only one ac/dc converter is necessary, due to the inherent galvanic isolation of the current sensor. Furthermore, the current sensor can have its full scale modified depending on the measured current level (10 or 20A). Scale changes are done through a jumper inside the circuit.