DISSERTAÇÃO DE MESTRADO Nº 917

METHODOLOGY FOR ANALYSIS OF NOISE SUSCEPTIBILITY AND DESIGN SPACE EXPLORATION OF INTEGRATED CURRENT SENSORS FOR DETECTION OF TRANSIENT FAULTS

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DATA DA DEFESA: 25/04/2016

Universidade Federal de Minas Gerais

Escola de Engenharia

Programa de Pós-Graduação em Engenharia Elétrica

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Dissertação de Mestrado submetida à Banca Examinadora designada pelo Colegiado do Programa de Pós-Graduação em Engenharia Elétrica da Escola de Engenharia da Universidade Federal de Minas Gerais, como requisito para obtenção do Título de Mestre em Engenharia Elétrica.

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Belo Horizonte - MG

Abril de 2016

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Methodology for analysis of noise susceptibility and design space exploration of integrated current sensors for detection of transient faults

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April 25, 2016

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Methodology for analysis of noise susceptibility and design space exploration of integrated current sensors for detection of transient faults

Thesis presented to the Graduate Program in Electrical Engineering of the Federal University of Minas Gerais in partial fulfillment of the requirements for the degree of Master in Electrical Engineering.

Federal University of Minas Gerais

Graduate Program in Electrical Engineering

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April 25, 2016

Para meus pais, Márcia e João, minha irmã, Ana Catarina, e Renata.
Vocês são as fundações sobre as quais este trabalho foi construído.

Acknowledgements

Ao meu orientador, Prof. Frank Sill Torres, pela peculiar dedicação ao trabalho de orientador;

Ao Prof. Davies William, por ter me recebido de volta à UFMG com valiosos conselhos;

À Profa. Linnyer Beatrys, por seu acolhimento e posterior apoio na minha busca pelo sucesso no Mestrado;

A Clarice Renè Oliveira, por sua importante ajuda nos resultados deste trabalho;

A Dayane Reis, pela ajuda inestimável no ensino da formatação desta dissertação;

A todos os integrantes e ex-integrantes do grupo $OptMA^{Lab}$ e ART pela experiência social e amizade rara no cotidiano do desenvolvimento do trabalho de Mestrado.
Muito obrigado a todos!

Resumo

A indústria de semicondutores tem se desenvolvido desde a década de 1960 de forma notável, seguindo a previsão feita por Gordon Morre naquela época: a densidade espacial de transistores, o componente fundamental dos microchips, dobraria a cada nó de tecnologia de projeto e fabricação. Tal lei somente começou a não mais ser obedecida no momento em que este trabalho é escrito, e levou a impressionantes melhorias de funcionalidade de circuitos integrados. Apesar da revolução causada na vida cotidiana que o avanço da tecnologia de semicondutores traz, várias são as ameaças à funcionalidade dos microchips em tecnologias contemporâneas.

Um número de fenômenos físicos e a alta densidade de transistores cotribuem para falhas na operação de circuitos, desta forma, o desenvolvimento de sistemas de detecção de e reação a falhas é de suma importância. Como o aumento nos níveis de ruído são consequência inevitável do avanço da tecnologia de semicondutores, tais sistemas são, eles mesmos, ameaçados por esses sinais indesejados.

Neste trabalho, um sistema que detecta correntes induzidas potencialmente capazes de introduzir erros, chamado mBBICS, foi submetido a ruído em diversas simulações, e seu comportanto, analizado. Dois tipos de ruído são considerados no estudo: ruído de chaveamento e ruído de dispositivo. Ruído de chaveamento é gerado por circuitos digitais e propagado pelo substrato do chip, possivelmente afetando o mBBICS, e é diretamente relacionado à densidade de transistores na pastilha.

Ruído de dispositivo ocorre devido a efeitos quânticos que ocorrem dentro do canal do transistor. Ruído de chaveamento foi verificado, neste trabalho, ser uma ameaça a mBBICS projetados em tecnologia de 90nm, enquanto ruído de dispositivo não tem magnitude suficiente para ameaçar sua funcionalidade. Entretanto, considerando os atuais avanços na tecnologia de semicondutores, existe a possibilidade de que o ruído de dispositivo se torne um problema.

A fim de oferecer uma metologia que oferece preparação para essa possibilidade, alguns parâmetros do mBBICS foram modificados e seu comportamento verificado frente à presença de ruído de dispositivo. Mais especificamente, a robustez a ruído do circuito foi analisada. Tal robustez foi mensurada com a forma com a qual um aumento na sensibilidade do mBBICS incorre em susceptibilidade a ruído. Não obstante um aumento na sensibilidade necessariamente causa um aumento na vulnerabilidade a ruído, a metodologia executada resultou na definição de parâmetros elétricos e geométricos ótimos, que favorecem a sensibilidade, enquanto apresentam menor penalidade na susceptibilidade ao ruído. Isso

permite um projetista a guiar seu projeto com base nos parâmetros presentes em grupos definidos que são mais promissores a um design robusto.

Keywords: Confiabilidade, Ruído, CMOS, VLSI, Modelagem do substrato.

Abstract

The semiconductor industry is being developed since the decade of 1960 in a remarkable fashion, by being able to follow the prediction that Gordon Moore stated at that time: the spatial density of transistors, the most fundamental components of microchips, would double at each technology node. Such law only began to be inaccurate at the date of this writing, and lead to an outstanding enhancement of functionality of integrated circuits. Despite the revolutions in human daily life the technology scaling produces, many are the threats to chips functionality in contemporary technologies.

Numerous physical phenomena and very high spatial transistor density contribute to disrupt a circuit's operation, so the development of detection and counteraction systems is of utmost importance. Since noise levels increase also accompany technology scaling, such systems are also endangered by those undesired signals.

In this work, a system that senses potentially error-causing currents, called the modular Bulk Built-In Current Sensor (mBBICS), is submitted to noise in several simulations, and its behavior is studied. Two types of noise are considered in the study: switching noise and device noise. Switching noise is generated by switching circuits and propagated through the chip's Silicon substrate, possibly affecting the mBBICS, and is directly related to the device density in the chip. Device noise takes place due to quantum effects inside the transistor's channel. Hereby, switching noise was verified to be a threat to an mBBICS designed in a 90nm technology, whereas device noise is not high enough to pose a threat. However, with technology advancements, there is the possibility that device noise turns into an issue.

In order to contribute to this possibility, a few parameters of the mBBICS were adjusted and its behavior in the presence of device noise, verified. More specifically, the circuit's robustness to noise was analyzed, which was measured by how a sensitivity increase in the sensor leads also to vulnerability to noise. Nevertheless an increase in sensitivity necessarily causes an increase in susceptibility to noise, the performed methodology lead to optimal dimensional and electrical parameters, that highly favor sensitivity, while presenting little penalty in noise susceptibility. This empowers a designer to drive his or her circuit development based on the parameters' design space that better leads to a robust behavior.

Keywords: Reliability, Noise, CMOS, VLSI, Substrate modeling.

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1 Introduction

Contemporary personal and industrial/commercial electronic devices are small sized, computationally efficient and consume sufficiently low power to be carried in a pocket or embedded in larger pieces of apparatus, relying on batteries. The pervasion of microchips in society's daily lives and cultures is implacable due to the practicality they provide. This is a consequence of the fast paced evolution of semiconductor technology generations (also known as *nodes*, which is directly related to the miniaturization of on-chip devices) [1].

The technology evolution of *integrated circuits* (ICs) is registered and projected by the *International Technology Roadmap for Semiconductors* (ITRS). Throughout the history of ITRS, the main development driver observed is Moore's Law, which for decades has been predicting fairly accurately that electronic components density in chips doubles at each technology node [1]. At the present date, processors with a technology size as small as 14nm are widely commercialized.

Such outstanding technological achievements do not arise free of costs. An increasingly important price is systems reliability. Circuits in chips are made with components such as transistors. The smaller they are built, the more susceptible to several physical phenomena the components become. Among those, there are interactions with radioactive particles and vulnerability to random electrical signal fluctuations, which is referred to as *noise*.

Technology node scaling is prone to other effects that threaten reliability. For example, it is possible that wires in the chip gradually disintegrate, incurring in open circuits. This can be caused by Electromigration or Stress migration, which are caused, respectively, by quantum effects in the presence of electrical currents and by stress gradients in the integrated circuit manufacture process. In addition, transistor's oxides wear out with time, eventually breaking down. Another effect, called thermal cycling, can cause fatigue in chip structures and possibly result in their disruption. Studies in the field of reliability aim to produce solutions to issues such as the aforementioned [2].

On one hand, there is a myriad of error detection and/or correction alternatives to deal with undesired events such as radioactive particle interaction with on-chip devices. However, noise could threaten the functionality of these contingencies. As an example, electrical surges that lead to transient faults are very small quantities in current technologies, and could be similar to noise in magnitude. The aforementioned susceptibility scenarios imposed by the state of the art in semiconductor technologies encourage studies aiming to investigate noise impact on reliability systems. The term *reliability systems* is used hereby

to refer to error resilient systems, designed to detect potential causes of system failure, such as radioactive particle strikes.

1.1 Motivation

Until about the year 2000, nanometric technologies were yet to emerge. Chips were already known to suffer from transient faults induced by radiation both in aerospace applications and in memory circuits at ground level [3]. Devices in more advanced technology nodes tend to experience more faults induced by radioactive particles [4]. Furthermore, combinational logic circuit blocks already are, along with memory, potential victims of radioactive particle strikes [5].

The effects of those can temporarily change a bit value in a circuit. It is possible that this bit will be involved in computations before the restoration, which may lead to critical scenarios. Information corruptions caused by transient faults belong to the class of *soft errors*, given that data is compromised, but the hardware remains intact [3]. One example for transient fault detection systems are the Bulk Built-In Current Sensors, or BBICS. The circuits in this category work by sensing an electrical current, which is generated together with the transient fault, and signalling to a further system that the fault has occurred [5]. Such system will then take proper action to manage the event.

In addition, the possibility of noise to impact soft error detection stands as a menace to error resilient circuits. If electrical noise is not considered at design time, it may interfere with the transient fault sensing, eventually signalling faults that did not occur. This motivates the investigations in this work, given that technology scaling leads to smaller noise margins. Thorough studies regarding noise impact in soft error resilient circuits are then of considerable importance.

1.2 Objectives

Given the aforementioned threats, radiation induced soft errors, together with CMOS technology scaling challenges related to noise, may drive nanometric fault detection circuits distrustful. The necessity for reliance in these circuits is the main purpose of the study hereby presented. More specifically, it is intended to investigate:

- noise levels that invalidate error detection by mBBICS (topology of BBICS);
- potential invalidation caused by noise generated by on-chip circuitry;
- error signalling corruption caused by noise generated by internal transistor effects;
- mBBICS malfunction by noise propagated through the substrate;

- manipulation of mBBICS to enchance robustness to noise.

To address those, firstly, it is intended to verify the possibility of noise to disturb the functionality of the sensor. Transient faults are to be modelled and applied to the circuit as well. Once the analyses are obtained, alternatives to enhance the mBBICS's robustness to noise are to be proposed, by adapting different circuit's characteristics. This will be followed by comparison with the original results, providing evidence about robustness to noise improvement.

1.3 Document structure

This document is organized as follows: chapter 2 provides theoretical background about the knowledge areas involved in the discussions here presented. They are the basic theory of MOS transistors, techniques for modeling the substrate, forms of noise generation inside the chip, how radioactive particles can induce a transient fault and a description of the exemplary circuit, the mBBICS. Chapter 3 presents related works. Chapter 4 describes the workflows conceived for the investigations of interest. Such investigations encompass mBBICS's behavior in the presence of transient faults and noise. Chapter 5 presents the execution of the planned simulations. They were conceived aiming implementation of the concepts in chapter 4 and the analyses of the results. Chapter 6 explores the propositions for robustness to noise improvement. Simulations and related discussions support such exploration. Chapter 7 concludes the work.

2 Background

This chapter presents the theoretical background that supports the work hereby presented. Firstly, the *Metal-Oxide-Semiconductor* (MOS) transistor is described, as the subsequent sections depend on its understanding. The concepts behind modeling the chips's substrate and its importance are presented next. This section is followed by the description of usual noise sources that appear in *Very Large Scale of Integration* (VLSI) designs. The basic mechanisms and modeling of radiation induced transient faults are then described, and the chapter finishes with the presentation of the mBBICS's mode of operation.

2.1 MOS devices

In this section the *Metal-Oxide-Semiconductor* transistor is presented. While MOS refers to a structural characteristic of the device, the term *Field Effect Transistor* (FET) refers to its principle of operation, which will be described later in this section, leading to MOSFET as a usual name for this kind of transistor.

Understanding the semiconductor's crystalline structure and the effect of implanting in it other elements (also known as *impurities*) is fundamental to comprehend the MOSFET's operational mechanism. Hereby, silicon (Si) will be used as the representative semiconductor material, given that it is the most widely used in chip fabrication [6]. The location of Si in the periodic table of elements shows that it has four valence electrons. A Si atom, in a pure material sample, makes four covalent bonds each with other Si atoms in its vicinity. By applying this concept to all atoms in the material, it results, theoretically, in a formation without free electrons. In reality, there are very few free electrons due to thermal excitation, however, the quantity is not sufficient to produce appreciable currents. Since free *charge carriers*, such as electrons, are necessary to conduct electrical current, pure silicon is a poor conductive material [7].

This scenario changes if atoms of other materials, called *dopants*, such as phosphorus (P) or boron (B) are introduced in the silicon lattice [6], by means that are beyond the scope of this work. Consider the introduction of an element such as P in the lattice, *i.e.*, the process of *doping*. This element has five valence electrons, which means that, upon its introduction in a Si structure, four covalent bonds are established with Si atoms, while the remaining electron has no acceptor atom to create a bond. Elements that incur in this extra electron are called *donors*. The insertion of various P atoms throughout a Si sample makes it, hence, conductive, since free electrons are available for current conduction being usually referred to as *charge carriers*. The resulting material after doping with donor

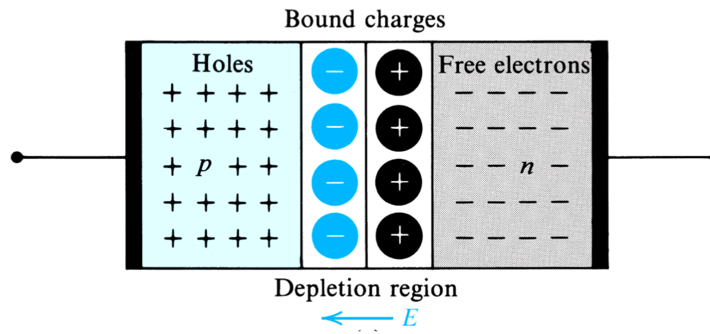

Figure 1 – PN junction with bound charges and electric field shown. [7].

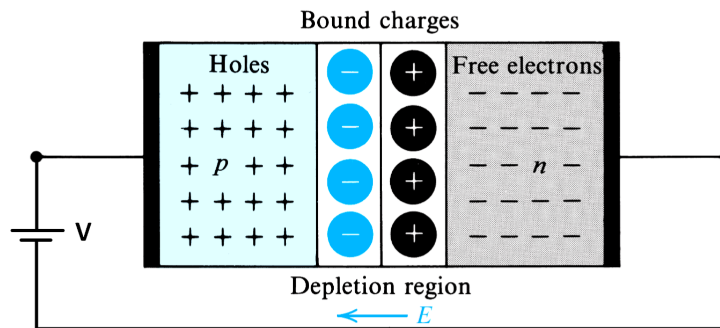

Figure 2 – PN junction with applied V voltage. [7].

elements is called an *n-type* material, since charge carriers are negative [7].

Boron, in contrast, presents three electrons in the valence energy level. Analogously to the case of *P*, the insertion of *B* in a *Si* sample originates three covalent bonds with neighbouring atoms, however, one *Si* atom is left with one acceptor energy state in its valence level. This can be not so intuitive as in the case of electron exceedance. Even though, the lack of electrons for the accepting energy states is akin to it in terms of current conduction. Such lack is denominated a *hole*, and can be interpreted as a charge carrier, as well as the electron. Doping with *B* also causes the material do be conductive, due to the holes, that are available for conduction. Materials doped in this way are said to be *p-type* materials, given that the charge carriers are positive.

Generating an interface between n-type and p-type materials leads to useful properties. As a theoretical approach, consider two rectangular blocks of *Si*, an n-type and a p-type, as shown in Figure 1. If one puts those blocks together, the negative charge carriers in the *n* region would be attracted to the positive potential that originates from the p-type material. Similarly, the positive charge carriers in the *p* region would tend to flow to the *n* region. These charge carriers tend to traverse the material interface to the opposite charge material via a process called *diffusion current*. Electrons that reach the p-type region recombine with the holes in the material, creating a neutralized portion of *Si* in the vicinity of the interface, *i.e.* a region that is *depleted* of electrons. However, some of the electrons do not recombine, since holes are also moving from the p-type region,

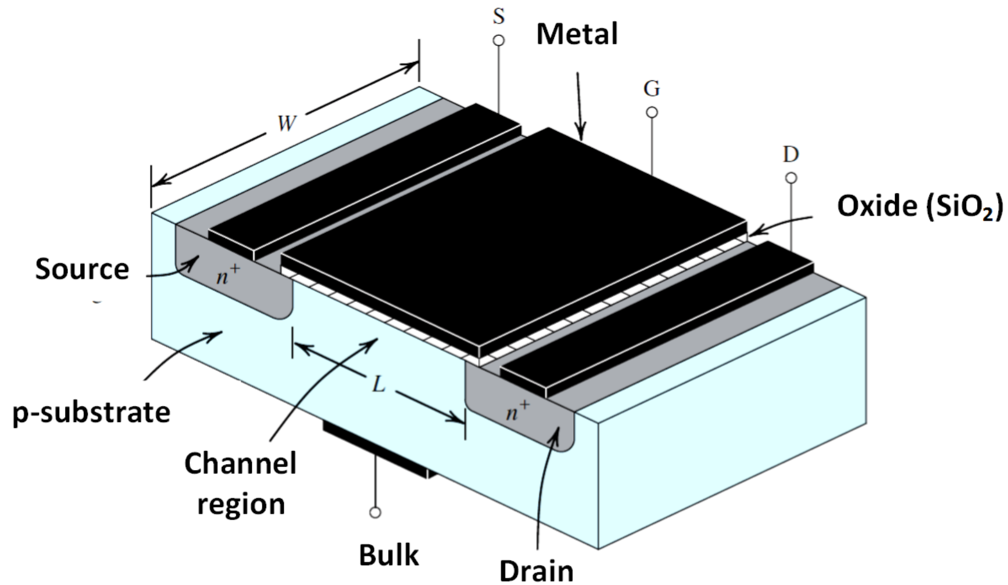

Figure 3 – Profile of an N-type MOSFET device. [7].

resulting in a lack of holes for recombination. This originates a boundary of negative charges in the p-type region. The analogous occurs to holes that diffuse to the n-type material. Therefore, the depletion region is bounded by negative charges in the p-type region and positive charges in the n-type region. This results in the presence of an electric field across the depletion layer [8].

If the *p* and the n-type *Si* blocks regions can be connected by a wire to a voltage source, two possible situations may apply. Firstly, consider connecting a voltage source V to the described *Si* structure (Figure 2), with the positive terminal in contact with the p-type region and the negative one to the n-type region. The source's positive potential would accelerate the holes off the p-type region through de depletion region, as well as attract the electrons in a similar fashion. The negative potential will do the opposite. Therefore, a current will be constantly conducted through the semiconductor structure, which is then *forward biased*. If the connections to the source are inverted, the positive potential will attract the electrons of the n-type region. Analogously, the negative potential will attract the holes of the *p* region. Hence, no electric current will be present, and the structure is said to be *reversed biased* [7].

Once the *pn* junction's behavior is known, the structure of the MOS transistor can be introduced and is presented in Figure 3. The basic structure for building transistors is a thin *Si* round plate, which is known as the *substrate*. Such plate is referred to as a *Si wafer*, due to the grid pattern that results after the integrated circuit fabrication is finished, which is similar to a biscuit that is known in gastronomy by the same name. In MOS transistors fabrication, the *Si* wafer is the starting structure, initially doped either with a *p* or *n* type dopant. Hereby, an initial p-type doping is considered. A layer of dielectric material

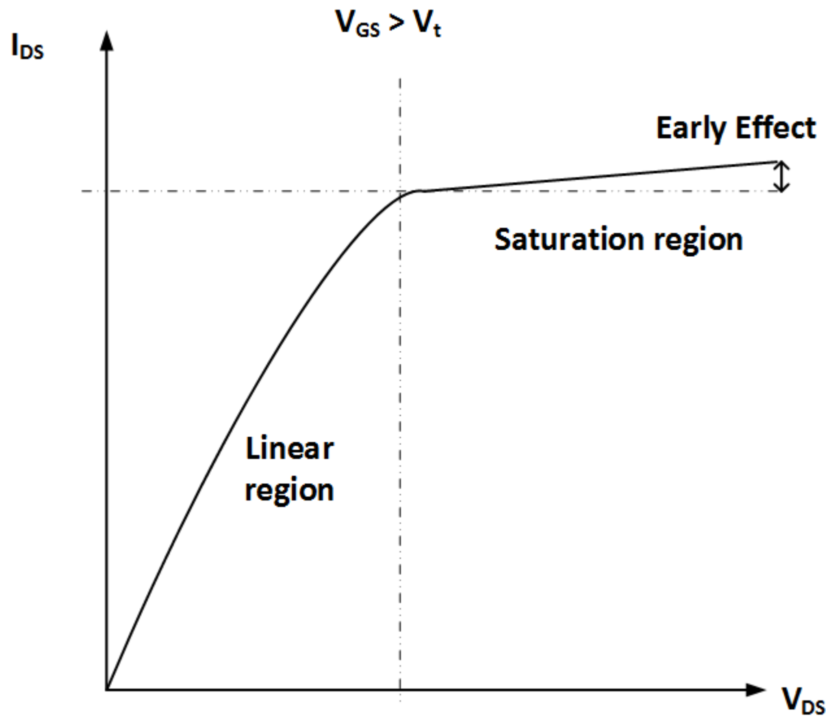

Figure 4 – Regimes of operation of the MOS transistor.

(namely, SiO_2, usually referred to simply as the *oxide*), followed by a metallic layer, forms the *gate* terminal and the Metal-Oxide-Semiconductor configuration that originates the device's name. Since the semiconductor part is doped, it is a conductive material, and a Conductor-Dielectric-Conductor scheme is being dealt with. The *Si* parts close to the edges of the oxide are doped with donors, constituting n-type regions. A metallic layer is placed atop the n-type diffusions, thus known as the *drain* and *source* terminals [6]. These structures are only distinguished after biasing is applied to the device, otherwise, they present no functional differences.

With the physical structure clarified, it is possible to conclude the MOS transistor's operation description. Firstly, a DC voltage source V_G is connected to the structure, such that the positive terminal is connected to the metallic layer above the *oxide*, which is known as the *gate*. The negative terminal is connected to the bottom of the *Si* substrate, referred to as the *bulk* terminal. When V_G increases, the result is that the gate contact's potential becomes more positive than the substrate below the oxide. Consequently, negative charge carriers accumulate in that region, being attracted by the gate contact. This charge carrier concentration assumes different properties, in accordance to the level of the gate voltage. For low enough positive values of V_G, the concentration of negative charge carriers reaches a state called *accumulation*. If V_G reaches a specific voltage, denoted as V_t (for *threshold*), the concentration of negative carrier below the oxide is high enough to turn that region, which is originally a p-type, into an n-type region. At this state, a charge carrier *channel* is said to be formed, and by applying a positive V_{DS} voltage from the drain to the source

terminals, a negative charge-carrier current can be conducted through the channel. The formation of the channel by a potential applied to the gate contact occurs due to the presence of an electric field that attracts negative charge carriers and repels the positive ones. This characteristic is what justifies the *Field Effect Transistor* nomenclature.

Different values for the V_G voltage were explored, however, regarding the source and drain terminals, there is still more to analyse. It is usually convenient to set the bulk and the source terminals to the same potential, therefore, the voltage V_G can be equally expressed throughout this text by the *gate to source voltage* V_{GS}. Even though a V_{GS} voltage, above V_t, is applied, a V_{DS} voltage above zero is necessary to accelerate the charge carriers in the formed channel. The channel, although it is a conductive region, is not ideal and presents an electrical resistance, denominated r_{DS} for *drain to source resistance.* Given that a voltage V_{DS} across a resitance r_{DS} is configured, there is a linear relationship between V_{DS} and the resultant channel current (which is, in reality, an approximation), hereby I_{DS}, as depicted in Figure 4, on page 8. This relationship is mathematically described by [8]:

$$V_{GS} > V_t; V_{DS} < V_{GS} - V_t \tag{2.1}$$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_t\right) V_{DS} \tag{2.2}$$

Where:

μ_n : mobility of negative charge carriers
C_{ox} : oxide capacitance
W : width of the device
L : length of the device
V_{GS} : gate to source voltage
V_t : threshold voltage
V_{DS} : drain to source voltage

This situation, however, does not stand true as V_{DS} is increased above a specific point. The reason is that as V_{DS} rises, the voltage at the drain terminal also rises, thus attracting the channel more vigorously near the drain. At a sufficiently high V_{DS}, there is a situation in which the gate to drain voltage V_{GD} drops below V_t, thus disabling the channel formation at that point. The channel is, then, said to be *pinched-off* (Figure 5), and as V_{DS} increases, virtually no change occurs in the value of I_{DS}. The MOSFET is said, then, to be in the *saturation region*, which can be expressed mathematically as:

$$V_{GS} > V_t; V_{DS} > V_{GS} - V_t \tag{2.3}$$

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_t\right) \tag{2.4}$$

In reality, changes in V_{DS} in the saturation region do incur in small changes in I_{DS}, which is a phenomenon called the *Early Effect*. This occurs because increasing V_{DS} further than $V_{GS} - V_t$ moves the pinch-off point in the channel towards the source terminal, thus slightly increasing the channel resistance [7].

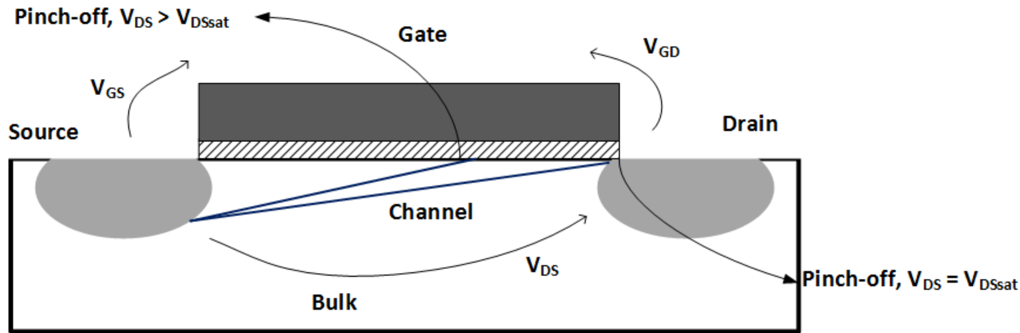

Figure 5 – MOSFET channel pinch-off (refer to equation 2.3 in page 9).

The physical structure of the MOSFET presents a few configurations that are prone to capacitive parasitic effects, presented in Figure 6. One of these configurations is the oxide and gate metallic terminal disposition. Given that the channel region is conductive, a conductor-dielectric-conductor disposition takes place, which characterizes a capacitor. This parasitic capacitance is referred to as C_{gd}, for *gate to drain capacitance*.

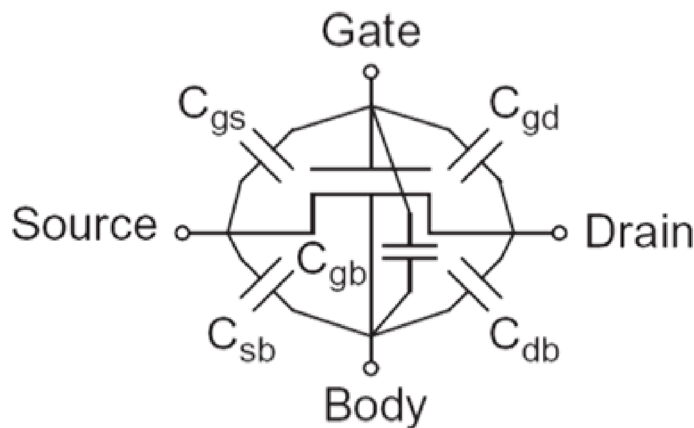

Figure 6 – Parasitic capacitances of a MOS device [9]

The conductor-dielectric-conductor scheme manifests a few more time in the device. The source and drain diffusions interface with the substrate by a depletion region, which is commonly reverse biased or at nearly zero voltage drop. The potential barrier imposed by the depletion region, which is thus non-conductive, separates the substrate and the diffusion. This capacitive characteristic disposition origins C_{db} and C_{sb}, which are, respectively, the *drain to bulk capacitance* and the source to bulk capacitance.

The transistor structure, once built, is then covered with insulating material, usually, silicon nitride (Si_3N_4). The gate, drain and source metallic terminals, which are relatively close to which other, are then separated by a dielectric, and configure C_{gd} and C_{gs}. Those are the *gate to drain capacitance* and *gate to source capacitance*, respectively.

These are not the only capacitive mechanisms present in the MOSFET. For instance, process imperfections commonly cause an overlap between the gate oxide and a portion of source and drain diffusions. However, these mechanisms analysis introduce details that go beyond the scope of this work.

Finally, a complementary type of MOSFET is widely used, which is built based on an n-type doped substrate or, more commonly, on an n-type region created over a p-type doped substrate, called the *n-well*. This device, called the *PMOS transistor*, operates with a p-type channel, and the biasing characteristics are similar but opposite to those of the NMOS transistor. A summary of the biasing characteristics follow.

- The formation of the *p-channel* occurs by applying a negative potential to the gate contact. The channel is formed when V_{GS} is lower than the threshold voltage V_t, which is negative:

$$V_{GS} < V_t < 0 \tag{2.5}$$

- The linear region of operation is defined for V_{GS} being lower than V_t and V_{DS} higher than $V_{GS} - V_t$:

$$V_{GS} - V_t < 0; V_{DS} < V_{GS} - V_t \tag{2.6}$$

$$I_{DS} = \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_t) V_{DS} \tag{2.7}$$

  Where:

  μ_p : mobility of positive charge carriers

- The saturation region occurs for V_{GS} lower than V_t and V_{DS} lower than $V_{GS} - V_t$:

$$V_{GS} < V_t; V_{DS} < V_{GS} - V_t \tag{2.8}$$

$$I_{DS} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_t) \tag{2.9}$$

Generally, MOS transistors are used with its source terminal short circuited with the bulk terminal, since the bulk should be at the lowest potential (in the case of the PMOS transistor, in the highest potential) in order to guarantee that the junctions with source and drain are reversed biased. However, by making the voltage between source and bulk different than zero, one can turn it easier or harder for the conducting channel to form. As a result, one can control the value of the threshold voltage V_t, which is primarily determined at manufacture time, at design time, by biasing it properly. Mathematically, the threshold voltage is modulated as follows.

$$V_t = V_{t0} + \frac{\sqrt{2\epsilon_s q N_a}}{C_{OX}} \left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right) \tag{2.10}$$

Where:

$V_t is the threshold voltage for the NMOS transistor$:

ϵ_s	: Electrical permitivity of Silicon
q	: Modulus of the electron charge
N_a	: Acceptor concentration
C_{OX}	: Gate oxide capacitance
Φ_F	: Surface potential
V_{SB}	: Source do body voltage

$$V_t = V_{t0} + \frac{\sqrt{2\epsilon_s q N_d}}{C_{OX}} \left(\sqrt{2\Phi_F + V_{BS}} - \sqrt{2\Phi_F} \right) \tag{2.11}$$

Where:

$V_t is the threshold voltage for the PMOS transistor$:

ϵ_s	: Electrical permitivity of Silicon
q	: Modulus of the electron charge
N_d	: Donor concentration
C_{OX}	: Gate oxide capacitance
Φ_F	: Surface potential
V_{BS}	: Body to source voltage

2.2 Substrate modeling

In order to analyze the effects of the substrate parasitic effects, an appropriate model is required. Such a model consists of interconnected electrical components, which values are obtained by applying electromagnetic differential equations to mathematically delimited substrate regions [10]. Constituent material, doping and region geometry determine the parasitic components values. The electrical components modeling can be achieved by

techniques that suit in three different categories: numerical methods, analytical methods and empirical methods.

Analytical methods rely on approximate mathematical models based on electromagnetic laws. Although it involves the neglecting of various physical effects, such methods provide acceptable accuracy. Given that their implementations comprise intensive mathematical computation, they are not recommended for the extraction of layouts with large numbers of interconnects.

The empirical methods, in turn, make use of vast collections of experimental data, which are then fitted to a mathematical model. In a typical IC design, layout configurations are usually too complex to derive analytical formulae from. This approach would be impractical, given the complexity of the structures. In contrast, the empirical technique involves computationally intensive functions such as logarithms and exponentials, which constitutes one drawback of this method [11].

Finally, there are the numerical methods, *e.g.* the *Finite Element Method* (FEM) approach, which is the chosen method in this work. Hereby, the substrate is discretized into cubes. The cube is translated into an electrical circuit composed by resistances and capacitances, as depicted in Figure 7. Letter i represents the center of the cube, and j represents each face. Components R and C are resistance and capacitance, respectively. Their values depend on the dimensions of the cuboid and the electrical characteristics of the material [12]. The reintegration of the entire substrate is accomplished by interconnecting the appropriate nodes, obeying the spatial disposition of each element.

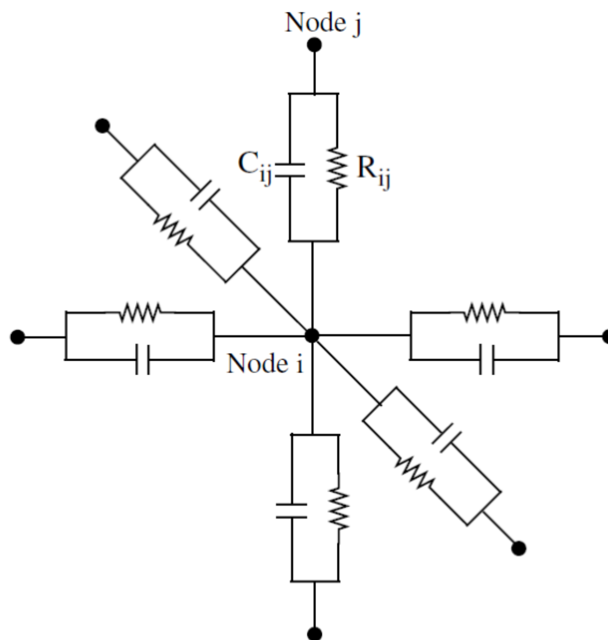

Figure 7 – Planar representation of the substrate finite element. [10].

Finite Element Method provides a three dimensional modeling of the entire substrate. However, in order to obtain satisfactory modeling resolution, the computational time can easily reach impractical values. Consequently, a technique of fine discretization is suitable exclusively for more heterogeneous areas, *e.g.* junctions and interfaces with growth oxides (thus, closer to the surface). Deeper regions in the substrate tend to be more homogeneous, and a coarser discretization is preferred to improve calculation time [13].

Another approach is the *Boundary Element Method* (BEM), which implements a discretization of selected structures, for example, contacts, well and substrate taps, as well as diffusion regions [14]. Those structures are two dimensional, and thus, BEM provides a 2-D substrate model, comprising only regions of the substrate surface. Although BEM is efficient in terms of computational effort, it cannot model deepest substrate characteristics [12].

2.3 On-chip generated noise

The operation of integrated circuits generates signal disturbances in the chip's substrate, signal wires and power rails, due to steep transition times and substrate coupling mechanisms [10]. The operation of millions or billions of transistors combined, injecting noise in the same substrate, culminates in on-chip noise caused by normal circuit switching. As well as that, undesirable quantum effects take place in the channel and junctions of MOSFET devices. These are potential problems for circuit reliability, particularly concerning mixed-signal chips, where noise generated by a digital aggressor affects sensitive analog circuitry [13]. This section presents noise generation mechanisms that are capable of interfering in circuits functionality. The first category of noise sources discussed is *device noise*, which refers to internal undesired transistor phenomena. Subsequently, forms of noise introduction in the *Si* substrate by aggressor circuits are explored. Such forms are known by *switching noise coupling*.

2.3.1 CMOS device noise

The term *CMOS device noise* refers to quantum effects that take place in the transistor's channel and junctions. Such effects cause random fluctuations in the current that flows through the device. Three noise generation mechanisms compose device noise: Thermal Noise and Shot Noise (which can be referred to as *White Gaussian Noise* (WGN), due to their independence on frequency), and Flicker Noise [10].

Thermal Noise is physically caused by random motion of charge carriers. These are only capable of composing an electrical current if electrons have enough energy to lie in the *conduction energy band*, which is a set of discrete energy states that an electron can be

in [8]. Once electrons are in the conduction band, agitation induced in them by thermal energy is observed as random dislocations of charge. These are dependent on temperature, but occur at virtually any frequency [10].

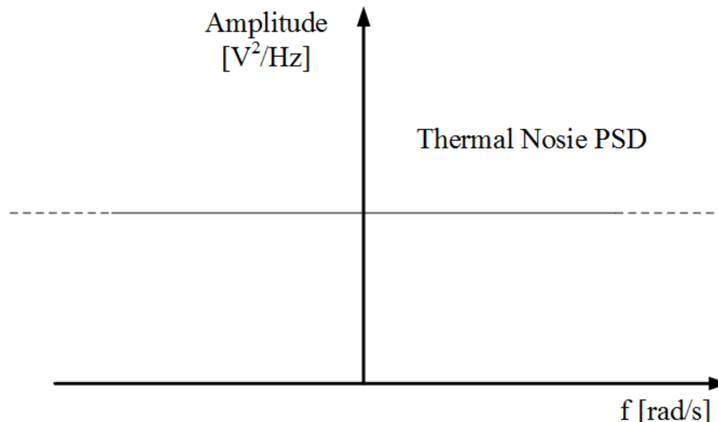

Figure 8 – *Power Spectral Density* (PSD) of Thermal Noise.

To express Thermal Noise mathematically, the *Power Spectral Density* (PSD) concept is used. The PSD is a representation of noise in the frequency domain, which indicates the distribution of noise magnitudes along frequency ranges for a given waveform [15]. Given that Thermal Noise is independent of frequency, one can conclude that its PSD format, at least ideally, is a constant function, as the one shown in Figure 8. The mathematical formula for the PSD of Thermal Noise, henceforth $S_{TN}(f)$, is the one in 2.12, and has the units of $\frac{V^2}{Hz}$ [10]. Notice that f does not appear at the right hand side of the equation, evidencing frequency independence.

$$S_{TN}(f) = 4k_bT\gamma g_m \tag{2.12}$$

Where:

S_{TN} : Power Spectral Density of Thermal Noise
k_b : Boltzmann constant
T : Temperature
γ : Technology node dependent parameter
g_m : Transconductance of the transistor

Another characteristic noise in semiconductor devices, called Shot Noise, results from the discrete nature of charge carriers. The physical mechanism of this kind of noise takes place in potential barriers, *e.g.* pn-junctions. Consider the forward-biased pn-junction in Figure 9. The current through the junction consists in the charge carriers that have enough energy to cross the potential barrier imposed by the depletion layer. The total numbers of each charge carrier across such layer are considered random and independent

events. Thus, the number of charge carriers fluctuates in different time intervals, due to the emission of a random number of electrons from the n-region and collection by the p-region (the inverse applies to holes) [16].

The PSD of Shot Noise is:

$$S_{SN}(f) = 2qI_o \tag{2.13}$$

Where:

S_{SN} : Power Spectral Density of Shot Noise
q : Absolute value of electron charge
I_o : Average current through the junction

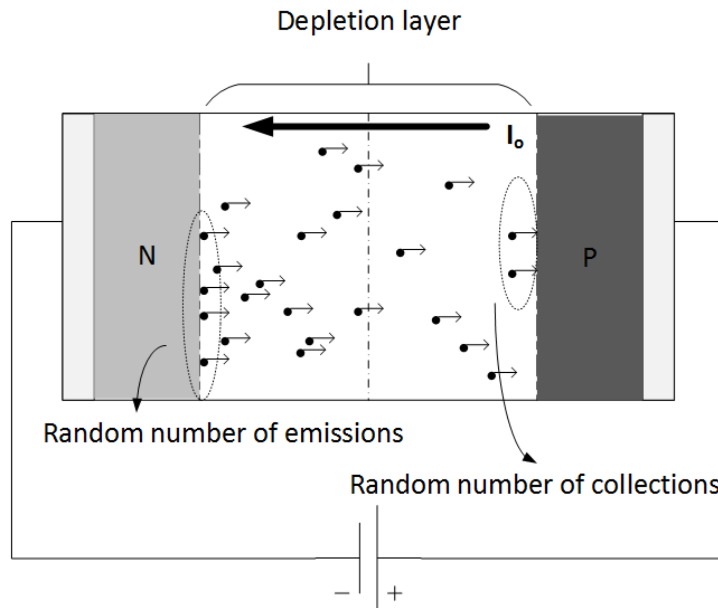

Figure 9 – Shot Noise physical mechanism.

Since the definition of Shot Noise involves current fluctuations, the units are $\frac{A^2}{Hz}$. Clearly, it is independent of frequency, by analyzing equation 2.13, like Thermal Noise. The PSD of Shot Noise is, hence, equal to that of Thermal Noise (Figure 8), with amplitude given by equation 2.13 and the aforementioned change of unit in the vertical axis (Figure 10) [10]. Furthermore, it is also independent of temperature, as can be seen in equation 2.13.

It is important to state that equation 2.13 was deduced for carriers on *ballistic trajectories*, which means that they don't interact with other particles or with the lattice atoms during transit. Therefore, the randomness of this noise mechanism is reduced in practice. Nevertheless, this restriction has less influence on reverse-biased junctions [16].

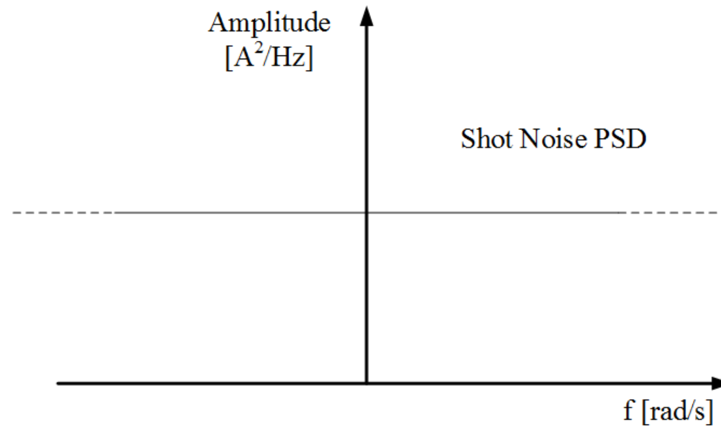

Figure 10 – *Power Spectral Density* (PSD) of Shot Noise.

These first two noise sources belong to the category of *White Noise*, given that their PSDs are ideally constant for all frequencies. An important property of White Noise is that each of its instantaneous values are uncorrelated with any previous ones, *i.e.* past noise values cannot predict any future ones [15].

The next noise type to be discussed is substantially different from the previous ones, as it does not belong to the class of White Noise. Flicker Noise, also known as $\frac{1}{f}$ Noise, Pink Noise and Excess Noise, is the dominant noise source in MOS devices at low frequencies such as tens of Hz and up to a few kHz [17], depending on the application.

The physical mechanism involved in $\frac{1}{f}$ noise generation is still subject of controversy [18]. One widely accepted hypothesis is the presence of discontinuities in the current conduction medium, *i.e.* the substrate (channel), in the case of a MOSFET device. Such discontinuities can be defects in the semiconductor lattice or the presence of unwanted impurity atoms. Those introduce energy states that do not exist in the propagation medium, which are called *traps*, since an electron that is part of the flowing current can occupy one of those energy states while it is traversing the channel (which should not occur in a defect-free material). This is referred to as *trapping.* As well, a trapped electron can acquire sufficient energy to re-occupy an energy state in the conduction band (*detrapping*). These phenomena present relatively long time constants, thus, are related to low frequency [16]. Such trapping and detrapping of electrons are considered to be the cause of $\frac{1}{f}$ current fluctuations observed in MOS transistors.

The name $\frac{1}{f}$ Noise was coined because its PSD decreases similarly to a straight line with $log(f)$, as can be seen in Figure 11. This decrease with frequency in the Flicker Noise's PSD occurs up to a frequency f_c, or the *crossover frequency.* From that value on, Flicker Noise ceases, and White Noise dominates, as the PSD becomes constant, regardless of the frequency.

The linearity of the decrease in the PSD can also be mathematically interpreted by

a decrease in approximately 3dB per octave [17]. This can be verified by three observations:

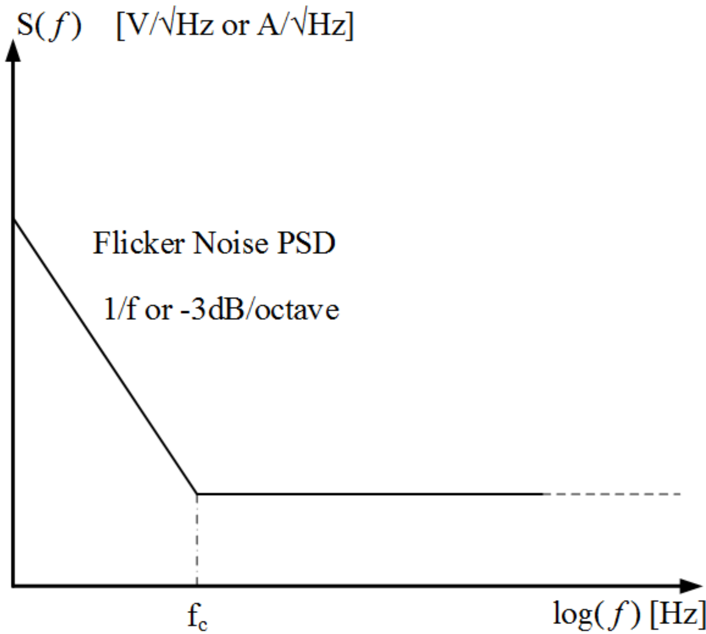

Figure 11 – *Power Spectral Density* (PSD) of Flicker Noise.

- To divide a value by two in a linear scale is equivalent to subtract 3dB from such value in a logarithmic one;
- A value, A, is said to be one octave above another value, B, if $A = 2B$;
- In a function such as:
  $y = \frac{1}{x}$
  doubling the value of x leads to half the value of y.

Therefore, stating that a function obeys the law:

$$S_{FN}(f) = \frac{1}{f} \qquad f \leq f_c \tag{2.14}$$

Where:

S_{FN} : Power Spectral Density of Flicker Noise
f : frequency

is equivalent to affirm that S_{FN} decreases at a rate of 3dB per octave.

A few mathematical models were proposed in order to model Flicker Noise. One of those is the Hooge model [19]:

$$S_F = \frac{q}{C_{OX}} \frac{\alpha_H}{WLf} (V_{GS} - V_t) \frac{A^2}{Hz} \tag{2.15}$$

Where:

S_F : PSD of Flicker Noise according to the Hooge model
q : Modulus of the electron charge
C_{OX} : Gate oxide capacitance
α_H : Hooge empirical parameter
W : Transistor's width
L : Transistor's length
V_{GS} : Gate to source voltage
V_t : Transistor's threshold voltage

The Hooge empirical parameter is observed to be in the order of magnitude of 10^{-6} in NMOS trasnistors, and 10^{-7} in PMOS ones [20]. Notice that, as described previously, the PSD is proportional do $\frac{1}{f}$.

2.3.2 Substrate noise coupling

Ideally, the chip substrate presents high conductivity [12], thus ideally not incurring in potential differences in all of its volume. However, in practice, it presents parasitic effects due to material resistivity, homogeneity imperfections, impurities, junctions and others. More specifically, digital circuits can add a significant amount of noise into the substrate, given that the logic state transitions are steep signals. This means they have high derivatives, thereby generating undesired signals due to parasitic capacitances and inductances, since electrical quantities are related in such components by a derivative of one another.

Digital circuits are thus known to their high potential on interfering with analog circuitry in the same substrate. The switching circuits generate noise that propagates through the substrate and are commonly sufficiently high to interfere with the analog circuitry nearby. Analog signals are much more sensitive to noise than digital signals, as many electrical values within a certain range may represent the same logical value in the latter.

More specifically, there are different mechanisms that govern noise injection by an aggressor and reception by a victim. One of those is capacitive injection through reverse biased junctions. The noise injection mechanism into the substrate is a result of the interaction of the digital signal's steep edges and the parasitic capacitances of the MOSFET (see Figure 6). By associating high signal derivatives (edges) with parasitic capacitances, the origin of switching noise comes to sight: current in a capacitor is proportional to voltage variation. Hence, steep signal edges between parasitic capacitances terminals yield substantial undesired effects. In MOS transistors, noise is usually a concern in drains in

digital gates [21]. In those circuits, the source and bulk terminals are kept at ground or V_{DD} , while the drain exhibits switching signal.

Noise is also injected through contacts. It is common that the power supply lines in digital circuits are strongly contaminated with noise. The power supply rails are used to bias the substrate, so the ohmic junction offers a path for noise. Furthermore, it is frequently necessary that contacts are placed in multiple locations across the chip to provide sufficient voltage levels, which also work as more paths to noise injection and affects the substrate more homogeneously [21].

Noise injection, naturally, does not occur if there are no noise reception mechanisms. When subjected to voltage disturbances, junction capacitances exhibit electrical currents. Such disturbances occur typically between the drain and the substrate in digital circuits [21]. Furthermore, the short channels in submicron technologies may result in a larger span of the diffusion depletion regions, in relation to longer channels. This incurs in an overlap between source/bulk and drain/bulk, allowing noise injection into the channel itself.

Noise generation and reception effects are dependent on layout and technology parameters. For instance, consider two devices at a certain distance from each other, in operation. Noise that is originated in one of the devices will be coupled to the substrate and eventually reach the other, in a way that depends on the distance that separates them. Firstly, noise will propagate through the substrate, thus, it is subjected to the material's imperfections. The absolute values of noise magnitude depend on the substrate doping level. For highly doped substrates, there are much more charge carriers and, therefore, a lower impedance throughout the material, in comparison to lightly doped ones. This lower impedance, associated with the connection of a backside biasing contact, offers a path to ground for substrate noise. Highly doped substrates were observed to contain from one to two orders of magnitude less noise than lightly doped ones. If noise cannot find return paths to ground in its propagation through the material, i.e. there is no grounded backplane or contacts to ground impedances are high, it becomes considerably less dependent of distance [21].

2.3.3 Switching noise

The term *Switching Noise* refers to undesired electrical disturbances that are caused by logic transitions in digital circuits. The signal variations observed in one arbitrary point in the substrate are composed by a superposition of the noise generated in each device, and propagated through the chip.

In addition, the switching activity also draws current through the power rails, for each switching logic block. This occurs because the change of logic level involves charging and discharging of capacitances that are experienced by the logic gate output. Usually, these

parasitic effects are the the total gate capacitance of the MOSFET device $C_{gb} + Cgd + C_{gs}$ [9]. The transistors must conduct currents to charge and discharge the capacitances, and these currents are drawn from their source terminals, which are connected to the power rails.

At first, this characterizes switching noise as a deterministic phenomenon. However, the number of noise generating components in a chip is very large, reaching the order of billions of devices at the present date. Therefore, switching noise can be considered a stochastic process, and still lead to useful studies [10].

The behavior of Switching Noise is observed to be comparable to that of Shot Noise [22]. Regarding the probability distribution of the discrete events that compose Shot Noise, it can be approximated by a Poisson distribution [22], whereas a Gaussian is also reported to provide valid approximation [16]. In both approaches, the White Noise spectrum is a common characteristic of those distributions, *i.e.* the instantaneous values are uncorrelated.

2.4 Radiation induced faults

The evolution of CMOS technology comes along with new challenges. Since the improvements are directly related to device miniaturization, phenomena that once could be disregarded must be addressed, in order to maintain system functionality.

Radioactive particles are one cause of soft errors and an increasingly concern as the CMOS technology advances [5]. The origins of those particles are many. To name a few, there are incoming particles from space, daughter particles due to the interaction of those with the atmosphere and decaying elements in IC packages, such as thorium-232 and uranium-238 isotopes. The nature of such particles also vary. They can be neutrons, alpha particles, protons, electrons and cosmic rays [3]. The first observations of radiation induced soft errors occurred in aerospace applications [5]. The energy of the particles are higher at high altitudes, namely, from 10 to 40km [3]. At ground level, these errors were observed only in memory elements. However, in the recent technologies, combinational logic blocks also are affected by radiation [5].

Soft errors can cause system failure or information falsification. Those errors can be called SEUs (Single Event Upsets) or SETs (Single Event Transients), depending on their nature. Both are caused by energetic particles that strike the integrated circuits and induce high levels of charge carrier generation through p-n junctions, which are then briefly short circuited. The fault current process is characterized by two phases, shown in Figure 12. Picture *12-a* shows the p-n junction in its normal configuration, as well as the induced carrier track. The first phase *(12-b)* is the charge collection, which occurs rapidly due to the high energy provision by the particle, and lasts for a few picoseconds.

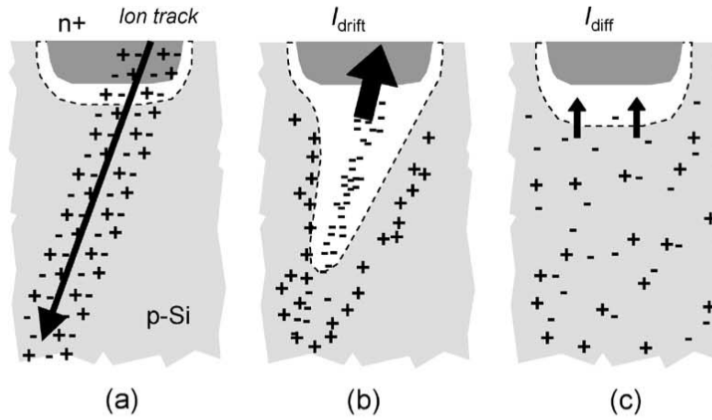

Figure 12 – *Effect of particle strike on a p-n junction [23]. a)Creation of electron-hole pairs track, b)Funnelling and drift current, c)Original configuration and diffusion current.*

It is dominated by the process of drift current (I_{drift} in figure 12). The depletion layer of the p-n junction is drastically distorted, assuming the shape of a funnel and accelerating electron-hole pairs that are in its expansion range, due to its electric field. The second phase *(12-c)* is slower, and is caused mainly by the diffusion process (I_{diff} in 12), during several hundreds of picoseconds [4], as the depletion layer returns to its original form [23]. The duration of the phases are different for each particle type, but lie around the aforementioned order of magnitude [3]. Each of these phases can also be visualized as a current waveform, as depicted in Figure 13.

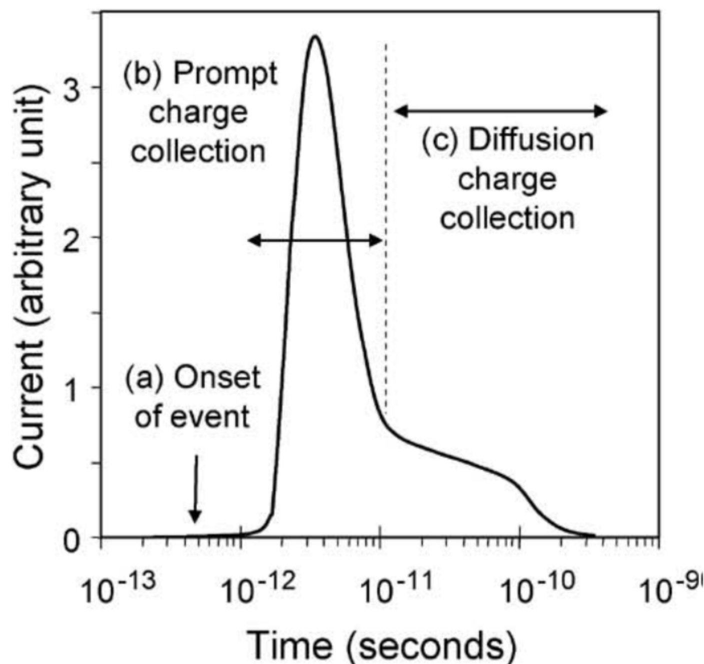

Figure 13 – *Measured profile of a fault current, generated by a particle strike [23].*

2.5 Bulk Built-In Current Sensor

As a solution to detect the fault currents caused by radioactive particle strikes (and hence potential soft errors), the Bulk Built-In Current Sensor (Bulk-BICS) circuit has been proposed. Its placement in a circuit is depicted in Figure 14. In this system, the sensing block is connected between the power rail (V_{DD} or GND, depending on the case) and the bulk of the transistor to be monitored. In this case, Figure 14 shows a monitored NMOS transistor in an inverter, thus, with a connection to GND. In logic circuits, the drain terminal of a MOSFET carries the voltage level that determines the state of the logic gate it composes. Source terminals are either connected to V_{DD} or GND. Therefore, the drain to bulk voltage of a MOSFET dtermines its logic state.

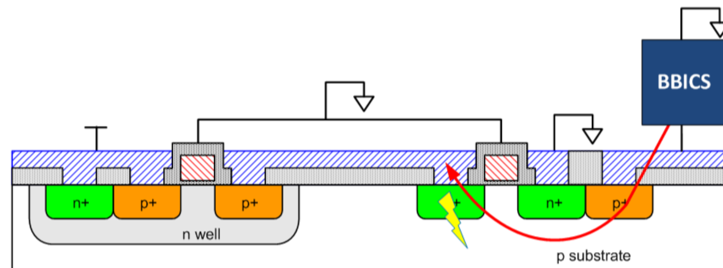

Figure 14 – BBICS placement in a logic gate [24].

To understand the principle that is involved in this measurement, it is necessary to emphasize a few characteristics of the phenomenon the causes the fault. First, the striking particle causes a short duration current through the reverse biased drain to bulk junction of the transistor [25, 26, 27]. This current is composed both by electrons and holes, hence, the fault current constituted by one charge carrier type is accompanied by a reverse current composed by the complementary one. This current is conducted from the transistor's bulk to the power source, and this is the phenomenon that can be measured. Therefore, the fault is indirectly detected, by measuring its side effect.

Notice that if the drain to bulk junction voltage is zero, a particle strike will not change the state of the node, hence, it does not affect the operation of the monitored circuit. On the other hand, if such junction is reverse biased, it may experience a logic state change in the presence of a strike, due to the voltage drop in which it results.

Amongst the several implementations, the mBBICS, shown in Figure 15 represents a promising trade-off between sensitivity to fault currents, response time, robustness and area offset [5]. Further, its basic concept is similar to other BBICS. Hence, it was chosen as representative circuit in this work.

The mBBICS has one topology for monitoring NMOS transistors, and another for PMOS. The NMOS sensor is composed by two functional blocks: the head and the tail (see Figure 15). The head circuits are connected to the bulk of the monitored transistors,

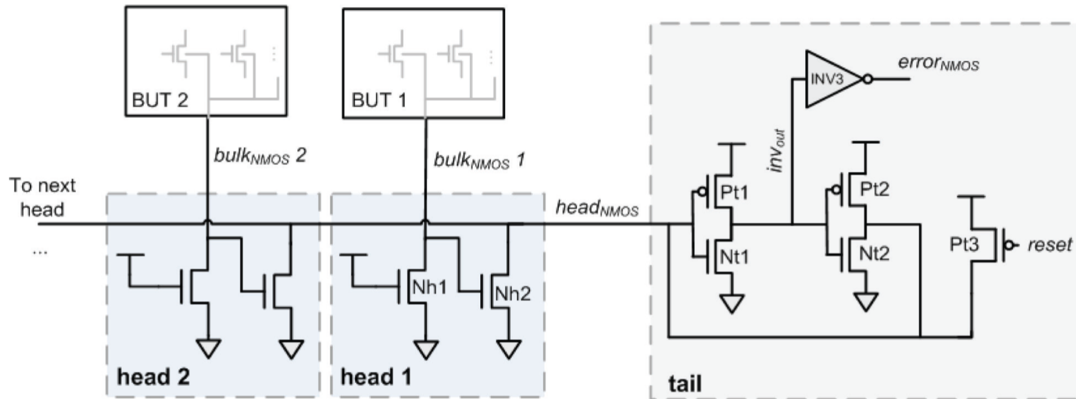

Figure 15 – Modular Bulk Built-In Current Sensor (mBBICS) for NMOS transistors [5]. Notice, in the tail, the latch composed by two inverters, the Reset transistor (Pt3) and the output inverting buffer (inv3). BUT stands for Block Under Test.

while the tail circuit latches the output signal of several head circuits. In detail, the drain of transistor N_{h1} is connected to the bulk of the monitored transistors, its source is at GND, and its gate connected to V_{DD}. In normal operation, the drain of N_{h1} acts as a virtual GND while the drain of N_{h2} is at V_{DD} level. In the event of a strike, the fault current is conducted through N_{h1}. The consequent voltage drop increases the gate voltage of N_{h2}, which is switched on and pulls down the signal *headNMOS* that is connected to the drain of N_{h2} and the input of the tail circuit. The latter latches the input and activates the error flag. The circuit remains in that state, until the reset transistor is activated, causing the circuit to go to initial state and be ready for another detection [5].

Considering that the chip substrate is doped with p-type impurities, one should notice that the circuit would not function for monitoring an NMOS device. Since the transistor's bulk is the substrate itself, the current to be measured would bypass the Bulk BICS's input transistor, which is likely to have a higher resistance than the substrate path. Hence, the monitored circuit should be inside a triple well structure. In that way, the bulk of the NMOS transistor is separate mass from the substrate, electrically isolated. PMOS transistors will not suffer from this issue, since they are isolated from the substrate by construction. Of course, if the substrate doping was n-type, the opposite situation would be true.

The bulk-BICS approach counts on a number of different topologies, namely, the dyn-BBICS [4], which is applicable to dynamic memory cells, the Single-BBICS [26], which uses only one detection circuit for both NMOS and PMOS devices, the Tbulk-BICS [28], capable of having its configuration modified to cope with performance, among others.

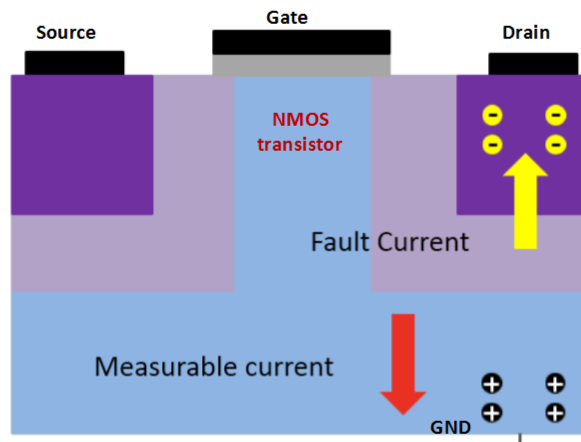

Figure 16 – Fault current, in yellow, and the measured current, in red. The presented structure is an NMOS transistor.

2.6 Related works

There are several related works that explore and propose countermeasures to substrate coupling noise, device noise and their effects in the chip's circuits. However, to the best of the author's knowledge, no other author has previously addressed device and switching noises analyses of integrated substrate sensors. The published works that resulted from the development of this thesis are [29], [30] and [31].

Regarding Switching Noise modeling, an investigation of the validity of a model for switching noise is reported in [32]. Switching Noise is proposed to be modeled as a Shot Noise stochastic process. This relies on the assumption that Switching Noise can be approximated by a statistical phenomenon in a digital chip, even though it is deterministic. Based in characteristics of the switching currents, its PSD can be derived. Such characteristics are obtained from transistor level simulations. The effectiveness of the approach is demonstrated by simulation and experiment results comparison.

The authors of [33] address a similar approach, also statistically modeling the Switching Noise. However, the theory of Markov Chains is used for such. In addition to on-chip generated noise, *Printed Circuit Board* (PCB) and off-chip connections are also considered, by obtaining a transfer function that relates operation switching signals with generated noise. The approach is as well validated by comparing the results of simulations and of a mixed-signal prototype.

Considering substrate modeling techniques, Milan and Krstic' investigate in [13] an estimation approach, to be used before floorplanning, of how noise propagates through the substrate. The technique applies a coarse model for coupling of switching noise through lightly doped substrates. Assumptions are considered in order to achieve feasible modeling, *e.g.*, ground bounces are uniform along the chip. Package parasitics are also considered, and the authors conclude that regular spacing of contacts is a valid assumption in a pre-

floorplanning scenario, comparing models generated with different contact distributions.

Bronckers et al. [34] analyze propagated noise based on the analog operation of a transistor. A framework is developed and applied to an exemplary circuit, resulting in the determination of the dominant substrate coupling mechanism. The conclusion is that there is an optimal value for the ground resistance, below which substrate noise dominates interference in the device, whereas for higher values ground bounce is the dominant coupling mechanism.

In [35], the coupling of noise injected by digital circuits into the substrate is demonstrated to affect MOSFET devices due to variation of the threshold voltage, caused by the potential fluctuations in the substrate. These approaches target the noise influence in signals in the device, and, differently from this work, not in the substrate itself.

In [36], the authors investigate by simulation how noise generated by a ring oscillator through substrate coupling affects the performance of an *analog-to-digital converter* (ADC). The authors use the *Spurious-Free Dynamic Range* (SFDR) as the performance criterion, and observed that the SFDR of a noisy simulation is 5dB higher than the case with no substrate noise coupling. The substrate modeling method is similar to that used in [13].

Similarly, Min Xu *et al* [37] present a study about substrate noise influence in the operation of a *Low Noise Amplifier* (LNA). The digital aggressor signal is emulated, by arbitrarily generating logic level transitions, *i.e.*, no functional digital circuit was used. The authors conclude that the spectral distribution of substrate noise affects its impact in a substantial way. Therefore, even though substrate noise power may be several orders of magnitude higher than signal power, only noise components within particular frequency ranges incur in degradation of the LNA performance.

Wolfel et al. [38] demonstrate a method to reduce the influence of Flicker Noise contribution in the measurement of optical and X-ray signals by a photon detector. The detector used is based on a device which functions as follows: the drain to source current is modulated by the amount of incident photons in the substrate. Such structure is called the DEPFET device. The authors developed a noise mitigation technique that made single photon detection possible (e.g., they show the ability of the sensor to distinguish from 100 to 101 photon-generated electrons). Even though it explores a bulk-signal based device, the approach involves a novel measurement procedure, and not a fault detection system.

Table 1 correlates the aforementioned works with the present document.

Table 1 – Related works correlation.

WORKS	Statistical noise modeling	Substrate modeling	Substrate Noise Coupling	Analog circuits as victims	Flicker Noise in Bulk sensors
[32]	x				
[33]	x				
[13]		x	x	x	
[34]			x	x	
[35]			x	x	
[36]		x	x	x	
[37]			x	x	
[38]					x
This work	x	x	x	x	x

3 Methodology

This chapter focuses on the propositions of hypotheses aimed to investigate how changes in parameters of the mBBICS are responsible for alterations in sensitivity and noise susceptibility. The understanding of such mechanisms allow not only to be aware of the physical aspects that govern the circuit, but also empowers one to propose robustness improvement actions towards the mBBICS. Therefore, the present chapter aims to describe the premises used to compare the effects of fault currents and noise.

It begins by describing the ways in which noise could lead the mBBICS to falsely indicate that a transient fault occurred. Next, the main simulation methodology used throughout this work is explained, which constitutes a non-analytical procedure to determine minimum values. The transient fault and noise waveforms generation procedures to be used in the simulations are detailed.

Once the simulations concepts and workflows are defined, the behavior investigating premises are presented. These comprise time exposure to noise, arbitrary noise waveform injection and propagation, noise generation by switching circuit, transistors dimensions and biasing.

3.1 Impact of noise on BBICS

The principle of operation of the mBBICS challenges its reliability in the presence of noise. The electrical current that flows through the channel of N_{h1} (see Figure 15, on page ??) determines the activation of the sensor, indicating the presence of a possible soft error.

The resulting drain voltage due to device current noise observed in MOSFET devices could, hypothetically, activate the mBBICS. A similar scenario may occur in a digital or mixed signal chip, by the influence of switching noise. Bit transitions that are electrically coupled to the substrate can propagate through the chip and affect the voltage level of the drain of N_{h1}, once again, falsely denouncing a soft error.

Depending on the magnitudes of the fault currents for which the sensor was designed, the resulting noise in the drain of N_{h1} can be negligible, or it can induce unrealistic soft error accusation.

The fault currents caused by particle strikes can be very small signals, with peaks in the order of hundreds of μA and lasting for only tens of ps [25]. A hypothesis may then be proposed that noise could assume values that are comparable to those of the fault currents. It is desired, hence, to investigate how noise can affect the behavior of the circuit.

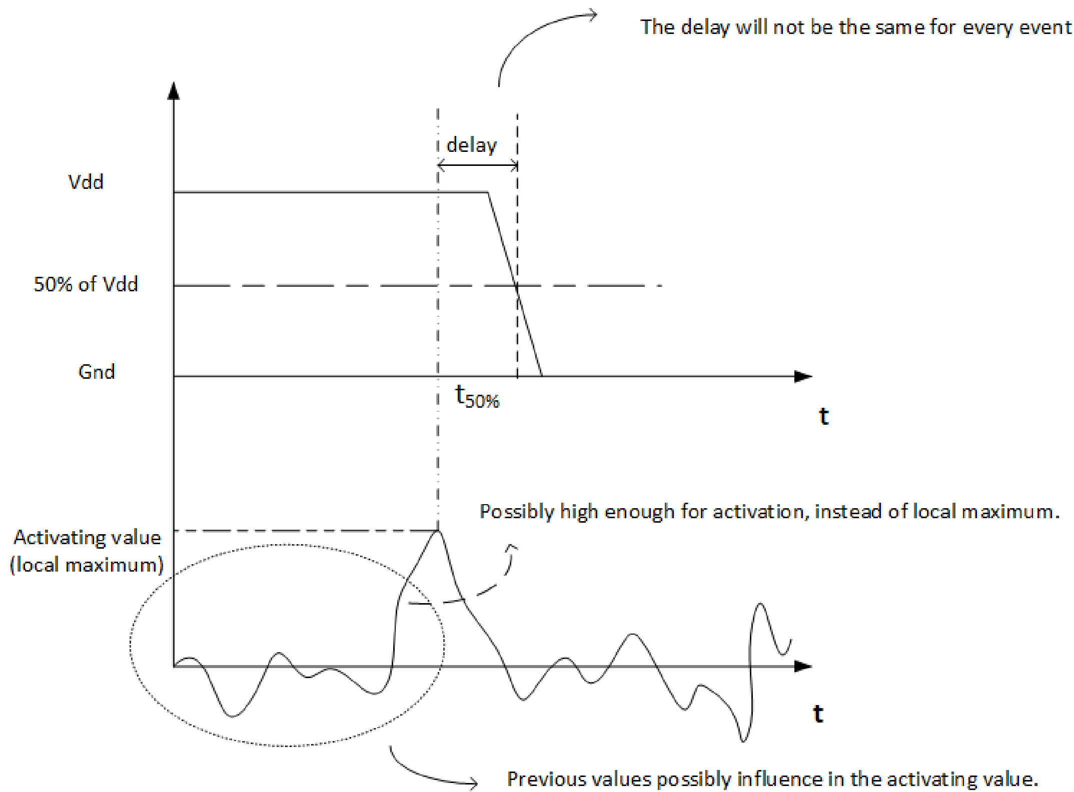

Figure 17 – Inaccurate interpretations for the term *noise value* for mBBICS activation.

If such values are actually reached, the sensor would accuse a fault when there is not, thus degrading the overall system functionality or simply showing itself non-reliable.

Therefore, one way to analyze if the Bulk-BICS is robust to noise or not is to determine the minimum current value for sensor assertion, as well as the minimum noise value for such. The comparison of the results should lead to the conclusion. However, it is not straightforward, given the different nature of the fault current and noise.

The definition of noise value for activation requires a few considerations, depicted in Figure 17. It cannot be a local peak in the noise waveform, because 1) a lower value, and yet high enough, could have flipped the flag or 2) the error flag flip is not instantaneous.

First of all, a more thorough definition is necessary for current value and noise value. The fault current waveform is predictable and has a peak, so the peak current is potentially a good choice to use as the "current value". Noise, however, is not as convenient to analyze.

One possibility would be to consider the local noise maximum as the activating factor, where local would mean the vicinity of the instant when the circuit activates. This instant, in turn, also needs a definition, say, the instant $t_{50\%}$ when the error signal crosses 50% of V_{DD} (given that the error flag signal is digital and can assume only V_{DD} or ground values at steady state). But a problem arises in that framework: the sensor's response is not instantaneous, so one cannot state the noise value at $t_{50\%}$ was in fact the one that

caused the flag flip. In addition, *a priori*, there is no information that allows to assume a time value that, subtracted from $t_{50\%}$, gives the correct or most probable value.

Considering a fixed delay, such as the difference between the instant at which the flag reaches 50% of V_{DD} and the local peak instant also does not pose a solution. This is because there is no guarantee that such difference is constant. On the contrary, it is highly dependent on many aspects of the circuit state.

Furthermore, given that there are parasitic effects such as capacitances, previous values of the waveform may affect the overall behavior of the circuit, making it less or more prone to activation. For example, consider the mBBICS in a time instant where parasitic capacitances are highly charged, *i.e.* previous values are positive. A lower noise swing may assert the sensor, if compared to the mBBICS without parasitics.

Based on the aforementioned scenarios, using an exact noise value, at an exact time instant, is not likely to be a promising technique. A better approach would be to classify "noise value" as an RMS value of noise for which the sensor activates. In that way, there is no longer a dependence on an instantaneous noise value, but it can be numerically distinguished by a single number, which is a function of all of its values. This framework considers that low RMS noise values are consequence of low peaks and low overall values, which justifies a normal operation, thus the sensor should not activate. Analogously, high RMS values are associated with false error reporting. This correlation between RMS and peak values can be considered due to the Gaussian nature of the noise types that are under analysis in this work.

3.2 Simulations workflow

A drawback of the usage of RMS noise values involves analysis complexity. The act of changing the RMS value is not an obstacle, it is sufficient to scale the noise waveform by a constant and feed it to the simulation software. Hence, increasing or decreasing the scaling factor has the same effect in the RMS value. The difficulties arise with the scaling factor *variation*. More specifically, how the value must vary in order to effectively narrow the search for the minimum RMS activating value.

To overcome these, an iterative exploration can be used. Each scaled noise waveform that is simulated will yield either activation or no activation. Consider the result of one simulation, fed by a noise waveform with an arbitrary scaling factor. If activation occurs, scaling values greater than the current one certainly will also activate, thus not leading to the minimum RMS activating value. The search for the minimum value must then continue by decreasing the scaling factor. On the other hand, in a non-activating scenario, the minimum scaling factor for activation is certainly greater than the present one, which must then be increased in order to continue the search.

Furthermore, during a search, a candidate scaling factor can be eliminated in two situations, which will lead to a smaller range of candidates:

- It activates the mBBICS, and the following value in the search also does;
- It does not activate the mBBICS, as well as the following value in the search.

By testing several values and restricting the range progressively, a minimum value for activation will eventually be achieved. An exact minimum value is impractical, due to the number of simulations and computer number representation limitations. Therefore, one possible indicating parameter is the ratio between the activating and non-activating values, minus the unity. The result is the percentage difference between those, and the result is as more reliable as the difference is smaller.

3.3 Signals generation and injection

3.3.1 Transient fault current

The waveform in Figure 13 (page 22) should be used for modeling the effect of a particle strike. However, it would have to be measured and stored as a digital file, which will depend on equipment and facilities which use are outside the scope of this work. Instead, an analytical curve obtained by the sum of two exponentials, one increasing and the other decreasing, with different time constants, is widely used in the literature as an approximation[5, 25, 39]. The curve is represented in Figure 18, which is obtained by 3.1.

$$I_{peak} = \frac{Q}{T_F - T_R} \left(e^{-t/T_F} - e^{-t/T_R} \right) \tag{3.1}$$

Where:

I_{peak} : Fault current
Q : Charge generated by the particle strike
T_F : Fall time
T_R : Rise time

3.3.2 Flicker and White noises

As stated in sections 2.3.1 and 2.3.3, Thermal and Shot noises generated in the channel of MOSFET devices, as well as the Switching Noise are both *White Gaussian Noise* (WGN). Hence, they can be modeled by a Gaussian random variable. Thus, as far as device noise is concerned, both Thermal and Shot noises can be modeled by one single random variable, given that the sum of two Guassian random variables is another random variable. Moreover [15]:

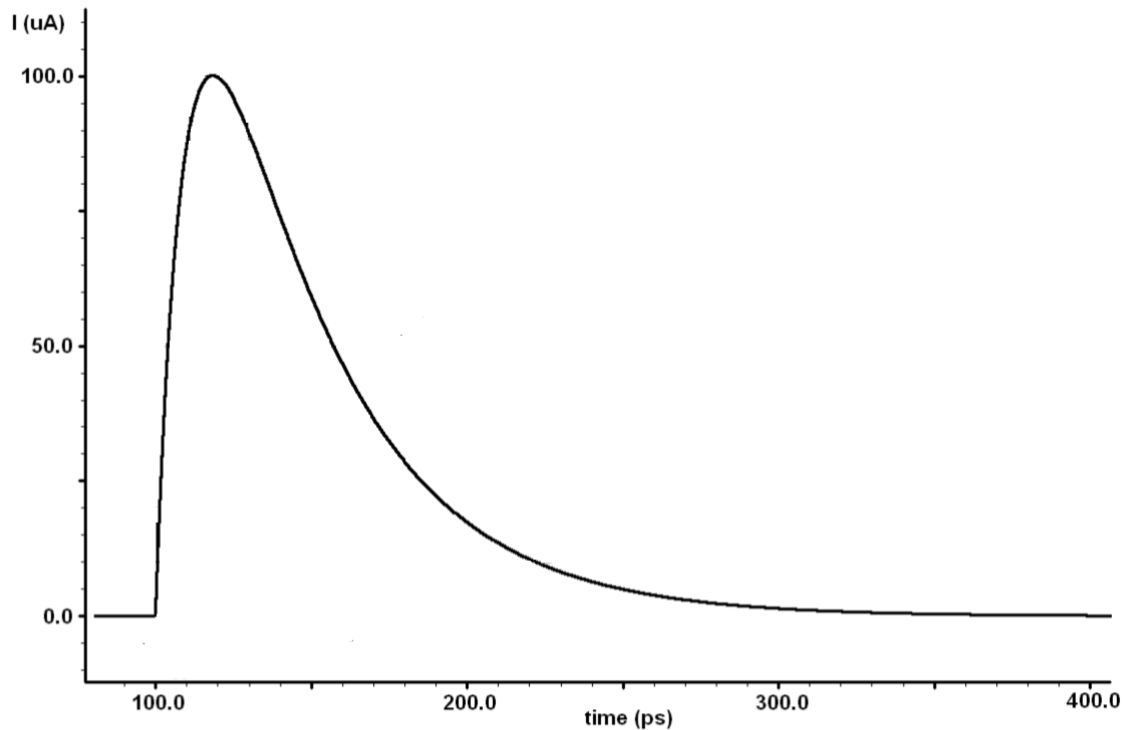

Figure 18 – *Approximated curve used to describe the current that is induced by a radioactive particle strike.*

- the mean of the resulting random variable is the sum of the means of the added ones;
- the squared variance of the resulting random variable is the sum of the squared variances of the added ones;

$$\nu_{WGN} = \nu_{thermal} + \nu_{shot} \tag{3.2}$$

$$\mu_{WGN} = \mu_{thermal} + \mu_{shot} \tag{3.3}$$

being ν the variance and μ the mean of the random variables.

One approach that can be used to model Flicker noise (in fact, any correlated type of noise) is to apply the WGN to a *Linear Time Invariant* (LTI) system, more specifically, to a sequence of filters [40], as represented in Figure 19. The output of the filter comprises the category of colored noise, since it no longer presents all frequencies with the same power density. Flicker noise is compounded by a specific spectral shape, as are other different types of colored noise, and that shape is what defines each.

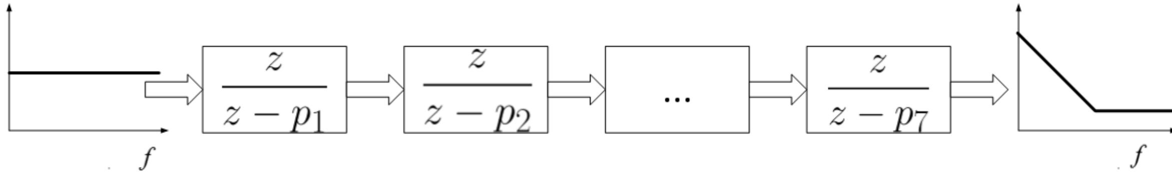

Figure 19 – *WGN filtering to obtain Flicker Noise.*

To obtain Flicker Noise from WGN, the technique is to use a number of cascaded first order filters, shaping the frequency response to a drop of 3 dB per octave [41] by alternating poles and zeros accordingly. Only one filter cannot be used, since its magnitude frequency response decreases 20 dB per decade, which is much steeper than that of Flicker Noise. Notice that the carefully placed zeros compensate the respective previous poles' effects, keeping the frequency response from absolutely increasing its inclination and disrupting the linear drop characteristic. Figure 20 illustrates the effect of cascading four first order filters (straight line), as well as the effect of each filter separately (low-pass characteristics).

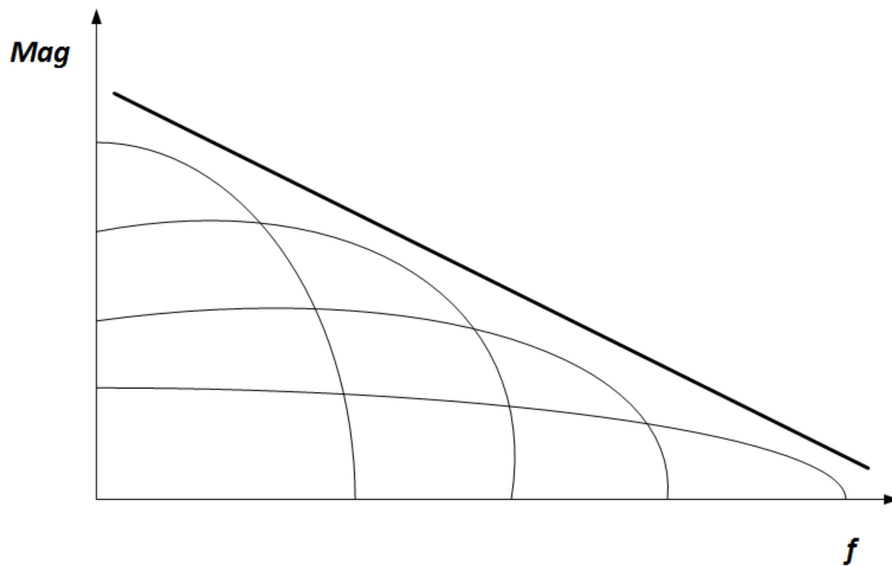

Figure 20 – *Individual frequency responses of the filters that, when summed, lead to the overall filtering effect that will define the Flicker Noise PSD. Frequency and magnitude are qualitative.*

3.4 Influence of simulation time

All the simulations presented in this work were performed with a stop time of $1\mu s$. One could question if this duration is sufficient to draw reliable conclusions about the noise susceptibility of the Bulk-BICS, given that it has a stochastic nature. In other words, it is possible that less probable signal swings in the noise waveform could not have happened due to insufficient duration, thus masking possible rare but important events. Therefore,

the validity of the results can be verified by performing a set of the same simulations again, for different stop times. If the results are not significantly different, then the simulations until now realized are valid in terms of simulation time span. Figure 21 shows a case in which a simulation of 600 ns would not cause sensor activation, whereas one of 1 μs would, for the same circuit.

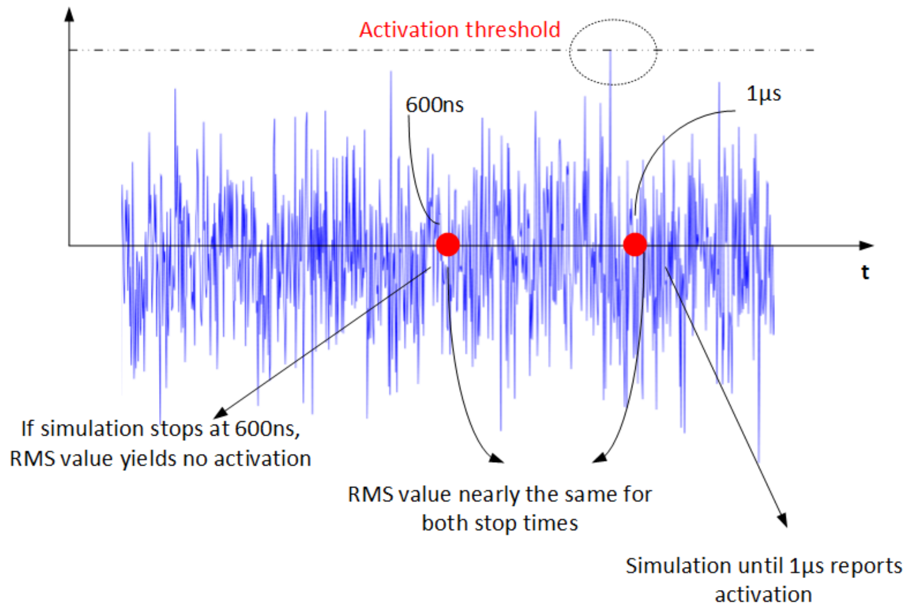

Figure 21 – *Impact of simulation time in the mBBICS noise analysis.*

The noise waveform characteristics pose an issue when considering different simulation times. If different stop times will be used, only part of the waveform has to be injected, namely, from zero to the new stop time (*e.g.*, from zero to 600ns in Figure 21). Otherwise, the spectral content of the applied noise would change, and the comparison would not be valid. For higher stop times, an additional part of the noise waveform would have to be attached. Despite it is not a problem for White Noise, given that any signal swing is possible (noise values are not correlated), it can introduce an event that would not happen in a single Flicker Noise generation, since the samples are correlated. Hence, the best approach is to determine the longest waveform to be used and take only parts of it to simulate the lower duration simulations. For example, generate a 1 μs long noise waveform, consider the simulation with stop time 1 μs the original case (longest noise waveform) and compare with the results for the stop times 100ns, 400ns, 600ns and 800ns. If a high enough peak for activating the mBBICS occurs only at 800ns, one can conclude that simulations of 100ns, 400ns and 600ns would not be enough to verify that the noise RMS level is actually capable of activating the error flag.

3.5 Substrate noise conduction

As highlighted in section 2.3 undesired currents and voltages can propagate through a chip's substrate, affecting circuit blocks that are sensitive to them. Such phenomenon is an especially hazardous issue in mixed signal circuits. A substrate electrical model can be used to predict, up to a certain accuracy, in which intensity noise reaches a victim circuit block, given the location in which it was generated.

In order to make use of such substrate model, a signal can be applied to a substrate contact, thus emulating a noise injection. A contact in another region of the chip can have its voltage acquired, and by comparing the injected and the obtained noise values, one can estimate quantitatively how noise degrades with distance.

Therefore, if one has both the introduced and the resultant noise RMS values, the ratio between the latter and the former can be used as an indicating parameter for noise degradation. By doing such for a set of injection-to-measurement-point distances, it is possible to obtain a curve that indicates the relative intensity of noise in different points on the substrate, given a noise generating point. Thus, the cumulative noise in a certain point can be estimated, by adding the contributions originated from different noise sources.

3.6 Dimensions of N_{h1}/P_{h1}

Transistors N_{h1} and P_{h1} are define on Figure 15, on page 24. One circuit parameter to be approached is the input transistor N_{h1}'s length, henceforth L_{Nh1} (see Figure 15). In the case of the PMOS mBBICS, those are referred to as P_{h1} and L_{Ph1}, respectively. From this point on, for the sake of simplicity, the focus of descriptions will be the NMOS version of the mBBICS. The descriptions presented are to be analogously applied to P_{h1} as well, unless if explicitly mentioned not to.

As stated in previous sections, N_{h1} functions as a resistive load, whose voltage should lead to error flag assertion or logical state maintenance. By increasing L_{Nh1}, the voltage drop between drain and source should be higher for a specific fault current, consequently, to a specific particle strike. In other words, fault currents are, for this analysis, considered to be fixed at a minimum value for causing a soft error. Lower values, therefore, do not cause soft errors, whereas higher current values do.

The downside of exploring sensitivity improvement by increasing the channel resistance is that the voltage drop caused by current noise will also yield higher voltage values. However, it is valuable to emphasize that the induction of fault currents by particle strikes have different mechanisms than noise generation. Hence, it is possible that sensitivity and noise susceptibility vary differently as N_{h1}'s length is modified. If they behave as such, there is the possibility of existence of optimal values for L_{Nh1}, which are consequences

of the best relative behavior of activations by particle strike and noise in face of device length alteration.

3.7 Transistors biasing

3.7.1 Gate to source voltage

It was already verified that the channel resistance of N_{h1} / P_{h1} has direct influence on its drain voltage in the presence of device channel current noise. In addition to device length modification, there is another parameter of the mBBICS that, when altered, affects the channel resistance: the gate to source voltage V_{GS}, and by varying it and maintaining the length of the device, the drain voltage also varies, for a given I_{DS} (see equation 2.2 and Figures 22 and 23). As previously stated, the input transistor N_{h1} / P_{h1} is operating in the linear regimen, which means that the drain current I_{DS} is proportional to the drain to source voltage V_{DS}.

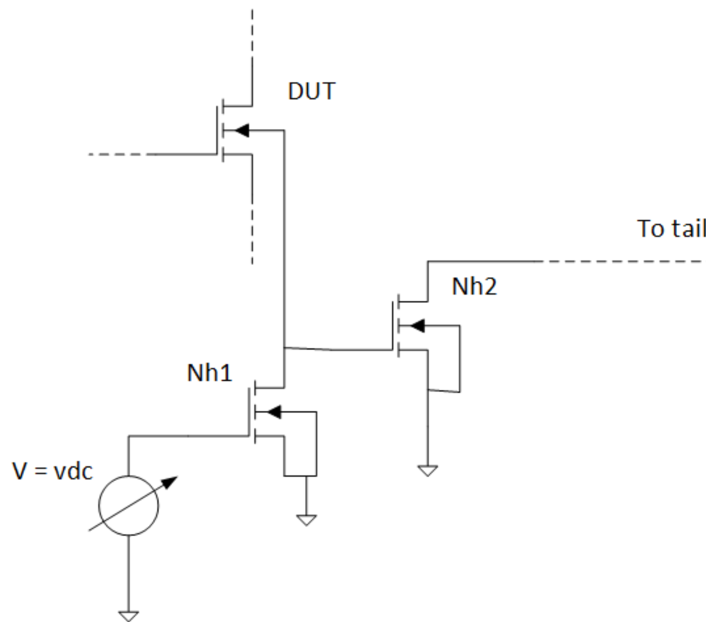

Figure 22 – *Schematic for simulating variation of V_{GS}, N-type mBBICS.*

As in the case of varying L_{Nh1}, decreasing the susceptibility to noise by making V_{GS} lower (V_dc in Figures 22 and 23) should diminish the sensor's sensitivity. However, it is not known in which manner sensitivity and susceptibility alter with V_{GS}, which could be explored in order to determine if one is less or more penalized than the other with V_{GS} variation. This may bring new capabilities in terms of design trade-offs.

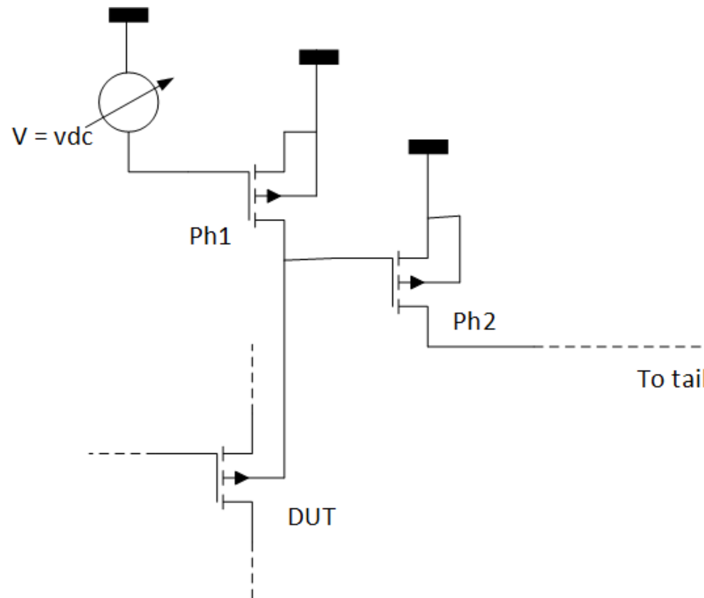

Figure 23 – *Schematic for simulating variation of V_{GS}, P-type mBBICS.*

3.7.2 Body biasing

Transistor N_{h2}/P_{h2} also participates in determining how sensitive the circuit is, by its V_t value. The threshold voltage V_t, in turn, can be modulated by varying the source to bulk voltage, V_{SB}, accordingly. This occurs due to the body effect, which is governed by equation 2.10 for the NMOS transistor and by equation 2.11 for the PMOS transistor.

By analyzing equation 2.10, if V_{SB} is increased, the threshold voltage should also increase. Hence, one way to improve the sensitivity of the mBBICS is, then, to decrease V_{SB}. Once again, the comparison between the effect in sensitivity in face of that in noise susceptibility should result in valuable information for design choices. The analysis for the P-type mBBICS is complementary, therefore, the voltage that should be decreased to improve sensitivity is V_{BS}. The schematic for such simulations can be seen in Figures 24 and 25.

3.8 Load effect on BBICS

Consider the following situation, in which it is desired to monitor logic cells for transient faults. For the sake of simplicity, assume the monitoring of the NMOS transistor of several inverter circuits. To monitor a device is only justifiable if it is in the cut-off state, as described in section 2.5. Therefore, the inverter will be simplified by showing only the NMOS transistor, *i.e.* the only one that is susceptible to a transient fault, with input at low logic value (GND) and drain voltage V_{DD}, with respect to GND. This can be seen in Figure 26.

By referring to Figure 6 and considering the described configuration, one can

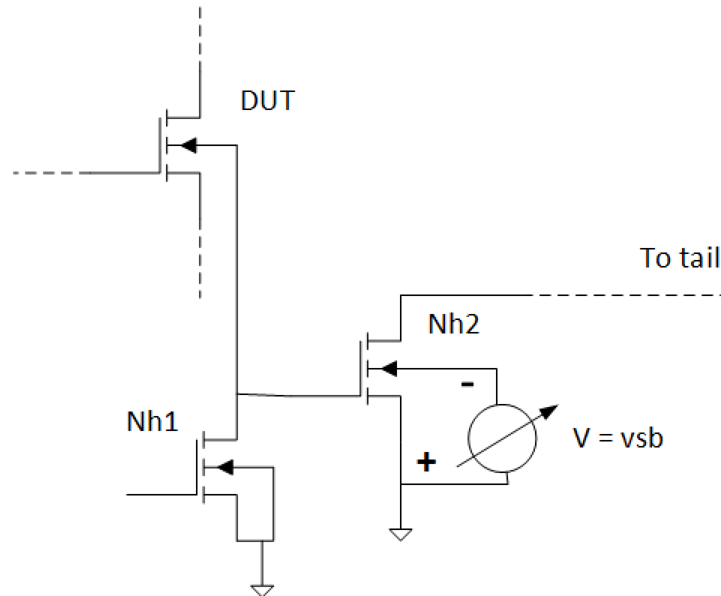

Figure 24 – *Schematic for simulating variation of V_{SB}, N-type mBBICS.*

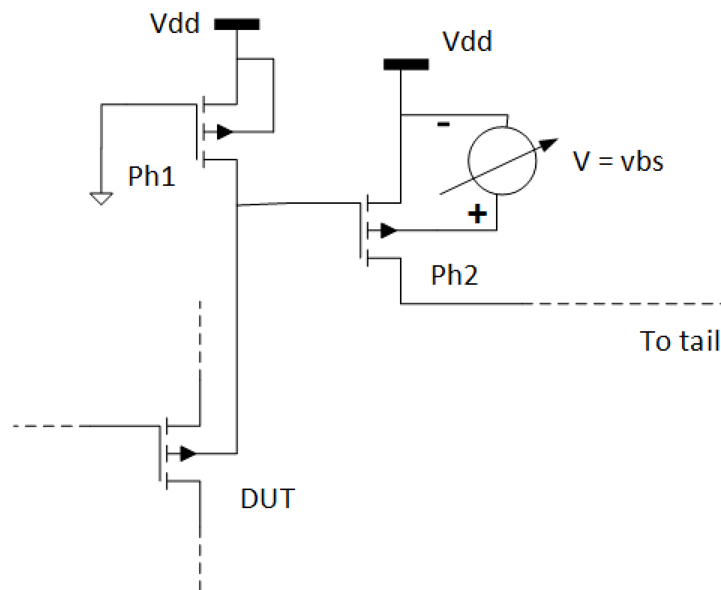

Figure 25 – *Schematic for simulating variation of V_{BS}, P-type mBBICS.*

acknowledge that:

- C_{gs} is disregarded, because the Source and Gate terminals are at the same voltage;
- C_{gd} presents a constant potential difference of V_{DD} between Gate and Drain;
- C_{db}, C_{sb} and C_{gb} are connected to the Bulk terminal, which will have its potential altered as a result of a wavering current (noise) and the resistive behavior N_{h1}. Hence, they are in parallel from the Bulk's point of view, being then able to be expressed as one capacitance. Such capacitance's value is the sum of C_{db}, C_{sb} and C_{gb}.

Another important acknowledgement to be presented in this section is that multiple NMOS transistors of inverters, being monitored by the same mBBICS, are in parallel, since their Bulk terminals are short circuited. This is represented in Figure 26 by the dashed arrows, which indicate the same voltage drop, *i.e.*, the Bulk terminals of all load transistors and the drain of N_{h1} are the same node, thus, have the same potential with respect to GND. Therefore, the overall capacitance seen by the input of the mBBICS (N_{h1}) is the sum of the equivalent capacitances of each monitored device.

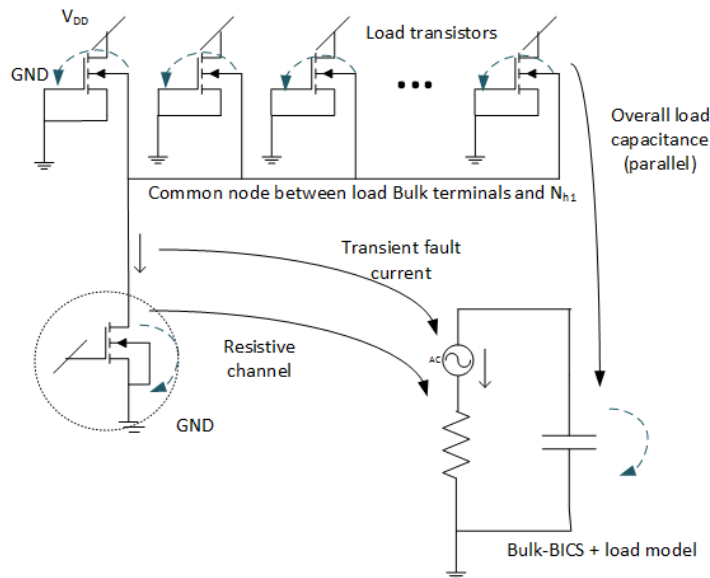

Figure 26 – *Effect of including monitored transistors in one mBBICS.*

These observations lead to the hypothesis that the voltage drop to take place across N_{h1}'s channel due to a transient fault current can be attenuated by this load capacitance, which is in parallel with the channel resistance and opposes to voltage variation. Since the voltage drop through the channel is responsible for activating the sensor, it could be possible that, by adding load to the mBBICS, device noise could be mitigated, simultaneously addressing the issue of area budgeting of the circuit. In other words, the more load devices that are connected to one mBBICS, the better it is to the area budget of the circuit. Figure 26 presents a model for the configuration, where the resistance represents the N_{h1}'s channel, the capacitance represents the overall parasitic capacitance of the load and the current source represents device noise. Notice that the voltage drop between the current source is always zero, since the transient fault is composed only by current.

Despite these advantages, one could expect that the transient fault should also be attenuated. A fact that contributes to this affirmative is that transient faults usually last a few hundreds of *ps*, thus, present steep swings and, as a consequence, high frequency content. The resulting voltage should experience attenuation due to the capacitive reactance of the load parasitic effects.

4 Analysis of impact of noise on mBBICS

In the last chapter, hypotheses brought by the questioning of the mBBICS's behavior in the face of noise were discussed. This chapter covers the means by which such hypotheses were verified. First, the simulation environments are described. Afterwards, the text focuses on the conceptualized simulations, and how they correlate to the investigations propositions. It is verified how the mBBICS behaves in the presence of directly applied noise, both device and switching. Then, the switching noise that is propagated through the substrate is verified, as well as its potential of activating the mBBICS. After this verification, a switching circuit is simulated, with the substrate modeled, and the noise that is injected into the substrate is analyzed. Finally, the results obtained by changing the simulation time are presented.

4.1 Simulation environment

The simulation environment to be described consists in a circuit schematic and layout, developed in design software widely used in the semiconductor industry.

The design of the mBBICS was separated in this work in the head and the tail components. Each of those was implemented as a schematic and represented by a symbol in the software, *i.e.* a circuit block to be used in other schematic files, eliminating the need to remake the transistor description of head and tail repeatedly.

Once the symbols for the head and the tail are made, they are interconnected in a third schematic file, known as the *testbench*. In the testbench, the electrical stimuli are applied to the circuit, namely, the biasing sources, the fault current source, when applicable, and the noise current or voltage sources, depending on the case (this is both for device and switching noise, there is no distinction between them as far as the testbench is concerned).

The testbench simulation validates the circuit's functionality and, once it is done, the designer can proceed with the physical implementation. This is made by combining geometries in different layers, which ultimately correspond to the physical structures of the integrated circuit. Figures 27 and 28 show the layout of the physical implementation of the NMOS and PMOS mBBICS, respectively.

The last procedure to be executed with the design software is to include in the circuit the electrical parasitic effects introduced by interconnects, junctions, and many other entities of the circuit. The tool is also capable of extracting the substrate parasitics, which is the procedure used in the simulations hereby presented. The output of such tool

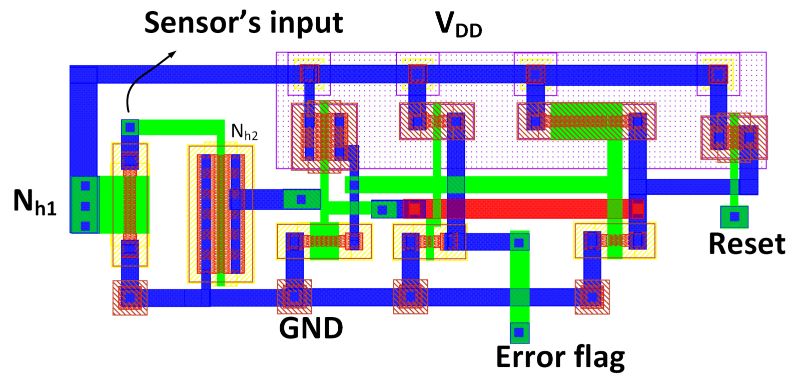

Figure 27 – Layout implementation of the NMOS mBBICS.

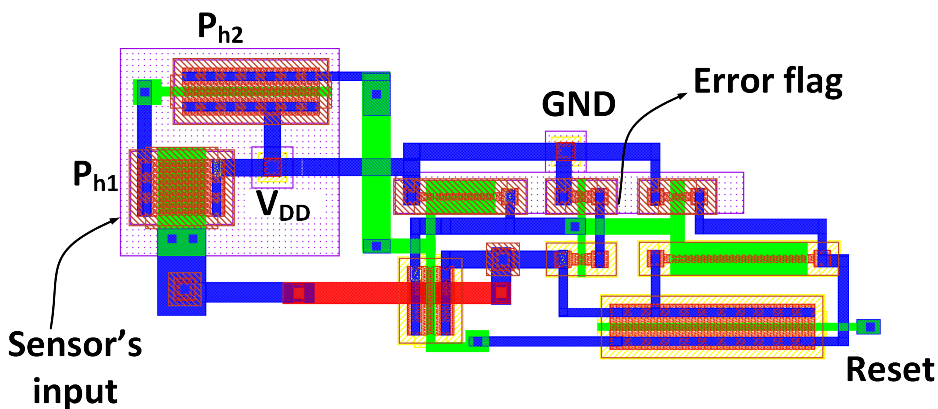

Figure 28 – Layout implementation of the PMOS mBBICS.

is a schematic to be simulated, with the circuit and substrate parasitics included. It was chosen to extract only the substrate parasitic effects in this work, because it is intended hereby to analyze the influence of those alone.

In the subsequent sections, the values of the sources, as well as those of the mBBICS's transistors, are to be progressively varied, so as to verify the sensor's behavior alterations in the occurrence of those. These variations are those described in chapter 3, and are the implementation of the hypotheses thereby presented.

4.2 Analysis of BBICS susceptibility to noise

To verify how the mBBICS can have its functionality affected by noise, the latter was applied directly to the sensor's input transistor, N_{h1}/P_{h1}, and activation of the error flag was checked. As stated in section 3.2, the noise waveforms were progressively rescaled, until reaching a point where the activating and the non-activating values differ by less than 1%.

The simulations were performed for both device and switching noises, and for the

NMOS and PMOS monitoring mBBICS. For the verification of device noise, the noise injection was made by the means of an independent current source, with one terminal connected to ground, and the other connected to the drain of N_{h1}/P_{h1}, since device noise is characterized by current generation in the channel. Both WGN and Flicker Noise were simulated, the former representing Thermal and Shot Noises. For switching noise, only WGN was simulated, since it is modelled as Shot Noise. It was introduced by a voltage source connected between GND and the drain of the input transistor, given that switching noise is commonly treated as voltages throughout the substrate in the literature [10],[42].

The injected noise waveforms were previously generated in MATLAB. One waveform was generated for WGN, and another for Flicker Noise. The technique for generating those was that described in section 3.3.2, which is followed by the storage of the generated waveforms in *comma separated values* (CSV) files, and the waveforms are included in the circuit by the means of a *piecewise linear*, described in a *file* (PWLF) voltage or current source.

The results for minimum activating RMS values are shown in Tables 2 and 3. The letter F means Flicker Noise, W means WGN, I indicates that the noise waveform was injected as current, and V, as voltage. For noise injected as current, the RMS of the resulting noise voltage waveform was considered. The values are in terms of V_{DD}, for easy eventual comparison with systems in other operating voltages.

Table 2 – Minimum RMS voltage at the drain of N_{h1} for sensor activation.

Noise type	Minimum RMS for activation (% of V_{DD})	Peak (mV)
F-I	6.4	165.3
W-I	5.1	238.4
W-V	4.9	319.3

Table 3 – Minimum RMS voltage at the drain of P_{h1} for sensor activation.

Noise type	Minimum RMS for activation (% of V_{DD})	Peak (mV)
F-I	7.7	972.3
W-I	6.5	823.8
W-V	8.7	727.4

In related works, switching noise was reported to reach similar values for the same technology and operating voltage. In [42], the operation of a PLL was simulated and noise peaks at its vicinity reached up to 90.9mV in a time domain analysis. In the results here presented, 4.9% of V_{DD} corresponds to $58.8mV$, which is an RMS value. The highest peak value registered in the simulation for switching noise is $319.3mV$, which is less than one order of magnitude higher than the reported one. Therefore, two conclusions can be drawn hereby. At first, the noise peak responsible for mBBICS activation is higher from the

reported measured values. Nevertheless, considering that many variables, such as circuit topology, complexity, transistor sizes and parameters, can be different between compared works, it is plausible to assume that switching noise influence on mBBICS functionality should not be disregarded at design time, given the magnitude of the difference.

It is also important to verify if the same is true for device noise. Based on equation 2.12, the PSD for thermal noise voltage can be described in terms of the channel resistance, assuming the place of γ and g_m, yielding:

$$v_{TN}(f) = \sqrt{4k_bTr_{ds}}\frac{V}{\sqrt{(Hz)}} \tag{4.1}$$

Where:

S_{TN} : Power Spectral Density of Thermal Noise
k_b : Boltzmann constant
T : Temperature
r_{ds} : MOSFET's channel resistance

The thermal noise waveform used in the simulations in this work was generated by sampling a Gaussian PDF every $1ps$. Therefore, according to Nyquist's Sampling Theorem, this waveform is composed of frequencies up to one half of the sampling frequency:

$$f_S = (10^{-12}s)^{-1} = 1THz \tag{4.2}$$

Where:

f_S : Waveform sampling frequency

$$f_{MAX} = \frac{f_S}{2} = \frac{1THz}{2} = 500GHz \tag{4.3}$$

Where:

f_S : Waveform sampling frequency

Therefore, one can notice that the Thermal Noise PSD goes as far as $500GHz$ in frequency, as it cannot be infinite in real systems. The RMS power in the channel can be calculated by the area under its PSD along frequency, from zero to $500GHz$. Hence, the RMS voltage of the Thermal Noise waveform in the time domain is the square root of the power PSD:

$$v_{TH,RMS} = \sqrt{4 \cdot 1.38 \cdot 10^{-23}\frac{J}{K} \cdot 300K \cdot 100 \cdot 10^{-3}\Omega \cdot 500 \cdot 10^{9}Hz} = 287.8\mu V \tag{4.4}$$

Where:

$v_{TH,RMS}$: RMS value of Thermal Noise voltage

Regarding Shot Noise, notice that it only happens if a current is flowing through the transistor's channel (refer to equation 2.13). However, by definition, the current in the channel, and thus through the source-bulk and drain-bulk junctions, is zero in the context of the presented analyses. Therefore, Shot Noise shall not be considered.

As can be seen in tables 2 and 3, Thermal Noise values (W-I) that are necessary to activate the mBBICS are three orders of magnitude higher than the approximate calculated level in 90nm devices. Nevertheless, technology scaling is historically known to has a high potential of worsening the noise characteristics of devices. Thus, the Thermal Noise accountability may be justified in more advanced nodes, that eventually present higher noise values which, in turn, threaten the mBBICS functionality.

Considering the Hooge model (equation 2.3.1) to verify if the values found for Flicker Noise are usual, one should then integrate it over frequency.

The Hooge empirical parameter presents the order of magnitude of 10^{-6} as mentioned in section 2.3.1 for NMOS transistors, while C_{OX} has typically one of $10^-2\frac{F}{m^2}$ for 90nm devices [43]. Considering that V_{GS} is 1.2V, W and L are typically 180nm in this work, and V_t is verified in simulations to be approximately 200mV:

$$S_F = \frac{1.6 \cdot 10^{-19}}{10^{-2}} \frac{10^{-6}}{(180 \cdot 10^{-9})^2}(1.2 - 0.2) \cdot \frac{1}{f} = 493.8 \cdot 10^-12 \cdot \frac{1}{f}\frac{A^2}{Hz} \tag{4.5}$$

The Flicker Noise RMS value can be obtained by integrating such curve in frequency. For the sake of simplicity, the lower integral limit was chosen to be 1Hz, and the high limit, 1kHz, which is an usual value for Flicker Noise's corner frequency [44],[45]. Since the integral of $1/f$ is $ln(f)$:

$$A_{F,RMS} = \sqrt{49.4 \cdot 10^{-12} \cdot (ln(10 \cdot 10^3) - ln(1))} = 21.3\mu A \tag{4.6}$$

Where:

$A_{F,RMS}$: RMS value of Flicker Noise

If one multiplies that RMS current by a typical value of channel resistance, $1m\Omega$, the result will be 21.3nV RMS, which again is orders of magnitude lower than the activating values.

4.3 Substrate noise injection and propagation

As stated in section 2.3, digital circuits can introduce noise into the substrate. This noise will propagate throughout the silicon, eventually reaching sensitive circuit elements, such as analog parts. It is intended, thus, to verify how noise can propagate from a certain point in the substrate, and if, after the traversal, it can or not activate the mBBICS.

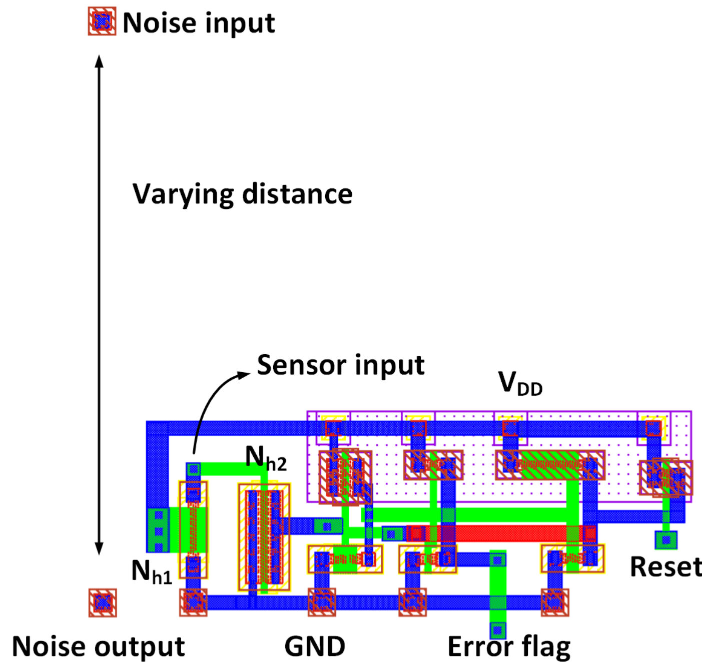

Figure 29 – Layout configuration for noise injection and propagation analysis. Injection and measurement at the substrate.

To the simulation workflow described in section 4.1, was added one action: two extra substrate contacts were included in the layout, one very close to the mBBICS's input, and the other, at an arbitrary distance. This distance was varied, and noise injected in the substrate contact and measured on the one that is close to the input, *i.e.*, after it traverses the distance in the substrate. By adjusting the input noise waveform until it reaches a sufficiently close value to the ones found in section 4.2, one can determine the minimum RMS noise that has to take place at a certain distance from the mBBICS and activate it.

It is important to state that this investigation aims to determine the necessary noise level for error flag activation, therefore, depending on the distance, the RMS value of such noise may be higher than V_{DD}.

The result can be found in Figure 31. Notice that for distances as far as $50\mu m$, the propagated noise RMS value is already 47% of the injected one, *i.e.*, 53% of the injected noise was attenuated. As expected, the minimum injected noise magnitude for sensor activation increases with distance. From ca. $75\mu m$ to $100\mu m$, the curve shows a decreasing characteristic. This can be explained by to the fact that for distances as far as that, the

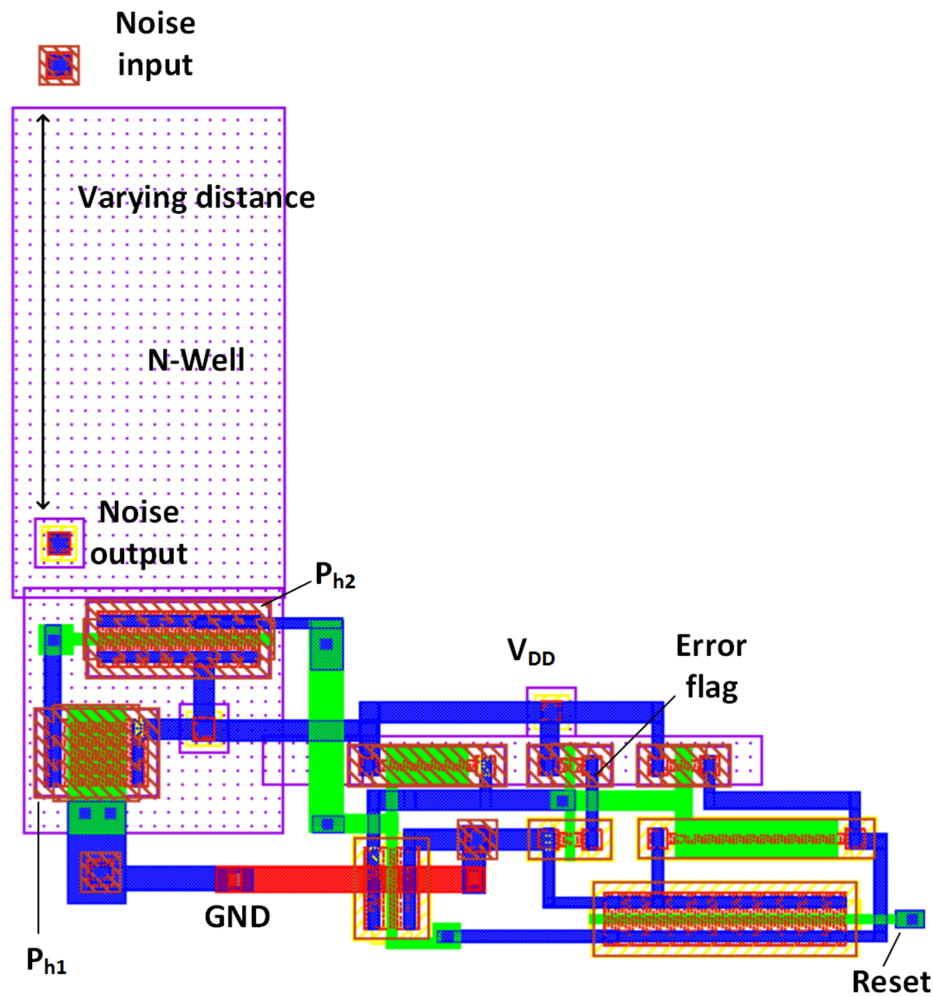

Figure 30 – Layout configuration for noise injection and propagation analysis. Injection in the substrate and measurement at the N-Well.

injected RMS noise has to be so high that the simulated devices leave the linear region of operation, although they continue to be treated as linear by the tool, as it cannot do differently. This conclusion was obtained by referring to error messages from the simulation software.

This simulations was also executed for the PMOS mBBICS, by injecting noise at the substrate and measuring it at the N-Well. Even for the shortest distances, an unrealistic level of noise had to be injected for sensor activation, in the order of tens of V RMS. This is due to the fact that the N-Well, together with the substrate, form a reversed biased PN junction, therefore, switching noise is unable to significantly affect a circuit inside an N-Well.

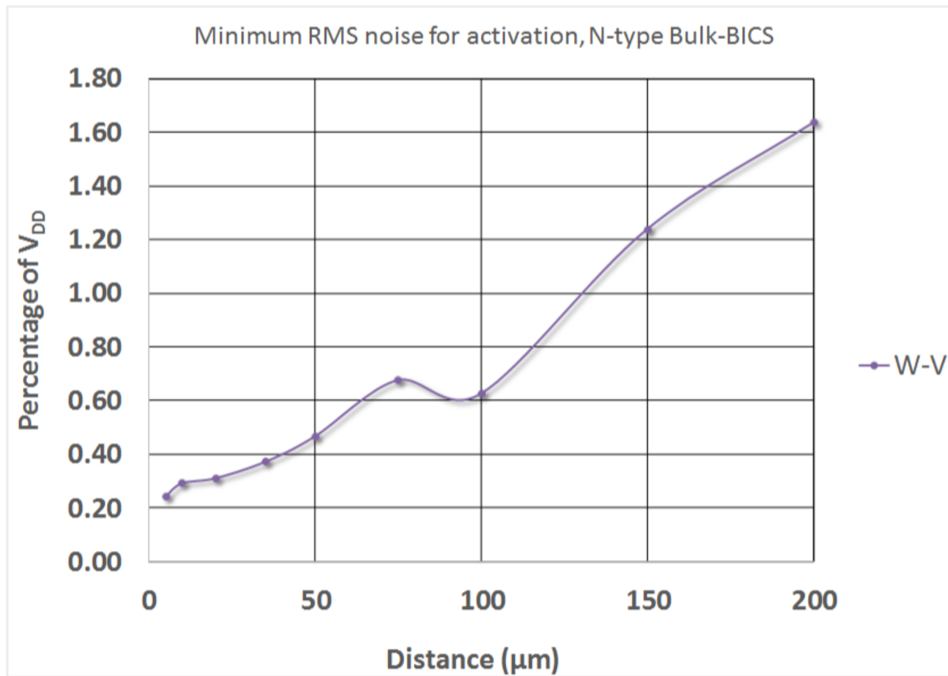

Figure 31 – Simulation results for the injected noise propagation, emulating switching noise.

4.4 Noise induced by switching activity

Previously, an arbitrary noise waveform was injected in a point in the substrate. In this section, noise was not injected as a mathematically generated signal, but by using the design tool's device and substrate models. Those models implement the parasitic effects of the MOS device, and with the input square wave, inject noise into the substrate. In addition, its propagation is also to be analyzed. In order analyze noise propagation, a circuit composed of ten inverter chains, with ten inverters in each chain (*i.e.*, 100 inverters in total) was designed, and a switching signal was applied to each chain. The switching signal is the same for every chain, however, with a different phase shift for each one. It is expected, then, that the switching activity will inject noise into the model of the substrate extracted by the design tool, and that noise will propagate to a certain distance.

As in the previous section, a substrate tap was located in a central position of the layout, so it is possible to investigate noise coming from multiple sources and adding up in the measuring point. The closest distance from the tap to an inverter is 3μm, while the farther is approximately 30μm. An n-well tap was also placed in the most central possible position inside the n-well, to observe how noise behaves inside it. For the N-well tap, the distances are similar.

It is also intended to verify if the layout disposition of inverters can significantly influence the noise that propagates to a certain point. Therefore, three different layout topologies of the same circuit are proposed hereby. Given their visual characteristics, they

are named *rectangular inverter chains* (because of the rectangular distribution of the transistors), *stacked inverter chains* (because the inverter chains are distributed in two stacks of five chains) and *back-to-back inverter chains* (back-to-back meaning that pairs of inverters are symmetrically positioned in relation to the N-well). The three configurations are presented, respectively, in Figures 32, 33 and 34. The rectangular inverter chain's representation (Figure 32) details the inverter layout of the circuit.

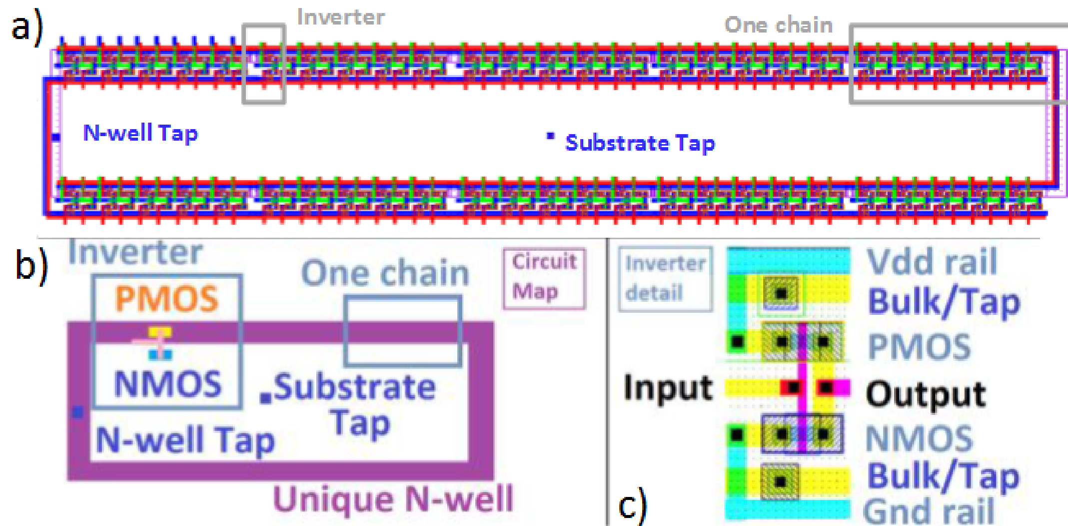

Figure 32 – Rectangular arrangement of inverter chains. a)Layout, b)Circuit map, c)Inverter detail.

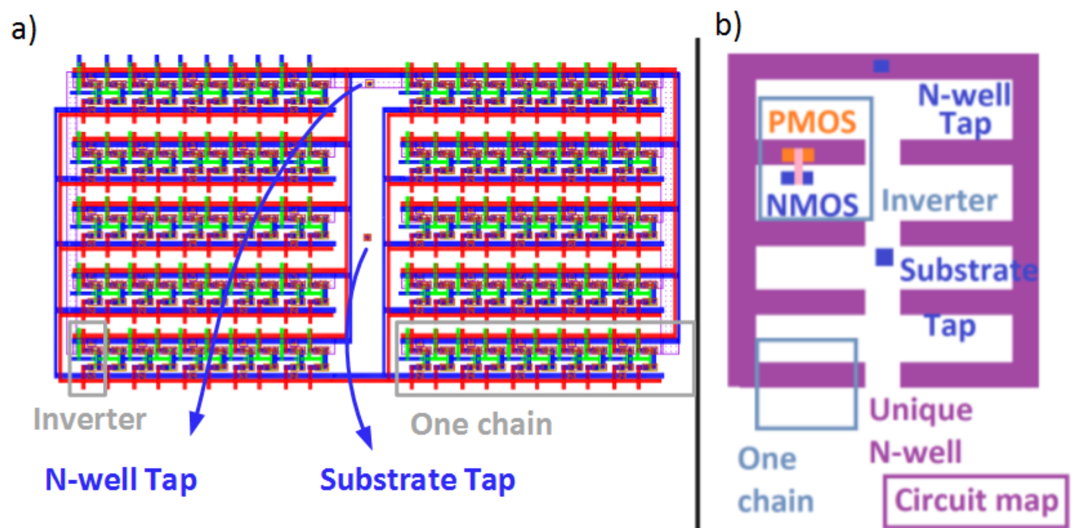

Figure 33 – Stacked arrangement of inverter chains. a)Layout, b)Circuit map.

For each of the inverter chains configurations, the noise injection and propagation is to be analyzed as depending on two factors:

- The frequency of the stimulus signal. Frequencies simulated were 500MHz, 750MHz,

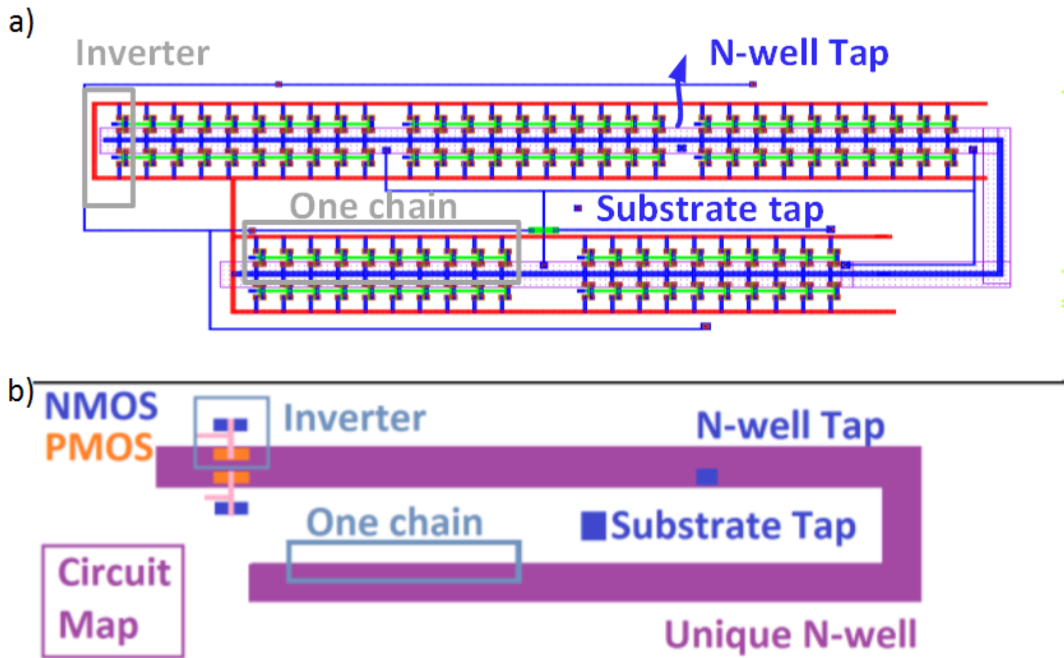

Figure 34 – Back-to-back arrangement of inverter chains. a)Layout, b)Circuit map.

Table 4 – RMS noise values in % of V_{DD} at the substrate tap. Stacked inverter chains.

$f/t_r,t_f$	1.00%	3.25%	5.50%	7.25%	10.00%
500 MHz	2.3	2.34	2.48	2.16	2.11
750 MHz	2.75	2.67	2.45	2.44	2.47
1 GHz	3.23	3.12	3.02	2.92	2.78
2 GHz	4.76	4.83	4.78	4.79	4.76
3 GHz	6.76	6.93	7.25	7	7.65

1GHz, 2GHz and 3GHz. The higher the frequency is, the more transitions will take place in a time interval, thus contributing to the injected noise.

- The transition time (rise and fall times) of the stimulus signal. The simulated transition times were 1%, 3.25%, 5.5%, 7.25% and 10% of the square wave's period. Higher transition times mean higher derivatives, and the noise injection mechanisms depend mathematically on those.

Notice that the frequency presents much more influence on the results than the transition times.

In table 4, focusing on the adjacent variations from 500MHz to 750MHz and from 750MHz to 1GHz, almost all the values variations are higher between frequencies than those between transition times. This consideration is made to deal only with the linear variation of frequencies. The only exception is for 5.5% to 7.25% at 500 MHz, that exceeds the variation from 500MHz to 750Mhz at 5.5% by 0.03% of V_{DD}. The variation between

Table 5 – RMS noise values in % of V_{DD} at the N-Well tap. Stacked inverter chains.

f/t_r,t_f	1.00%	3.25%	5.50%	7.25%	10.00%
500 MHz	3.01	3.07	3.08	3.29	3.3
750 MHz	4.17	4.37	4.27	4.41	4.37
1 GHz	5.32	5.35	5.41	5.39	5.4
2 GHz	8.97	9.07	9.17	9.38	9.18
3 GHz	12.14	12.66	12.83	12.81	12.53

Table 6 – RMS noise values in % of V_{DD} at the substrate tap. Rectangular inverter chains.

f/t_r,t_f	1.00%	3.25%	5.50%	7.25%	10.00%
500 MHz	2.3	2.34	2.37	2.17	2.11
750 MHz	2.75	2.67	2.44	2.43	2.47
1 GHz	3.22	3.1	3	2.9	2.76
2 GHz	5.32	5.35	5.42	5.38	5.4
3 GHz	6.66	6.84	7.19	6.9	6.58

Table 7 – RMS noise values in % of V_{DD} at the N-well tap. Rectangular inverter chains.

f/t_r,t_f	1.00%	3.25%	5.50%	7.25%	10.00%
500 MHz	3	3.06	3.1	3.3	3.31
750 MHz	4.17	4.39	4.29	4.41	4.37
1 GHz	4.7	4.78	4.73	4.73	4.71
2 GHz	8.99	9.07	9.17	9.39	9.2
3 GHz	12.18	12.71	12.87	12.82	12.56

transition times is 0.32% of V_{DD}. In the case of noise measured on the N-well tap (table 5), all the variations in frequency are higher than those in transition times.

Hereby, the results found for the Rectangular chains and the Back-to-back chains follow, in order to compare the behavior with the other topologies. Similarly to the previous case, for the rectangular chain, it is possible to see higher variations with frequency than with transition times in all cases, both in the substrate tap results (Table 6) and in the N-well ones (Table 7). Tables 8 and 9 present the data for the Back-to-back configured chains, that are in accordance to the same analysis of the Rectangular chains.

Given the results, one can conclude that, for the transition time range considered, there is not as much influence in the noise value by the transition times in comparison to frequency. At first, this conclusion contrasts with the theory presented in section 2.3.2. However, it is possible that this result is different for ranges of shorter t_r and t_f, *i.e.*, the simulated transitions were not steep enough to cause considerable noise generation. A reasonable explanation for noise levels increasing with frequency is that more transitions are occurring in a certain amount of time, therefore, there are more noise injection sources

Table 8 – RMS noise values in % of V_{DD} at the substrate tap. Back-to-back inverter chains.

$f/t_r,t_f$	1.00%	3.25%	5.50%	7.25%	10.00%
500 MHz	2.41	2.44	2.46	2.26	2.41
750 MHz	2.84	2.77	2.55	2.58	2.58
1 GHz	3.35	3.22	3.14	3.12	3
2 GHz	4.91	4.96	4.96	5.03	4.97
3 GHz	6.75	6.9	7.38	7.02	6.65

Table 9 – RMS noise values in % of V_{DD} at the N-well tap. Back-to-back inverter chains.

$f/t_r,t_f$	1.00%	3.25%	5.50%	7.25%	10.00%
500 MHz	2.97	3.04	3.05	3.27	3.3
750 MHz	4.17	4.34	4.26	4.39	4.39
1 GHz	5.31	5.32	5.4	5.4	5.37
2 GHz	9.03	9.07	9.19	9.5	9.21
3 GHz	12.21	12.76	12.95	12.9	12.66

that add together in such time length. Therefore, even though the transitions do not contribute much to noise due to their own characteristics, it is possible that, if a sufficiently large number of such transitions can be summed, they will contribute significantly to noise.

It is intended at this point to verify how the obtained values relate to what can be found in the literature. Focusing on the simulation of the Stacked chains, with 3GHz signal and 1% of the period rise and fall times, the approximate peak value measured in the substrate tap is $35mV$ (see Figure 35. In [10], the results for measured substrate noise in a distance of $20\mu m$ from the noise source reached up to peaks of $7mV$, which is in the same order of magnitude of the results here presented. The digital agressor circuit is a processor core for an industrial transceiver, with 200 standard cells. The clock frequency is not mentioned.

In turn, the RMS voltage for activating the mBBICS is $58.8mV$, which leads to peaks as high as $318mV$. Therefore, the propagated noise is higher in this work, for a same traversed distance. The conclusion that can be drawn, recalling that the highest value, or at least its vicinity, is responsible for sensor activation, is that an mBBICS that is located at $20\mu m$ distance from a noisy circuit will not be activated by propagated noise.

This simulation presents highly correlated noise due to its periodic appearance, even though it is not strictly periodic. This can be explained by the fact that, despite presenting a number of logic gates in the same order of magnitude of the circuits in [22], the NMOS have all the same parameters, as well as the PMOS. Moreover, the input signal is very similar in each chain, and their operations are highly correlated, *i.e.* the output of each chain can be completely predicted by knowing their inputs.

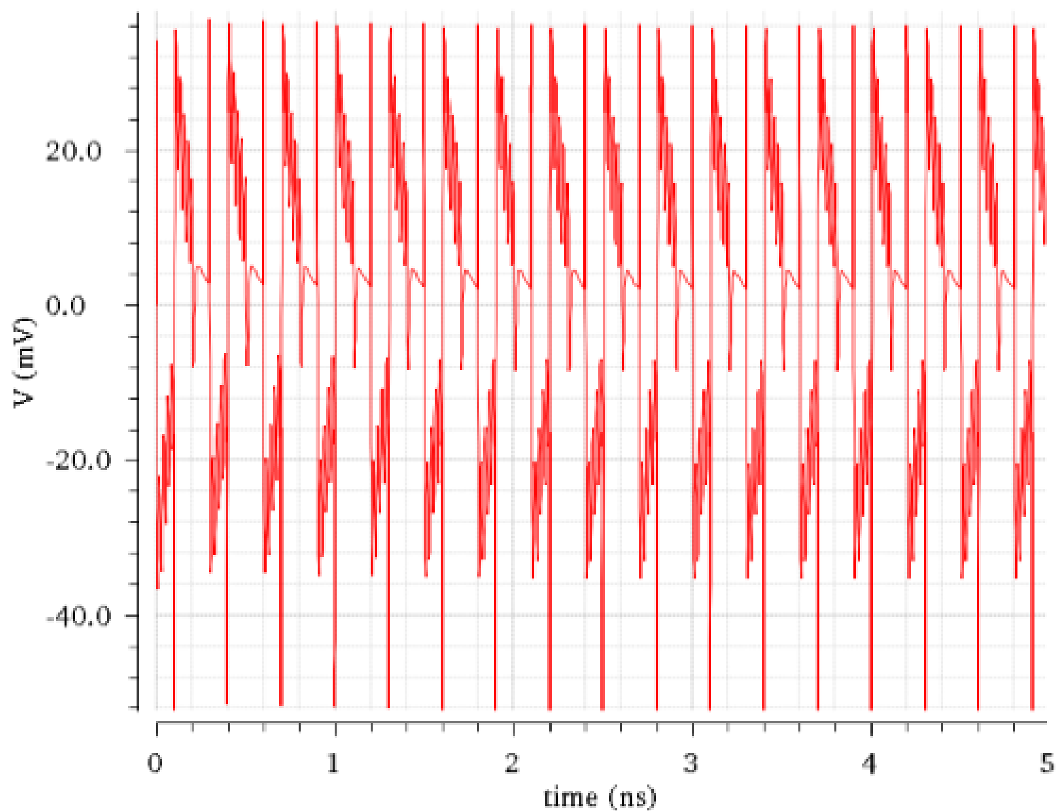

Figure 35 – Simulation results for Stacked inverter chain, 3GHz input, t_r,t_s = 1% of period, output measured at the substrate tap.

4.5 Effect of the duration of exposure to noise

In order to study the effects caused by different exposure times, the already known iterative procedure for detection of minimum noise RMS values that lead to sensor activation was repeated for durations of 200, 300, 400, 500, 600, 700, 800, 900 and 1000 ns.

By analyzing Figures 36 and 37, it is possible to notice the general behavior of higher variation of threshold values for lower stop times, as well as smaller variations for those closer to 1μs. The fact of lower variation at the larger stop times suggests that the least probable higher noise values occurred, because the waveform had more time to swing, *i.e.*, the random variable that represents noise was realized more times. Therefore, the stop time can become large enough to a point that it is much less likely that an even higher peak (than the highest at that point) occurs, keeping the RMS value inside a small range.

In Figure 37, a particularity occurs near $1\mu s$, where the necessary RMS voltage for activation decreases steeply. An explanation for such event is that the highest peaks are occurring at these time values. Until approximately $900ns$, the variations in the threshold values were progressively diminishing, indicating that highest total values were occurring closer to previous ones, as opposed to the beginning of the trace. However, even higher peaks occurred near $1\mu s$, which diminished the RMS value. This leads to the conclusion that, for switching noise, a stop time of $1\mu s$ is not enough time to simulate the mBBICS

in the presence of noise and draw consistent conclusions.

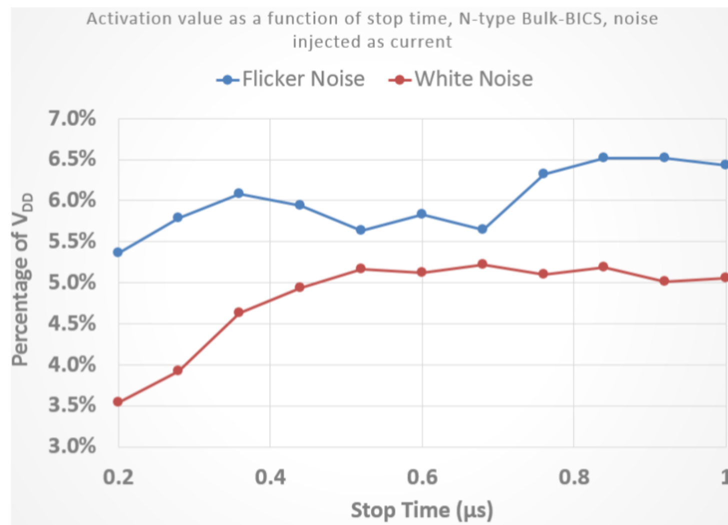

Figure 36 – Simulation results for error flag activation, for different stop times, noise injected as current.

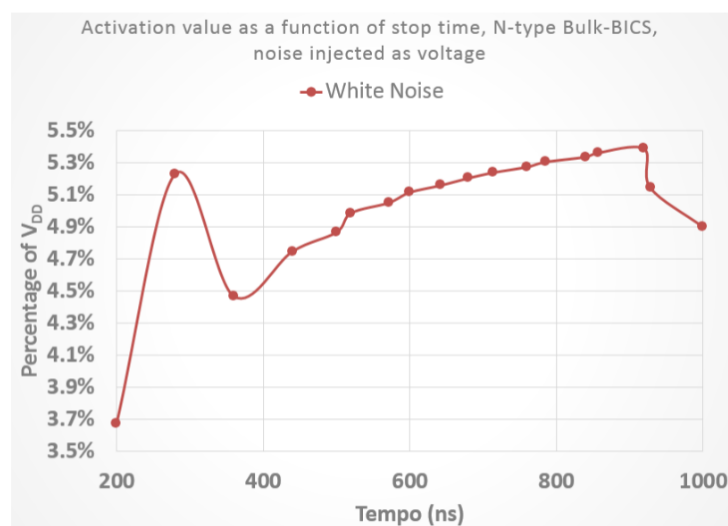

Figure 37 – Simulation results for error flag activation, for different stop times, noise injected as voltage.

5 Strategies for robustness enhancement

In the previous chapter, different manners in which noise can influence the behavior of the mBBICS were studied. Once in posession of this knowledge, it is aimed to make changes in the studied system parameters, in order to try to achieve better sensor robustness to noise. As a general idea, actions in the direction of increasing the circuit's sensitivity to a transient fault have the same effect on susceptibility to noise. If those occur at the same degree, the actions have no benefit to robustness improvement. However, the effects can be less or more pronounced to sensitivity and noise vulnerability, *i.e.*, they may lead to the same direction, but at different degrees. The objective of this chapter is to verify if different adjustments in the mBBICS lead to different degrees in change of behavior, as well as to analyze if the degree of change is beneficial or not to robustness enhancement of the sensor.

5.1 Variation of transistor parameters

This section is intended to verify if the variation of N_{h1}'s/P_{h1}'s length can serve as a robustness enhancement for the mBBICS. The variation of the transistor's length leads to different channel resistances, which can favor or worsen both sensitivity and susceptibility to device noise.

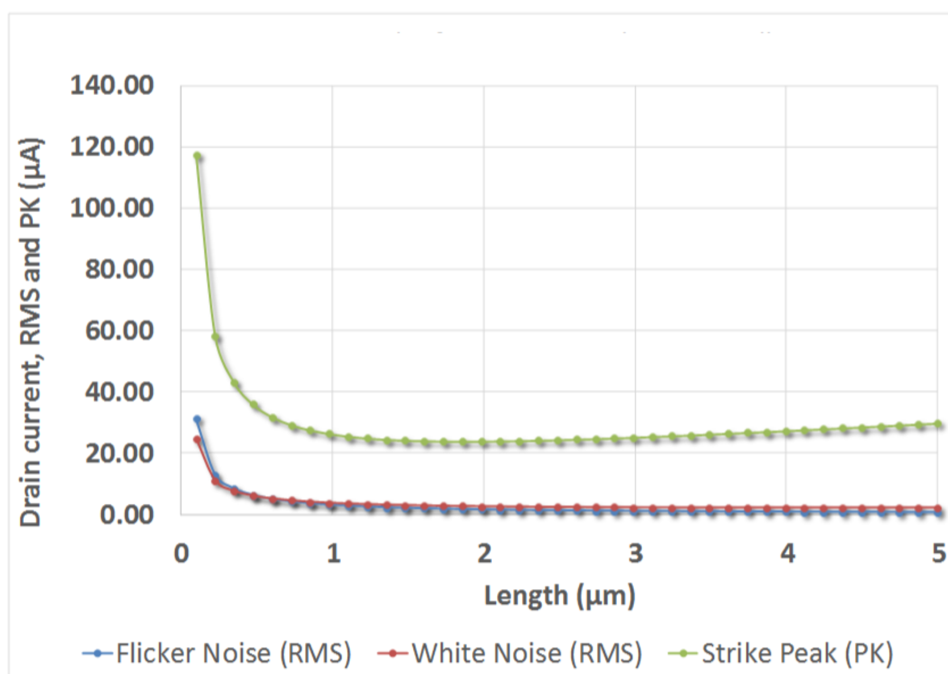

Figure 38 – Activation minimum value for varying lengths, N-type mBBICS.

A set of 40 different lengths was selected, from the minimum length allowed by the technology ($100nm$) to $50L_{min}$ ($5\mu m$). For each length, the minimum activation value was determined with the technique described in section 3.2, both for device noise and the transient fault current. The results are shown in Figure 38 for the NMOS mBBICS and in Figure 39 for the PMOS.

It can be visually perceived that the minimum peak value for activation decreases much more with the transistor's length than the noise curves, until about $8.3L_{min}$ ($1\mu m$). This means improvement in robustness, since the sensitivity of the sensor is increasing, while the penalty in vulnerability to noise is much smaller. A noticeable conclusion is that this occurs mainly for low values of L, thus, robustness is better achieved together with low area penalty.

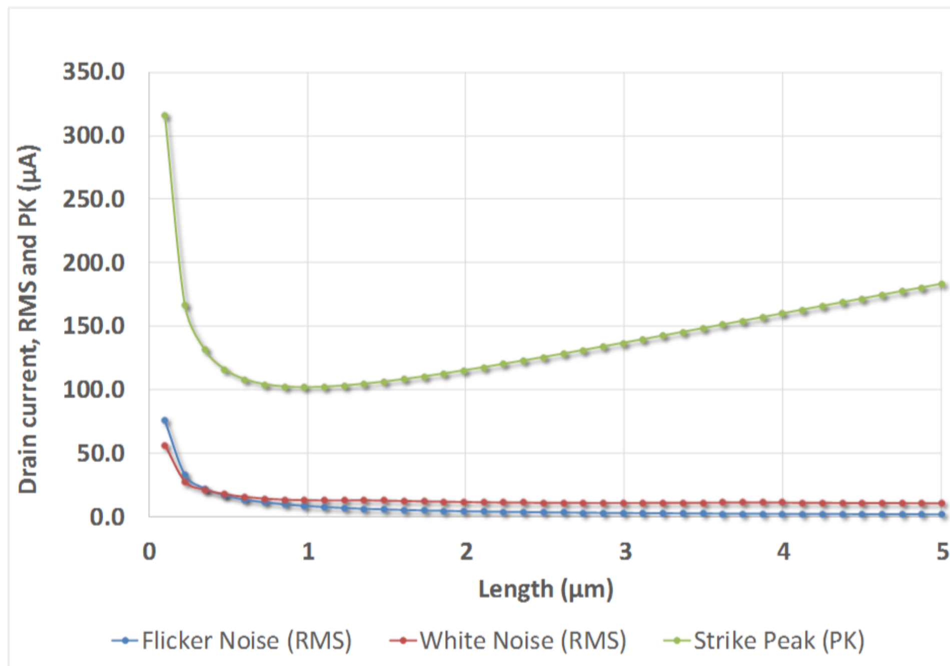

Figure 39 – Activation minimum value for varying lengths, P-type mBBICS.

For the N-type mBBICS, the sensitivity of the sensor increases by $93.6\mu A$, from the length of $100nm$ to $1.86\mu m$. In the same length range, the susceptibility to Flicker Noise increases by $29.5\mu A$, while that for White Noise increases by $22.1\mu A$. The transient fault sensitivity increasing corresponds to 317.5% of the Flicker Noise increase and 423.7% for White Noise, in respect to the transient fault sensitivity increasing.

For the P-type mBBICS, the increases are $133.2\mu A$ for transient fault (from 100nm to $1\mu m$), and $74.1\mu A$ for Flicker Noise and $45.4\mu A$ for White Noise. The transient fault increase corresponds to 179.9% of that for Flicker Noise and 293.3% of that for White Noise.

5.2 Variation of terminal voltages

In the previous section, the length of the transistor was varied, so the channel resistance was varied too. Hereby, it is proposed to alter the channel resistance by using another parameter, that does not affect the area of the mBBICS circuit, at least directly. Such parameter is the gate to source voltage, V_{GS}.

By referring to 2.2, one can notice that V_{GS} is one of the components of the parameter that correlates I_{DS} with V_{DS}, *i.e.*, it's variation also alters the proportionality constant defined by the geometry and the process parameters of the transistor, which is the channel resistance.

A set of 40 different voltages was selected, from 0.4V to V_{DD}. For each voltage, the minimum activation value was determined with the technique described in section 3.2, both for device noise and the transient fault current. The results are shown in Figure 40 for the NMOS mBBICS and in Figure 41 for the PMOS. Below 0.4V, the behavior was very different and lead to no useful conclusions.

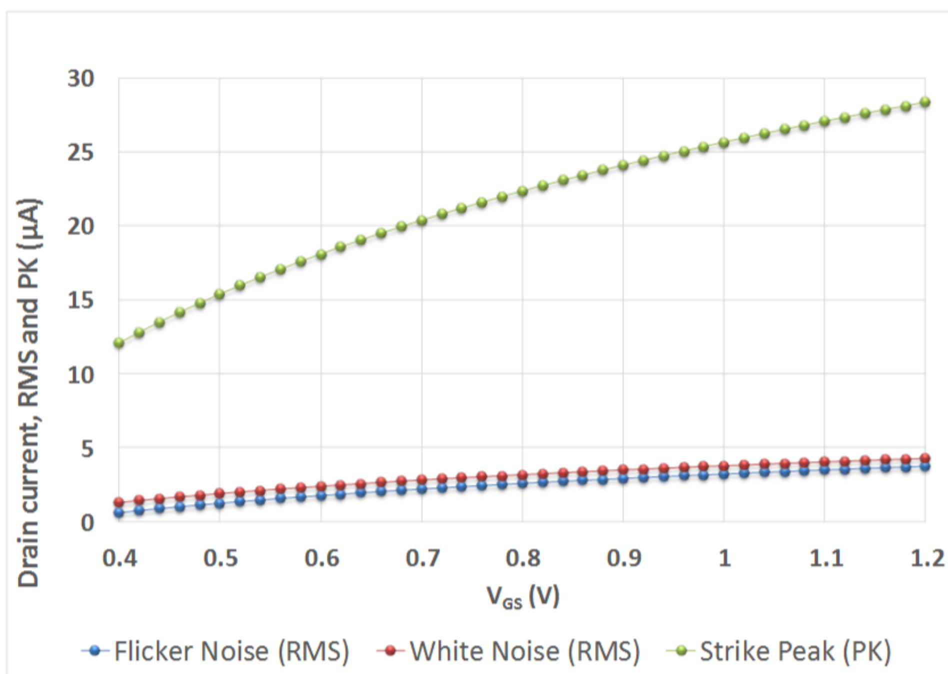

Figure 40 – Combined activation threshold profiles for the N-type mBBICS.

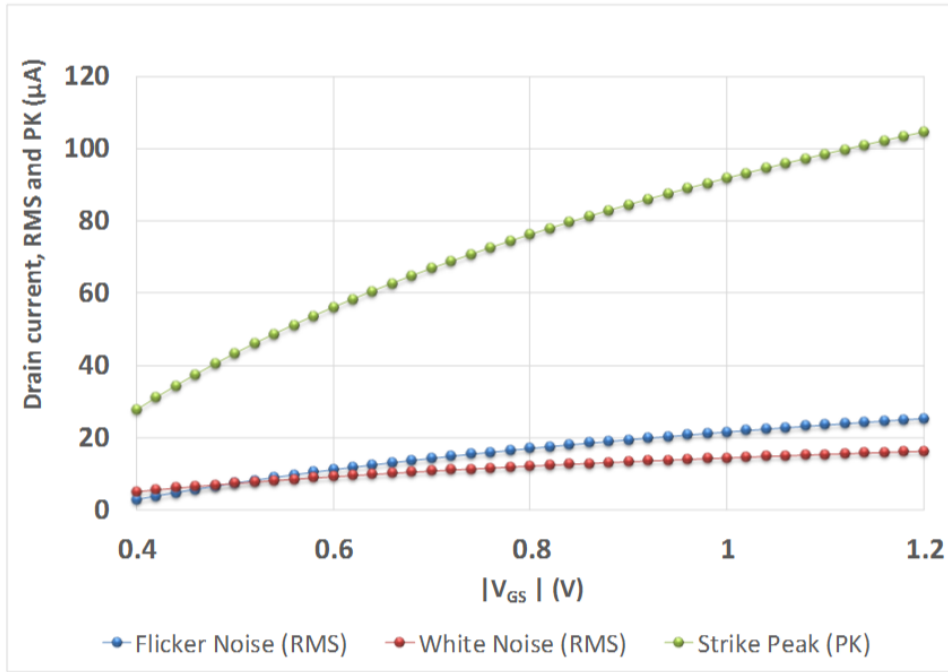

Figure 41 – Combined activation threshold profiles for the P-type mBBICS.

The N-type mBBICS activation can be visually seen to be more sensitive by diminishing V_{GS} and, more specifically, the sensitivity is more increased for the transient fault peak than for noise, which is desirable for the goals of this work. The vulnerability for Flicker Noise increases by $3.1\mu A$, and similarly, that for White Noise increases by $3.0\mu A$. The sensitivity for the strike peak, contrastingly, increases by $16.3\mu A$, which is approximately 540% of the factors related to noise.

For the P-type mBBICS, the increases are $77.0\mu A$ for transient fault sensitivity, and $22.6\mu A$ for Flicker Noise and $11.2\mu A$ for White Noise, which corresponds to 29.4% and 14.5%, respectively.

5.3 Exploration of body effect

Adjustment of biasing voltages in the mBBICS proved to have an effect in the robustness of the sensor. Another biasing characteristic that can potentially be taken advantage of is the bulk biasing. By doing such, one is capable of altering the threshold voltage of a transistor. This threshold voltage modulation by the bulk bias is called the *body effect*.

In the present case, the biasing to be altered should not be that of N_{h1} / P_{h1}, but N_{h2} / P_{h2}. Varying the threshold voltage of this transistor should cause it to reach the on-state with a lower or higher input from N_{h1} / P_{h1}, consequently changing the sensor's sensitivity.

A set of 40 different voltages was selected, from $0V$ to $-0.6V$, referring to V_{SB} in the N-type mBBICS case, and to V_{BS} for the P-type one. For each voltage, the minimum activation value was determined with the technique described in section 3.2, both for device noise and the transient fault current. The results are shown in Figure 42 for the NMOS mBBICS and in Figure 43 for the PMOS. Below -0.6V, the behavior was very different and lead to no useful conclusion.

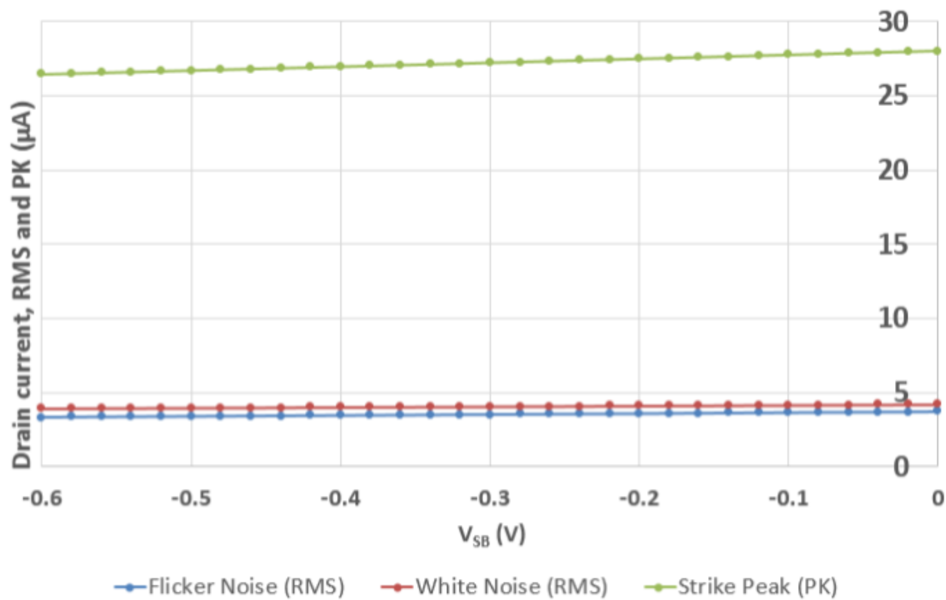

Figure 42 – Combined activation threshold profiles for the N-type mBBICS.

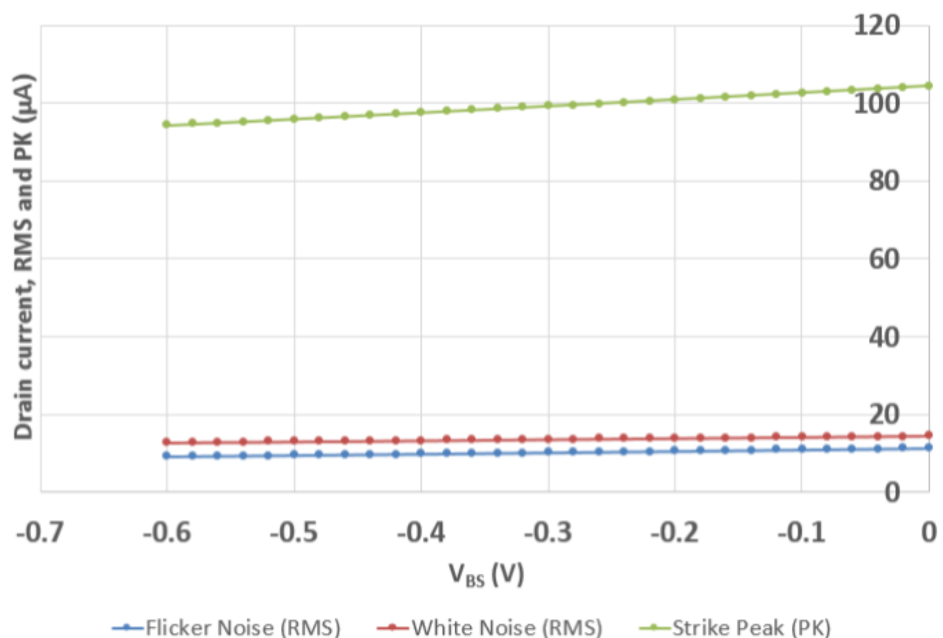

Figure 43 – Combined activation threshold profiles for the P-type mBBICS.

In the case of the N-type mBBICS, the activating value for the transient fault peak drops by 1.58μA, while it does so by 0.38μA and 0.28μA for Flicker Noise and White Noise, respectively. Hence, the variation of V_{GS} causes a greater influence in the sensitivity of the sensor than in its vulnerability to noise, namely, 564.3% for White Noise and 415.8% for Flicker Noise.

For the P-type mBBICS, the increases are 133.2μA for transient fault sensitivity, and 74.1μA for Flicker Noise and 45.4μA for White Noise. The increase which corresponds to 55.6% and 34.1%, respectively.

5.4 Variation of the number of monitored transistors

Including more transistors to be monitored is expected to increase the overall capacitance experienced by the input of the mBBICS. In order to verify the actual behavior of the sensor in such situations, the setup described in section 3.8 was implemented and submitted to Flicker Noise and White Noise.

The simulations were performed for sets of load counts of 10 to 160 transistors, being each set greater than the previous by 10 transistors. In other words, sets of 10, 20, 30 until 160 transistors were simulated. Also, a single load transistor was included in the simulation. More than 160 transistors were not simulated, given that they offered enough parasitic capacitance to prevent true transient fault detection. The results can be seen in Figure 44.

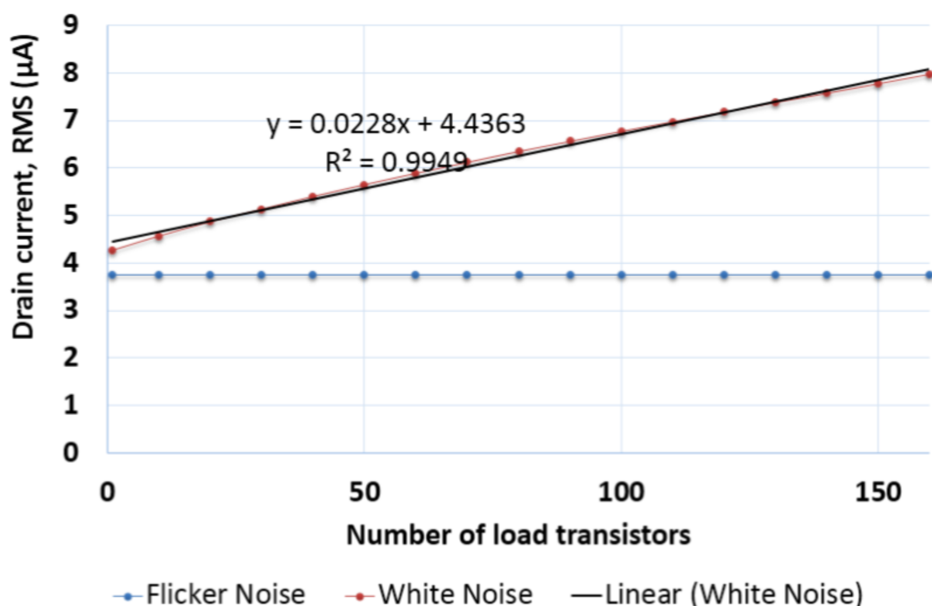

Figure 44 – Simulation results for different load transitor numbers, NMOS mBBICS.

It is possible to notice an increase in robustness to White Noise that is very close to a linear behavior, as a first order function can be fit with a coefficient of determination of 0.9949. However, the mBBICS shows virtually no change in behavior for Flicker Noise, whose swings lie in the order of pA, and cannot event be distinguished in the present scale. This can be explained by the hypothesis that the input transistor of the mBBICS, together with the overall parasitic capacitance, characterizes a low-pass filter. The values for channel resistance and parasitic capacitance are small enough to characterize a very high cut-off frequency. Therefore, this frequency is much higher than the highest frequency of Flicker Noise, whereas it does perform filtering action for the higher frequencies of White Noise, that reach up to 500GHz in the present case.

5.5 Results discussion

The results presented in this chapter indicate that the robustness of the mBBICS can be increased by altering its parameters. It is important to notice that increase in robustness does not mean that susceptibility to noise is decreased with increasing of sensitivity. It can be observed that an improvement in the sensor's sensitivity incurs also in more vulnerability to noise. Nevertheless, the robustness improvement lies on the fact that sensitivity increases in much higher rates than susceptibility to noise, by correctly selecting the parameters' ranges.

Increasing the length of the input transistor lead to both high increase in sensitivity and area saving, as it can be better improved in relation to noise vulnerability in smaller length values. Regarding V_{GS} variation, the same benefit in sensitivity improvement can be noticed. Furthermore, this technique does not imply in enlarging the transistor's area. The benefit of higher increase in sensitivity was also observed for bulk biasing, however, it can be concluded that the traditional configuration, where the bulk terminal is short-circuited to the source terminal, already leads to the better relationship between sensitivity and noise susceptibility. Finally, the filtering effect of the parasitic capacitances of load transistors was verified to counteract White Noise, whereas no change took place for Flicker Noise.

6 Conclusion

The fast pace of semiconductor technology scaling has been made it possible to society to largely improve its well-being, from the entertainment industry to business and health. Such scaling means that the fundamental components of microchips are acquiring progressively smaller dimensions, which make them susceptible to more physical phenomena each time a step is given towards semiconductor node advance. Such characteristic of the semiconductor industry demands failure circumventing systems, that must, in turn, be reliable.

Effects that occur in MOS devices that are prone to unreliability were presented, as well as non-idealities of a silicon substrate, important noise types that are present in nano-scaled circuits, radioactive particles incidence in a chip and how it can disrupt the functionality of a circuit and a transient fault detection system, which is the mBBICS.

Simulations were performed that lead to important information about how such system can be affected by noise. By submitting the mBBICS directly to device and switching noises (*i.e.*, applying noise to the circuit's input), the minimum noise values for activation were determined for the sensor. The fact that the activating and non-activating values are different from each other by less than 1% makes it possible to interpret the obtained results as the minimum ones with considerable accuracy. These values were more conveniently expressed as RMS values, given that an exact definition of sensor triggering cause would be impracticable, if even possible. For reference, the peak values of the noise waveforms were also registered. It was verified that switching noise has the potential to activate the mBBICS, accusing false error, when compared to similarly simulated values in the literature. Device noise, however, do not pose a threat to this concern about the mBBICS. Both Thermal and Flicker noises present levels that are orders of magnitude lower than those necessary to activate the sensor, while Shot Noise does not apply, as no current takes place at the input transistor when there is no transient fault. Nevertheless, CMOS advances both in device sizing and structuring may lead to a situation in which device noise could have a considerable effect.

It was verified that noise injected by a switching circuit and propagated through the chip's substrate presented similar values in this work when compared to another noise propagation simulation in the literature, *i.e.*, the obtained order of magnitude was the same. In addition, even though the value found in this work was one order of magnitude lower than the values necessary for activation, circuits with different topologies, sizes, parameters and fabrication processes may vary significantly the generated noise, indicating that switching noise should not be disregarded in an mBBICS design. Furthermore, the

switching noise generated by the inverter chains in this work was not White Noise, given the small number of noise generating devices, which may as well have simplified the environment.

In a possible future scenario, in that device noise affects a circuit such as the mBBICS, the investigation of changes in parameters for robustness improvement provided valuable results. By altering the mBBICS's input transistor's length, gate to source voltage, source to body voltage and number of monitored transistors, the robustness of the mBBICS was enhanced, in the sense that its sensitivity to a transient fault changes at rates higher than those of susceptibility to noise. In other words, it is possible to strategically select certain values for the analyzed parameters, such that the sensitivity of the circuit can be increased with minimum noise penalty. It is most important to emphasize in concluding this work that the methodology hereby developed aims to determine the best trade-offs between sensitivity to a particle strike and susceptibility to noise, given that sensitivity improvement is necessarily accompanied by a level of susceptibility to noise.

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